USB1.1 Snap On Board

Reference Manual

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Performance data may depend on the operating environment, the area of application, the configuration, and method of control, as well as on other conditions of use; these may deviate from the technical specifications, the Design Guide specifications, or other product documentation. The actual performance characteristics can be determined only by measurements subsequent to integration.

The reference designs were tested in a reference environment for compliance with the legal requirements applicable to the reference environment.

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rm_scusb11_1.6

About this Manual

Introduction

This manual helps users to know about the hardware features of the USB 1.1 Snap On Board.

Table below shows the revision history of USB 1.1 Snap On Board.

Version	Date	Description
1.6	May 2008	• Changed introduction section
1.5	December 2007	• Changed pin configuration of Santa Cruz Header J1.
1.4	October 2007	Updated document as per the board version 4.0; • Changed pin configuration of Santa Cruz Headers J1, J2, J3 • Changed pin configuration of general purpose IO header J4.
0.1.3	January 2007	Change layout design.
0.1.2	May 2005	Made Pin assignments more descriptive
0.1.1	October 2004	First Publication of the User Manual

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Ctrl + N to open to the Go To Page dialog box.
- Bookmarks serve as an additional table of contents.
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Typographic Conventions

The USB 1.1 Snap On Board reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: **Introduction, Block Diagram.**
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: ***Figure 1-1. USB 1.1 Snap On Board Side View, Table 1-1.*** *USB 1.1 Snap On Board Components and Interfaces*
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
•	Bullets are used in a list of items when the sequence of items is not important.
☞	The hand points to special information that requires special attention
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.

Visual Cue	Meaning
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

Contents

1. Introduction

The SLS USB 1.1 Snap On board is designed to provide connectivity between USB 1.1 host controller (computer) and USB 1.1 Function IP Core. The USB 1.1 Snap On board provides extra signals, which may be used to snap onto any development board having santa cruz headers.

Features

Functions of SLS USB 1.1snap on board are as follows:

- Complies with Universal Serial Bus specification 1.1
- Supports Full Speed (12 MbPS) and Low Speed (1.5 MbPS)
- Snaps on any board with Altera standard Santa Cruz header
- Supports 3.3V
- Supports single-ended data interface

Figure 1-1. shows the USB 1.1 Snap On Board angle view.

Figure 1-1. USB 1.1 Snap On Board Angle View

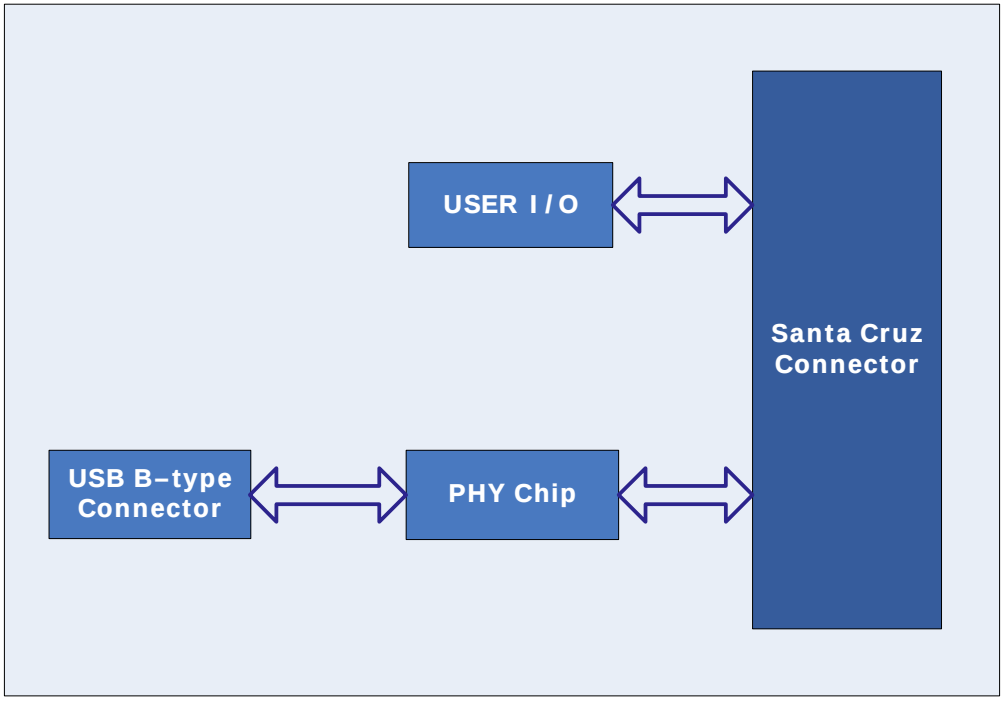
Block Diagram

USB 1.1 Snap On board includes following components:

- USB B-type connector
- USB PHY for converting the differential line into three transmit and three receive signals
- Debug header (male) - J4 - unused pins from the Santa Cruz header given out to debug the core
- Headers J1, J2, J3 forming a standard-footprint called Santa Cruz short expansion headers (female)

The three headers J1, J2, J3 are female headers on USB 1.1 Snap On board which snaps on Santa Cruz connectors. Figure 1-2. below shows functional diagram of USB 1.1 Snap On Board.

Figure 1-2. USB 1.1 Snap On Board Functional Block Diagram



Next chapter explains overview of all the board components.

2. Board Components

This section contains brief overview of the important components on the USB 1.1 Snap On Board. Figure 2-1. below shows the components on the USB 1.1 Snap On Board.

Figure 2-1. USB 1.1 Snap On Board Components

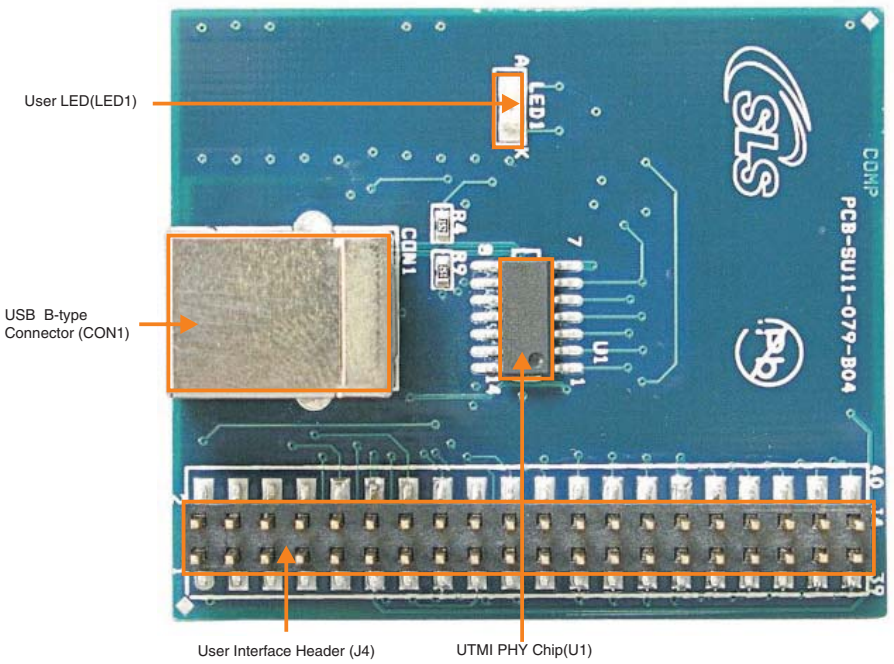


Table 2-1. USB 1.1 Snap On Board Components & Interfaces

Board Reference	Name	Description	Page
Featured Device			
U1	USB1T11A	UTMI (USB1.1 Transceiver Macro-cell Interface) -- PHY Chip	5
User Interfaces			
CON1	USB 1.1 Connector	One USB 1.1Device Connector (B-Type)	6
Expansion Connectors			
J1, J2, J3	Expansion Prototype Connector	These are the three female connectors used for mounting daughter card (In this case its USB1.1 Snap On Board) on the Development Kit having standard Santa Cruz short expansion male interface.	7
General Connectors			
J4	User Interface Header	All the unused pins of SantaCruz connector are taken out for the user to use it for any other applications like debug or use it as standard I/O.	8
LEDs			
LED1	User LED	User can use this LED1 as an indication of any required output	10

Featured Device

PHY Chip(U1)

A PHY-Chip is the intermediate between FPGA & the 2 differential lines. It converts the differential line in the three transmit and three receive signals as shown in Figure 2-1. No level shifting is required for USB since it uses 3.3V for its operation as there is no direct connection between the USB & FPGA.

The signals at PHY chip are shown in Table 2-2 below.

Table 2-2. PHY Chip Signal

Pin #	Signal Name	Type	For NIOS Cyclone Dev Kit (EP1C20)#	General Description
1	Mode		---	Selection depends on the basis of the Jumper J1 on USB1.1 Snap On Board
2	OE		U9	tx_oe of USB1.1 IP---
3	RCV		V9	rx_d of USB1.1 IP---
4	VP		Y8	rx_dp of USB1.1 IP---
5	VM		W8	rx_dn of USB1.1 IP---
6 & 7	GND		---	Supply Ground
8	NC		---	No Connection
9	Speed		---	The speed is selected according to the jumper J4 on USB1.1 Snap On Board
10	D-		---	---
11	D+		---	---
12	VPO		R9	tx_dp of USB1.1 IP---
13	VMO / FSEO		T9	tx_dn of USB1.1 IP---
14	VCC		---	Supply Voltage

User Interface

This section describes user interfaces which includes USB1.1 B-Type Connector.

USB B-type Connector(CON1)

USB 1.1 Snap On board incorporates USB B-Type Connector connected with PHY chip. Figure 2-1. displays the USB B-Type connector which is mounted on the board. This connector requires an interface device in order to communicate with FPGA.

The 2 pins of B-Type connector connects to the Phy-chip as shown in Table 2-3 . These are data transfer and data receive lines.

Table 2-3. USB B-Type Connector to PHY Chip Connection

B-type Connector Pin#	Signal	PHY-Chip (USB1T11A) Pin#
1	NC	--
2	D-	10
3	D+	11
4	GND	--

Expansion Connectors

This section describes the expansion connectors on the USB1.1 Snap On board.

Expansion Prototype Connectors(J1,J2,J3)

Headers J1, J2, and J3 collectively form the standard-footprint called Santa Cruz short expansion headers (female), which are 14 pins, 40pins and 20pins respectively. These are mechanically stable connections that can be used for mounting daughter card (USB 1.1 Snap On Board) on to any Development Kit having standard Santa Cruz short expansion male interface.

The expansion prototype connector interface includes

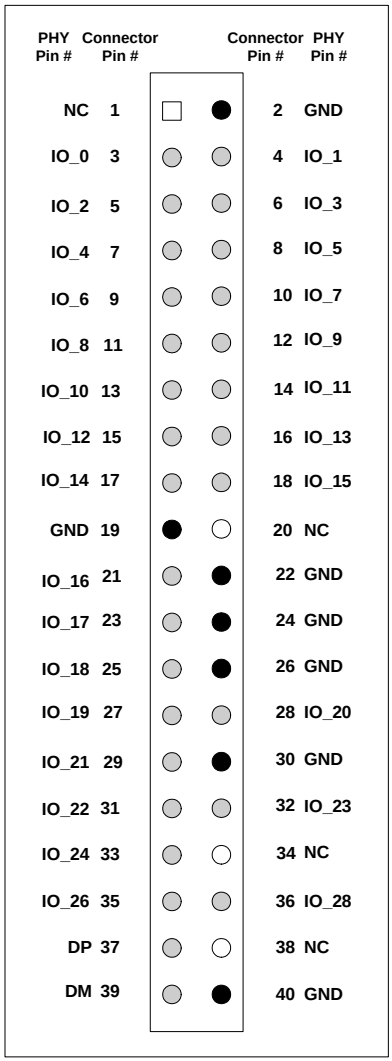
- 74 pins for prototyping (Out of which 43 I/O pins connect to user I/O pins and 3 dedicated clock pins on the Cyclone device)
- An Active LOW Power On Reset signal
- Five regulated 3.3V power-supply pins (1A total max load)
- One regulated 5V power-supply pin. (1A total max load)
- Numerous ground connections

The output logic level on the expansion prototype connector pins is 5 Volts.

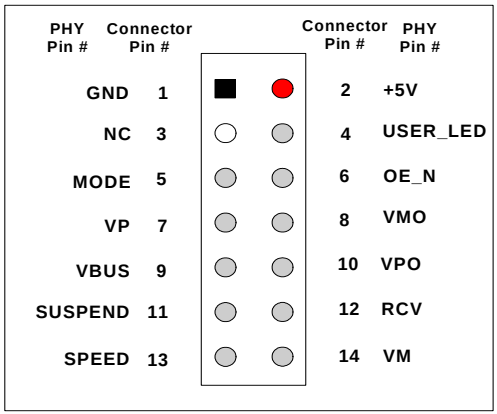
Figure 2-2. shows the pin description of the connectors J1, J2 & J3.

Figure 2-2. Pin Description of Expansion Prototype Connector-J1, J2, J3

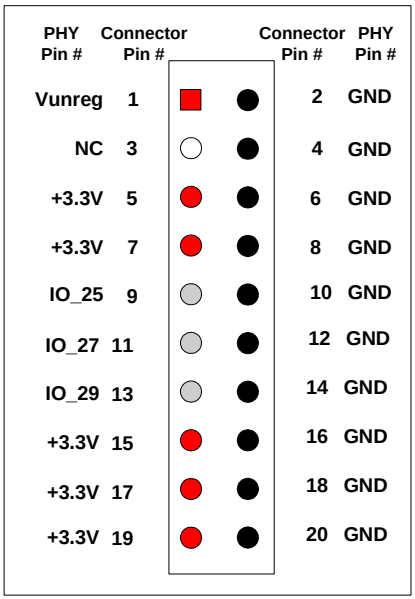
J2



J1



J3



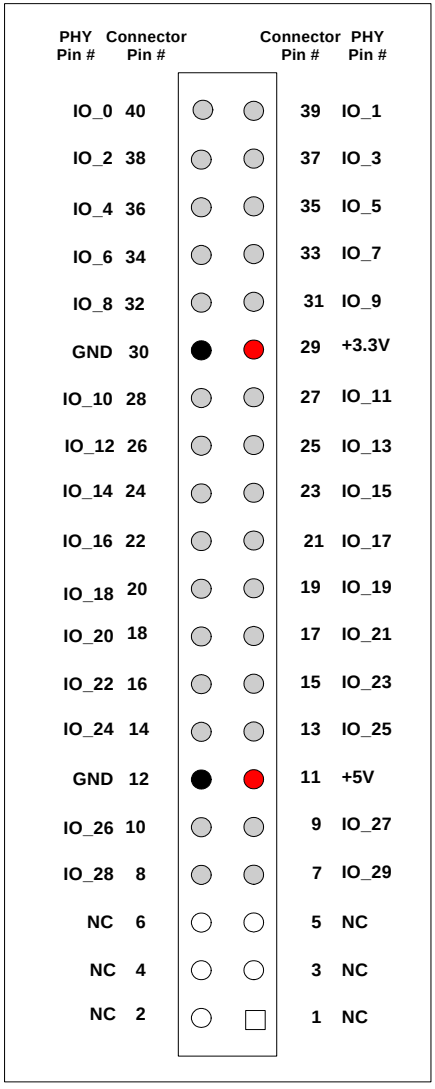
General Connectors

This section describes the general connector on the USB 1.1 Snap On board.

User Interface Header(J4)

There are four user interface headers namely J4 (20x2) on USB1.1 Snap On board as displayed in Figure 2-1. All the unused I/O of the Santa Cruz connector are taken out in the form of headers on to J4. User can use these headers for debug purpose or some other purpose. Figure 2-3. shows the pin description of the connector J4.

Figure 2-3. Pin Description of User Interface Header (J4)



LEDs

This section describes the User LED (LED1) on USB 1.1 Snap on board.

LED(LED1)

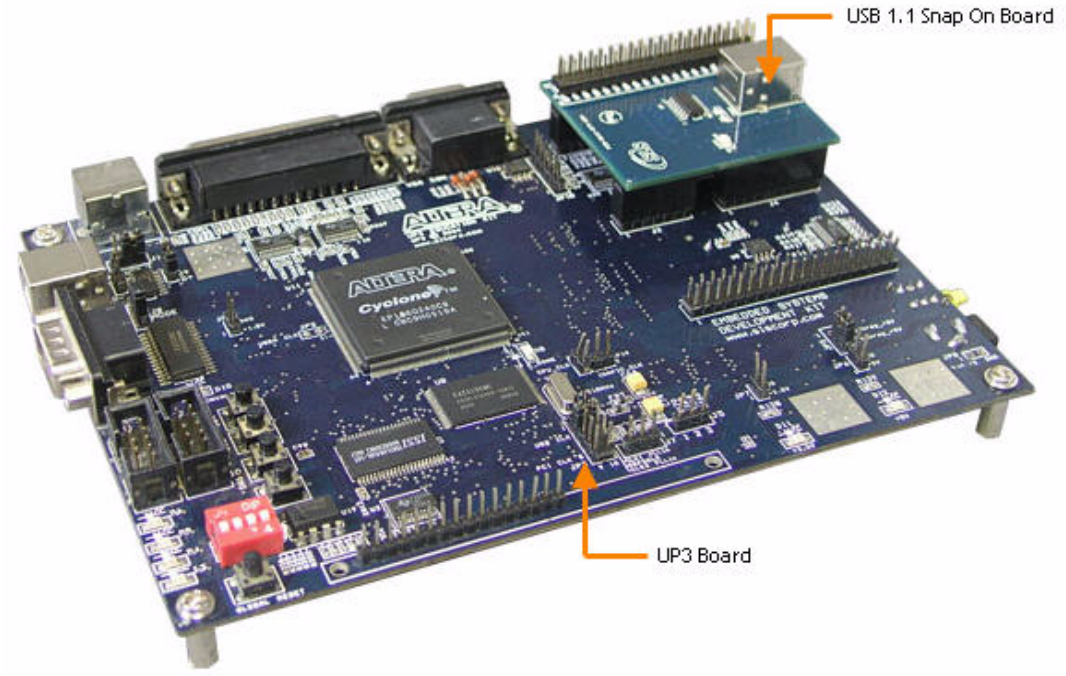
The USB 1.1 Snap On Board has 1 general purpose user LED (LED1) as shown in Figure 2-1.

User can use this LED1 as an indication of any required output.

3. Signal Mapping

The three (F) headers (J1,J2,J3) on USB 1.1 Snap On board snaps on to three (M) SantaCruz headers (J2,J4,J3) of UP3 Education kit
Figure 3-1. below shows how the USB Snap On Board snaps on the Santa Cruz connector. Nios Board is used as the example.

Figure 3-1. Connection of USB 1.1 Snap On Board with UP3 Education Kit



Mapping PHY Pins with Core IO

The Table 3-1 below shows the mapping of Core IO signal with SantaCruz Pin.

Table 3-1. Mapping the Core IO with SC Pin & IP Signals

Signal (IP)	Signal on Santa Cruz Connector	Santa Cruz Pin No.
rx_d	RCV	J1.12
rx_dp	VP	J1.7
tx_oe	-OE	J1.6
tx_dp	VPO	J1.10
tx_dn	VMO/FSEO	J1.8
rx_dn	VM	J1.14

Unused pin Maping

There is one debug header (J4) and its pins are routed to the Santa Cruz connector. So, the headers directly connects with FPGA pins when the board Snaps-On. Thus these headers can be used for debugging purpose.

The Table 3-2 below shows how one can map these unused pins

Table 3-2. Debug Header (J4) table

Debug Header (J4)	Signal Name on Santa Cruz connector	I/O
J4.40	J2.3	IO_0
J4.39	J2.4	IO_1
J4.38	J2.5	IO_2
J4.37	J2.6	IO_3
J4.36	J2.7	IO_4
J4.35	J2.8	IO_5
J4.34	J2.9	IO_6
J4.33	J2.10	IO_7
J4.32	J2.11	IO_8
J4.31	J2.12	IO_9
J4.28	J2.13	IO_10

Table 3-2. Debug Header (J4) table

Debug Header (J4)	Signal Name on Santa Cruz connector	I/O
J4.27	J2.14	IO_11
J4.26	J2.15	IO_12
J4.25	J2.16	IO_13
J4.24	J2.17	IO_14
J4.23	J2.18	IO_15
J4.22	J2.21	IO_16
J4.21	J2.23	IO_17
J4.20	J2.25	IO_18
J4.19	J2.27	IO_19
J4.18	J2.28	IO_20
J4.17	J2.29	IO_21
J4.16	J2.31	IO_22
J4.15	J2.32	IO_23
J4.14	J2.33	IO_24
J4.13	J3.9	IO_25
J4.10	J2.35	IO_26
J4.9	J3.11	IO_27
J4.8	J2.36	IO_28
J4.7	J3.13	IO_29
J4.30	-	GND
J4.12	-	GND