E-Gasket

(DE1/DE2 to Santa Cruz Header Interface)

Reference Manual

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About this Manual

Introduction

This manual provides information about the E-Gasket and the DE1/DE2 to Santa Cruz Header Interface.

Table below shows the revision history of E-Gasket Reference Manual.

Version	Date	Description
1.2	August 30, 2007	• GPIO header pin (J17.20) mapping information with DE2 board is corrected. • Version no. and document part no. format is changed.
1.1	August 4, 2007	Second publication of the E-Gasket Reference Manual • Placed Pin Description information in Chapter 2. • Placed the Board Connection information in Chapter 1.
1.0	September 2006	First Publication of the E-Gasket Reference Manual

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Shift + Ctrl + N to open to the Go To Page dialog box.
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Typographic Conventions

The E-Gasket Reference Manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital Letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: ***Board Components, DE1/2 Header.***
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: ***Figure 2-1. E-Gasket Side View, Table 3.1. Pin Mapping of J3 Header for DE1 and DE2 Board***
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
• ■	Bullets are used in a list of items when the sequence of items is not important.
☞	The hand points to special information that requires special attention
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.

Visual Cue	Meaning
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

Contents

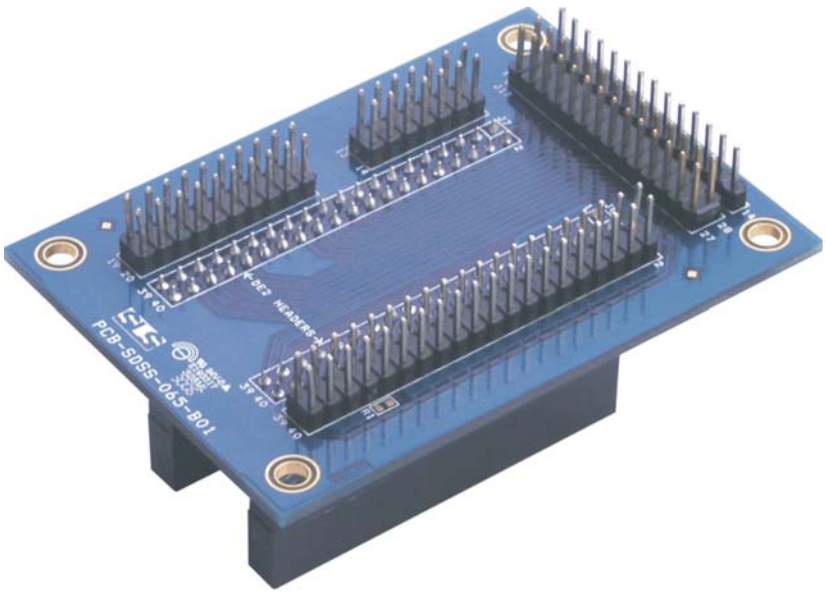
1. Introduction

DE2 and DE1 come with two 40 pin expansion headers with the motive of increasing the IOs and board expansion capabilities. A number of vendors manufacture Snap On Boards that fit/snap on Altera Standard Santa Cruz header. Altera Standard Santa Cruz header is also a kind of expansion header that comes as a set of 3 (40-14-20 pin) headers with similar motive.

In order to use Altera standard Santa Cruz Snap on boards with DE1 or DE2, we have a DE1/2 interface to Santa Cruz converter, here after referred as "E-Gasket"(A board act as interface between the DE1/2 and the Snap On Board).

Figure 1-1. shows the E-Gasket Top View.

Figure 1-1. E-Gasket Top View



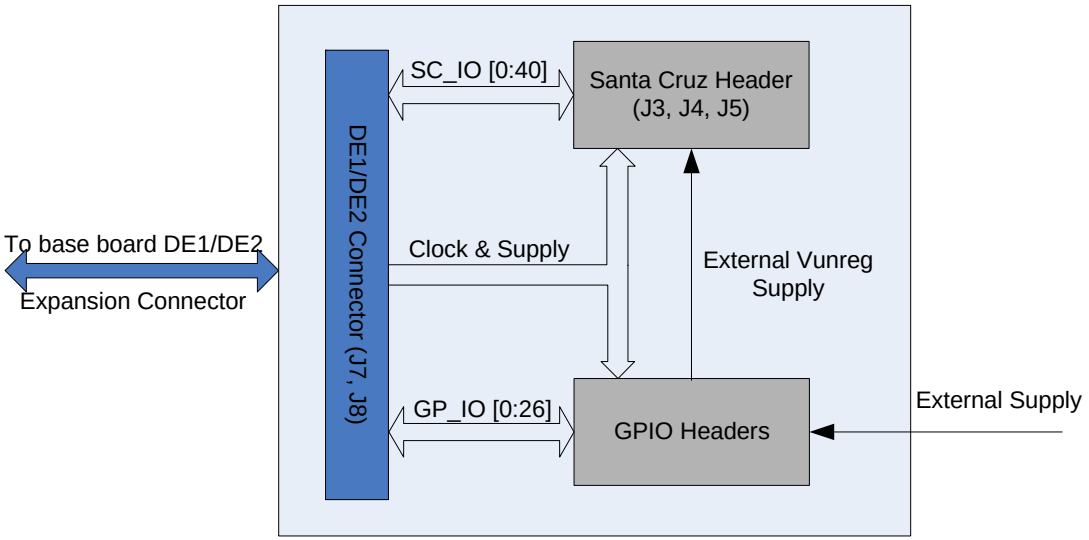
Block Diagram

The E-Gasket includes following components:

- Santa Cruz Headers (M): J3, J4, J5.
- DE1/2 Headers(F): J7, J8.
- GPIO Headers: J17, J18.

Two headers J7, J8 are female headers on the E-Gasket board which connects on headers JP1(M), JP2(M) of DE1 or DE2 board.
Figure 1-2. below shows block diagram of the E-Gasket.

Figure 1-2. E-Gasket Block Diagram



Next Chapter explains overview of all the board components.

Board Connections

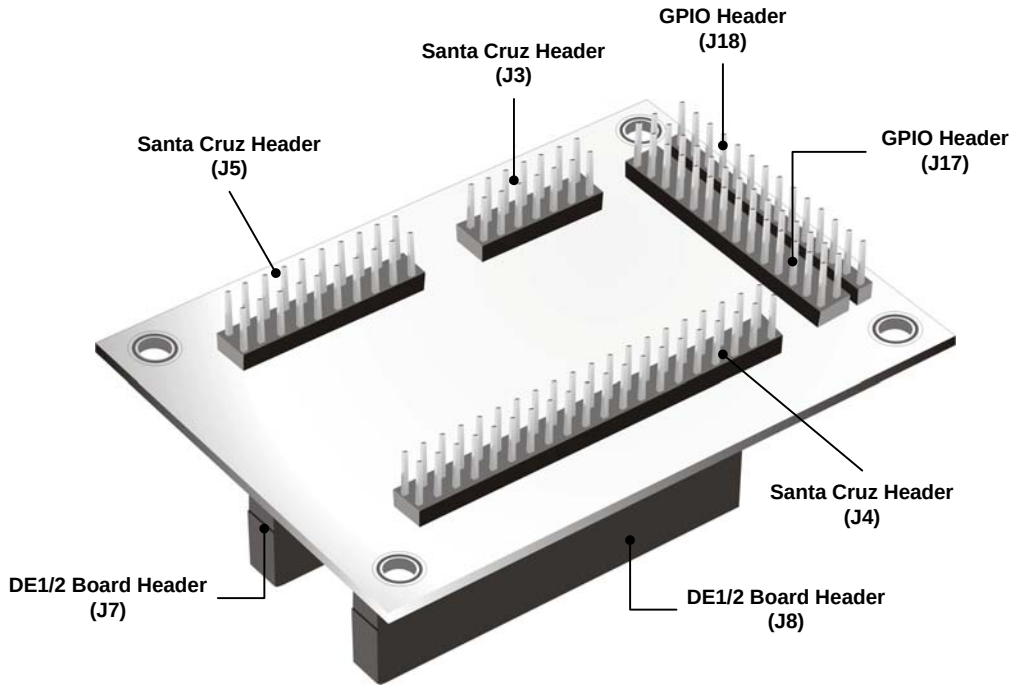
Two male headers (J6, J7) of the E-Gasket are connected to two male header (JP1, JP2) of DE1 or DE2 board as shown in Figure 1-3.

Figure 1-3. Connection of E-Gasket with DE2 Board

2. Board Components

This section contains brief overview of the components on the E-Gasket. Figure 2-1. below shows the components on the E-Gasket.

Figure 2-1. E-Gasket Components



DE1/2 Headers

The E-Gasket Board provides DE1/2 header interface as shown in Figure 2-2. DE1/2 headers of the E-Gasket are connected on DE1 or DE2 board.

Figure 2-2. DE1/2 Headers (J7, J8)

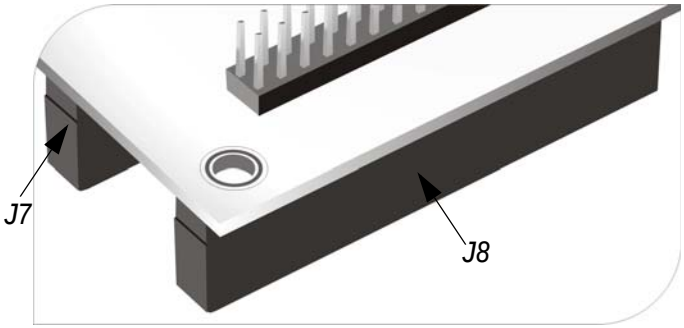


Figure 2-3. shows DE1/2 Headers (J7, J8) pin description.

Figure 2-3. DE1/2 Headers (F) - J7, J8

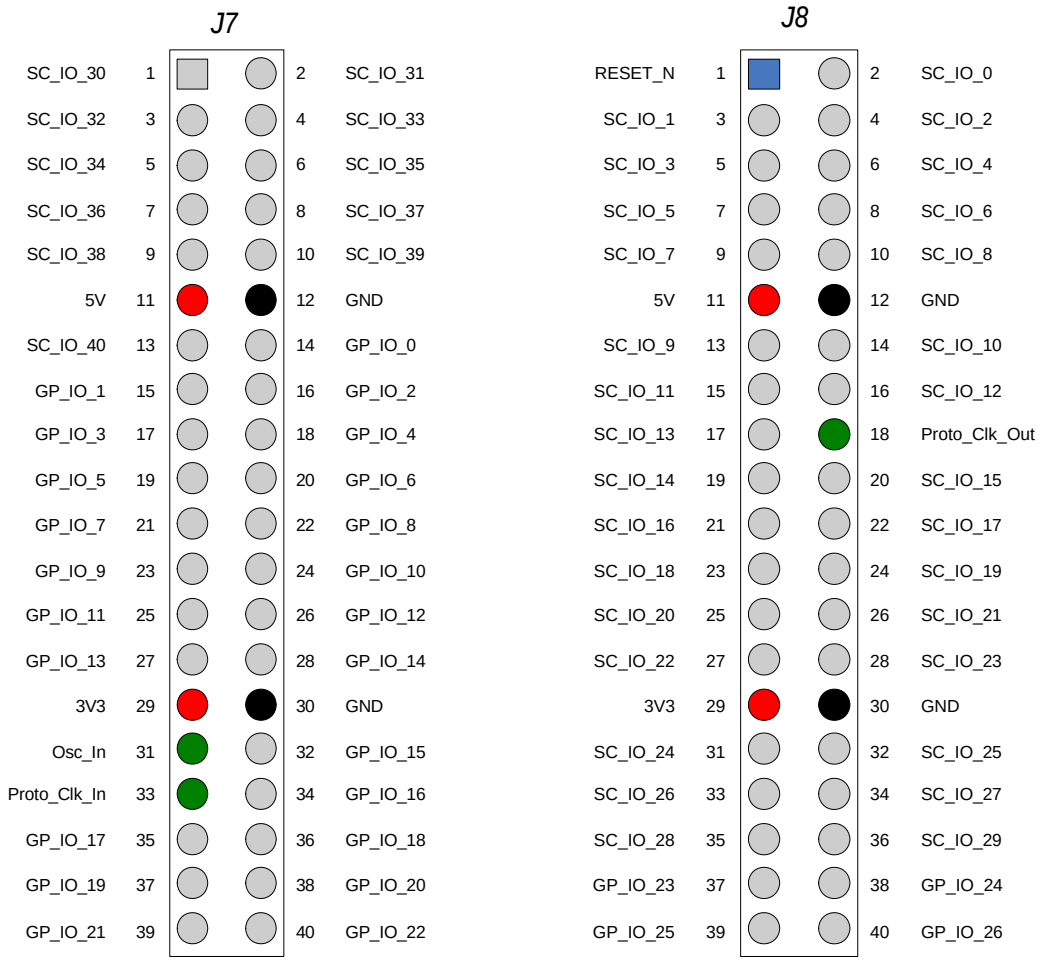


Table 2-1 lists DE1/2 header (J7) pin mapping to DE(1/2)'s FPGA.

Table 2-1. DE1/2 Header (J7) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J7.1	SC_IO_30	A13	D25
J7.2	SC_IO_31	B13	J22
J7.3	SC_IO_32	A14	E26
J7.4	SC_IO_33	B14	E25
J7.5	SC_IO_34	A15	F24
J7.6	SC_IO_35	B15	F23
J7.7	SC_IO_36	A16	J21
J7.8	SC_IO_37	B16	J20
J7.9	SC_IO_38	A17	F25
J7.10	SC_IO_39	B17	F26
J7.11	5V	-	-
J7.12	GND	-	-
J7.13	SC_IO_40	A18	N18
J7.14	GP_IO_0	B18	P18
J7.15	GP_IO_1	A19	G23
J7.16	GP_IO_2	B19	G24
J7.17	GP_IO_3	A20	K22
J7.18	GP_IO_4	B20	G25
J7.19	GP_IO_5	C21	H23
J7.20	GP_IO_6	C22	H24
J7.21	GP_IO_7	D21	J23
J7.22	GP_IO_8	D22	J24
J7.23	GP_IO_9	E21	H25
J7.24	GP_IO_10	E22	H26
J7.25	GP_IO_11	F21	H19
J7.26	GP_IO_12	F22	K18

Table 2-1. DE1/2 Header (J7) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J7.27	GP_IO_13	G21	K19
J7.28	GP_IO_14	G22	K21
J7.29	3.3V	-	-
J7.30	GND	-	-
J7.31	OCS_IN	J21	K23
J7.32	GP_IO_15	J22	K24
J7.33	Proto_Clk_in	K21	L21
J7.34	GP_IO_16	K22	L20
J7.35	GP_IO_17	J19	J25
J7.36	GP_IO_18	J20	J26
J7.37	GP_IO_19	J18	L23
J7.38	GP_IO_20	K20	L24
J7.39	GP_IO_21	L19	L25
J7.40	GP_IO_22	L18	L19

Table 2-2 lists DE1/2 header (J8) pin mapping to DE(1/2)'s FPGA.

Table 2-2. DE1/2 Header (J8) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J8.1	Reset_N	H12	K25
J8.2	SC_IO_0	H13	K26
J8.3	SC_IO_1	H14	M22
J8.4	SC_IO_2	G15	M23
J8.5	SC_IO_3	E14	M19
J8.6	SC_IO_4	E15	M20
J8.7	SC_IO_5	F15	N20
J8.8	SC_IO_6	G16	M21

Table 2-2. DE1/2 Header (J8) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J8.9	SC_IO_7	F12	M24
J8.10	SC_IO_8	F13	M25
J8.11	5V	-	-
J8.12	GND	-	-
J8.13	SC_IO_9	C14	N24
J8.14	SC_IO_10	D14	P24
J8.15	SC_IO_11	D15	R25
J8.16	SC_IO_12	D16	R24
J8.17	SC_IO_13	C17	R20
J8.18	Proto_Clk_Out	C18	T22
J8.19	SC_IO_14	C19	T23
J8.20	SC_IO_15	C20	T24
J8.21	SC_IO_16	D19	T25
J8.22	SC_IO_17	D20	T18
J8.23	SC_IO_18	E20	T21
J8.24	SC_IO_19	F20	T20
J8.25	SC_IO_20	E19	U26
J8.26	SC_IO_21	E18	U25
J8.27	SC_IO_22	G20	U23
J8.28	SC_IO_23	G18	U24
J8.29	3.3V	-	-
J8.30	GND	-	-
J8.31	SC_IO_24	G17	R19
J8.32	SC_IO_25	H17	T19
J8.33	SC_IO_26	J15	U20
J8.34	SC_IO_27	H18	U21
J8.35	SC_IO_28	N22	V26

Table 2-2. DE1/2 Header (J8) Pin Mapping			
Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J8.36	SC_IO_29	N21	V25
J8.37	GP_IO_23	P15	V24
J8.38	GP_IO_24	N15	V23
J8.39	GP_IO_25	P17	W25
J8.40	GP_IO_26	P18	W23

Santa Cruz Headers

The E-Gasket provides Santa Cruz interface as shown in Figure 2-4. Any short Santa Cruz compatible snap on board can be snapped on to Santa Cruz headers of the E-Gasket.

Figure 2-4. Short Santa Cruz Headers (J3, J4, J5)

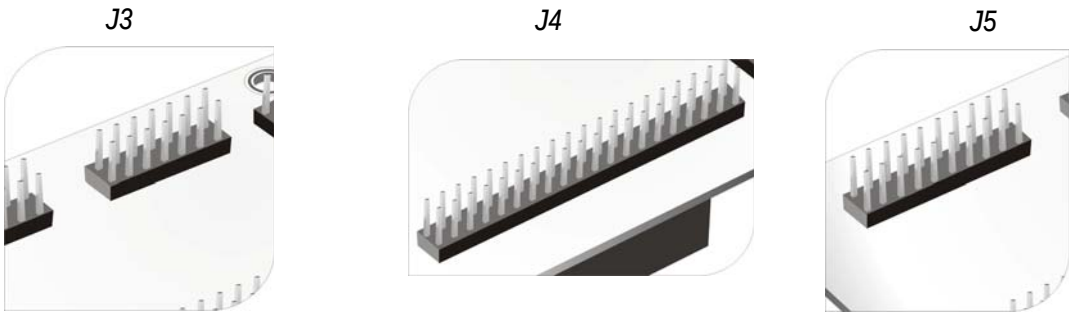


Figure 2-5. shows Santa Cruz headers (M) J3, J4, J5 pin description.

Figure 2-5. Santa Cruz Headers (M) - J3, J4,J5 Pin Description

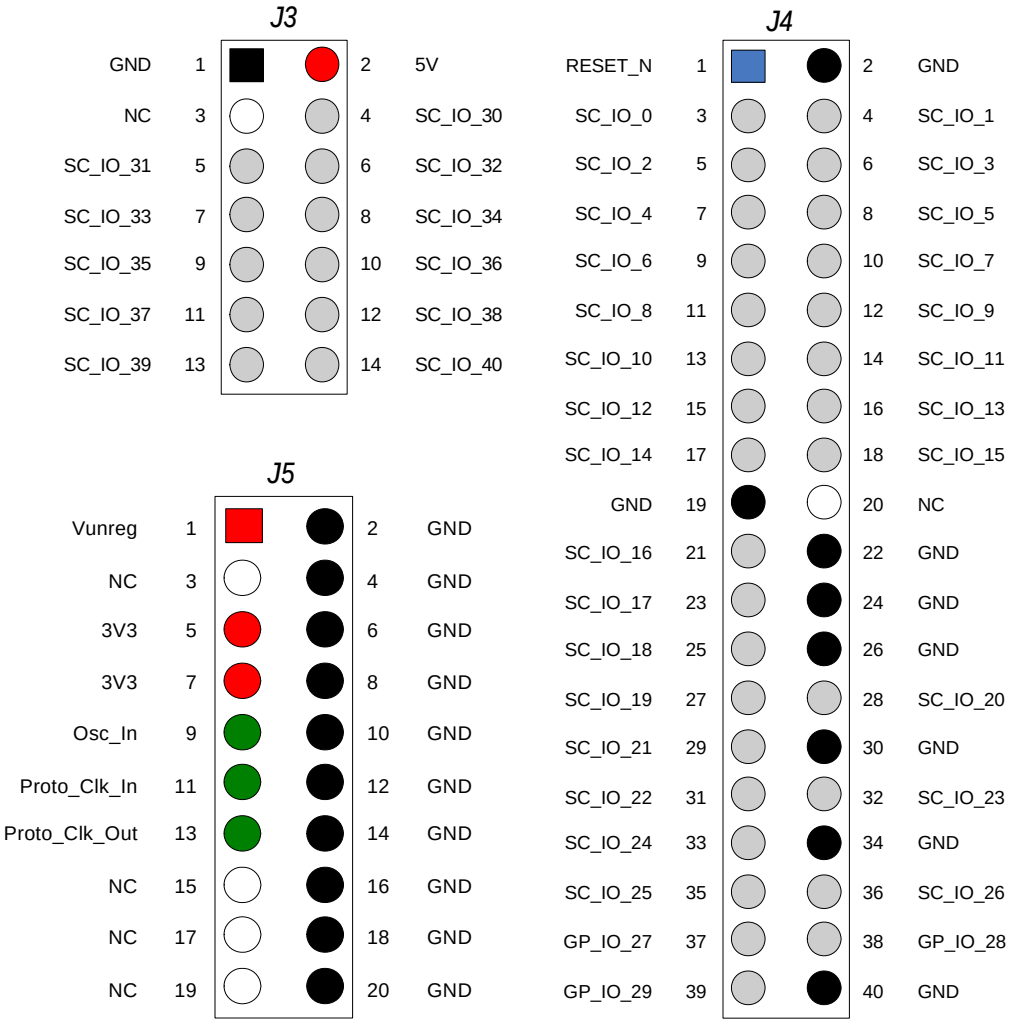


Table 2-3 lists Santa Cruz Header (J3) pin mapping to DE(1/2)'s FPGA.

Table 2-3. Santa Cruz Header (J3) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J3.1	GND	-	-
J3.2	5V	-	-
J3.3	NC	-	-
J3.4	SC_IO_30	A13	D25
J3.5	SC_IO_31	B13	J22
J3.6	SC_IO_32	A14	E26
J3.7	SC_IO_33	B14	E25
J3.8	SC_IO_34	A15	F24
J3.9	SC_IO_35	B15	F23
J3.10	SC_IO_36	A16	J21
J3.11	SC_IO_37	B16	J20
J3.12	SC_IO_38	A17	F25
J3.13	SC_IO_39	B17	F26
J3.14	SC_IO_40	A18	N18

Table 2-4 lists E-Gasket header (J4) pin mapping to DE(1/2)'s FPGA.

Table 2-4. Santa Cruz Header (J4) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J4.1	RESET_N	H12	K25
J4.2	GND	-	-
J4.3	SC_IO_0	H13	K26
J4.4	SC_IO_1	H14	M22
J4.5	SC_IO_2	G15	M23
J4.6	SC_IO_3	E14	M19
J4.7	SC_IO_4	E15	M20

Table 2-4. Santa Cruz Header (J4) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J4.8	SC_IO_5	F15	N20
J4.9	SC_IO_6	G16	M21
J4.10	SC_IO_7	F12	M24
J4.11	SC_IO_8	F13	M25
J4.12	SC_IO_9	C14	N24
J4.13	SC_IO_10	D14	P24
J4.14	SC_IO_11	D15	R25
J4.15	SC_IO_12	D16	R24
J4.16	SC_IO_13	C17	R20
J4.17	SC_IO_14	C19	T23
J4.18	SC_IO_15	C20	T24
J4.19	GND	-	-
J4.20	NC	-	-
J4.21	SC_IO_16	D19	T25
J4.22	GND	-	-
J4.23	SC_IO_17	D20	T18
J4.24	GND	-	-
J4.25	SC_IO_18	E20	T21
J4.26	GND	-	-
J4.27	SC_IO_19	F20	T20
J4.28	SC_IO_20	E19	U26
J4.29	SC_IO_21	E18	U25
J4.30	GND	-	-
J4.31	SC_IO_22	G20	U23
J4.32	SC_IO_23	G18	U24
J4.33	SC_IO_24	G17	R19
J4.34	GND	-	-

Table 2-4. Santa Cruz Header (J4) Pin Mapping			
Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J4.35	SC_IO_25	H17	T19
J4.36	SC_IO_26	J15	U20
J4.37	SC_IO_27	H18	U21
J4.38	SC_IO_28	N22	V26
J4.39	SC_IO_29	N21	V25
J4.40	GND	-	-

Table 2-5 lists Santa Cruz Header (J5) pin mapping to DE(1/2)'s FPGA.

Table 2-5. Santa Cruz Header (J5) Pin Mapping			
Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J5.1 [1]	Vunreg	-	-
J5.2	GND	-	-
J5.3	NC	-	-
J5.4	GND	-	-
J5.5	3V3	-	-
J5.6	GND	-	-
J5.7	3V3	-	-
J5.8	GND	-	-
J5.9	Osc_In	J21	K23
J5.10	GND	-	-
J5.11	Proto_Clk_In	K21	L21
J5.12	GND	-	-
J5.13	Proto_Clk_Out	C18	T22
J5.14	GND	-	-
J5.15	NC	-	-
J5.16	GND	-	-

Table 2-5. Santa Cruz Header (J5) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J5.17	NC	-	-
J5.18	GND	-	-
J5.19	NC	-	-
J5.20	GND	-	-

Note(s) :

(1) Refer notes in Table 2-7

GPIO Headers

Excess pins which are not routed on Santa Cruz Header from DE1/2 Header are fed to header J17. While header J18 is used as a test point for some standard santa cruz input/output and supply signal like Osc_In, Proto_Clk_In, Proto_Clk_Out, 5V, 3V3 and GND. J18 is also used to feed unregulated voltage. Figure 2-6. displays header J17 and J18.

Figure 2-6. GPIO Headers (J17, J18)

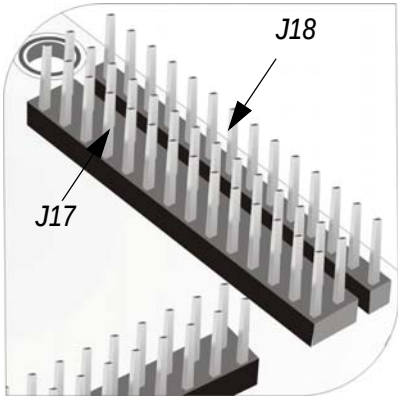


Figure 2-7. shows the pin description of GPIO (M) Headers, J18 and J17.

Figure 2-7. GPIO Headers (M) - J18, J17 Pin Description

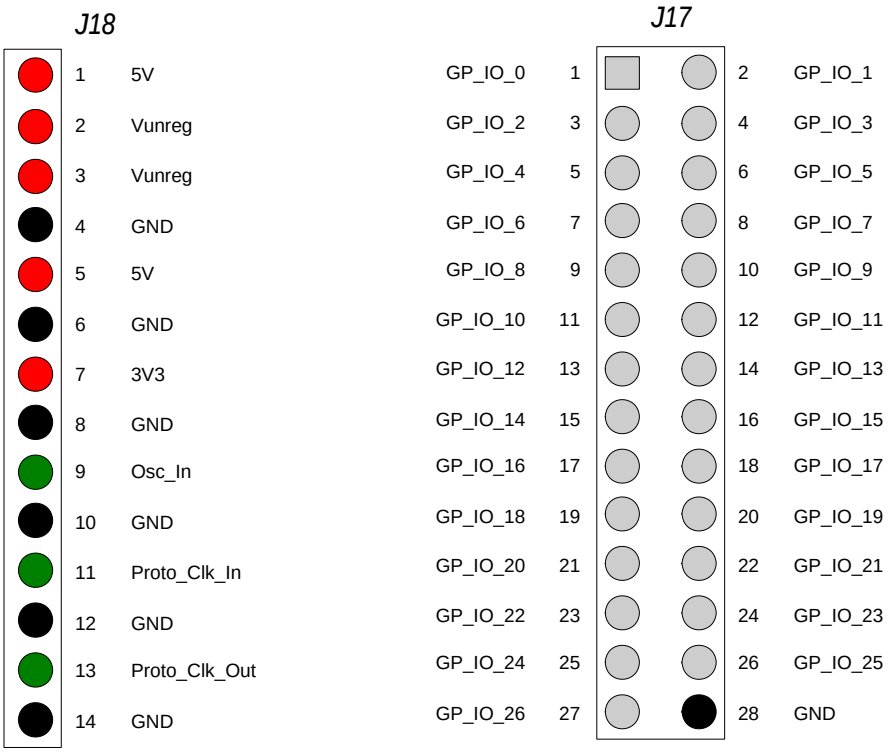


Table 2-6 lists GPIO header (J17) pin mapping to DE(1/2)'s FPGA.

Table 2-6. GPIO Header (J17) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J17.1	GP_IO_0	B18	P18
J17.2	GP_IO_1	A19	G23
J17.3	GP_IO_2	B19	G24
J17.4	GP_IO_3	A20	K22
J17.5	GP_IO_4	B20	G25
J17.6	GP_IO_5	C21	H23

Table 2-6. GPIO Header (J17) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J17.7	GP_IO_6	C22	H24
J17.8	GP_IO_7	D21	J23
J17.9	GP_IO_8	D22	J24
J17.10	GP_IO_9	E21	H25
J17.11	GP_IO_10	E22	H26
J17.12	GP_IO_11	F21	H19
J17.13	GP_IO_12	F22	K18
J17.14	GP_IO_13	G21	K19
J17.15	GP_IO_14	G22	K21
J17.16	GP_IO_15	J22	K24
J17.17	GP_IO_16	K22	L20
J17.18	GP_IO_17	J19	J25
J17.19	GP_IO_18	J20	J26
J17.20	GP_IO_19	J18	L23
J17.21	GP_IO_20	K20	L24
J17.22	GP_IO_21	L19	L25
J17.23	GP_IO_22	L18	L19
J17.24	GP_IO_23	P15	V24
J17.25	GP_IO_24	N15	V23
J17.26	GP_IO_25	P17	W25
J17.27	GP_IO_26	P18	W23
J17.28	GND	-	-

Table 2-7 lists GPIO header (J18) pin mapping to DE(1/2)'s FPGA.

Table 2-7. GPIO Header (J18) Pin Mapping

Pin Number	Signal Name	FPGA Pin No. (DE1)	FPGA Pin No. (DE2)
J18.1 [1]	5V	-	-
J18.2 [1]	Vunreg	-	-
J18.3 [2]	Vunreg	-	-
J18.4 [2]	GND	-	-
J18.5	5V	-	-
J18.6	GND	-	-
J18.7	3V3	-	-
J18.8	GND	-	-
J18.9 [3]	Osc_In	J21	K23
J18.10	GND	-	-
J18.11 [3]	Proto_Clk_In	K21	L21
J18.12	GND	-	-
J18.13 [3]	Proto_Clk_Out	C18	T22
J18.14	GND	-	-

Note(s) :

(1) Connect jumper on J18.1 and J18.2 to get 5V on J5.1(Vunreg) pin.

(2) Use J18.3 and J18.4 to feed external supply on J5.1 (Vunreg) pin.

(3) Pin J18.9, J18.11 and J18.13 are generally used for probing.

(4) "Vunreg" options can be omitted if the Santa Cruz Header Snap On Board doesn't use "Vunreg". If the Santa Cruz Header Snap On Board uses "Vunreg", then any one of the options (Note (1) or Note (2)) must be used in order to get the Snap On Board working properly