AN11226

TTL bias switching

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Document information

Info	Content
Keywords	BLA6H0912-500, gate switching, IFF transponder, LDMOS transistor, high-power, FET, MTF
Abstract	Modern Identification Friend or Foe (IFF) systems require high dynamic range transmit and receive paths and the ability to transmit in excess of 1 kW of power. These requirements on the transmit path require the use of amplifier modules with multiple stages operating near to Class A or heavily biased Class AB. To increase the performance of such systems a gate bias switching circuit is proposed.

Revision history

Rev	Date	Description
01	20120810	Initial version

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1. Introduction

Modern Identification Friend or Foe (IFF) systems require high dynamic range transmit and receive paths and the ability to transmit in excess of 1 kW of power. These requirements on the transmit path require the use of amplifier modules with multiple stages operating near to Class A or heavily biased Class AB.

Amplifiers that draw high bias current have an advantage in that they operate in the linear region but also have two main disadvantages. First the device is less efficient so requires a higher amount of prime power, costing more to operate the system. The second concern is that as a result of drawing higher bias current, the devices have an elevated junction temperature and usually produce a lower peak power which decreases the linear range of the amplifier and reduces the operating lifetime of the transistor.

2. Solution

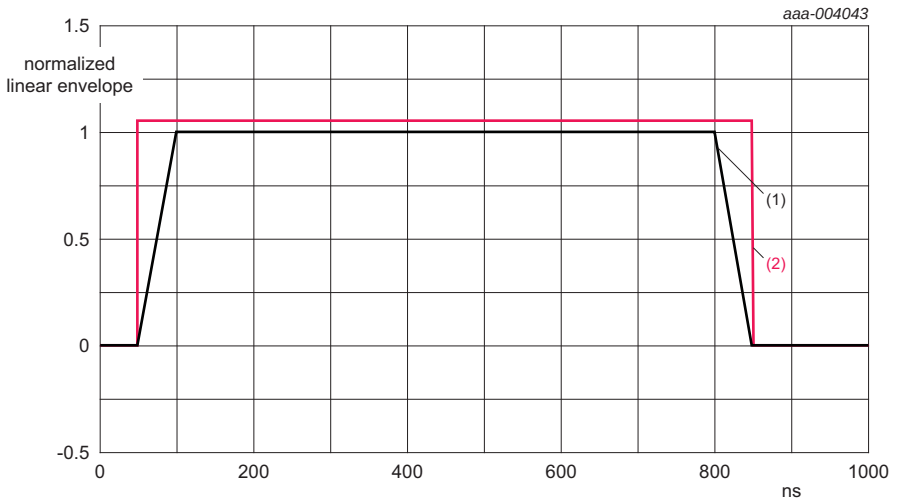
IFF transponders have several different timing schemes but the basic building blocks are of short, high-powered pulses that operate at low long-term duty cycles <10 %. The presence and timing of these pulses are known, as they are generated by the IFF system in response either to a received request or an initiation by the pilot. As information about these pulses is known, a transponder system can generate a trigger that could “gate” or “window” the voltage that is used to bias the transistor. The term “window” is used here to avoid confusion with the term “gate voltage” which is used later.

The described approach deals with enhancement mode Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistors but this technique can be used for both depletion and enhancement mode FETs.

3. Requirements

The minimum pulse width used in IFF systems is 0.8 μs and with spectral mask concerns there are finite rise and fall times formed on the edges of the pulsed RF waveform. These rise and fall times are in the order of 50 ns at either end of the pulse. To maximize the benefit of the gated bias voltage, if possible, gate each pulse as tightly as possible with respect to the edges of the RF pulse itself.

In reality, the circuitry needs time to accept a signal and set up a stable voltage on the transistor gate. For this implementation the “Window” around the bias control is set up and reaches steady state in maximum 75 ns from when the control signal is detected; see Figure 1.



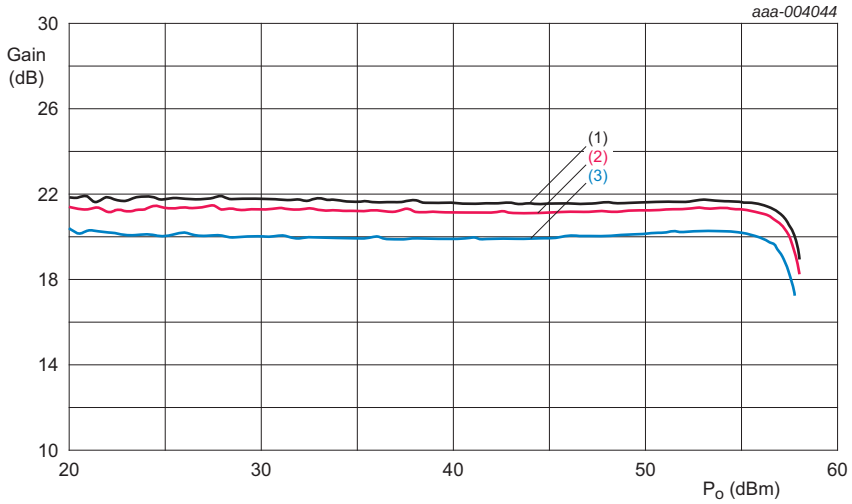
(1) RF envelope.

(2) Bias gate.

Fig 1. Ideal bias voltage gate timing; basic pulse shape 50 ns rise and fall times

4. LDMOS Bias conditions

LDMOS transistors are enhancement mode devices which require a positive voltage on the gate of the device in order to bias them. High-power amplifier transistors are considered here as they benefit most from windowing the gate voltage, but there are benefits to gating each device in the amplifier chain. Consider the BLA6H0912-500 which is a 500 W LDMOS device that can be biased as a linear amplifier giving the response shown in Figure 2.



(1) 4 °C.

(2) 22 °C.

(3) 80 °C.

Amplifier biased to 3 A minimum, 35 dB dynamic range; V_{DD} = 48 V; pulse 1µs, 2 %.

Fig 2. BLA6H0912-500 linear response

In order to get a wide dynamic range from a device with this power capability, a quiescent current (I_{Dq}) of 3 A is needed. The BLA6H0912-500 utilizes NXP Semiconductor high-voltage LDMOS technology, with a drain voltage (V_{DS}) of 50 V which results in 150 W of quiescent power required before there is any RF “work” done.

If we assume that $\theta_{(j-c)}$ taken from data sheet BLA6H0912-500 for a 2400 µs pulse is basically DC (or equal to the thermal time constant of the device) then the rise in junction temperature for this static DC condition is 30 °C. If this constant bias is reduced, the junction temperature is lower which causes an increase in MTF based on the curve in Figure 3. In the case where this assumption is not valid, the situation becomes more troublesome as $\theta_{(j-c)}$ increases and higher junction temperatures occur, further highlighting the need for some dynamic control of the gate voltage.

Table 1. BLA6H0912-500 thermal impedance data

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 450 W		
		t_p = 32 µs; δ = 2 %	0.03	K/W
		t_p = 128 µs; δ = 10 %	0.08	K/W
		t_p = 2400 µs; δ = 6.4 %	0.2	K/W

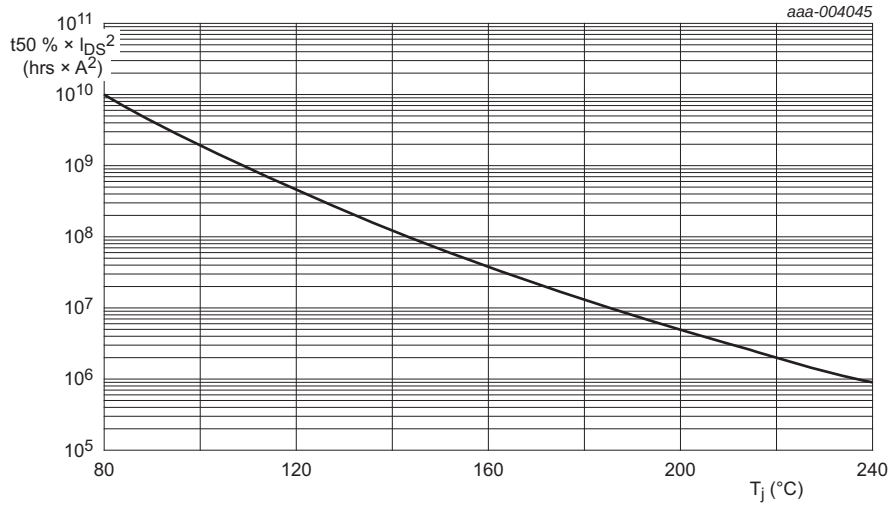


Fig 3. MTF data BLA6H0912-500

IFF waveforms have very low duty cycles in the order of 2 %. In this case the ideal power reduction using this windowing technique, given square pulses and zero setup and hold times, would result in the quiescent power consumption being:

$150 \times 0.02 = 3\ W_{AVG}$

The DC θ_{jc} is not used here but the lower pulsed value of 0.03 K/W taken from the data sheet BLA6H0912-500 is used and the resulting temperature is:

$T_{rise} = 3 \times 0.03 = 0.1\ °C$

This bias voltage is usually supplied from a low impedance bias controller similar to that described in NXP Semiconductors *Report R_10032: LDMOS bias module CA-330-11*. This bias voltage is commonly fed to the device through a shorted quarter wave section line that has been optimized for the design frequency. This bias line is an obvious location to insert the switch, which will either apply the proper gate voltage to the transistor, or pull it to ground through a resistor to drain the gate voltage on the falling edge.

5. Switch circuit

There are many fast switches on the market today that can meet the requirement of both switching and being stable within 75 ns. An analog switch, the Vishay DG4599 with a minimum switching speed of 30 ns was chosen which allows the switch to react fast enough for any conditioning if necessary.

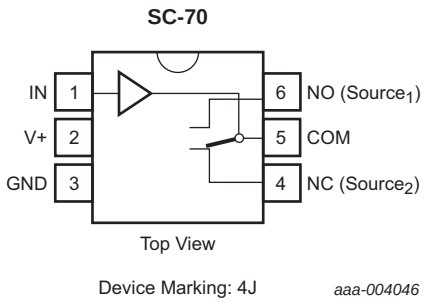


Fig 4. Analog switch Vishay DG4599

Table 2. Truth table

Logic	NC	NO
0[1]	ON	OFF
1[2]	OFF	ON

[1] Logic “0” ≤ 0.8 V

[2] Logic “1” ≥ 2.4 V.

The Vishay DG4599 accepts a TTL waveform as defined in Table 2 (taken from the data sheet DG4599). It requires a single 5 V supply and has a very low current draw of 1 μA. A simple solution to power this switch is to apply the 8 V regulator voltage on the LDMOS bias module R_10032 to a high impedance resistor divider to generate the required voltage.

Figure 5 shows the schematic diagram of the switching circuit. When a logic 1 is received, the switch presents the transistor with the correct bias voltage generated by the LDMOS bias module. When a logic 0 is received, the switch presents a 1.5 Ω impedance to the bias network to drain the voltage on the gate of the transistor. If the TTL signal is removed and the input is left floating, a 10 kΩ pull-down resistor (R3) ensures that the amplifier is not biased.

Alternatively if the failure condition was that the amplifier remained in the “on” mode, R3 could be pulled up to the V_{DD} of the switch. This would result in an increased junction temperature as earlier mentioned, but if this were a military application that failure mode would be preferable, considering that an incorrect response could instigate a missile launch.

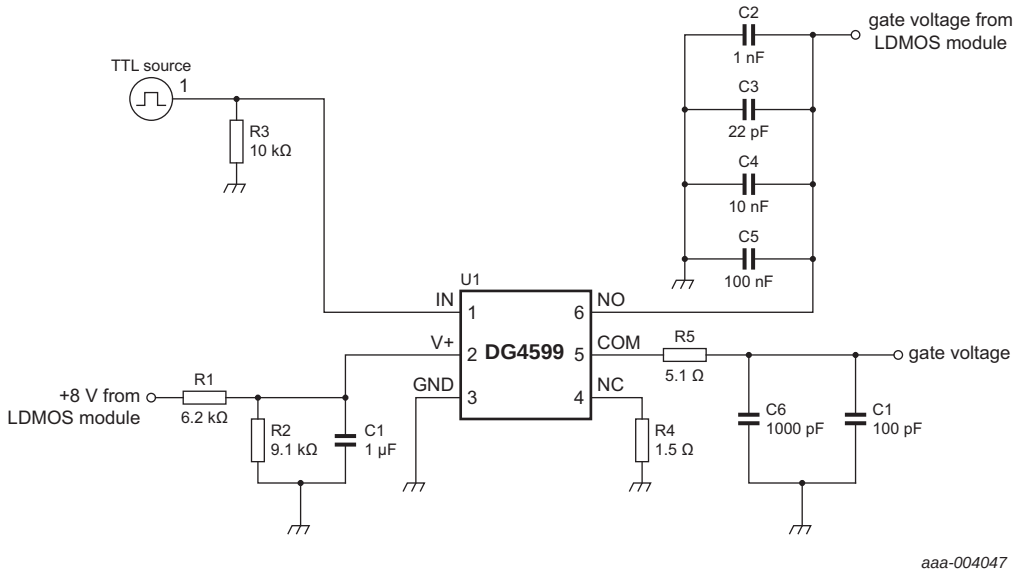
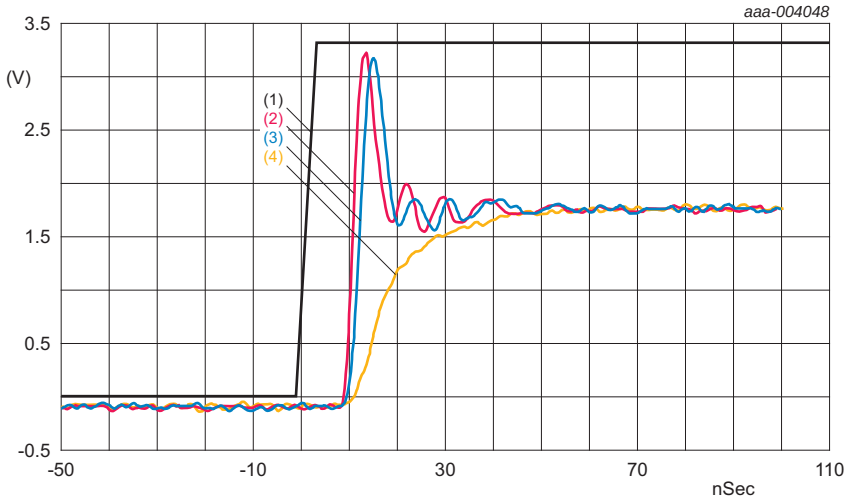


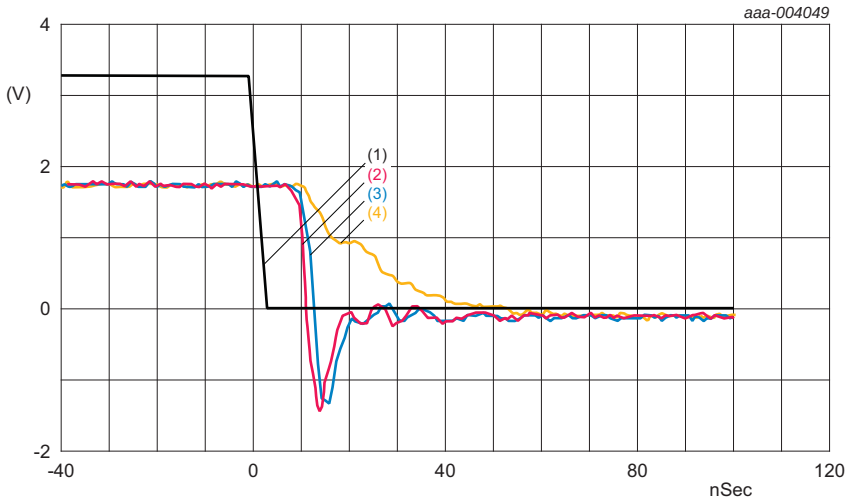
Fig 5. Gate voltage switching circuit

Figure 6 and Figure 7 show the respective results for the rising and falling edges during circuit testing. It can be seen that the switch turns on within 10 ns of receiving the control input and has an overshoot due to the fast switching time and inductance of the bias feed lines. Capacitor C1 provides the 100 pF gate bias decoupling required for proper RF operation and has a minimal effect on the ringing caused by the fast switching. Damped responses such as this are never ideal so capacitor C6 (1000 pF) is added to the bias line on the switch side of capacitor C1 to smooth the response. The final switching time is approximately 60 ns which presents a stable V_{GS} to the amplifier and does not add gate bias modulation onto the RF pulse.



(1) Trigger.
(2) No capacitors.
(3) 100 pF.
(4) 1100 pF.

Fig 6. Rising edge timing

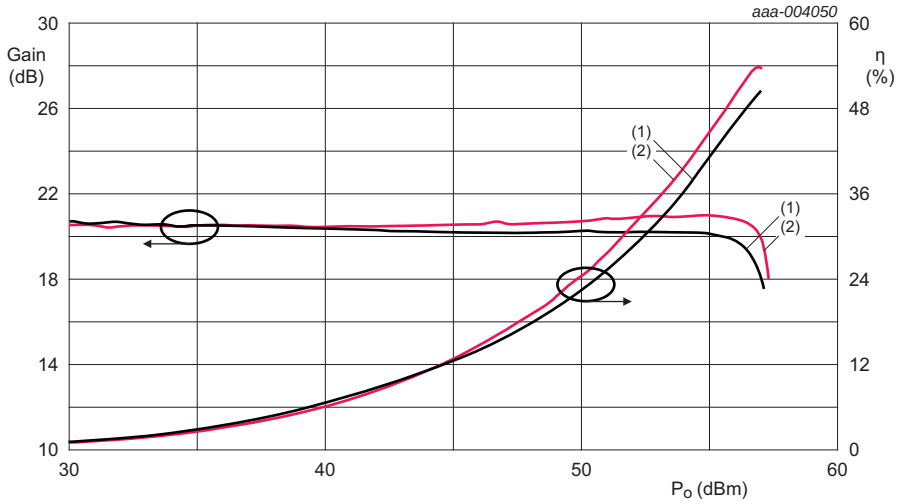


(1) Trigger.
(2) No capacitors.
(3) 100 pF.
(4) 1100 pF.

Fig 7. Falling edge timing

Figure 8 shows the measured response of the circuit with and without the gate circuit being gated. The windowed gate response provides 3 % more efficiency than the constant bias condition and approximately 25 W more power. The measured flange temperature for the constant bias condition with a cold plate temperature of 24 °C was 60 °C and the

flange temperature for the windowed bias case was 25 °C. Many military applications have an ambient temperature requirement of +85 °C and this 35 °C difference results in an MTF of $4e^8$ versus $6e^9$: a reduction factor of 15 times in device lifetime.

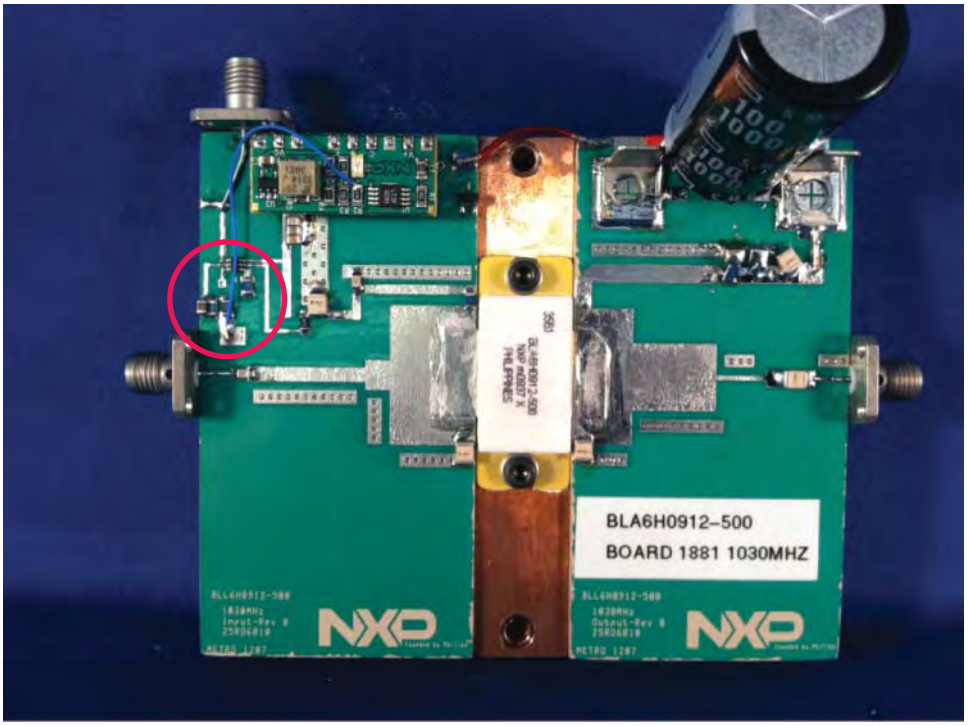


(1) Constant bias.

(2) Pulsed bias.

V_{DD} = 48 V; pulse 1μs, 2 %.

Fig 8. Windowed gate voltage as a function of constant bias performance



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Small switching circuit circled in red.

Fig 9. BLA6H0912-500 test circuit with switched bias control

6. Conclusion

Modern IFF systems require amplifiers with high linearity and high output power greater than 1 kW. In order to improve both reliability and dynamic range, a switch can be used to “window” the gate voltage of the transistor making the amplifier more efficient, providing a high dynamic range and reducing junction temperatures. Ultimately this leads to better reliability at higher output powers. Any system that can detect when a signal will be sent and operates at lower duty cycles can use this technique. There is an added benefit when this technique is used in pulsed radar applications. In modern radars, windowing the transmit power amplifiers during a receive operation can reduce the thermal noise that leaks through the duplexer into the receive path which would otherwise reduce the signal to noise ratio and limit the sensitivity of the system.

7. Abbreviations

Table 3. Abbreviations

Acronym	Description
IFF	Identification Friend or Foe
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Modulation Transfer Function
TTL	Transistor-Transistor Logic

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