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NTAG I²C demo application for Android

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Application note
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Document information

Info	Content
Keywords	NTAG I ² C, Android, NFC tag
Abstract	This Application note aims at describing the functionalities behind the Android App of the NTAG I ² C.



Revision history

Rev	Date	Description
1.0	20141006	Initial release of technical description

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1. Object

The objective of the document is to explain how to use the NTAG I²C App developed by NXP Semiconductors.

There are two distinctive purposes behind the NTAG I²C App:

The Demonstration purpose, to interact with the NTAG I²C demonstration boards and demonstrate the features behind the NTAG I²C.

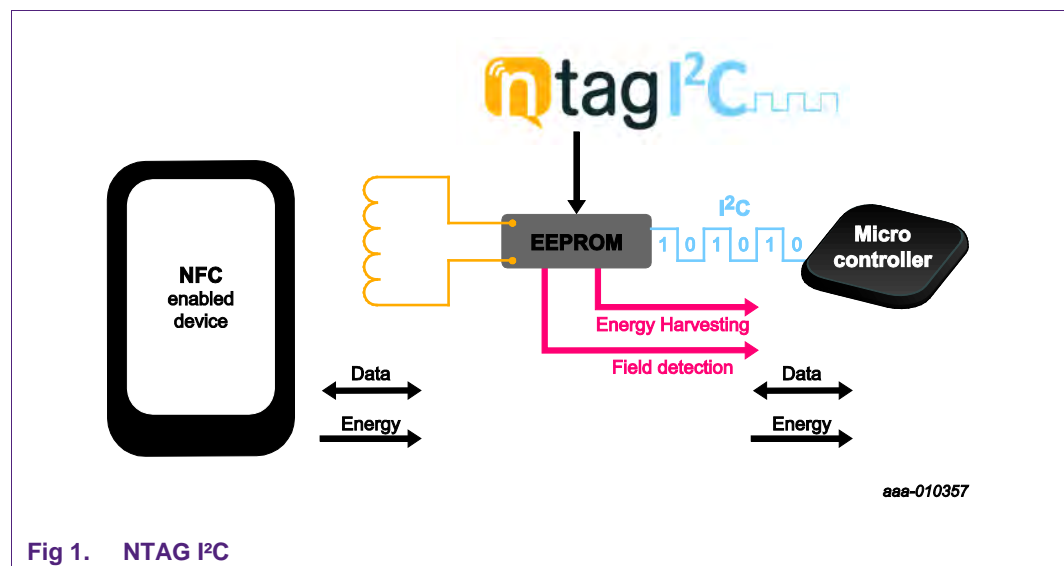
The Configuration purpose, to read or write configuration of the NTAG I²C chip (without necessarily any demo boards but at least with an antenna connected to the NTAG I²C).

Technical aspects related to the IC functioning (i.e. the configuration registers) are out of scope of this document. In order to get further technical details please consult the dedicated data sheet of the NTAG I²C – see the Appendix.

2. NTAG I²C introduction

The NTAG I²C is the first product of NXP’s NTAG family offering both contactless and contact interfaces. In addition to the passive NFC Forum compliant RF interface, the NTAG I²C product provides an I²C interface that allows the IC to communicate with the microcontroller when the chip is powered by an external device, i.e. a mobile phone.

The NTAG I²C operating in energy harvesting mode provides the possibility to supply external low power devices (e.g. microcontrollers) with the energy generated from the RF field of the external NFC device.



The NTAG I²C product has 2 types of memories.

1. EEPROM memory compliant with the NFC Forum type 2 Tag implementation.
2. 64-byte SRAM memory which is mapped within the EEPROM memory and is externally powered.

The NTAG I²C IC features a Pass-Through mode that allows fast download and upload of data from the RF interface to the I²C interface and vice versa. This functionality makes use of the SRAM memory that allows fast data transfer between interfaces without the EEPROM performance limitations.

NXP Semiconductors provides the NTAG I²C product in two different versions

1. NTAG I²C 1K version with 888 bytes freely available in the user memory
2. NTAG I²C 2K version with 1904 bytes freely available in the user memory

In addition to the I²C interface functionality, the NTAG I²C product features a Field Detection Pin for waking up the host connected devices or synchronize the data transfer between the 2 interfaces.

3. Hardware components

The NTAG I²C Android App is meant to be working with the NTAG I²C Explorer board, and an adjacent PCB or flex antennas to test all the features and functionalities the NTAG I²C is offering.

The below picture is a view of the NTAG I²C Explorer board and the Class 4 PCB antenna.

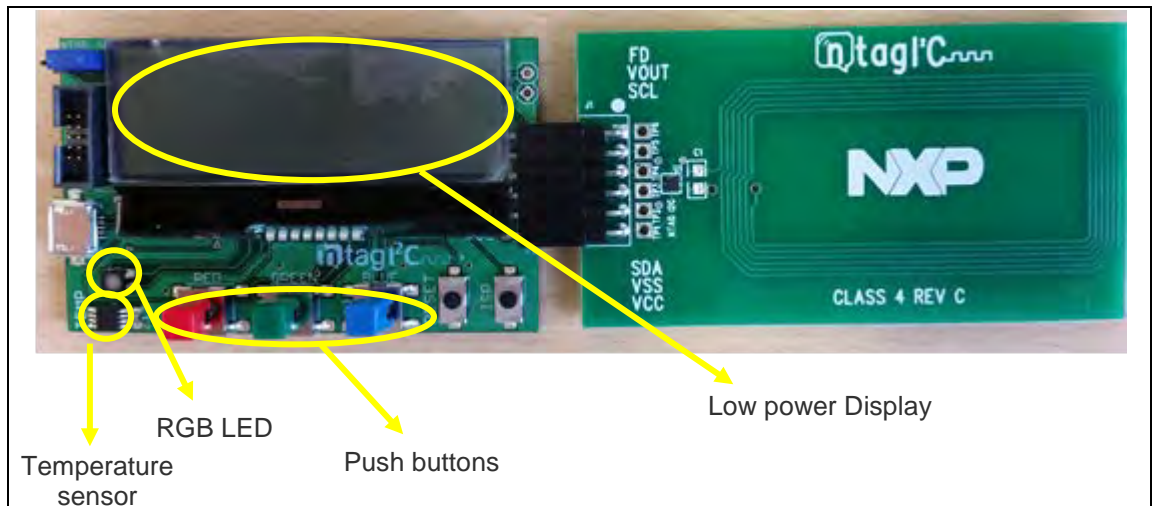


Fig 2. NTAG I²C Explorer board + PCB Class 4 antenna

The NTAG I²C Explorer board contains an NXP microcontroller (LPC11U24 Cortex-M0), a RGB LED and RGB push button as well as an NXP temperature sensor (PCT 2075) and an LCD screen to show the messages coming from the NTAG and the application.

The Android application, called NTAG I²C Demo, can be found and freely downloaded from the Google Play Store. This document applies to the NTAG I²C Demoboard application version 1.5 and above. The Android application is intended to operate on devices running Android version 4.0 and beyond. The application has been optimized for a correct visioning of the graphical elements in smartphones featuring different resolutions.

This Android application does also support the simple LED demonstration board with no display.

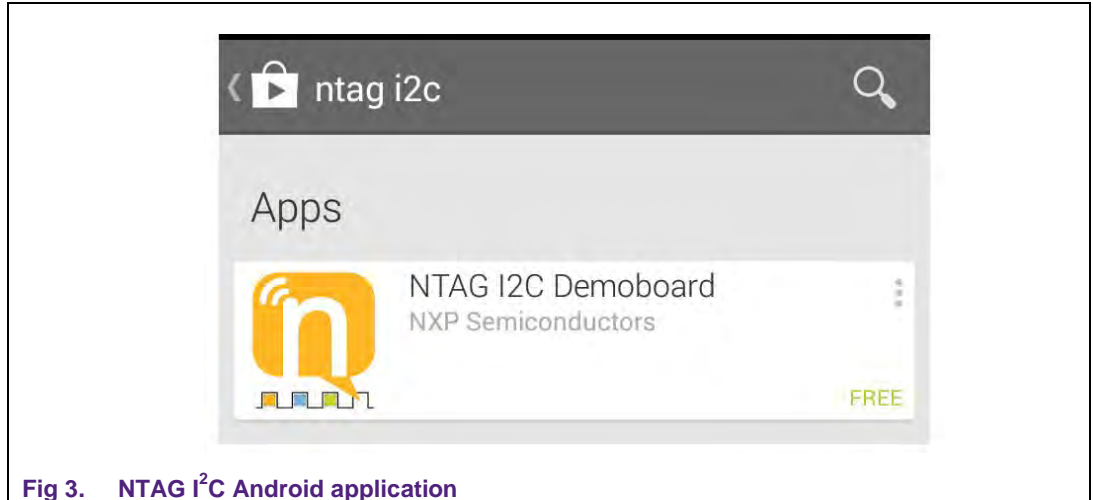


Fig 3. NTAG I²C Android application

4. NTAG I²C application

4.1 Splash window

The Splash window is the first activity to be displayed when the application is launched. This window will be automatically closed after 2 seconds.



Fig 4. Splash window

4.2 Functionalities structure

As it can be observed in Fig. 5, the application consists of four main tabs that can be launched from the main activity of the application and four additional sub tabs that are accessed from the Config tabs.

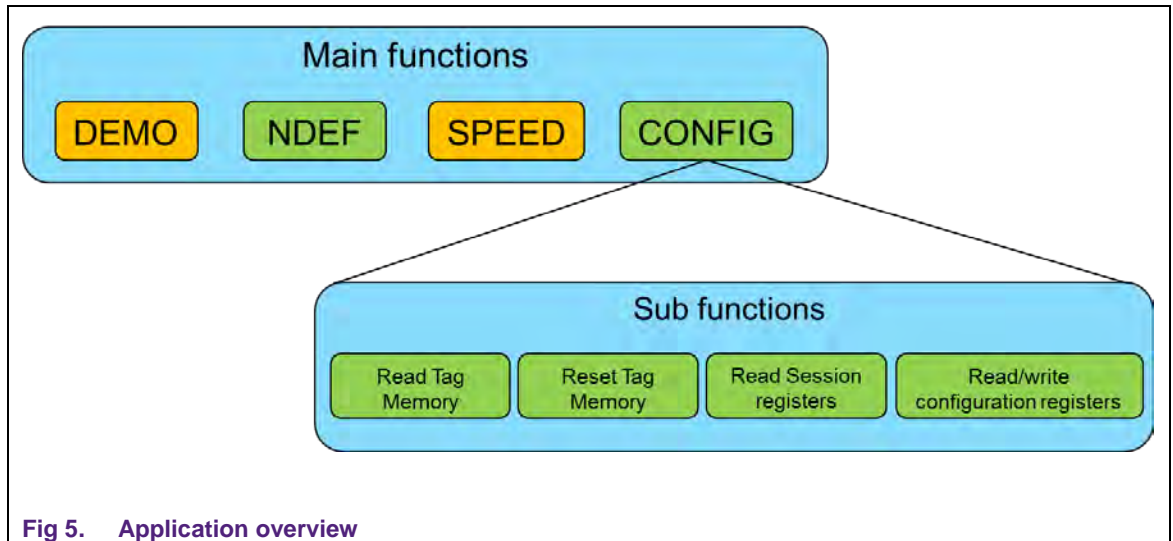


Fig 5. Application overview

5. DEMONSTRATION part

5.1 DEMO tab

Please see Fig. 6 for a snapshot of the demo section.

In this section, the user can change dynamically the color of the LED of the board by changing it in the application, and can see on the screen which push buttons are pressed on the board. The temperature and voltage measured by the board are on top displayed on both the display of the board and on the screen of the NFC device.

This section allows demonstrating:

- The Energy harvesting functionality of NTAG I²C IC that enables to power up the complete explorer board with the energy harvested from the RF interface without any battery.
- The RF to I²C communication by enabling to modify the LED color by pressing the right color on the NFC device screen
- The I²C to RF communication as the set of push buttons pressed by the user on the explorer board gets reflected on the NFC device screen
- The dynamic bi directional communication between the 2 interfaces as the temperature value as well as the Voltage on the Energy harvesting pin get dynamically updated on both the low power screen and the NFC device screen

The firmware version of the board can be seen on the information button on the upper-right corner of the application. Note that, as the firmware version of the board is shared with the application when the DEMO is performed, it will not be known to the application until this demo has been executed at least one time.

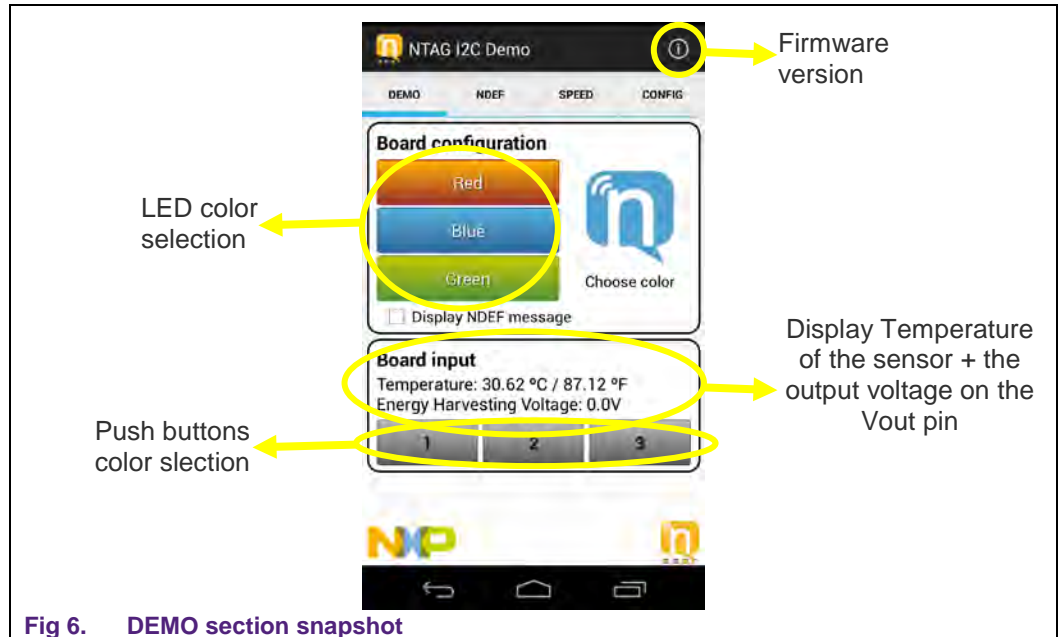


Fig 6. DEMO section snapshot

Additionally when tapping on the “i” at the top of the tab, one can use the App to get the version being used for the board design, firmware of the board and the Android App by tapping the board with the NFC enabled device – see Fig. 7 for a snapshot example.

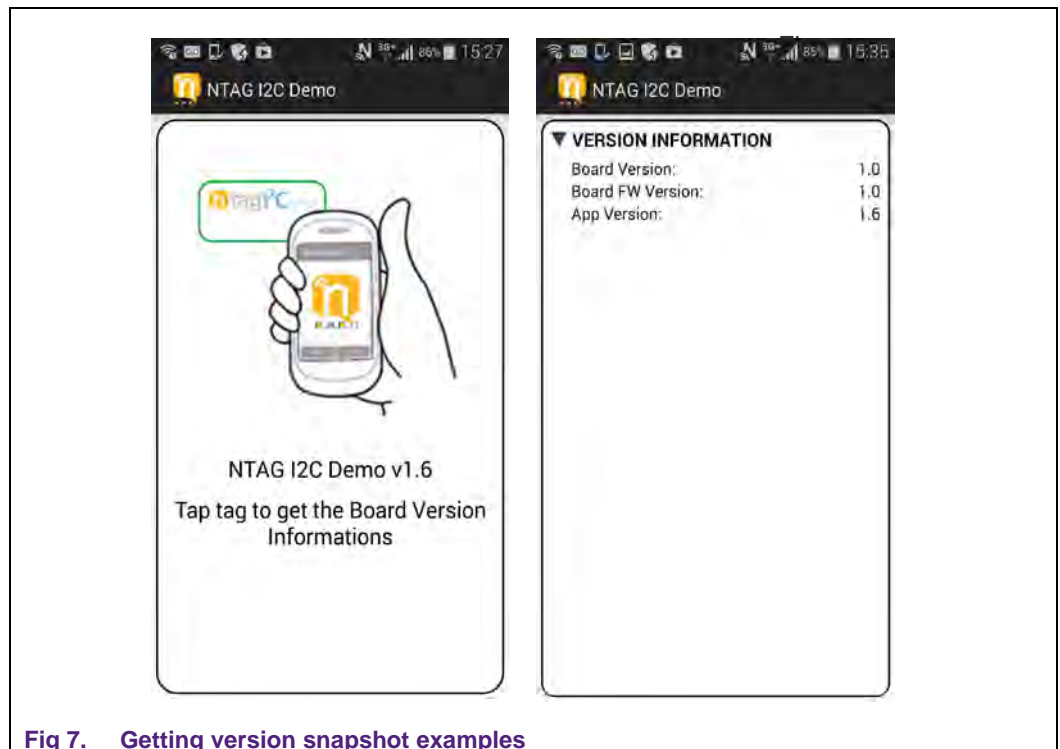


Fig 7. Getting version snapshot examples

5.2 SPEED tab

The SPEED section is about measuring the speed of data transfer when using the SRAM buffer to exchange data with the Microcontroller and the NFC device (SRAM selection) or when writing data to the EEPROM (EEPROM selection). See Fig. 8 for the snapshot of the Speed tab and Fig. 9 for the concept behind this tap.

The amount of data has to be selected first (with a 64bytes granularity to match the SRAM buffer size, 20 blocks value being the default one) and then the configuration of the data transfer (SRAM or EEPROM).

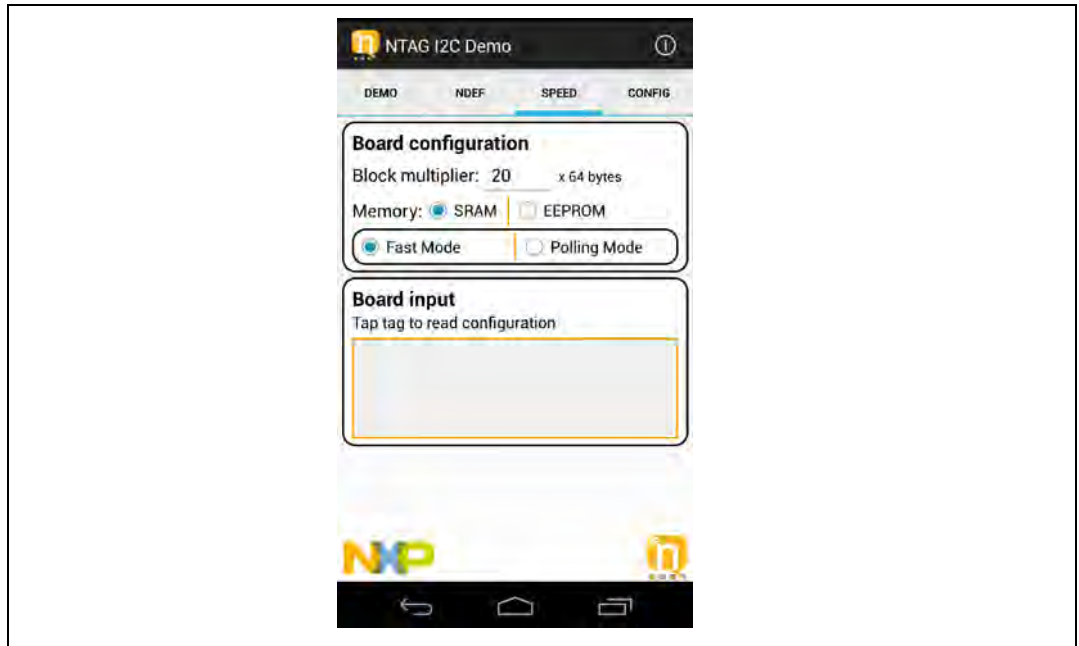


Fig 8. SPEED section snapshot

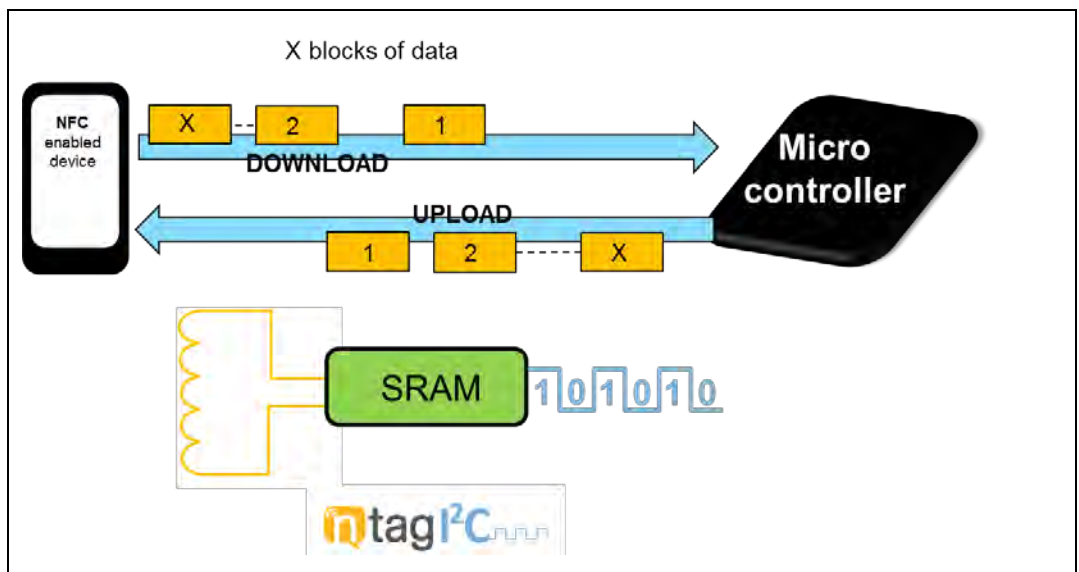


Fig 9. Data transfer speed measurement concept behind the SRAM selection

SRAM Selection

The SRAM Speed Test measures the speed at which the data is transferred from the application to the microcontroller through the SRAM memory (with the NTAG I²C in Pass-Through mode), and vice versa.

First, the application writes to the SRAM several times, and the microcontroller reads from it. Then once all the data has been transmitted from the NFC interface, the microcontroller starts writing to the SRAM memory the same amount of data, while the NFC interface reads from it.

The SRAM Speed Test can be run in two different modes: Fast Mode and Polling Mode:

- in Polling Mode the application checks if the transferred data has been read by the MCU before transferring a new block (from NFC to I²C) or checks if the MCU has written the new information before reading from the NFC interface the SRAM block (from I²C to NFC) by checking the appropriate session registers of the NTAG I²C.
- In Fast Mode the data is written and read to the NTAG as fast as the READ or WRITE command is performed, one block of data after the other

Typically the Fast Mode method will always return higher bit rates than the Polling Mode method due to the additional polling checks on the session registers.

The integrity of the data transferred in both directions is checked by appending a CRC32 value in the last block. The CRC32 is calculated for the whole message that has been transferred (for all the blocks). If the CRC32 from the message received by the application is right, it will show an "Integrity of the data: OK" message. Additionally, if the CRC32 from the message received by the board is right, it will also turn on the green LED at the end of the Speed Test on the Explorer board.

EEPROM selection

With the EEPROM selection, one can measure the speed at which the application is able to write and read to the EEPROM memory of the NTAG I²C.

The application creates first the NDEF message to be written by creating a string that contains the content from the textbox as many times as indicated, and adding the appropriate header. Then, it writes it to the EEPROM memory by sending as many NFC Forum standard type-2-tag Write commands as necessary, and measuring the time it takes to do so. Once it has finished writing, it reads the NDEF message by sending as many NFC Forum type-2-tag Read commands as necessary.

Once the test is finished, the application shows the number of bytes, mean speed and time for both the reading and writing process. The user can also check the content of the memory to ensure that the NDEF message has been written appropriately.

6. CONFIGURATION PART

6.1 NDEF Section

See Fig. 7 for a snapshot of the NDEF section.

The NDEF section allows the user to read or write any NDEF message to the NTAG I²C (it could be used to read or write an NDEF message to any NFC Forum type 2 tag).

On the Read NDEF mode, the application reads the NDEF message from the NTAG and returns its content and the type of NDEF message. This can be done by tapping the NTAG, or by pressing the Read NDEF button when the NTAG is in proximity.

On the Write NDEF mode, the application allows the user to write 3 types of information into the tag: simple text (“Text”), URI information (“URI”), or Bluetooth pairing type NDEF message (“BTpair”):

- Simple text will be to write text in ASCII such as “Hello World”
- URI information will be NDEF messages allowing the tag to trigger actions on the NFC device in one tap such as opening a webpage or sending an SMS message.
- Bluetooth pairing NDEF message allows the smartphone to be paired with a Bluetooth device by just tapping the tag.

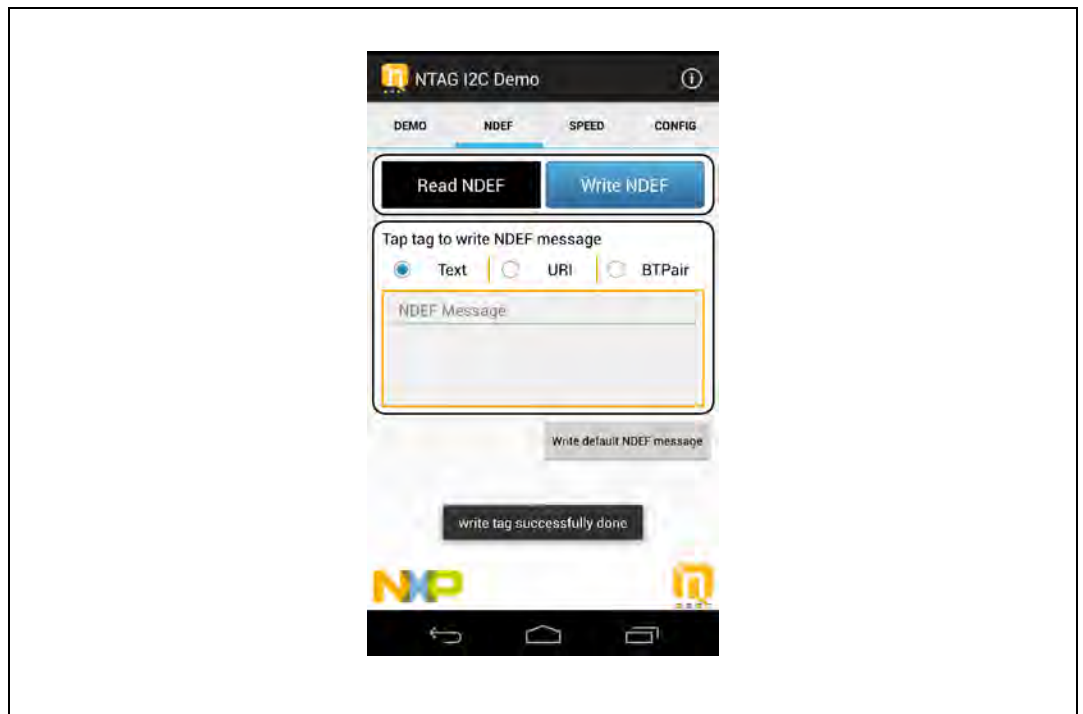


Fig 10. NDEF section snapshot

The NDEF Demo also contains a “Write default NDEF message” button. This button jumps to the Write NDEF mode, text type, and writes automatically the text “NTAG I2C EXPLORER” that gets displayed by default by the low power display.

When the NDEF message has been successfully written the “write tag successfully done” popup appears temporarily in the application informing the user that the message has been correctly written. There is no need to tap again the tag if the user wants to write multiple NDEF messages and read them in between.

In order to know more about the different types of NDEF messages and their related structure, please refer to the NFC Forum specification (see appendix).

How to display text on the LCD screen

Once a text message has been successfully written to the NTAG I²C chip, it is possible to have this message on the LCD screen of the board by enabling the “Display NDEF message” checkbox in the DEMO tab (see snapshot fig. 6) either before or after writing the message.

6.2 CONFIG section

See fig. 10 for the snapshot of the Config section.

This section shows a selection menu that provides access to the different configuration activities of NTAG I²C supported by the application.

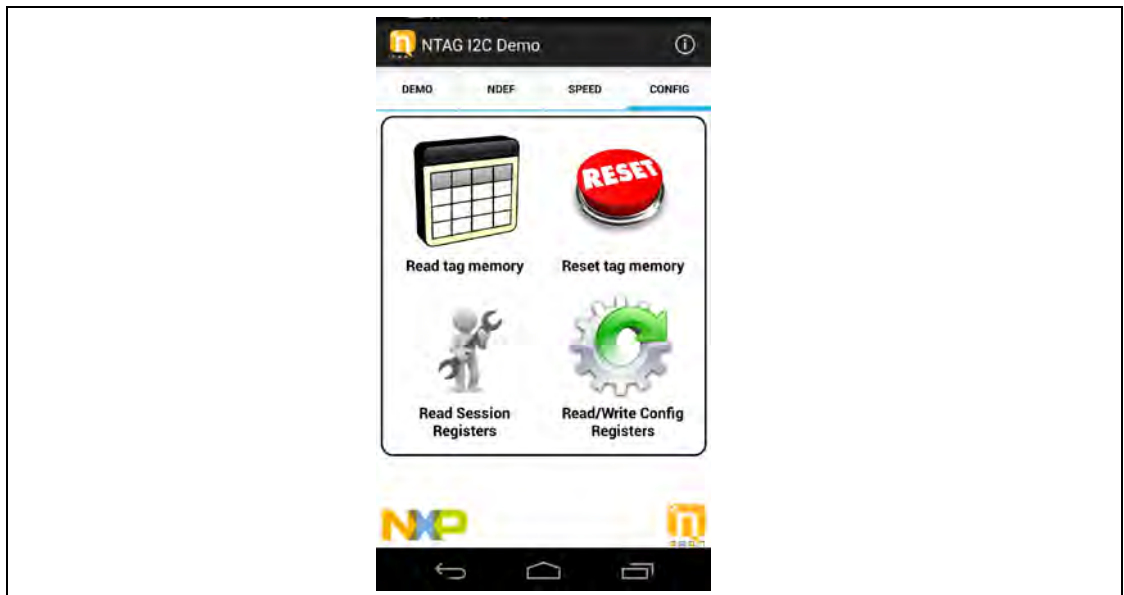


Fig 11. Configuration Section snapshot

6.2.1 Read tag memory

This activity reads and displays on the screen the content of the whole memory of the NTAG I²C product. The complete content can be scrolled on the screen. See Fig. 11 for an example of a snapshot of such memory reading.

The user should tap the NTAG I²C product for some time (about 2 or 3 seconds) to read the memory content. A dialog is displayed on the screen while the operation goes on.

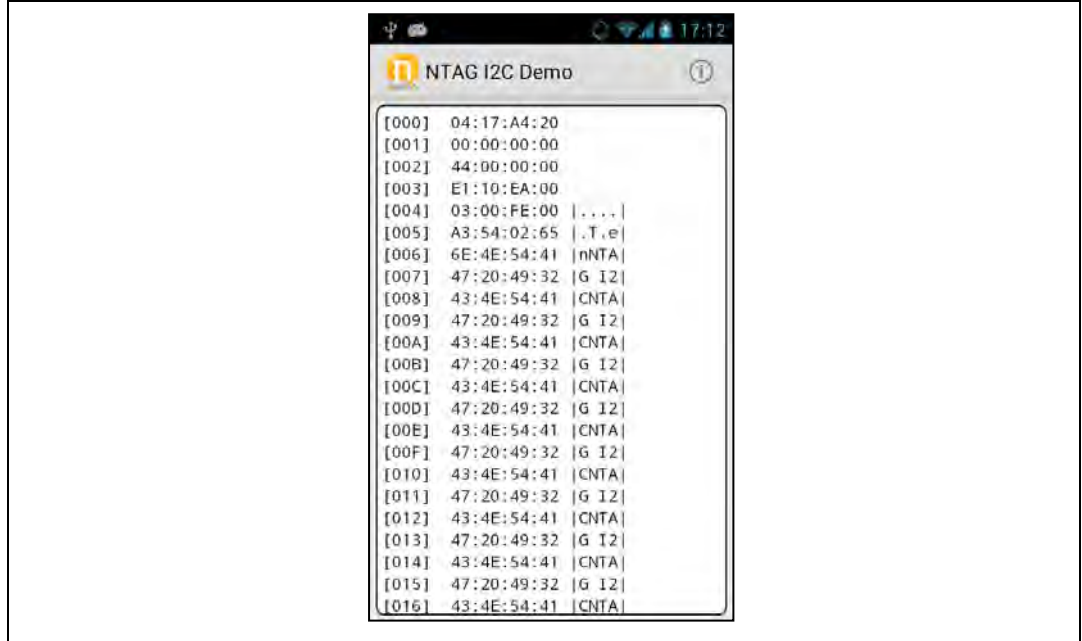


Fig 12. Read Tag Memory screenshot example

6.2.2 Reset tag Memory

This configuration functionality is about resetting the whole user memory of the NTAG I2C product to the original content that was programmed during production. This means setting the fifth page of the EEPROM memory to a known value (an empty NDEF message) and the rest of the memory to zero (the first four pages do not belong to the user memory). This way, the NTAG I2C is ready for an NDEF message to be written on it.

See Fig. 12 for a screenshot after a successful reset of the memory.

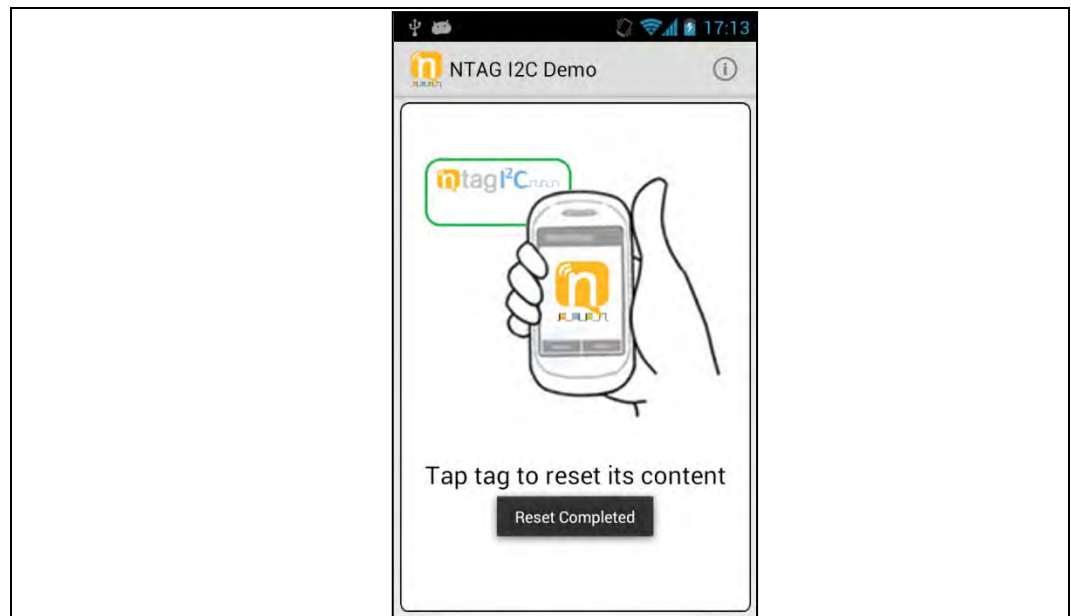


Fig 13. Reset Tag Memory screenshot example

The user should tap the NTAG I²C product for about 2 or 3 seconds to reset the memory content. A “reset completed” message will be displayed once the reset has been fully performed.

6.2.3 Read Session Registers

This activity displays the content of the session registers in the NTAG I²C. Session registers are used to configure or monitor the registers values of the current communication session. Session registers values can be modified within a particular communication session (only via the I²C interface, so the application is not able to modify them). However, after a Power-On Reset, these values go back to their default configuration values, which are obtained from the configuration registers.

Session registers values can be read at pages F8h to F9h (sector 3) via the RF interface, or at block FEh via the I²C interface.

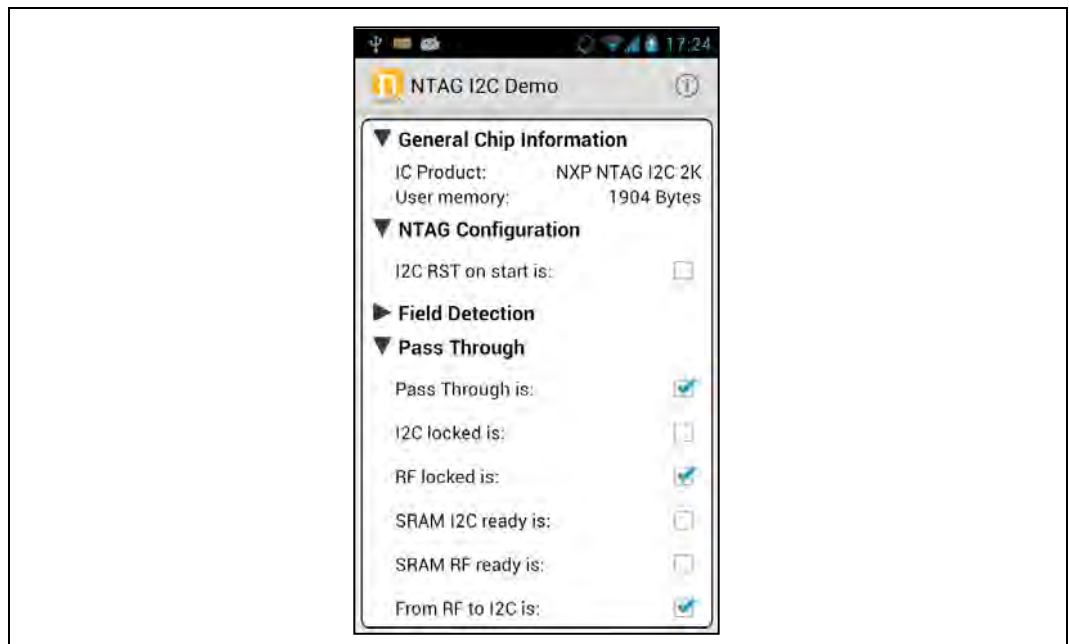


Fig 14. Read session register screenshot example

Session Registers values are displayed on the screen divided into different groups:

- **General Chip Information:** displays general information about the discovered NTAG I²C product. It shows the following information:
 - **IC Product:** NTAG I²C chip version (1K or 2K)
 - **User memory:** size of the user memory of the NTAG I²C chip
- **NTAG Configuration:** displays general NTAG configuration information:
 - **I2C RST on start is:** shows the content of the I2C_RST_ON_OFF bit, which is responsible for enabling a soft reset through an I²C repeated start.
- **Field Detection:** displays information related to the field detection functionality, which is used for the smart pairing with devices, as it triggers a signal to the connected host when the NTAG I²C product is powered by an external NFC device.

- **FD_OFF is:** shows the content of the FD_OFF bits, which define the event upon which the signal output on the field detection pin is brought up.
- **FD_ON is:** shows the content of the FD_ON bits, which define the event upon which the signal output on the field detection pin is brought down.
- **Last NDEF Block is:** shows the content of the LAST_NDEF_BLOCK byte, this is, the address of the last block (I²C interface addressing) of the NDEF message.
- **NDEF Data Read is:** shows the content of the NDEF_DATA_READ bit.
- **RF field present is:** shows the content of the RF_FIELD_PRESENT bit, which indicates if an RF field is detected.
- **Pass Through:** displays information related to the pass-through functionality, which allows the fast transfer of data between the RF and the I²C interface by using a 64 byte SRAM memory:
 - **Pass Through is:** shows the content of the PTHRU_ON_OFF bit, which is responsible for enabling the data transfer via the SRAM memory.
 - **I2C locked is:** shows the content of the I2C_LOCKED bit, which can lock the access to memory to the I2C interface.
 - **RF locked is:** shows the content of the RF_LOCKED bit, which can lock the access to memory to the RF interface.
 - **SRAM I2C ready is:** shows the content of the SRAM_I2C_READY bit, which indicates if the data in the SRAM memory is ready to be read by the I2C interface.
 - **SRAM RF ready is:** shows the content of the SRAM_RF_READY bit, which indicates if the data in the SRAM memory is ready to be read by the RF interface.
 - **From RF to I2C is:** shows the content of the PTHRU_DIR bit, which defines the data flow direction for the data transfer.
- **SRAM Memory Settings:** displays information about the SRAM mirroring feature. The SRAM memory can be mirrored in the User memory for RF access by enabling the SRAM Mirroring feature.
 - **SRAM Mirror is:** shows the content of the SRAM_MIRROR_ON_OFF bit.
 - **SRAM Mirror block is:** shows the content of the SRAM_MIRROR_BLOCK byte, which indicates the address of the first block (I2C interface addressing) of the mirror of SRAM memory.
- **I²C Settings:** Information about the I²C management configuration:
 - **WD_LS Timer is:** shows the content of the WDT_LS byte: the LSB of the watchdog time control register.
 - **WD_MSTimer is:** shows the content of the WDT_MS byte: the MSB of the watchdog time control register.
 - **I2C Clock stretch is:** shows the content of the I2C_CLOCK_STR bit, which is responsible for enabling the I2C clock stretching.

For further information about the session registers bytes please refer to the NTAG I²C product Datasheet – see appendix section.

6.2.4 Read/Write Config Registers

This configuration functionality displays the content of the configuration registers of the NTAG I²C, allowing to the user to change their values. Configuration registers define the default configuration of the NTAG I²C to be used for the communication after a Power-On Reset.

Configuration registers values can be read and written at pages E8h to E9h (sector 1) via the RF interface, or at block 78h via the I²C interface. The user can read or write the content of those registers by first selecting the Read Config or Write Config buttons and then tapping the NTAG I²C Explorer board.

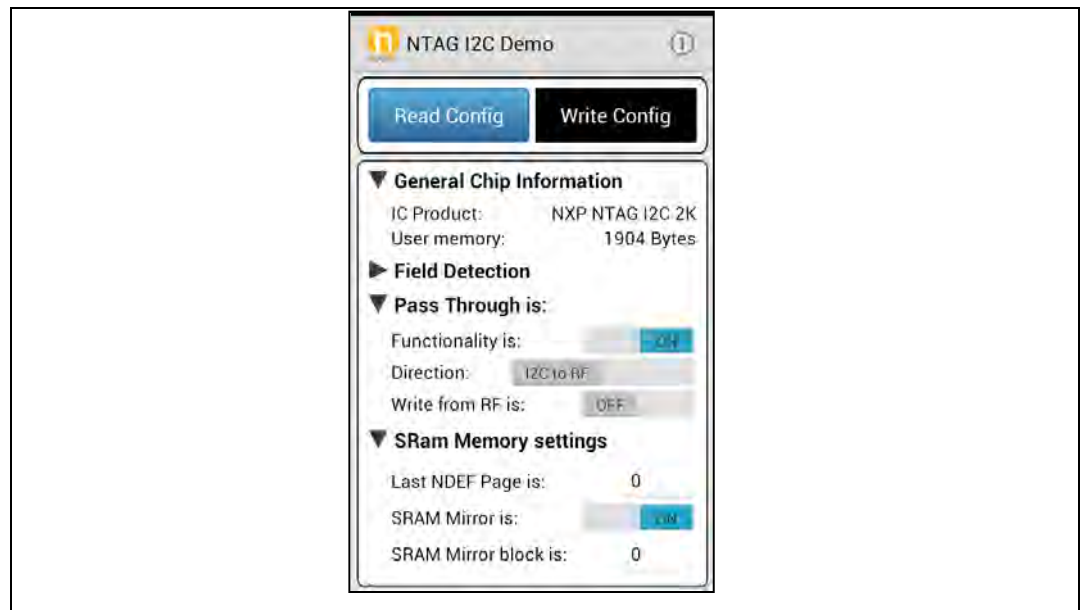


Fig 15. Read/Write Configuration Registers screenshot example

Configuration Registers values displayed on the screen are divided into the following groups:

- **General Chip Information:** displays general information about the discovered NTAG I²C product. It shows the following information:
 - **IC Product:** NTAG I²C chip version (1K or 2K)
 - **User memory:** size of the user memory of the NTAG I²C chip
- **Field Detection:** displays information related to the field detection functionality, which is used for the smart pairing with devices, as it triggers a signal to the connected host when the NTAG I²C product is powered by an external NFC device.
 - **FD_OFF is:** shows the content of the FD_OFF bits, which define the event upon which the signal output on the field detection pin is brought up.
 - **FD_ON is:** shows the content of the FD_ON bits, which define the event upon which the signal output on the field detection pin is brought down.
- **Pass Through:** displays information related to the pass-through functionality, which allows the fast transfer of data between the RF and the I²C interface by using a 64 byte SRAM memory:

- **Direction:** shows the content of the TRANSFER_DIR bit, which defines the data flow direction for the data transfer.
- **Write from RF is:** shows the content of the TRANSFER_DIR bit (same as Direction), which defines the data flow direction for the data transfer.
- **SRAM Memory Settings:** displays information about the SRAM mirroring feature. The SRAM memory can be mirrored in the User memory for RF access by enabling the SRAM Mirroring feature.
 - **Last NDEF Block is:** shows the content of the LAST_NDEF_BLOCK byte, this is, the address of the last block (I2C interface addressing) of the NDEF message.
 - **SRAM Mirror block is:** shows the content of the SRAM_MIRROR_BLOCK byte, which indicates the address of the first block (I2C interface addressing) of the mirror of SRAM memory.
- **I²C Settings:** displays information about the I²C management configuration:
 - **WD_LS Timer is:** shows the content of the WDT_LS byte: the LSB of the watchdog time control register.
 - **WD_MSTimer is:** shows the content of the WDT_MS byte: the MSB of the watchdog time control register.
 - **I2C Clock stretch is:** shows the content of the I2C_CLOCK_STR bit, which is responsible for enabling the I2C clock stretching.
 - **I2C RST on start is:** shows the content of the I2C_RST_ON_OFF bit, which is responsible for enabling a soft reset through an I2C repeated start.

For further information about the configuration registers bytes please refer to the NTAG I²C product Datasheet (see appendix).

7. Appendix

NFC Forum specifications – please refer to:

<http://www.nxp.com/redirect/nfc-forum.org/our-work/specifications-and-application-documents/specifications/nfc-forum-technical-specifications/>

<http://www.nxp.com/redirect/nfc-forum.org/our-work/specifications-and-application-documents/application-documents/>

NTAG I²C datasheet can be found online under:

http://www.nxp.com/documents/data_sheet/NT3H1101_1201.pdf

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9. Contents

1.	Object	3
2.	NTAG I²C introduction	3
3.	Hardware components.....	4
4.	NTAG I²C application	5
4.1	Splash window	5
4.2	Functionalities structure	6
5.	DEMONSTRATION part.....	6
5.1	DEMO tab	6
5.2	SPEED tab	8
6.	CONFIGURATION PART	9
6.1	NDEF Section	9
6.2	CONFIG section.....	11
6.2.1	Read tag memory.....	11
6.2.2	Reset tag Memory.....	12
6.2.3	Read Session Registers.....	13
6.2.4	Read/Write Config Registers.....	15
7.	Appendix.....	16
8.	Legal information	17
8.1	Definitions	17
8.2	Disclaimers.....	17
8.3	Licenses.....	17
8.4	Trademarks.....	17
9.	Contents.....	18

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