Document Number: MPC17531A
Rev. 7.0, 11/2014

700 mA Dual H-Bridge Motor Driver with 3.0 V Compatible Logic I/O

17531A

DUAL H-BRIDGE

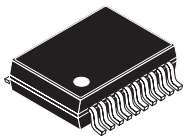
The 17531A is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar step motors and/or brush DC motors (e.g., cameras and disk drive head positioners).

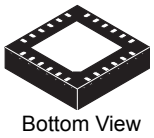
The 17531A operates from 2.0 to 8.6 V using the internal charge pump, with independent control of each H-Bridge, via a parallel MCU interface. The device features built-in shoot-through current protection and an undervoltage shutdown function.

The 17531A has four operating modes: Forward, Reverse, Brake, and Tri-state (high-impedance). The 17531A has a low total $R_{DS(on)}$ of 1.2 Ω (max @ 25 °C).

The 17531A efficiently drives many types of micromotors with low power dissipation owing to its low output resistance and high output slew rates. The H-Bridge outputs can be independently pulse width modulated (PWM'ed) at up to 200 kHz for speed/torque and current control.

This device is powered by SMARTMOS technology.





Bottom View

EV SUFFIX (PB-FREE)
98ASA10616D
20-PIN VMFP

EP SUFFIX (PB-FREE)
98ASA00474D
24-PIN QFN

Features

- Low total $R_{DS(on)}$ 0.8 Ω (Typ), 1.2 Ω (Max) @ 25 °C
- Output current 0.7 A (DC)
- Shoot-through current protection circuit
- PWM control input frequency up to 200 kHz
- Built-in charge pump circuit
- Low power consumption
- Undervoltage detection and shutdown circuit
- Power save mode with current draw ≤ 2.0 μA

ORDERING INFORMATION		
Device (for tape and reel, add an R2 suffix)	**Temperature Range (T_A)**	**Package**
MPC17531ATEP	-20 °C to 65 °C	24 QFN
MPC17531ATEV/EL		20 VMFP

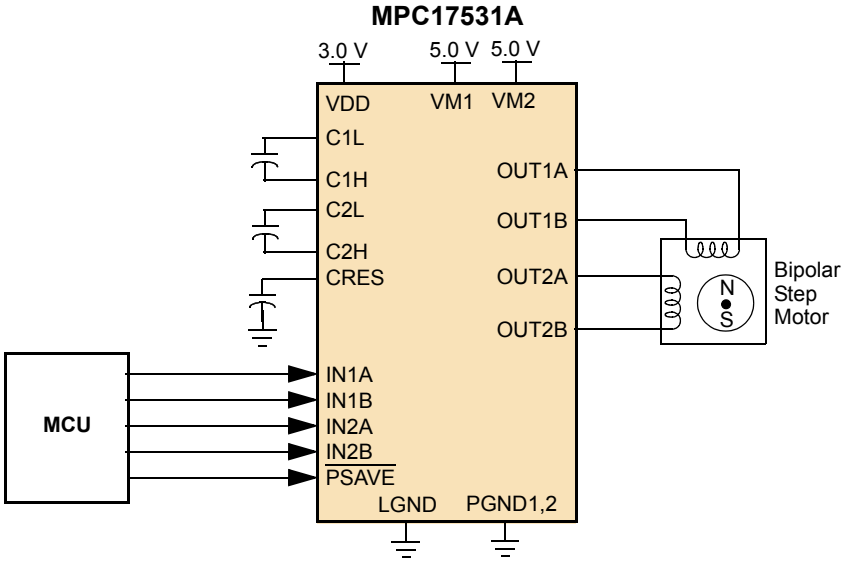


Figure 1. 17531A Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

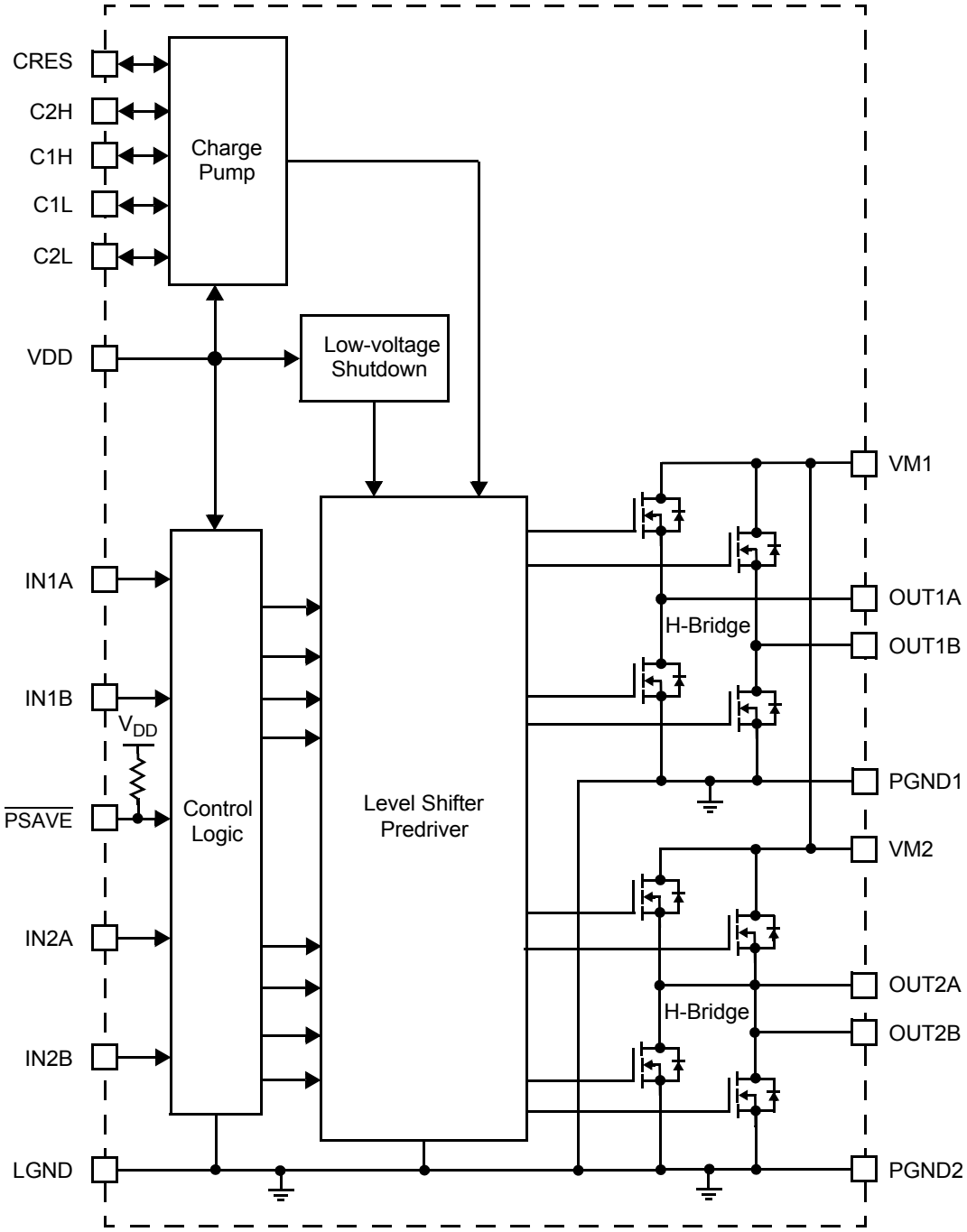


Figure 2. 17531A Simplified Internal Block Diagram

PIN CONNECTIONS

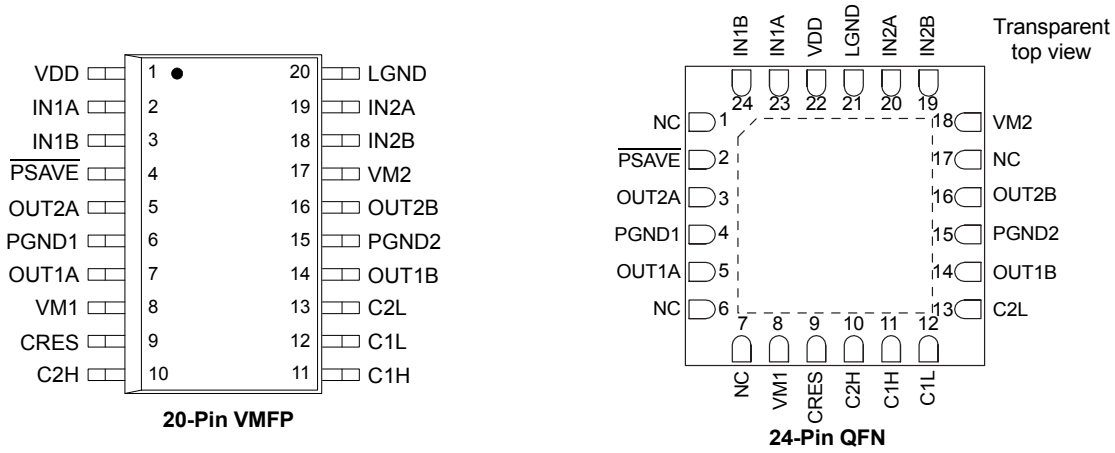


Figure 3. Pin Connections

A functional description of each pin can be found in the Functional Pin Description section beginning on page 9.

Table 1. 17531A, 20-Pin VMFP Definitions

Pin Number 20-Pin VMFP	Pin Number 24-Pin QFN	Pin Name	Formal Name	Definition
1	22	VDD	Logic Supply	Control circuit power supply pin.
2	23	IN1A	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 5, Truth Table, page 8).
3	24	IN1B	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 5, Truth Table, page 8).
4	2	$\overline{\text{PSAVE}}$	Power Save	Logic input controlling power save mode.
5	3	OUT2A	H-Bridge Output 2A	Output A of H-Bridge channel 2.
6	4	PGND1	Power Ground 1	High-current power ground 1.
7	5	OUT1A	H-Bridge Output 1A	Output A of H-Bridge channel 1.
8	8	VM1	Motor Drive Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Drive Power Supply).
9	9	CRES	Predriver Power Supply	Internal triple charge pump output as predriver power supply.
10	10	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
11	11	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
12	12	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
13	13	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
14	14	OUT1B	H-Bridge Output 1B	Output B of H-Bridge channel 1.
15	15	PGND2	Power Ground 2	High-current power ground 2.
16	16	OUT2B	H-Bridge Output 2B	Output B of H-Bridge channel 2.
17	17	VM2	Motor Drive Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Drive Power Supply).
18	19	IN2B	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 5, Truth Table, page 8).
19	20	IN2A	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 5, Truth Table, page 8).
20	21	LGND	Logic Ground	Low-current logic signal ground.
N/A	1, 6, 7, 17	NC	—	No Connect

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 11.0	V
Charge Pump Output Voltage	V_{CRES}	-0.5 to 14.0	V
Logic Supply Voltage	V_{DD}	-0.5 to 5.0	V
Signal Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (1)	 I_O I_{OPK}	 0.7 1.4	A
ESD Voltage (2) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±1200 ±150	V
Operating Junction Temperature	T_J	-20 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Thermal Resistance (3)	$R_{\theta JA}$	50	°C/W
Power Dissipation (4) WMFP QFN	P_D	 1.0 2.5	W
Pin Soldering Temperature (5)	T_{SOLDER}	260	°C
Peak Package Reflow Temperature During Reflow (5), (6)	T_{PPRT}	Note 6	°C

Notes

1. T_A = 25 °C, 10 ms pulse width at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. QFN24: 45 x 30 x 1 [mm] glass EPOXY board mount. (See: recommended heat pattern) VMFP16: 37 x 50 x 1.6 [mm] glass EPOXY board mount. When the exposed pad is bonded, Rsj is not performed.
4. Maximum at T_A = 25 °C. When the exposed pad is bonded, Rsj is not performed.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions T_A = 25 °C, V_{DD} = 3.0 V, V_M = 5.0 V, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Motor Supply Voltage (Using Internal Charge Pump) (7)	$V_{M\text{-}CP}$	2.0	5.0	8.6	V
Motor Supply Voltage (V_{CRES} Applied Externally) (8)	$V_{M\text{-}NCP}$	–	–	10	V
Gate Drive Voltage - Motor Supply Voltage (V_{CRES} Applied Externally) (9)	$V_{CRES\text{-}VM}$	5.0	6.0	–	V
Logic Supply Voltage	V_{DD}	2.7	3.0	3.6	V
Driver Quiescent Supply Current					µA
No Signal Input	I_{QM}	–	–	100	
Power Save Mode	$I_{QM\text{-}\overline{PSAVE}}$	–	–	1.0	
Logic Quiescent Supply Current					mA
No Signal Input (10)	I_{QVDD}	–	–	1.0	
Power Save Mode	$I_{QVDD\text{-}\overline{PSAVE}}$	–	–	1.0	
Operating Power Supply Current					mA
Logic Supply Current (11)	I_{VDD}	–	–	3.0	
Charge Pump Circuit Supply Current (12)	I_{CRES}	–	–	0.7	
Low V_{DD} Detection Voltage (13)	V_{DDDET}	1.0	1.6	2.5	V
Driver Output ON Resistance (14)	$R_{DS(ON)}$	–	0.8	1.2	Ohms
GATE DRIVE					
Gate Drive Voltage (12)	V_{CRES}				V
No Current Load		12	13	13.5	
Gate Drive Ability (Internally Supplied)	$V_{CRESLOAD}$				V
I_{CRES} = -1.0 mA		8.5	9.2	–	
Recommended External Capacitance (C1L–C1H, C2L–C2H, C_{RES}–GND)	C_{CP}	0.01	0.1	1.0	µF

Notes

7. Gate drive voltage V_{CRES} is generated internally. 2 x V_{DD} + V_M must be < $V_{CRES\ MAX}$ (13.5 V).
8. No internal charge pump used. V_{CRES} is applied from an external source.
9. $R_{DS(ON)}$ is not guaranteed if $V_{CRES\text{-}VM}$ < 5.0 V. Also, function is not guaranteed if V_{CRES} - V_M < 3.0 V.
10. I_{QVDD} includes the current to pre-driver circuit.
11. I_{VDD} includes the current to predriver circuit at f_{IN} = 100 kHz.
12. At f_{IN} = 20 kHz.
13. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. V_{CRES} is applied from an external source. 2 x V_{DD} + V_M must be < $V_{CRES\ MAX}$ (13.5 V).
14. I_O = 0.7 A source + sink.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions T_A = 25 °C, V_{DD} = 3.0 V, V_M = 5.0 V, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Inputs (2.7 V < V_{DD} < 3.3 V)					
High Level Input Voltage	V_{IH}	V_{DD} x 0.7	–	–	V
Low Level Input Voltage	V_{IL}	–	–	V_{DD} x 0.3	V
High Level Input Current	I_{IH}	–	–	1.0	µA
Low Level Input Current	I_{IL}	-1.0	–	–	µA
$\overline{\text{PSAVE}}$ Pin Input Current Low	$I_{IL\text{-}\overline{\text{PSAVE}}}$	–	50	100	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions T_A = 25 °C, V_{DD} = 3.0 V, V_M = 5.0 V, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (15)	t_R	–	–	1.0 (16)	μs
Input Pulse Fall Time (17)	t_F	–	–	1.0 (16)	μs
OUTPUT					
Propagation Delay Time (18) Turn-ON Time Turn-OFF Time	 t_{PLH} t_{PHL}	 – –	 0.1 0.1	 0.5 0.5	μs
Charge Pump Wake-up Time (19)	t_{VGON}	–	1.0	3.0	ms
Low Voltage Detection Time	t_{VDDDET}	–	–	10	ms

Notes
15. Time is defined between 10% and 90%.
16. That is, the input waveform slope must be steeper than this.
17. Time is defined between 90% and 10%.
18. Output load is 8.0 Ω DC.
19. C_{CP} = 0.1 μF.

TIMING DIAGRAMS

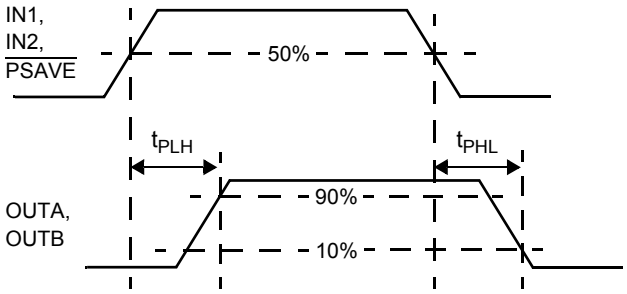


Figure 4. t_{PLH}, t_{PHL}, and t_{PZH} Timing

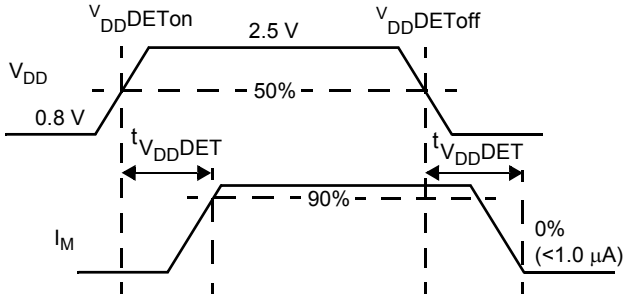


Figure 5. Low Voltage Detection Timing

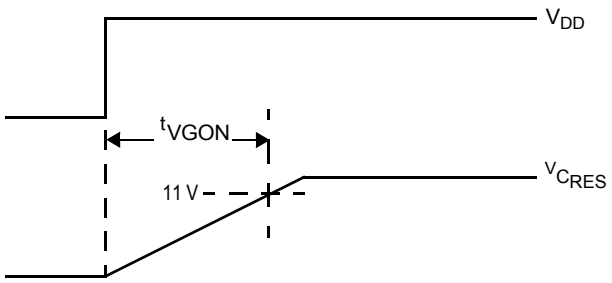


Figure 6. Charge Pump Timing

Table 5. Truth Table

INPUT			OUTPUT		Charge Pump and Low Voltage Detector
$\overline{\text{PSAVE}}$	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B	
L	L	L	L	L	RUN
L	H	L	H	L	RUN
L	L	H	L	H	RUN
L	H	H	Z	Z	RUN
H	X	X	Z	Z	STOP

H = High.
L = Low.
Z = High-impedance.
X = Don't care.
$\overline{\text{PSAVE}}$ pin is pulled up to V_{DD} with internal resistance.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17531A is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors, such as those found in camera lens assemblies, camera shutters, and optical disk drives. The device features an on-board charge pump, as well as built-in shoot-through current protection and under-voltage shutdown.

The 17531A has four operating modes: Forward, Reverse, Brake, and Tri-state (high-impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2\ \Omega$.

The 17531A can simultaneously drive two brush DC motors or one bipolar step motor. The drivers are designed to be PWMed at frequencies up to 200 kHz.

FUNCTIONAL PIN DESCRIPTION

LOGIC SUPPLY (VDD)

The VDD pin carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input pins control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to Table 5, Truth Table, page 8).

POWER SAVE ($\overline{\text{PSAVE}}$)

The $\overline{\text{PSAVE}}$ pin is a HIGH = TRUE power save mode input. When $\overline{\text{PSAVE}}$ = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (High-Z), regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states, and the internal charge pump and low voltage detection current are shut off to save power.

H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (see Figure 2, 17531A Simplified Internal Block Diagram, page 2).

MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the OUTput pins. All VM pins must be connected together on the printed circuit board.

CHARGE PUMP (C1L AND C1H, C2L AND C2H)

These two pairs of pins, the C1L and C1H, and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

PREDRIVER POWER SUPPLY (CRES)

The CRES pin is the output of the internal charge pump. Its output voltage is approximately three times of V_{DD} voltage. The V_{CRES} voltage is power supply for the internal predriver circuit of H-Bridges.

POWER GROUND (PGND)

Power ground pins. They must be tied together on the PCB.

LOGIC GROUND (LGND)

Logic ground pin.

TYPICAL APPLICATIONS

Figure 7 shows a typical application for the 17531A. When applying the gate voltage to the CRES pin from an external source, be sure to connect it via a resistor equal to or greater than $R_G = V_{CRES}/0.02\ \Omega$.

The internal charge pump of this device is generated from the V_{DD} supply; therefore, care must be taken to provide sufficient gate-source voltage for the high side MOSFETs when $V_M >> V_{DD}$ (e.g., V_M = 5.0 V, V_{DD} = 3.3 V), in order to ensure full enhancement of the high side MOSFET channels.

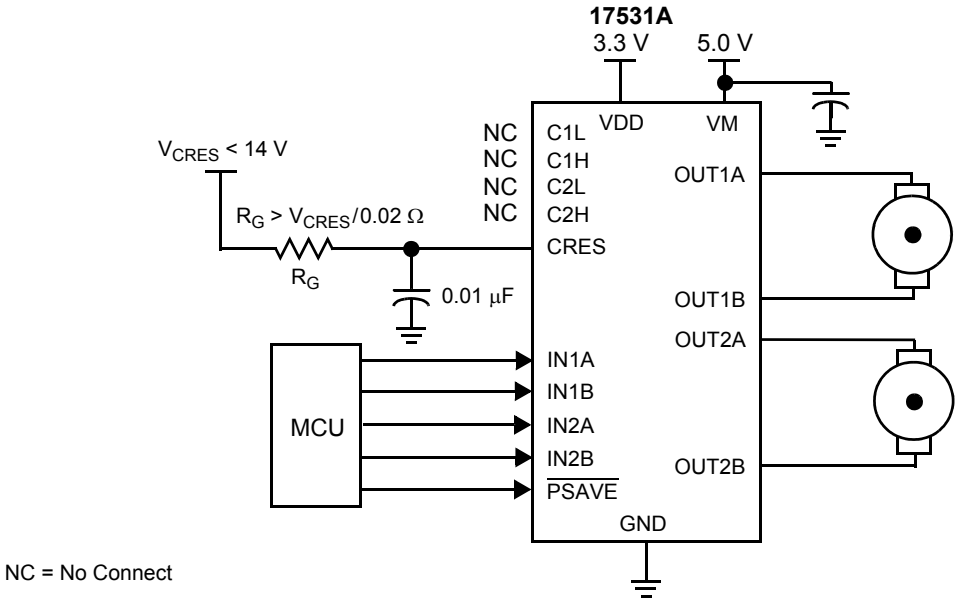


Figure 7. 17531A Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply pin (VM) (see Figure 8).

PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high current paths, use wide copper traces and the shortest possible distances.

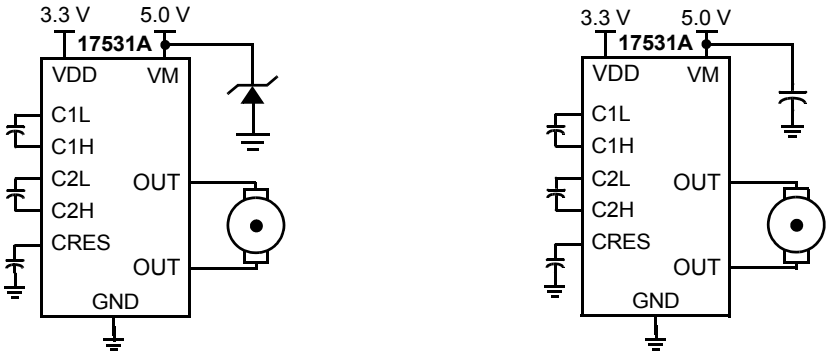
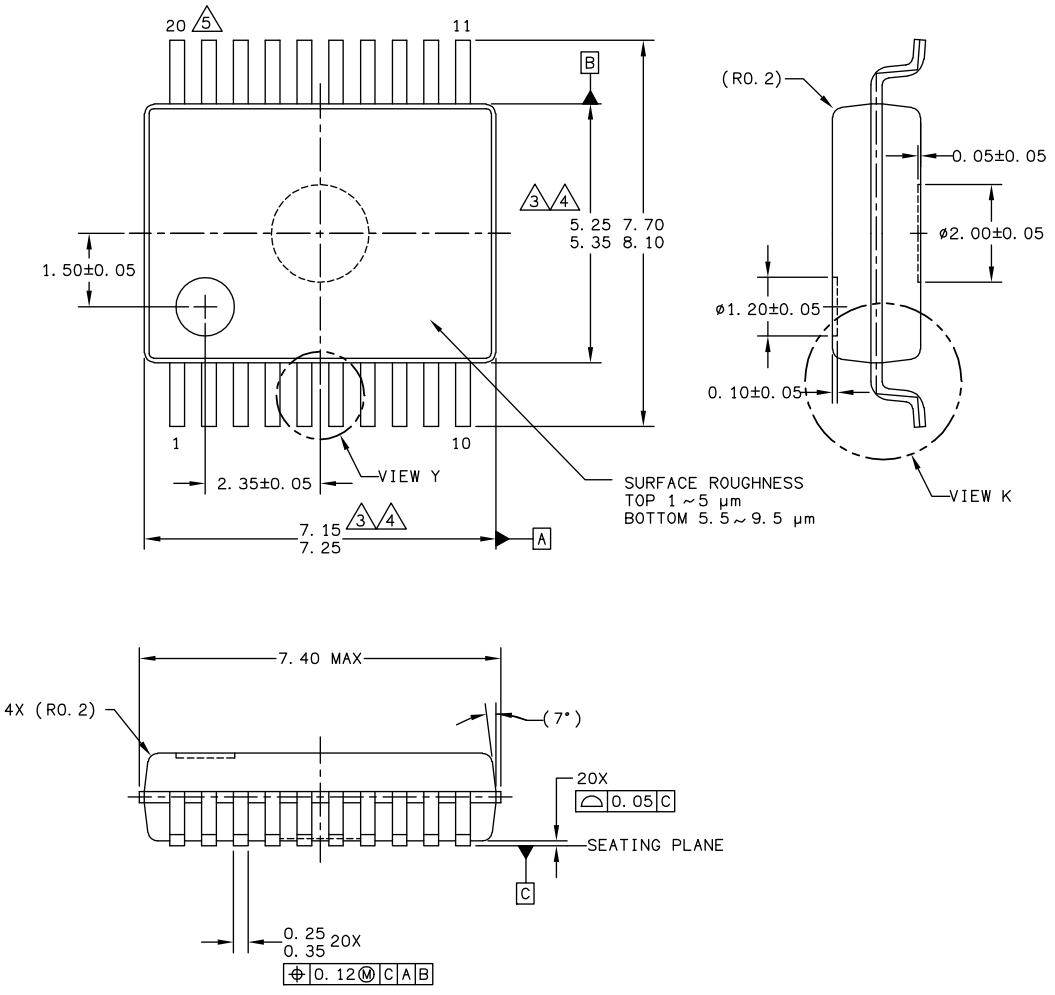


Figure 8. CEMF Snubbing Techniques

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” drawing number listed.



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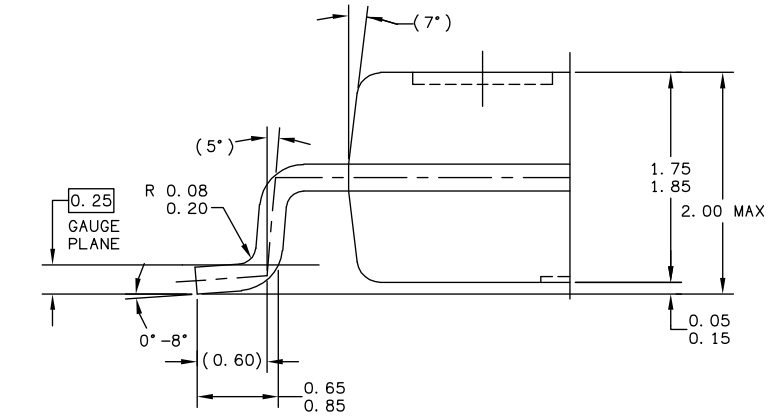
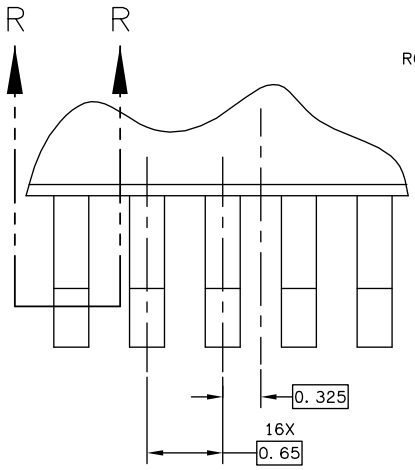
	CASE NUMBER: 1569–02	01 DEC 2006
	STANDARD: NON–JEDEC	

17531A





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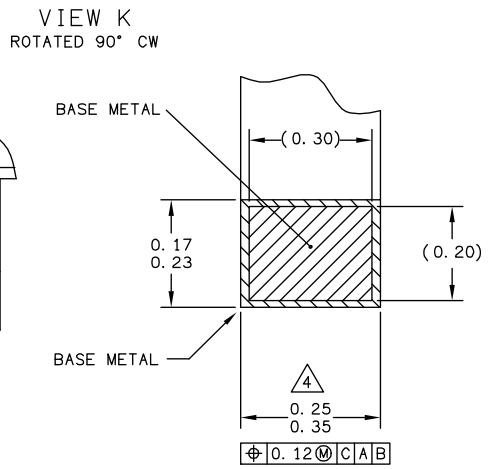

SECTION R–R

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	CASE NUMBER: 1569-02	01 DEC 2006
	STANDARD: NON-JEDEC	

17531A

NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.

2 ALL DIMENSIONS ARE IN MILLIMETERS.

3 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.10 ANY SIDE.
DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE.

4 DIMENSIONS ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY
EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH,
BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

5 TERMINAL NUMBER ARE SHOWN FOR REFERENCE ONLY.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10616D	REV: B
EIAJ VMFP 20LD, 0.65 PITCH	CASE NUMBER: 1569-02	01 DEC 2006
	STANDARD: NON-JEDEC	

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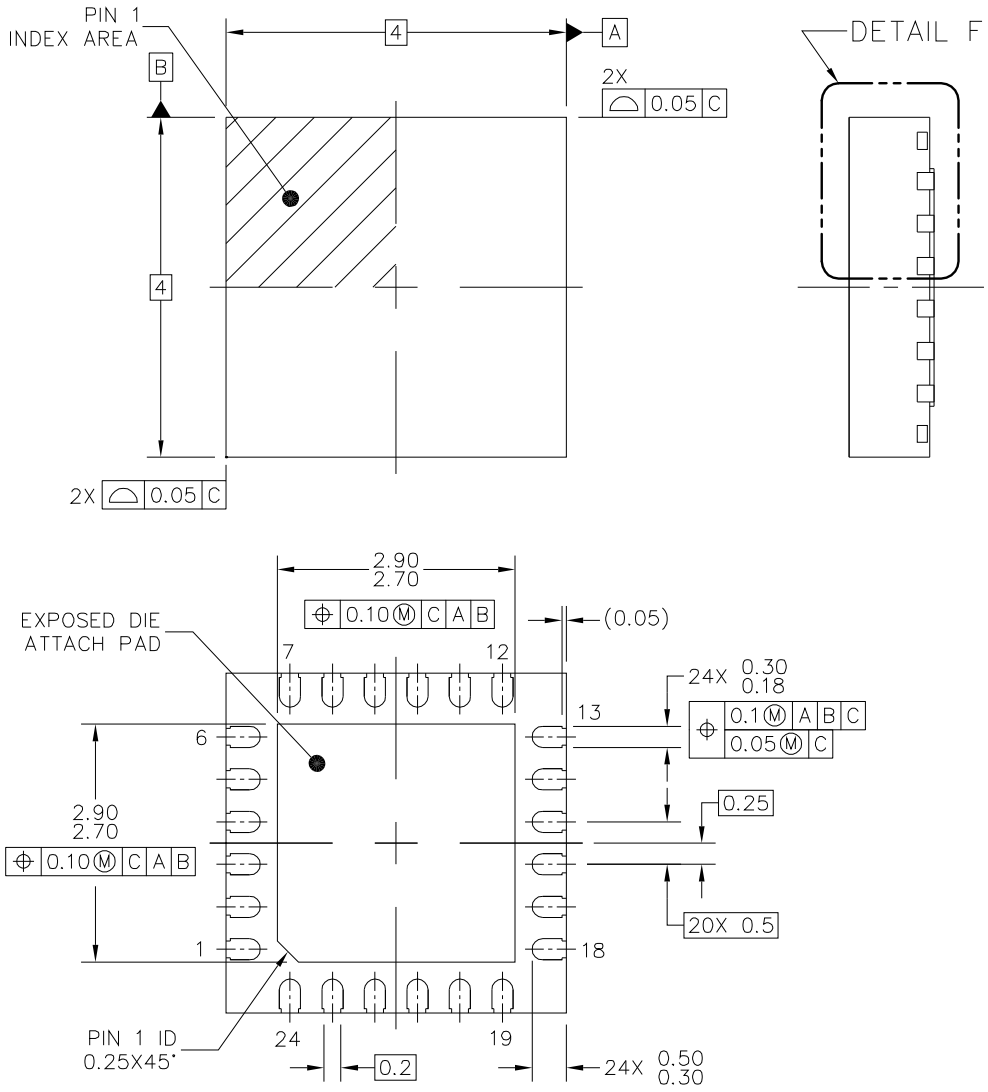

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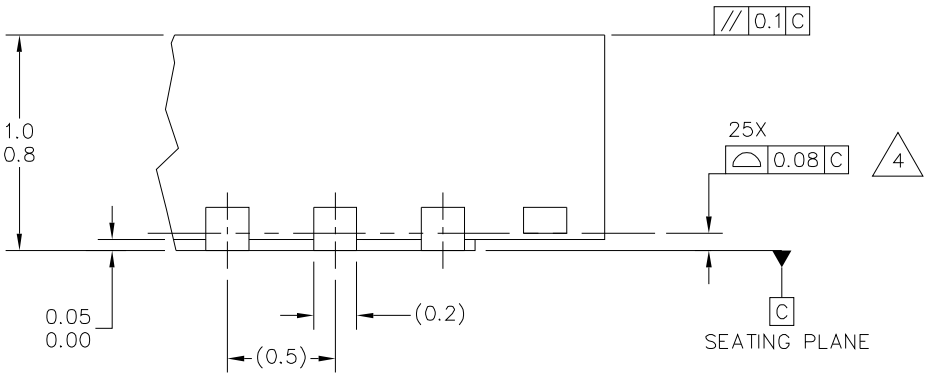
	CASE NUMBER: 2296-02	11 OCT 2012
	STANDARD: NON-JEDEC	

17531A



DETAIL F
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	CASE NUMBER: 2296-02	11 OCT 2012
	STANDARD: NON-JEDEC	

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QFN, THERMALLY ENHANCED 4 X 4 X 0.9, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00474D	REV: A
	CASE NUMBER: 2296–02	11 OCT 2012
	STANDARD: NON–JEDEC	

17531A

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	9/2005	Implemented Revision History page Converted to Freescale format
3.0	2/2008	Corrected Table 2, Pin Definitions on page 4.
4.0	5/2009	Corrected Note 7, in Static Electrical Characteristics table.
5.0	10/2013	Updated package drawings Corrected ordering information table to MPC17531ATEP and MPC17531ATEV/EL Added new back page and document properties
6.0	10/2013	Corrected packaging information on page 1
7.0	11/2014	Changed the QFN 98A to 98ASA00474D per PCN 16331 Corrected errors in ordering information

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