

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4514**

4-to-16 line decoder/demultiplexer  
with input latches

Product specification  
File under Integrated Circuits, IC06

September 1993

## 4-to-16 line decoder/demultiplexer with input latches

## 74HC/HCT4514

### FEATURES

- Non-inverting outputs
- Output capability: standard
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with "4514" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs ( $A_0$  to  $A_3$ ), with latches, a latch enable input (LE), and an active LOW enable input ( $\bar{E}$ ). The 16 outputs ( $Q_0$  to  $Q_{15}$ ) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on  $A_n$ . When LE goes LOW, the last data present at  $A_n$  are stored in the latches and the outputs remain stable. When  $\bar{E}$  is LOW, the selected output, determined by the contents of the latch, is HIGH. At  $\bar{E}$  HIGH, all outputs are LOW. The enable input ( $\bar{E}$ ) does not affect the state of the latch.

When the "4514" is used as a demultiplexer,  $\bar{E}$  is the data input and  $A_0$  to  $A_3$  are the address inputs.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $Q_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	23	26	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	44	45	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

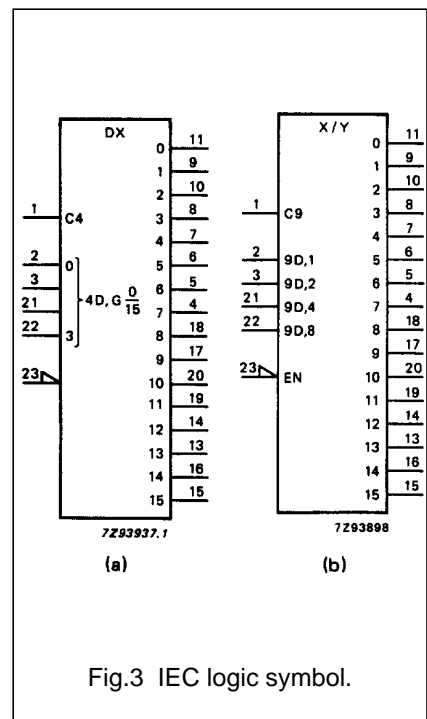
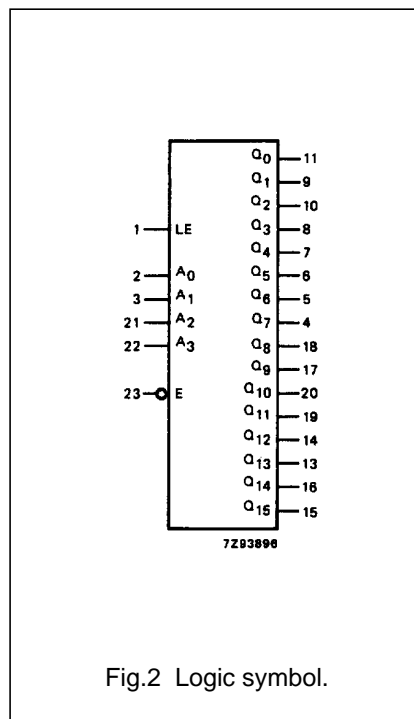
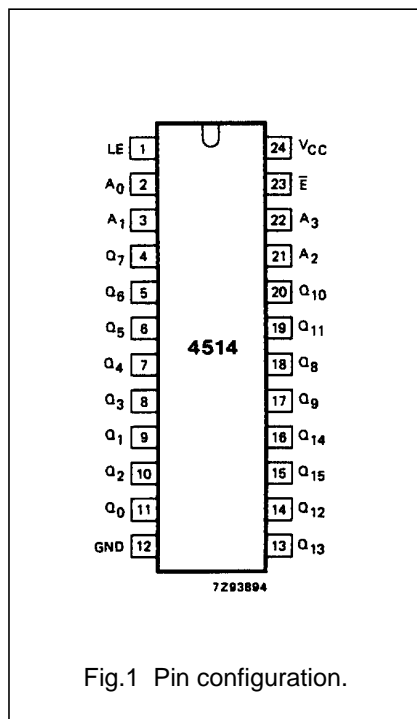
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# 4-to-16 line decoder/demultiplexer with input latches

## 74HC/HCT4514

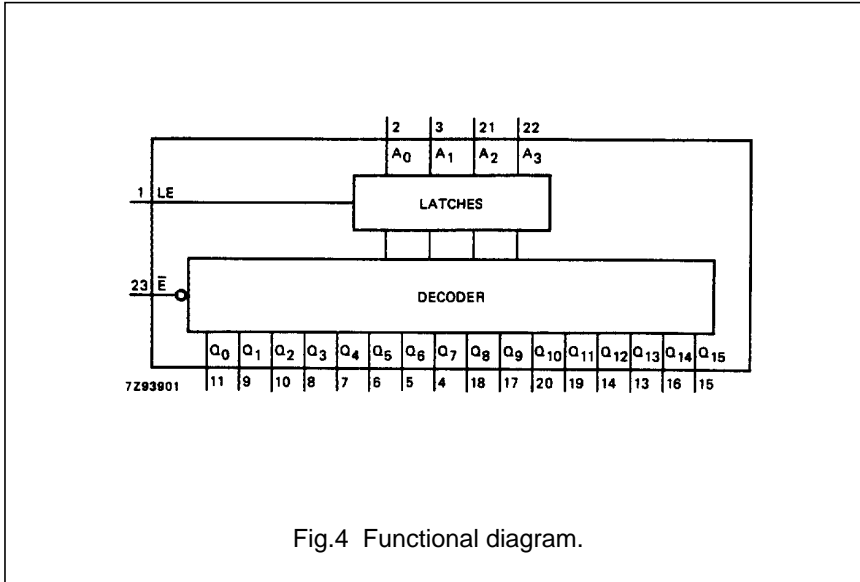
### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A <sub>0</sub> to A <sub>3</sub>	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q <sub>0</sub> to Q <sub>15</sub>	multiplexer outputs (active HIGH)
12	GND	ground (0 V)
23	$\bar{E}$	enable input (active LOW)
24	V <sub>CC</sub>	positive supply voltage



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### APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

Fig.4 Functional diagram.

### FUNCTION TABLE

INPUTS					OUTPUTS																
$\bar{E}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	Q <sub>8</sub>	Q <sub>9</sub>	Q <sub>10</sub>	Q <sub>11</sub>	Q <sub>12</sub>	Q <sub>13</sub>	Q <sub>14</sub>	Q <sub>15</sub>	
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

### Notes

1. LE = HIGH  
 H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

# 4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

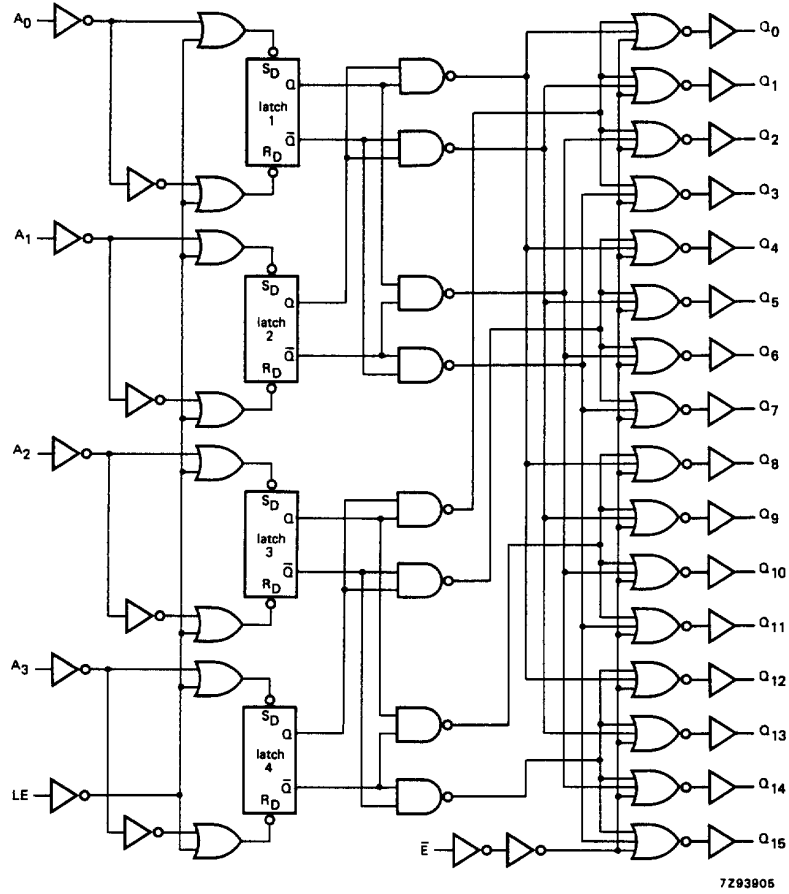


Fig.5 Logic diagram.

# 4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to Q <sub>n</sub>		41 15 12	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>SU</sub>	set-up time A <sub>n</sub> to LE	90 18 15	25 9 7		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig.7
t <sub>H</sub>	hold time A <sub>n</sub> to LE	1 1 1	-11 -4 -3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig.7

# 4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	0.65
LE	1.40
$\bar{E}$	1.00

## AC CHARACTERISTICS FOR 74HCT

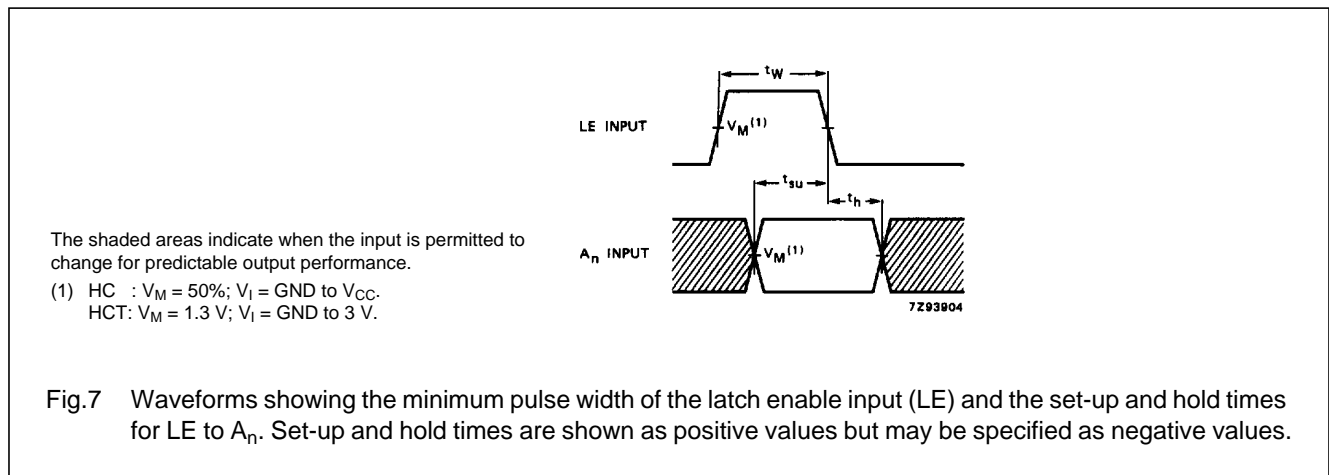
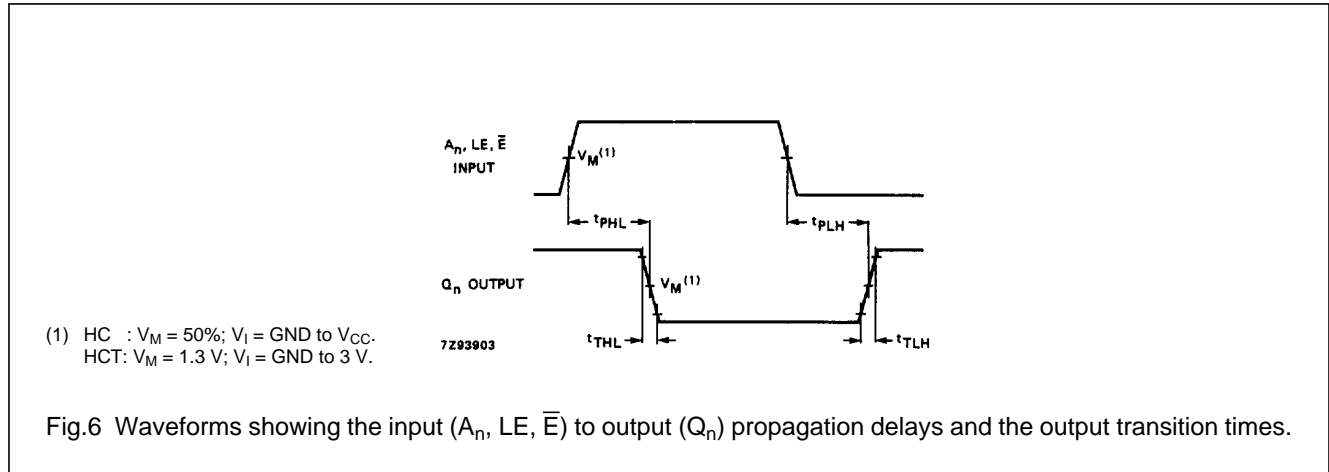
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		30	55		69		83	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		29	50		63		75	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to Q <sub>n</sub>		17	40		50		60	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>w</sub>	latch enable pulse width HIGH	16	4		20		24		ns	4.5	Fig.7
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	18	9		23		27		ns	4.5	Fig.7
t <sub>h</sub>	hold time A <sub>n</sub> to LE	3	-3		3		3		ns	4.5	Fig.7

# 4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

## AC WAVEFORMS





# 4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

## APPLICATION INFORMATION

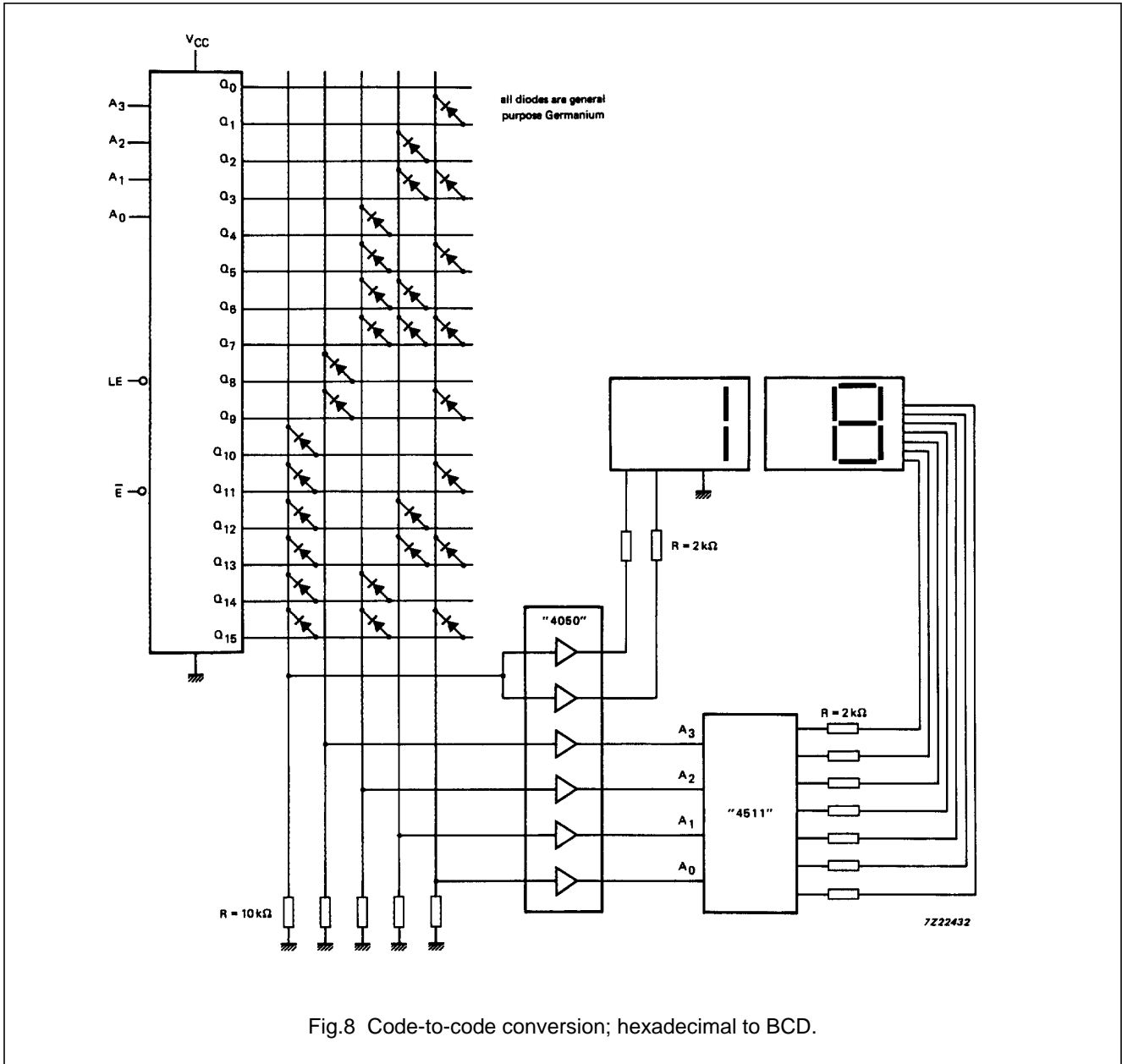
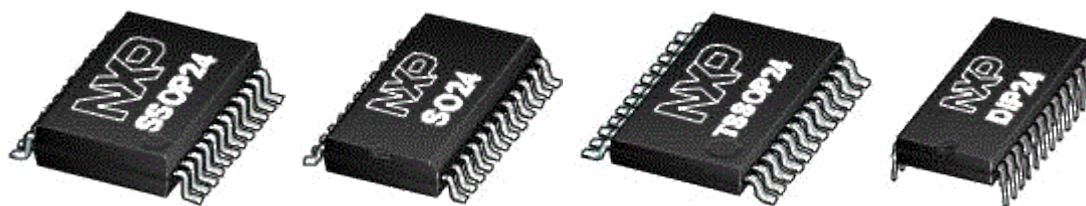


Fig.8 Code-to-code conversion; hexadecimal to BCD.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

# 74HC/HCT4514 Packaging Information



Type Number	Orderable Part Number	Package Name
74HC4514DB	74HC4514DB,118	SSOP24
74HC4514DB	74HC4514DB,112	SSOP24
74HC4514D	74HC4514D,653	SO24
74HC4514D	74HC4514D,652	SO24
74HC4514PW	74HC4514PW,118	TSSOP24
74HC4514PW	74HC4514PW,112	TSSOP24
74HC4514N	74HC4514N,652	DIP24
74HCT4514DB	74HCT4514DB,118	SSOP24
74HCT4514DB	74HCT4514DB,112	SSOP24
74HCT4514D	74HCT4514D,653	SO24
74HCT4514D	74HCT4514D,652	SO24
74HCT4514PW	74HCT4514PW,118	TSSOP24
74HCT4514PW	74HCT4514PW,112	TSSOP24
74HCT4514N	74HCT4514N,652	DIP24