

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT688 8-bit magnitude comparator

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit magnitude comparator

74HC/HCT688

FEATURES

- Compare two 8-bit words
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT688 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT688 are 8-bit magnitude comparators. They perform comparison of two 8-bit binary or BCD words.

The output provides $\overline{P = Q}$.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$			
	P_n, Q_n to $\overline{P = Q}$		17	17	ns
	E to $\overline{P = Q}$		8	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \quad \text{where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

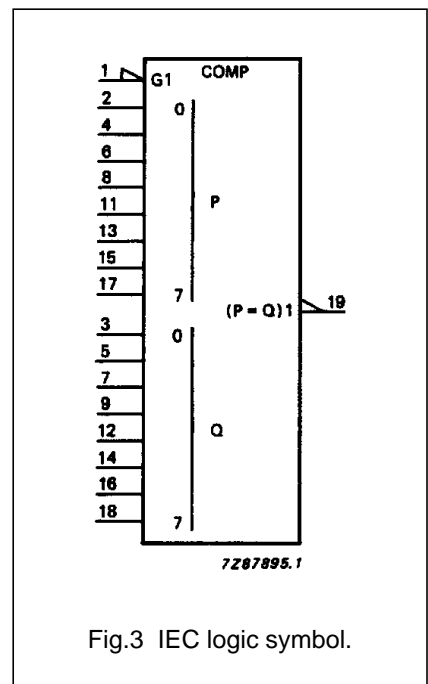
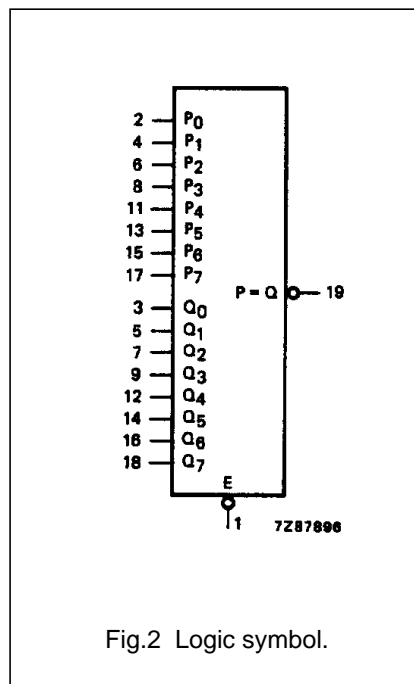
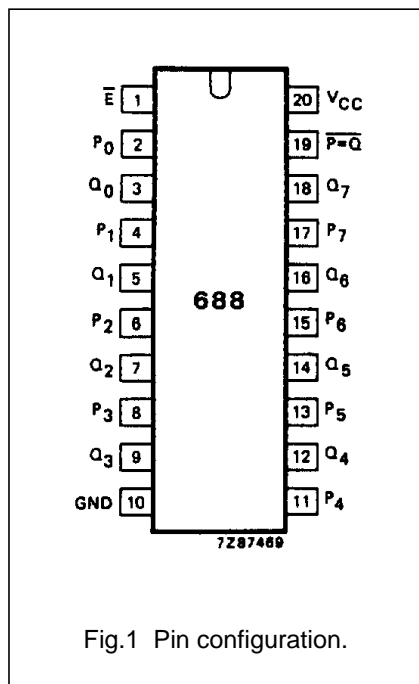
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-bit magnitude comparator

74HC/HCT688

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{E}	enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P_0 to P_7	word inputs
3, 5, 7, 9, 12, 14, 16, 18	Q_0 to Q_7	word inputs
10	GND	ground (0 V)
19	$\overline{P = Q}$	equal to output
20	V_{CC}	positive supply voltage



8-bit magnitude comparator

74HC/HCT688

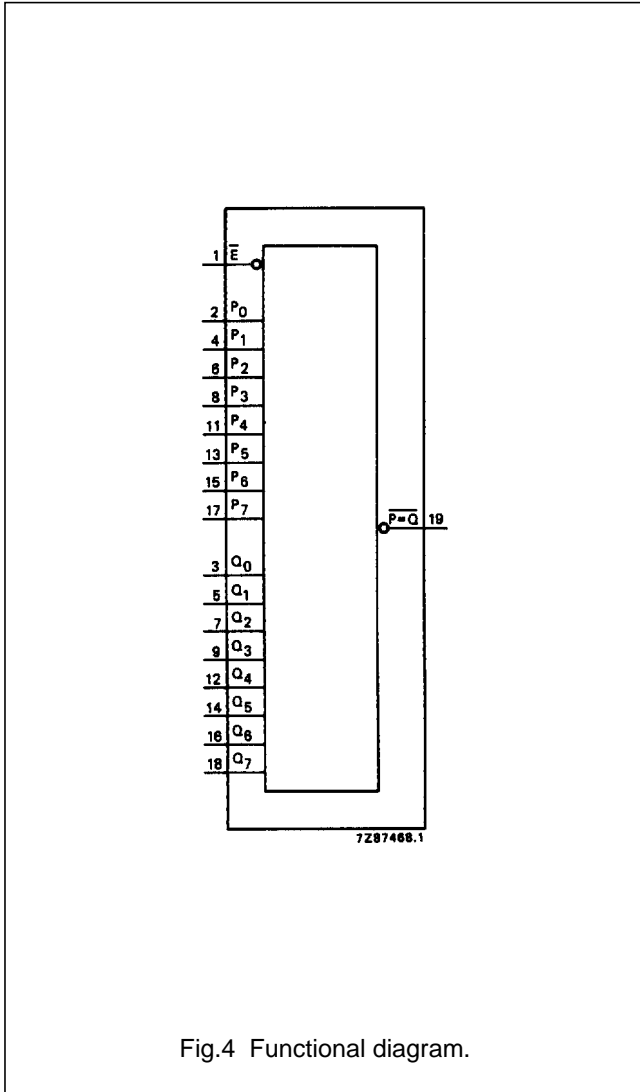


Fig.4 Functional diagram.

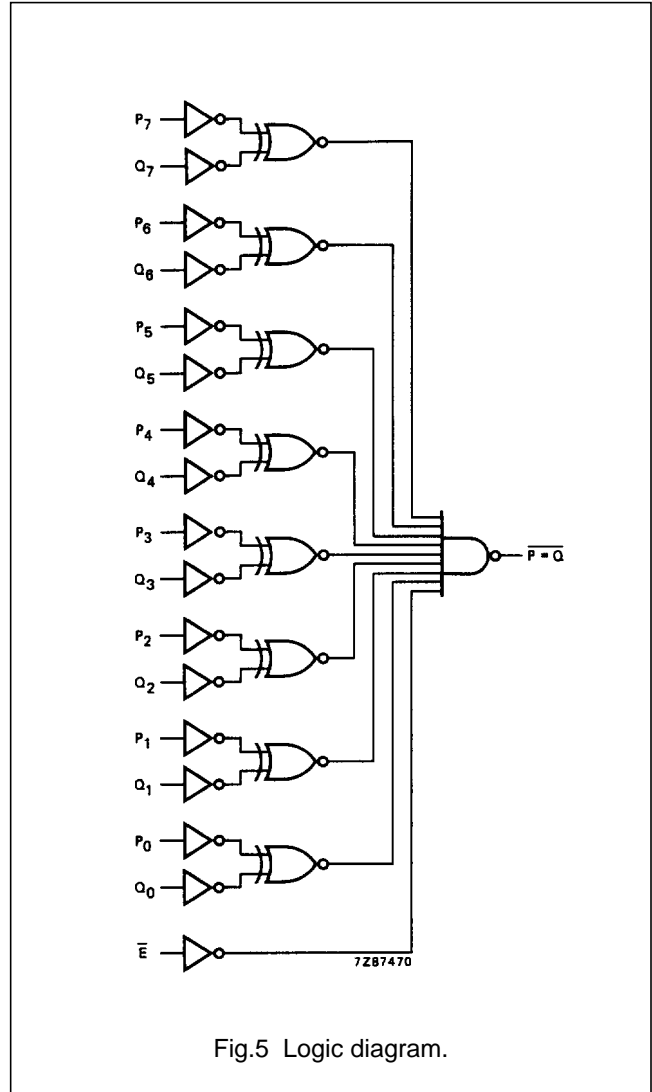


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P _n , Q _n	ENABLE Ē	P = Q̄
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care

8-bit magnitude comparator

74HC/HCT688

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay P _n , Q _n to $\overline{P} = \overline{Q}$		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay \overline{E} to P = Q		28 10 8	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

8-bit magnitude comparator

74HC/HCT688

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
P_n	0.35
Q_n	0.35
\bar{E}	0.70

AC CHARACTERISTICS FOR 74HCT

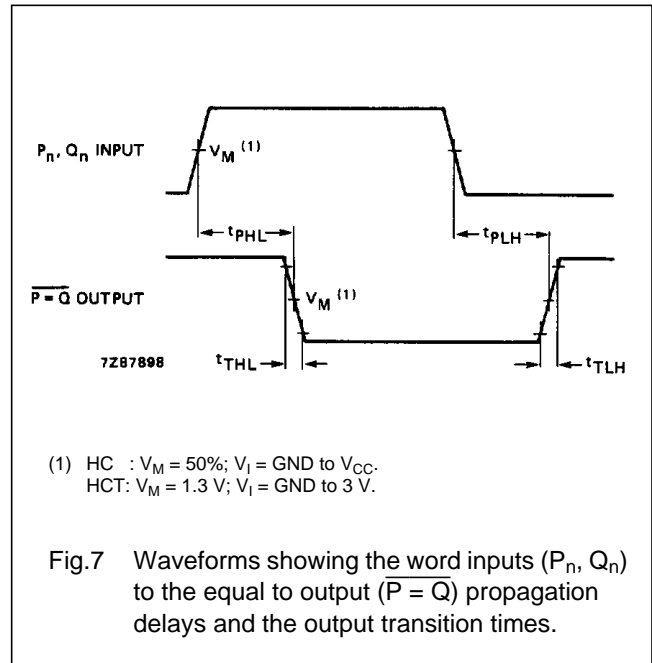
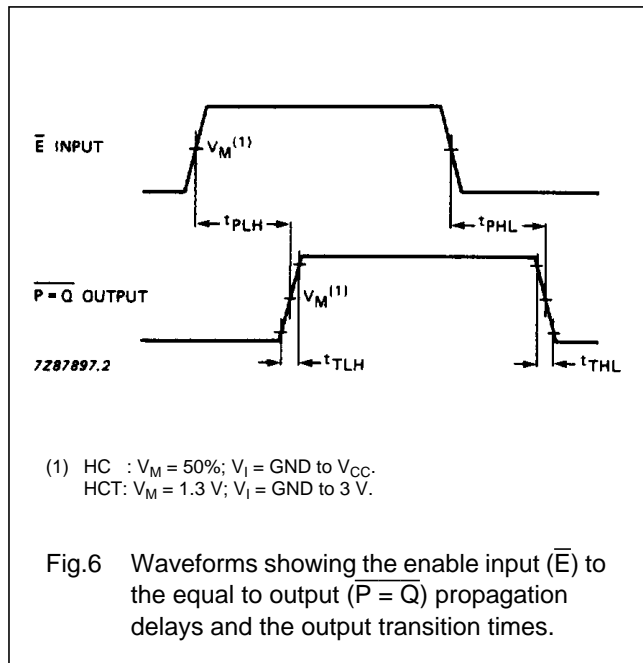
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V_{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay P_n, Q_n to $\bar{P} = \bar{Q}$		20	34		43		51	ns	4.5	Fig.6	
t_{PHL}/t_{PLH}	propagation delay \bar{E} to $P = Q$		18	24		30		36	ns	4.5	Fig.7	
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

8-bit magnitude comparator

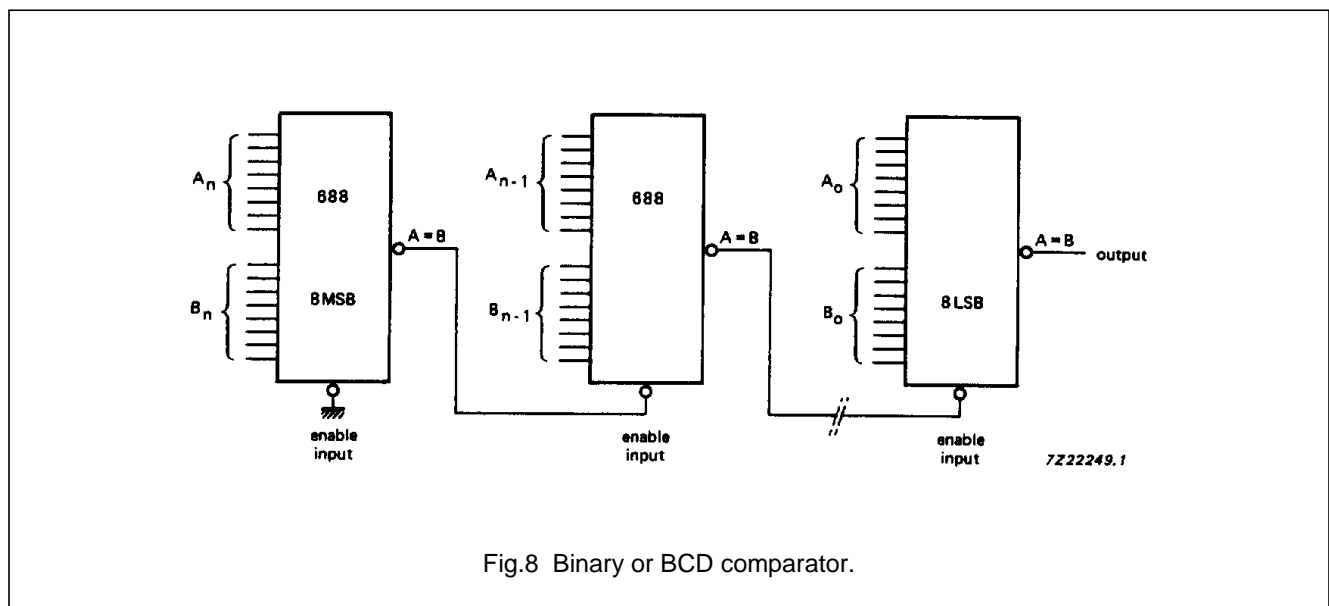
74HC/HCT688

AC WAVEFORMS



APPLICATION INFORMATION

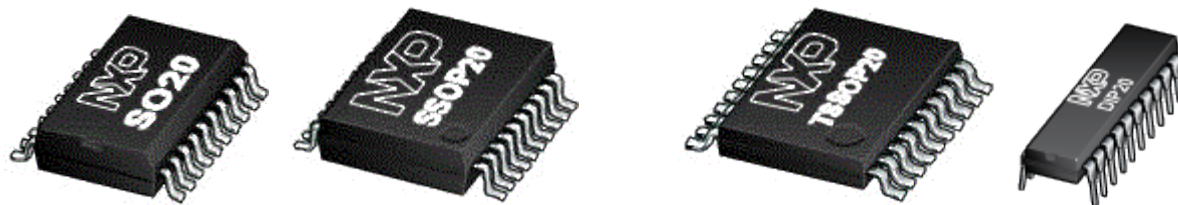
Two or more "688" 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits. An example is shown in Fig.8.



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

74HC/HCT688 Packaging Information



Type Number	Orderable Part Number	Package Name
74HC688D	74HC688D,653	SO20
74HC688D	74HC688D,652	SO20
74HC688DB	74HC688DB,118	SSOP20
74HC688DB	74HC688DB,112	SSOP20
74HC688PW	74HC688PW,118	TOSSP20
74HC688PW	74HC688PW,112	TOSSP20
74HC688N	74HC688N,652	DIP20
74HCT688D	74HCT688D,653	SO20
74HCT688D	74HCT688D,652	SO20
74HCT688DB	74HCT688DB,118	SSOP20
74HCT688DB	74HCT688DB,112	SSOP20
74HCT688PW	74HCT688PW,118	TSSOP20
74HCT688PW	74HCT688PW,112	TSSOP20
74HCT688N	74HCT688N,652	DIP20