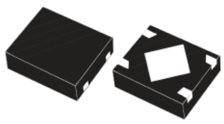
LD39020

200 mA very low quiescent current linear regulator IC

Datasheet - production data



DFN1x1-4L

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low dropout voltage (200 mV typ. at 200 mA load)
- Very low quiescent current (20 µA typ at no load, 0.03 µA typ in off mode)
- Output voltage tolerance: ±0.5 % (A version) or ± 2.0 % @ 25 °C (standard version)
- 200 mA guaranteed output current
- High PSRR (80 dB@1 kHz, 50 db@100 kHz)
- Wide range of output voltages available on request: from 0.8 V up to 5.0 V in 50 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Optional output voltage discharge feature
- Compatible with ceramic capacitor C_{OUT} = 0.47 µF
- Internal constant current and thermal protections
- Available in DFN 1x1-4L
- Operating temperature range: -40 °C to 125 °C

Applications

- Mobile phones
- Personal digital assistants (PDAs)
- Digital still cameras (DSC)
- Cordless phones and similar battery-powered systems
- Portable media players

Description

The LD39020 high accuracy voltage regulator provides 200 mA of maximum current from an input voltage ranging from 1.5 V to 5.5 V, with a typical dropout voltage of 200 mV.

It is available in DFN 1x1-4L package, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra low drop voltage, low quiescent current and low noise features, together with the internal soft-start circuit, make the LD39020 suitable for low power battery-operated applications.

An enable logic control function puts the LD39020 in shutdown mode allowing a total current consumption lower than 0.1 µA. Constant current and thermal protection are provided.

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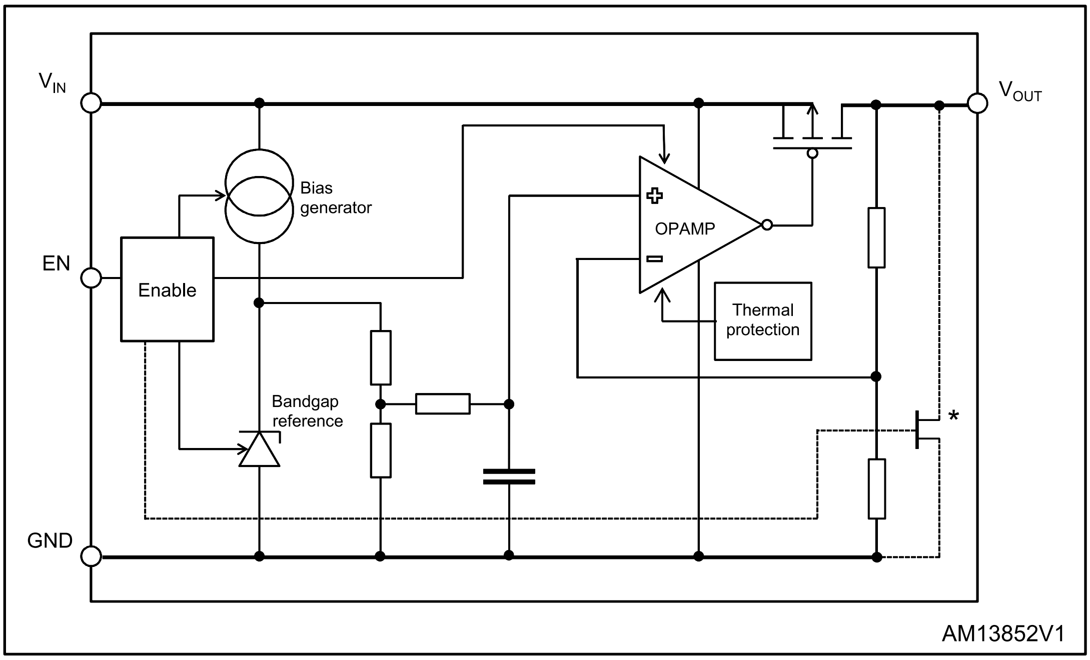
1 Diagram

Figure 1: Block diagram



The output discharge MOSFET is optional.

2 Pin configuration

Figure 2: Pin connection (top view)

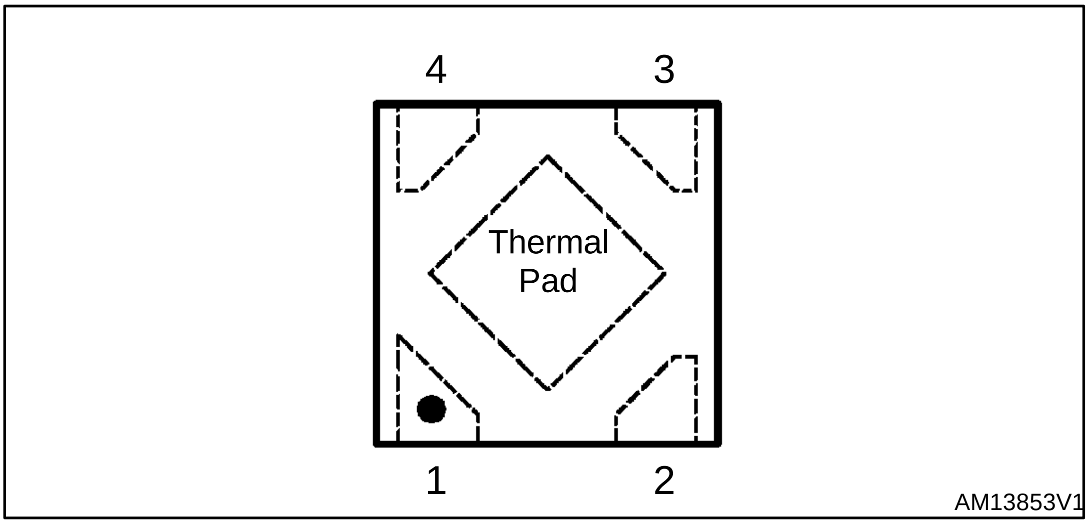
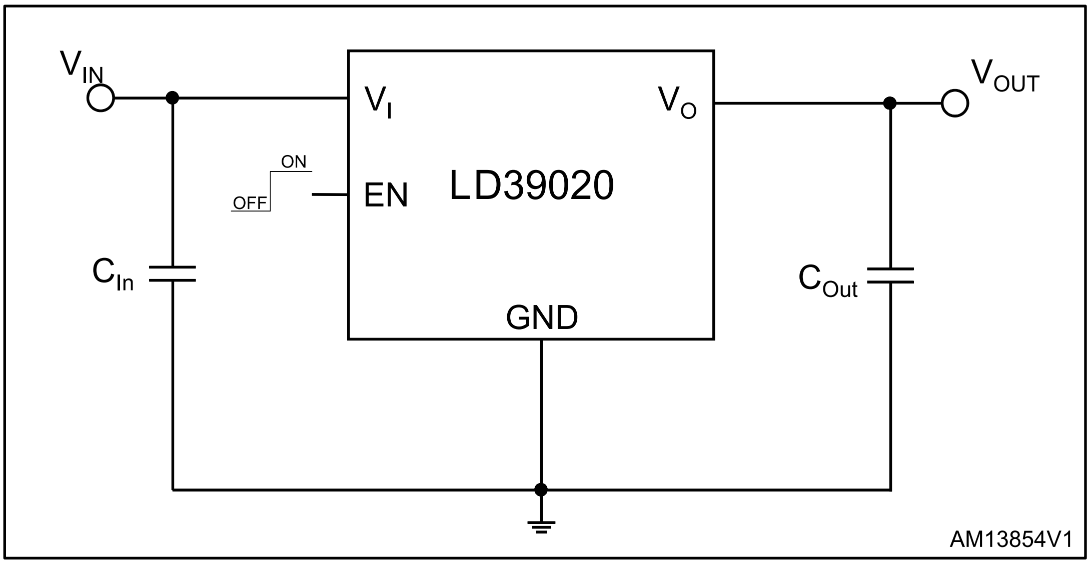


Table 1: Pin description

Pin n°	Symbol	Function
1	OUT	Output voltage
2	GND	Common ground
3	EN	Enable pin logic input: Low = shutdown, High = active
4	IN	Input voltage
Thermal pad	GND	Connect to GND on the PCB

3 Typical application

Figure 3: Typical application circuits



4 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	- 0.3 to 7	V
V_{OUT}	Output voltage	- 0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to 7	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 40 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	250	°C/W

Table 4: ESD Performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD Protection voltage	HBM	4	kV
		MM	400	V
		CDM	500	V

5 Electrical characteristics

T_J = 25 °C, $V_{IN} = V_{OUT(NOM)}$ + 1 V , $C_{IN} = C_{OUT}$ = 1 µF, I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, unless otherwise specified.

Table 5: Electrical characteristics for LD39020T, LD39020DT

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	I_{OUT} = 1 mA, T_J = 25 °C	-2		2	%
		I_{OUT} = 1 mA, -40 °C<T_J<125 °C	-3		3	%
ΔV_{OUT}	Static line regulation[(1)]	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		0.02		%/V
		-40 °C<T_J<125 °C			0.2	
ΔV_{OUT}	Static load regulation	I_{OUT} = 0 mA to 200 mA		10		mV
		-40 °C<T_J<125 °C			0.01	%/mA
V_{DROP}	Dropout voltage	I_{OUT} = 30 mA,V_{OUT} = 2.8 V		35		mV
		I_{OUT} = 200 mA, V_{OUT} = 2.8 V -40 °C<T_J<125 °C		200	350	
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 10 mA		45		μV_{RMS}
SVR	Supply voltage rejection	$V_{IN} = V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Freq .=1 kHz I_{OUT} = 30 mA		80		dB
		$V_{IN} = V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Freq. = 100 kHz I_{OUT} = 30 mA		55		
I_Q	Quiescent current	I_{OUT} = 0 mA		20	40	µA
		I_{OUT} = 200 mA		100		
$I_{Standby}$	Standby Current	V_{IN} input current in OFF MODE: V_{EN} = GND		0.03	1	µA
I_{SC}	Short circuit current	R_L = 0	250	350		mA
R_{ON}	Output voltage discharge MOSFET	(only on LD39020DT)		100		Ω
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V -40 °C<T_J<125 °C			0.4	V
	Enable input logic high	V_{IN} = 1.5 V to 5.5 V -40 °C<T_J<125 °C	1			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$			100	nA
TON[(2)]	Turn on time			100		µs
T_{SHDN}	Thermal shutdown			160		°C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see *Figure 17: "Stability area vs (COUT, ESR)"*)	0.47		22	µF

Notes:

(1)Not applicable for Vout(nom) > 4.5 V

(2)Turn-on time is time measured between the enable input just exceeding VEN high value and the output voltage just reaching 95 % of its nominal value

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V , C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 6: Electrical characteristics for LD39020AT, LD39020ADT

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	I_{OUT} = 1 mA, T_J = 25 °C	-0.5		0.5	%
		I_{OUT} = 1 mA, -40 °C<T_J<125 °C	-1.5		1.5	%
ΔV_{OUT}	Static line regulation (1)	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		0.02		%/V
		-40 °C<T_J<125 °C			0.2	
ΔV_{OUT}	Static load regulation	I_{OUT} = 0 mA to 200 mA		10		mV
		-40 °C<T_J<125 °C			0.01	%/mA
V_{DROP}	Dropout voltage	I_{OUT} = 30 mA,V_{OUT} = 2.8 V		35		mV
		I_{OUT} = 200 mA, V_{OUT} = 2.8 V -40 °C<T_J<125 °C		200	350	
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 10 mA		45		μV_{RMS}
SVR	Supply voltage rejection	V_{IN} = $V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Freq. = 1 kHz I_{OUT} = 30 mA		80		dB
		V_{IN} = $V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Freq. = 100 kHz I_{OUT} = 30 mA		55		
I_Q	Quiescent current	I_{OUT} = 0 mA		20	40	µA
		I_{OUT} = 200 mA		100		
$I_{Standby}$	Standby current	V_{IN} input current in OFF MODE: V_{EN} = GND		0.03	1	µA
I_{SC}	Short circuit current	R_L = 0	250	350		mA
R_{ON}	Output voltage discharge MOSFET	(only on LD39020ADT)		100		Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V -40 °C<T_J<125 °C			0.4	V
	Enable input logic high	V_{IN} = 1.5 V to 5.5 V -40 °C<T_J<125 °C	1			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}			100	nA
TON[(2)]	Turn on time			100		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see *Figure 17: "Stability area vs (COUT, ESR)"*)	0.47		22	µF

Notes:

[(1)]Not applicable for Vout(nom) > 4.5 V

[(2)]Turn-on time is time measured between the enable input just exceeding VEN high value and the output voltage just reaching 95 % of its nominal value

6 Application information

6.1 Soft start function

The LD39020 has an internal soft start circuit. By increasing the startup time up to 100µs, without the need of any external soft start capacitor, this feature is able to keep the regulator inrush current at startup under control.

6.2 Output discharge function

The LD39020 integrates a MOSFET connected between Vout and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

The device is available with or without auto-discharge feature.

See *Table 8: "Order codes"* for more details.

6.3 Input and output capacitors

The LD39020 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used but, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

Locating the input/output capacitors as closer as possible to the relative pins is recommended.

The LD39020 requires an input capacitor with a minimum value of 1 µF.

This capacitor must be located as closer as possible to the input pin of the device and returned to a clean analog ground.

The control loop of the LD39020 is designed to work with an output ceramic capacitor.

This capacitor must meet the requirements of minimum capacitance and equivalent series resistance (ESR), as shown in Fig17. To assure stability, the output capacitor must maintain its ESR and capacitance in the stable region, over the full operating temperature range.

The LD39020 shows stability with a minimum effective output capacitance of 220 nF.

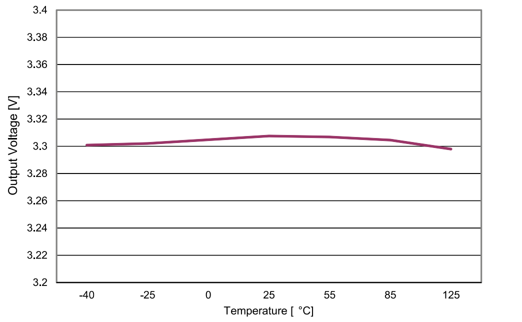
However, to keep stability in all operating conditions (temperature, input voltage and load variations), a minimum output capacitor of 0.47 µF is recommended.

The suggested combination of 1 µF input and output capacitors offers a good compromise among the stability of the regulator, optimum transient response and total PCB area occupation.

7 Typical characteristics

(C_{IN} = C_{OUT} = 1 µF, V_{EN} to V_{IN}, T_J = 25°C unless otherwise specified)

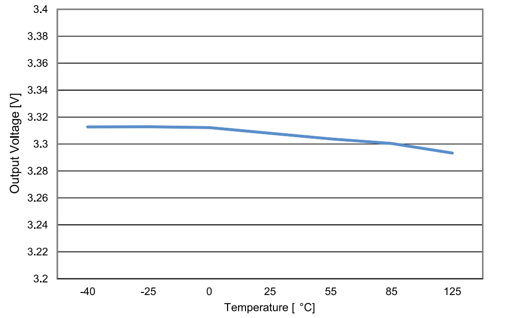
Figure 4: Output voltage vs. temperature (IOUT = 1 mA)



V_{IN}=4.3V, I_{OUT}=1mA

AM13855V1

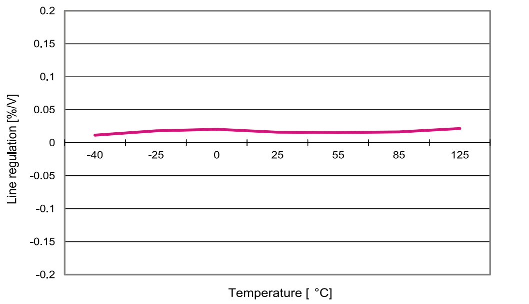
Figure 5: Output voltage vs. temperature (IOUT = 200 mA)



V_{IN}=4.3V, I_{OUT}=200mA

AM13856V1

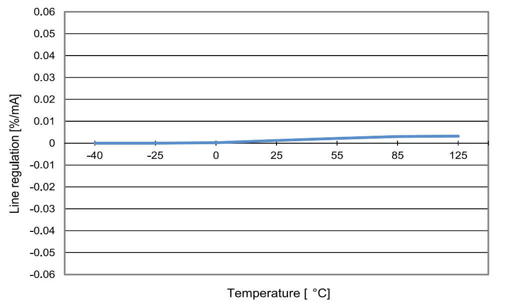
Figure 6: Line regulation vs. temperature



V_{IN}=4.3V to 5.5V, I_{OUT}=10mA

AM13857V1

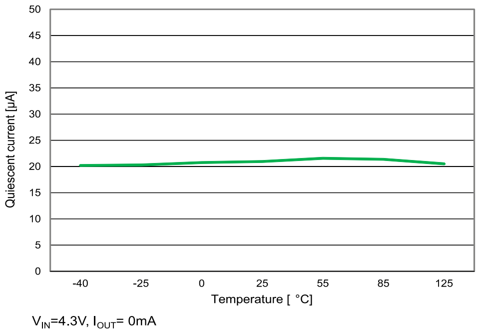
Figure 7: Load regulation vs. temperature



V_{IN}=4.3V, I_{OUT}= 0 to 200mA

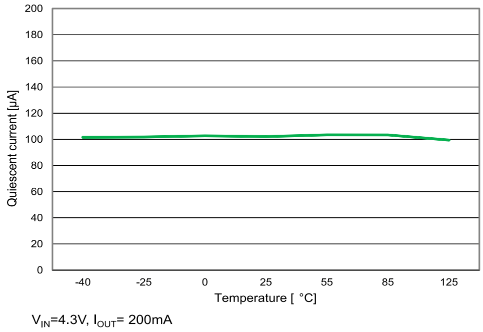
AM13858V1

Figure 8: Quiescent current vs. temperature (IOUT = 0 mA)



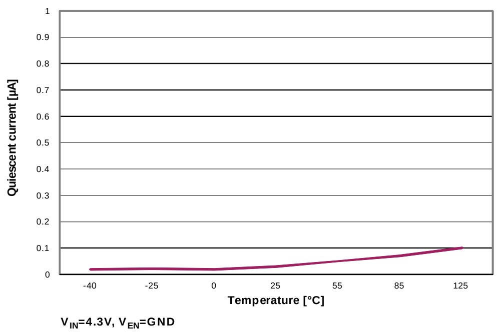
AM13859V1

Figure 9: Quiescent current vs. temperature (IOUT = 200 mA)



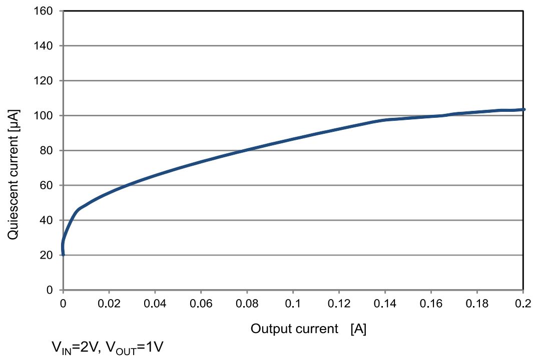
AM13860V1

Figure 10: Shutdown current vs. temperature



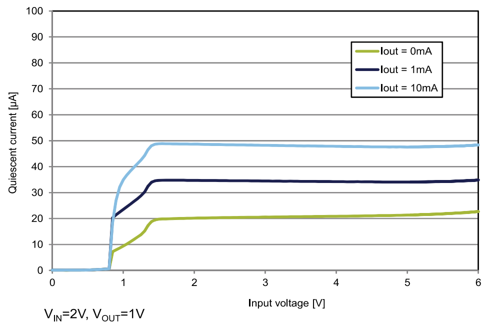
AM13861V1

Figure 11: Quiescent current vs. load current



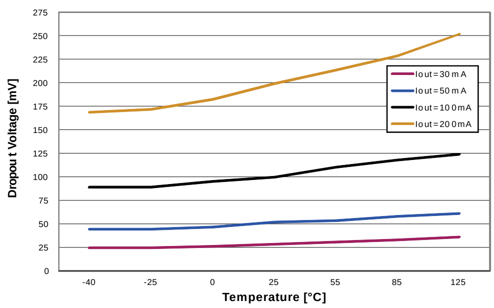
AM13862V1

Figure 12: Quiescent current vs. input voltage



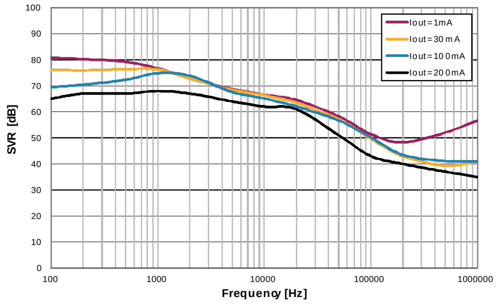
AM13863V1

Figure 13: Dropout voltage vs temperature



AM13864V1

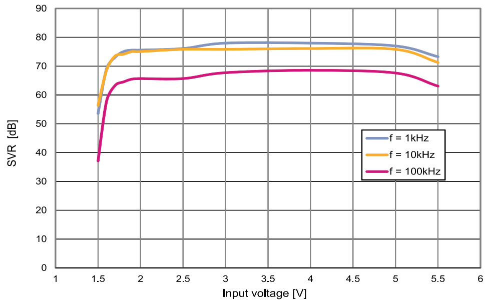
Figure 14: Supply voltage rejection vs. frequency



V_{IN}=2V +/- 200mV, V_{OUT}= 1V, C_{OUT}=1µF

AM13865V1

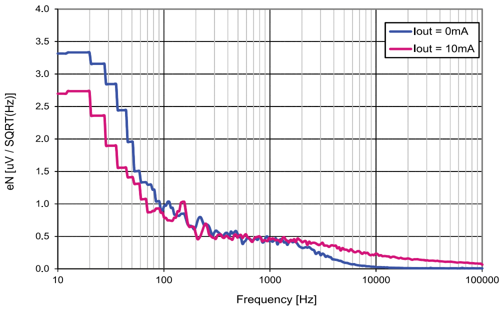
Figure 15: Supply voltage rejection vs. input voltage



I_{OUT}=30mA, V_{OUT}= 1V, C_{OUT} =1µF

AM13866V1

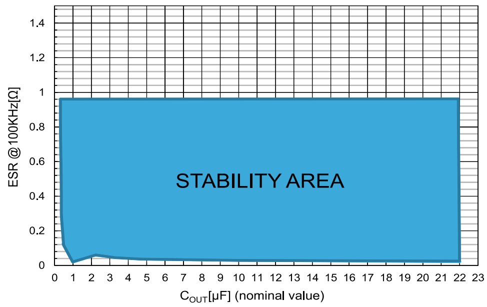
Figure 16: Output noise spectral density



V_{IN} = 2.0V, V_{OUT} = 1.0V, C_{IN} = C_{OUT} =1µF

AM13867V1

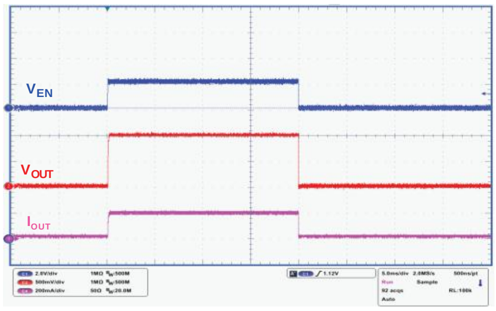
Figure 17: Stability area vs (COUT, ESR)



V_{IN} from 2 to 5.5V, I_{OUT} from 0 to 200mA, C_{IN}=1µF

AM13868V1

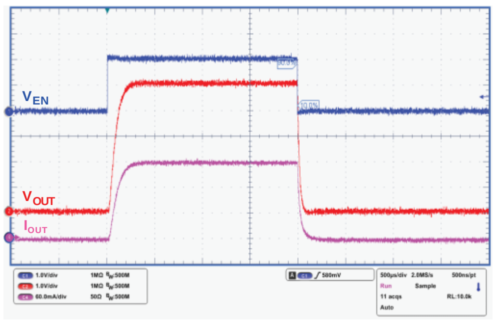
Figure 18: Enable startup (VOUT = 1 V)



V_{IN}=2V, V_{EN}=0V to V_{IN}, I_{OUT}=0.2A , V_{OUT}=1V, T_r=5µs

AM13869V1

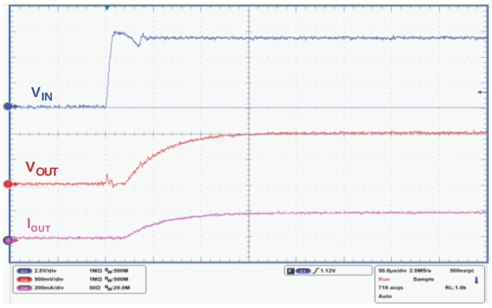
Figure 19: Enable startup (VOUT = 5 V)



V_{IN}=5.5V, V_{EN}=0V to 2V, I_{OUT}=0.2A , V_{OUT}=5V, T_r=5µs

AM13870V1

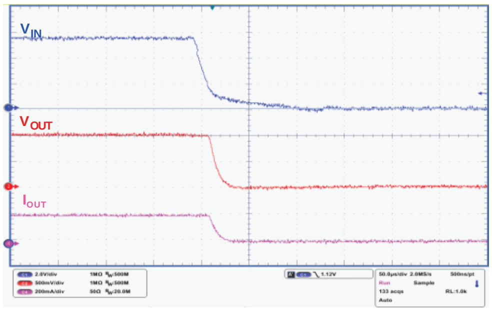
Figure 20: Turn-on time (VOUT = 1 V)



V_{IN}=V_{EN}= from 0V to 5.5V, I_{OUT}=0.2A , V_{OUT}=1V, T_r=5µs

AM13871V1

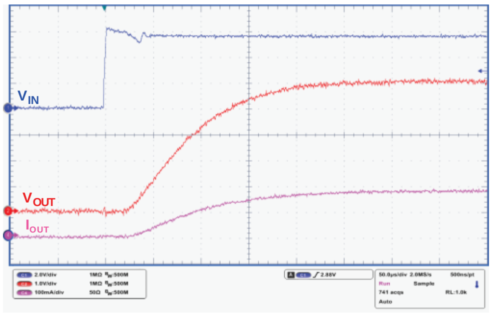
Figure 21: Turn-off time (VOUT = 1 V)



V_{IN}= V_{EN}= from 5.5V to 0V, I_{OUT}= 0.2A, V_{OUT}= 1V, T_f= 5µs

AM13872V1

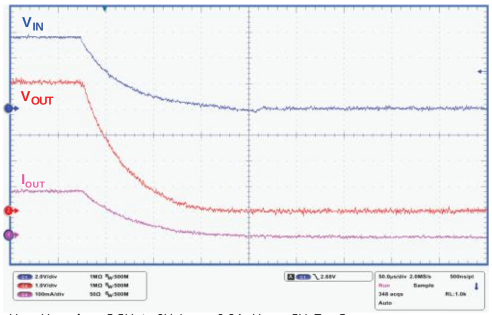
Figure 22: Turn-on time (VOUT = 5 V)



V_{IN}=V_{EN}= from 0V to 5.5V, I_{OUT}=0.2A , V_{OUT}=5V, T_r=5µs

AM13873V1

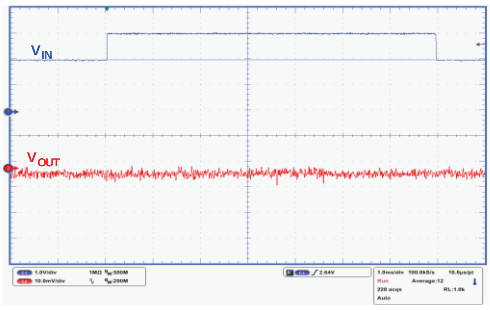
Figure 23: Turn-off time (VOUT = 5 V)



V_{IN}= V_{EN}= from 5.5V to 0V, I_{OUT}= 0.2A, V_{OUT}= 5V, T_f= 5µs

AM13874V1

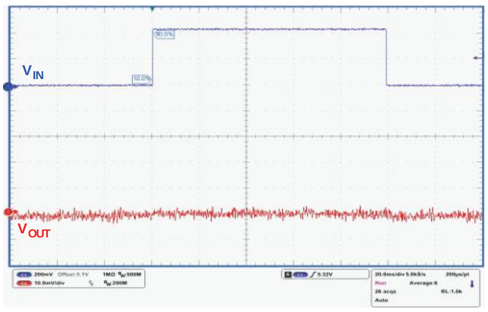
Figure 24: Line transient (VOUT = 1 V)



V_{IN}=V_{EN}=from 2V to 3V , I_{OUT}=10mA , V_{OUT}= 1V, T_r=T_f=5µs

AM13875V1

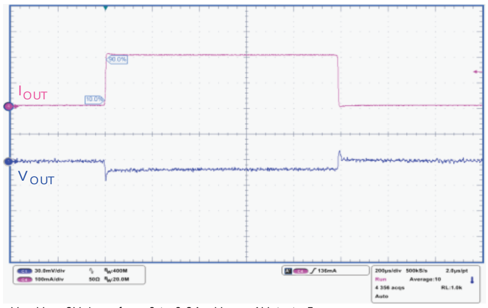
Figure 25: Line transient (VOUT = 5 V)



V_{IN}=V_{EN}=from 5.1V to 5.5V , I_{OUT}=10mA , V_{OUT}= 5V, T_r=T_f=5µs

AM13876V1

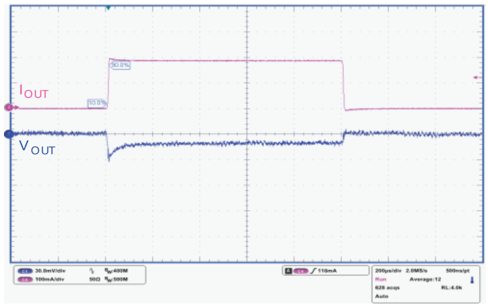
Figure 26: Load transient (VOUT = 1 V)



$V_{IN}=V_{EN}=2V$, I_{OUT}=from 0 to 0.2A , V_{OUT}= 1V, $t_r=t_f=5\mu s$

AM13877V1

Figure 27: Load transient (VOUT = 5 V)



$V_{IN}=V_{EN}=5.5V$, I_{OUT}=from 0 to 0.2A , V_{OUT}= 5V, $t_r=t_f=5\mu s$

AM13878V1

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.2 DFN4 1x1 package info

Figure 28: DFN 1x1-4L drawing

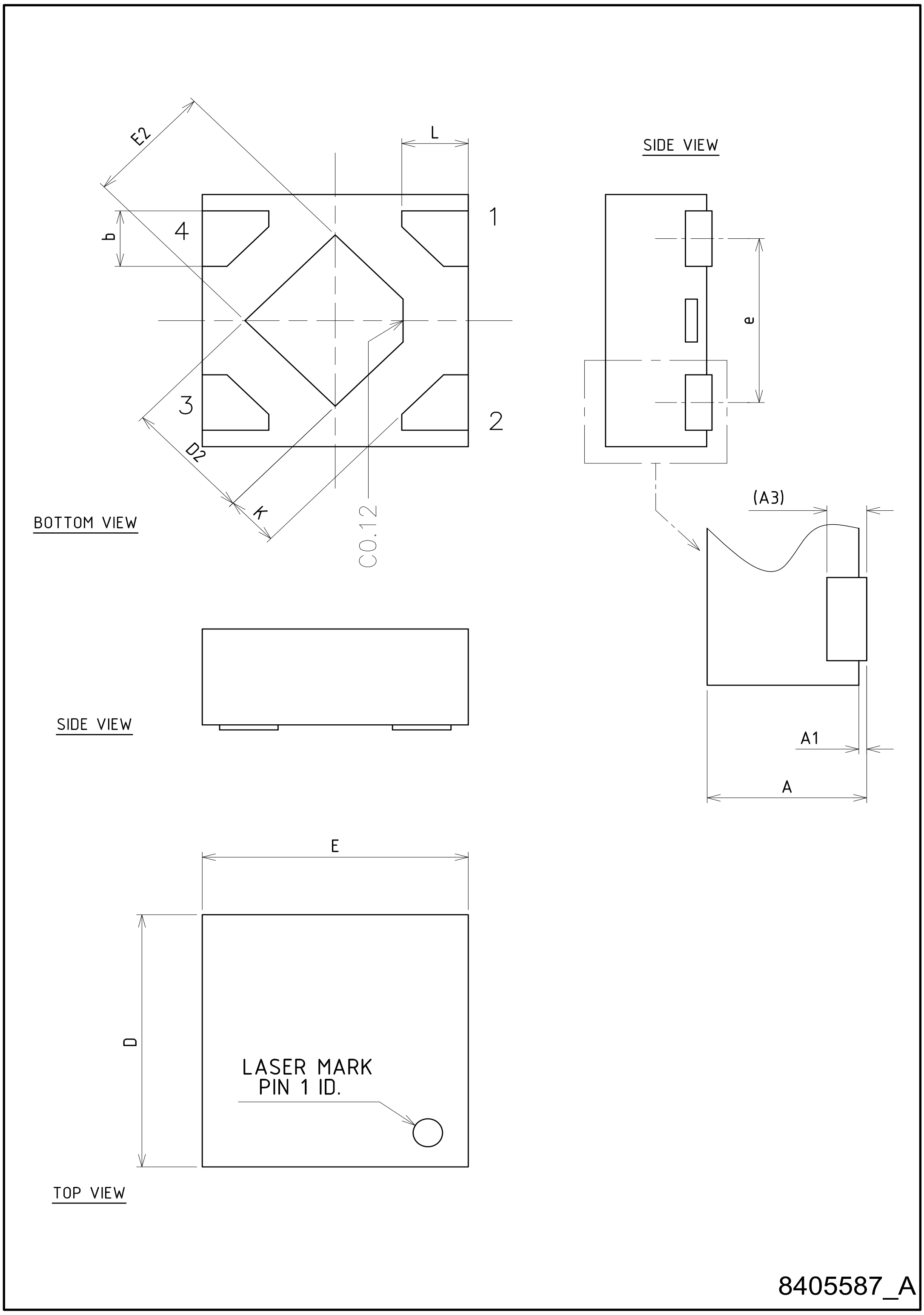
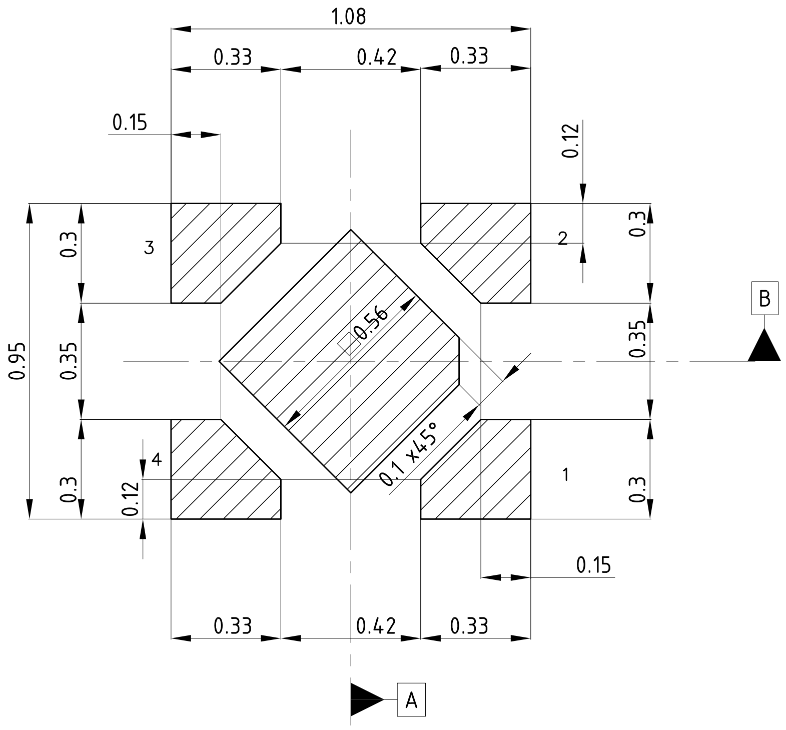


Table 7: DFN 1x1-4L mechanical data

Dim.	mm.		
	Min.	**Typ.**	**Max.**
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3		0.10	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
D2	0.43	0.48	0.53
E	0.95	1.00	1.05
E2	0.43	0.48	0.53
e		0.65	
L	0.20	0.25	0.30
K	0.15		

Figure 29: DFN 1x1-4L footprint



Notes:

1) This footprint is able to ensure insulation up to 10 Vrms (according to CEI IEC 664-1)

2) The device must be positioned within ⌖ | 0.02 | A | B

8405587_A

9 Order codes

Table 8: Order codes

Order code	Output voltage (V)	Auto-discharge	Tolerance (%)	Marking
LD39020ADTPU08R(1)	0.8	Yes	0.5	A1
LD39020DTPU08R			2	08
LD39020ATPU08R(1)		No	0.5	B1
LD39020TPU08R(1)			2	C1
LD39020ADTPU095R(1)	0.95	Yes	0.5	A2
LD39020DTPU095R			2	95
LD39020ATPU095R(1)		No	0.5	B2
LD39020TPU095R(1)			2	C2
LD39020ADTPU10R(1)	1	Yes	0.5	A3
LD39020DTPU10R			2	10
LD39020ATPU10R(1)		No	0.5	B3
LD39020TPU10R(1)			2	C3
LD39020ADTPU11R(1)	1.1	Yes	0.5	A4
LD39020DTPU11R			2	11
LD39020ATPU11R(1)		No	0.5	B4
LD39020TPU11R(1)			2	C4
LD39020ADTPU12R(1)	1.2	Yes	0.5	A5
LD39020DTPU12R			2	12
LD39020ATPU12R(1)		No	0.5	B5
LD39020TPU12R(1)			2	C5
LD39020ADTPU13R	1.3	Yes	0.5	AP
LD39020DTPU13R			2	13
LD39020ATPU13R(1)		No	0.5	BP
LD39020TPU13R(1)			2	CP
LD39020ADTPU15R(1)	1.5	Yes	0.5	A6
LD39020DTPU15R			2	15
LD39020ATPU15R(1)		No	0.5	B6
LD39020TPU15R(1)			2	C6
LD39020ADTPU18R(1)	1.8	Yes	0.5	A7
LD39020DTPU18R			2	18
LD39020ATPU18R(1)		No	0.5	B7
LD39020TPU18R(1)			2	C7

Order code	Output voltage (V)	Auto-discharge	Tolerance (%)	Marking
LD39020ADTPU20R(1)	2	Yes	0.5	A8
LD39020DTPU20R			2	20
LD39020ATPU20R(1)		No	0.5	B8
LD39020TPU20R(1)			2	C8
LD39020ADTPU21R(1)	2.1	Yes	0.5	A9
LD39020DTPU21R			2	21
LD39020ATPU21R(1)		No	0.5	B9
LD39020TPU21R(1)			2	C9
LD39020ADTPU25R(1)	2.5	Yes	0.5	AA
LD39020DTPU25R			2	25
LD39020ATPU25R(1)		No	0.5	BA
LD39020TPU25R(1)			2	CA
LD39020ADTPU27R(1)	2.7	Yes	0.5	AB
LD39020DTPU27R			2	27
LD39020ATPU27R(1)		No	0.5	BB
LD39020TPU27R(1)			2	CB
LD39020ADTPU28R(1)	2.8	Yes	0.5	AC
LD39020DTPU28R			2	28
LD39020ATPU28R(1)		No	0.5	BC
LD39020TPU28R(1)			2	CC
LD39020ADTPU285R(1)	2.85	Yes	0.5	AD
LD39020DTPU285R			2	85
LD39020ATPU285R(1)		No	0.5	BD
LD39020TPU285R(1)			2	CD
LD39020ADTPU29R(1)	2.9	Yes	0.5	AE
LD39020DTPU29R			2	29
LD39020ATPU29R(1)		No	0.5	BE
LD39020TPU29R(1)			2	CE
LD39020ADTPU30R(1)	3	Yes	0.5	AF
LD39020DTPU30R			2	30
LD39020ATPU30R(1)		No	0.5	BF
LD39020TPU30R(1)			2	CF
LD39020ADTPU31R(1)	3.1	Yes	0.5	AG
LD39020DTPU31R			2	31
LD39020ATPU31R(1)		No	0.5	BG
LD39020TPU31R(1)			2	CG

Order code	Output voltage (V)	Auto-discharge	Tolerance (%)	Marking
LD39020ADTPU32R[(1)]	3.2	Yes	0.5	AH
LD39020DTPU32R[(1)]			2	32
LD39020ATPU32R[(1)]		No	0.5	BH
LD39020TPU32R[(1)]			2	CH
LD39020ADTPU33R[(1)]	3.3	Yes	0.5	AJ
LD39020DTPU33R			2	33
LD39020ATPU33R[(1)]		No	0.5	BJ
LD39020TPU33R[(1)]			2	CJ
LD39020ADTPU36R[(1)]	3.6	Yes	0.5	AK
LD39020DTPU36R			2	36
LD39020ATPU36R[(1)]		No	0.5	BK
LD39020TPU36R[(1)]			2	CK
LD39020ADTPU40R[(1)]	4	Yes	0.5	AL
LD39020DTPU40R			2	40
LD39020ATPU40R[(1)]		No	0.5	BL
LD39020TPU40R[(1)]			2	CL
LD39020ADTPU47R[(1)]	4.7	Yes	0.5	AM
LD39020DTPU47R			2	47
LD39020ATPU47R[(1)]		No	0.5	BM
LD39020TPU47R[(1)]			2	CM
LD39020ADTPU50R[(1)]	5	Yes	0.5	AN
LD39020DTPU50R			2	50
LD39020ATPU50R[(1)]		No	0.5	BN
LD39020TPU50R[(1)]			2	CN

Notes:

[(1)]Available on request.

10 Revision history

Table 9: Document revision history

Date	Revision	Changes
04-Dec-2013	1	Initial release.
02-Apr-2014	2	Updated *Table 8: "Order codes"*.

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