Atmel ATWINC1500A-MU

IEEE 802.11 b/g/n Network Controller SoC

DATASHEET

Description

ATWINC1500A is a single chip IEEE® 802.11 b/g/n Radio/Baseband/ MAC network controller optimized for low-power mobile applications. ATWINC1500A supports single stream 1x1 802.11n mode providing up to 72Mbps PHY throughput. ATWINC1500A features fully integrated Power Amplifier, LNA, Switch, and Power Management. ATWINC1500A also features an on-chip microcontroller and integrated flash memory for system software. Implemented in 65nm CMOS technology, the ATWINC1500A offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWINC1500A supports 2, 3, and 4 wire Bluetooth coexistence protocols. The ATWINC1500A provides multiple peripheral interfaces including UART, SPI, I^2C, and SDIO. The only external clock source needed for the ATWINC1500A is a high-speed crystal or oscillator with a wide range of reference clock frequencies supported (12-40MHz). The ATWINC1500A is available in QFN packaging.

Features

- IEEE 802.11 b/g/n RF/PH/MAC SoC
- IEEE 802.11 b/g/n (1x1) for up to 72Mbps
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Supports China WAPI security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- Integrated Flash memory for system software
- SPI, SDIO, UART, and I^2C host interfaces
- 2/3/4-wire Bluetooth coexistence interface
- Operating temperature range of -30°C to +85°C
- Power save modes:

  - <4µA Deep Power Down mode typical @3.3V I/O
  - 280µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or host I/O transaction
- Fast boot options:
  - On-Chip Boot ROM (firmware instant boot)
  - SPI flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables
  - Fast AP re-association (150ms)
- On-Chip Network Stack to offload MCU:
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features: TCP, UDP, DHCP, ARP, HTTP, SSL, and DNS

1. Ordering Information

Ordering code	Package[1]	Description
ATWINC1500-MU-T	5x5 QFN	Single 802.11.b/g/n Chip
ATWINC1500-MR210PA	22 X 15mm	Certified module with ATWINC1500A-MU chip and PCB antenna
ATWINC1500-XSTK		Starter kit including XPlained Pro-D21 and an ATWINC1500-MU-XPRO wing board

Note: 1. The QFN package is a qualified Green Package.

2. Package Information

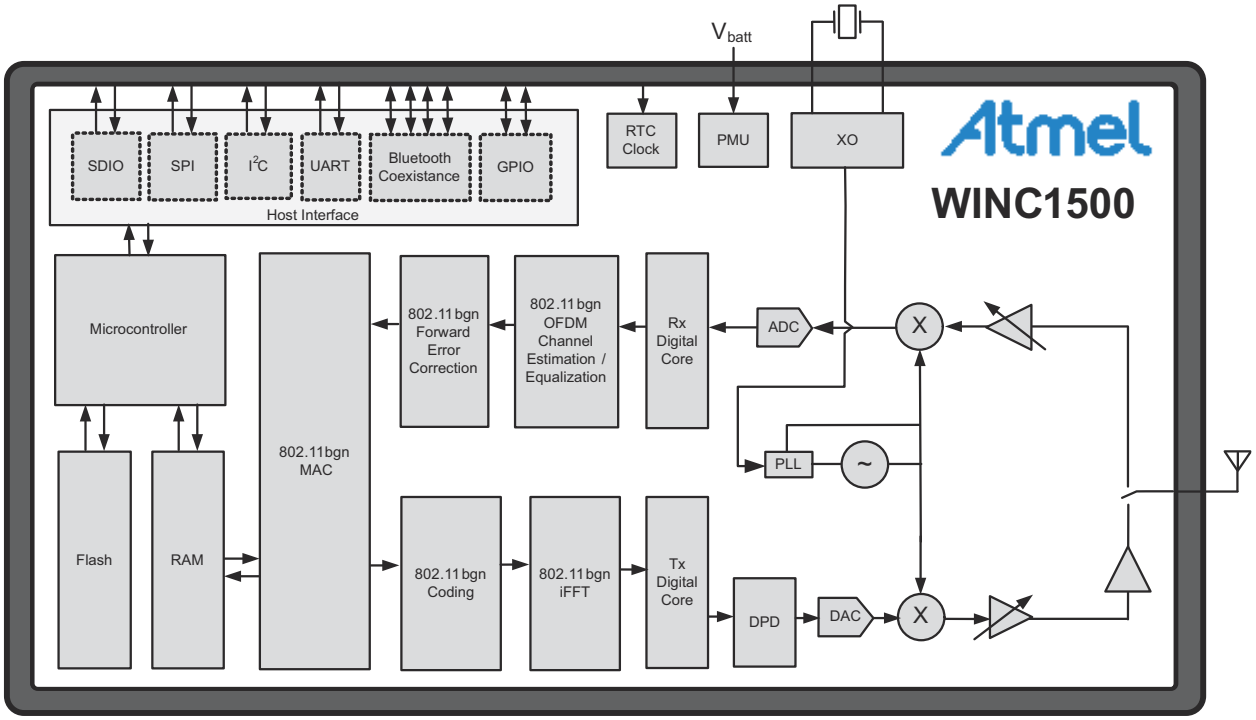
Table 2-1. ATWINC1500-MU QFN Package Information[1]

Parameter	Value	Units	Tolerance
Package Size	5 x 5	mm	±0.1mm
QFN Pad Count	40		
Total Thickness	0.85	mm	±0.05mm
QFN Pad Pitch	0.4	mm	
Pad Width	0.2	mm	
Exposed Pad Size	3.7 x 3.7	mm	

Note: 1. For the details, see “Package Drawing” on page 32.

3. Block Diagram

Figure 3-1. ATWINC1500-MU Block Diagram



4. Pinout Information

ATWINC1500A is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in Figure 4-1. The color shading is used to indicate the pin type as follows: green – power, red – analog, blue – digital I/O, yellow – digital input, grey – unconnected or reserved. The ATWINC1500A pins are described in Table 4-1 on page 6.

Figure 4-1. Pin Assignment

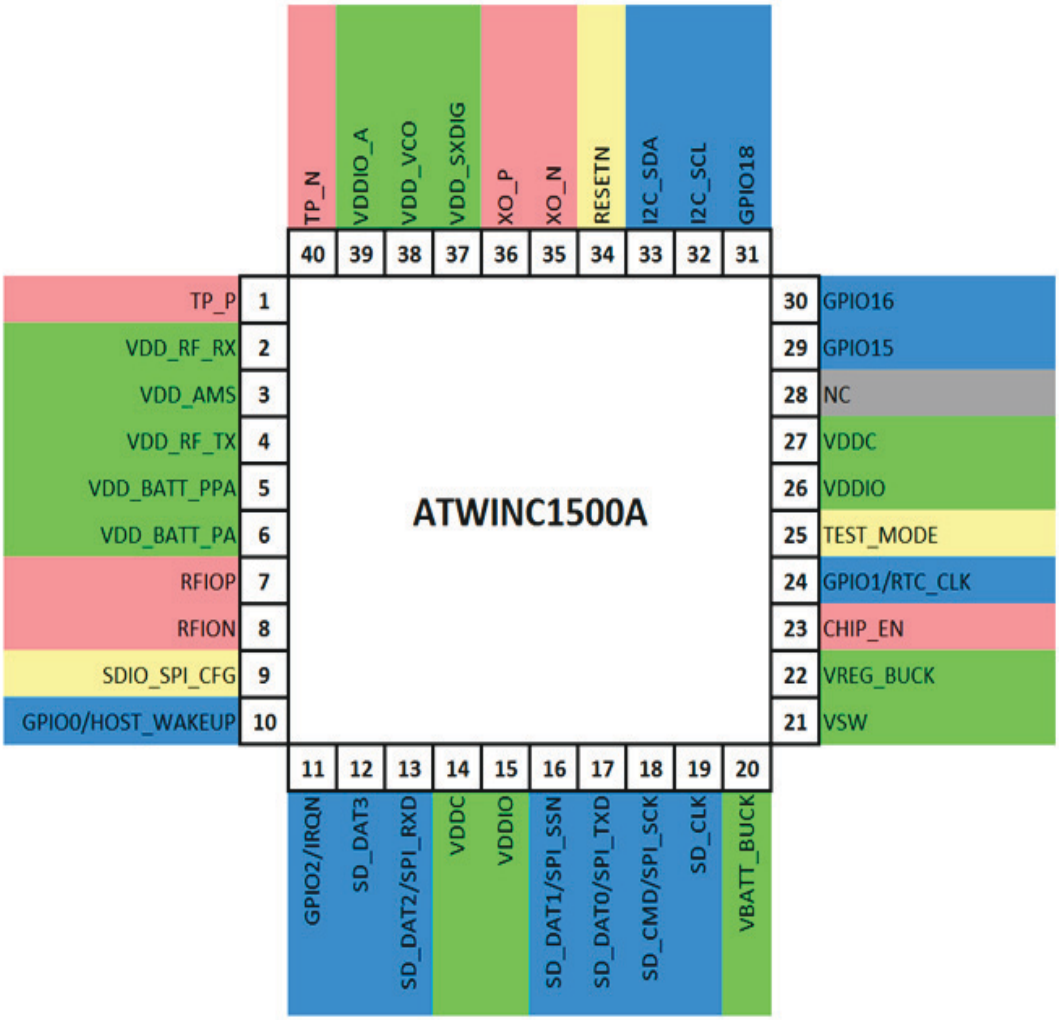


Table 4-1. Pin Description

Pin #	Pin Name	Pull up/down	Description
1	TP_P	Analog	Test Pin / Customer No Connect
2	VDD_RF_RX	Power	Tuner 1.2V RF Supply (See Section 5.1, “Power Architecture” on page 8).
3	VDD_AMS	Power	Tuner BB Supply (See Section 5.1, “Power Architecture” on page 8).
4	VDD_RF_TX	Power	Tuner BB Supply (See Section 5.1, “Power Architecture” on page 8).
5	VDD_BATT_PPA	Power	PA 1st Stage Supply (See Section 5.1, “Power Architecture” on page 8).
6	VDD_BATT_PA	Power	PA 2nd Stage Supply (See Section 5.1, “Power Architecture” on page 8).
7	RFIOP	Analog	Pos RF Differential I/O
8	RFION	Analog	Neg RF Differential I/O
9	SDIO_SPI_CFG	Digital input	Tie to 1 for SPI, 0 for SDIO
10	GPIO0/HOST_WAKE	Digital I/O, Programmable Pull-Up	GPIO0 / SLEEP Mode Control
11	GPIO2/IRQN	Digital I/O, Programmable Pull-Up	GPIO2 / Device Interrupt
12	SD_DAT3	Digital I/O, Programmable Pull-Up	SDIO Data3
13	SD_DAT2/SPI_RXD	Digital I/O, Programmable Pull-Up	SDIO Data2 / SPI Data Rx
14	VDDC	Power	Digital Core Power Supply (See Section 5.1, “Power Architecture” on page 8).
15	VDDIO	Power	Digital I/O Power Supply (See Section 5.1, “Power Architecture” on page 8).
16	SD_DAT1/SPI_SSN	Digital I/O, Programmable Pull-Up	SDIO Data1 / SPI Slave Select
17	SD_DAT0/SPI_TXD	Digital I/O, Programmable Pull-Up	SDIO Data0 / SPI Data Tx
18	SD_CMD/SPI_SCK	Digital I/O, Programmable Pull-Up	SPI Clock
19	SD_CLK	Digital I/O, Programmable Pull-Up	SDIO Command / SPI Clock
20	VBATT_BUCK	Power	Battery Supply for DC/DC Converter (See Section 5.1, “Power Architecture” on page 8).
21	VSW	Power	Switching output of DC/DC Converter (See Section 5.1, “Power Architecture” on page 8).

Table 4-1. Pin Description

Pin #	Pin Name	Pull up/down	Description
22	VREG_BUCK	Power	Core Power from DC/DC Converter (See Section 5.1, “Power Architecture” on page 8).
23	CHIP_EN	Analog	PMU Enable
24	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-Down	GPIO1 / 32kHz Clock Input
25	TEST_MODE	Digital input	Test Mode – Customer Tie to GND
26	VDDIO	Power	Digital I/O Power Supply (See Section 5.1, “Power Architecture” on page 8).
27	VDDC	Power	Digital I/O Power Supply (See Section 5.1, “Power Architecture” on page 8).
28	NC	Power	Customer no connect
29	GPIO15	Digital I/O, Programmable Pull-Up	GPIO15
30	GPIO16	Digital I/O, Programmable Pull-Up	GPIO16
31	GPIO18	Digital I/O, Programmable Pull-Up	GPIO18
32	I2C_SCL	Digital I/O, Programmable Pull-Up	I^2C Slave Clock
33	I2C_SDA	Digital I/O, Programmable Pull-Up	I^2C Slave Data
34	RESETN	Digital input	Active-Low Hard Reset
35	XO_N	Analog	Crystal Oscillator N
36	XO_P	Analog	Crystal Oscillator P
37	VDD_SXDIG	Power	SX Power Supply (See Section 5.1, “Power Architecture” on page 8).
38	VDD_VCO	Power	VCO Power Supply (See Section 5.1, “Power Architecture” on page 8).
39	VDDIO_A	Power	Tuner VDDIO Supply (See Section 5.1, “Power Architecture” on page 8).
40	TP_N	Analog	Test Pin / Customer No Connect
41	PADDLE VSS	Power	Connect to System Board Ground

5. Power Management

5.1 Power Architecture

ATWINC1500A uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in Figure 5-1 on page 9.

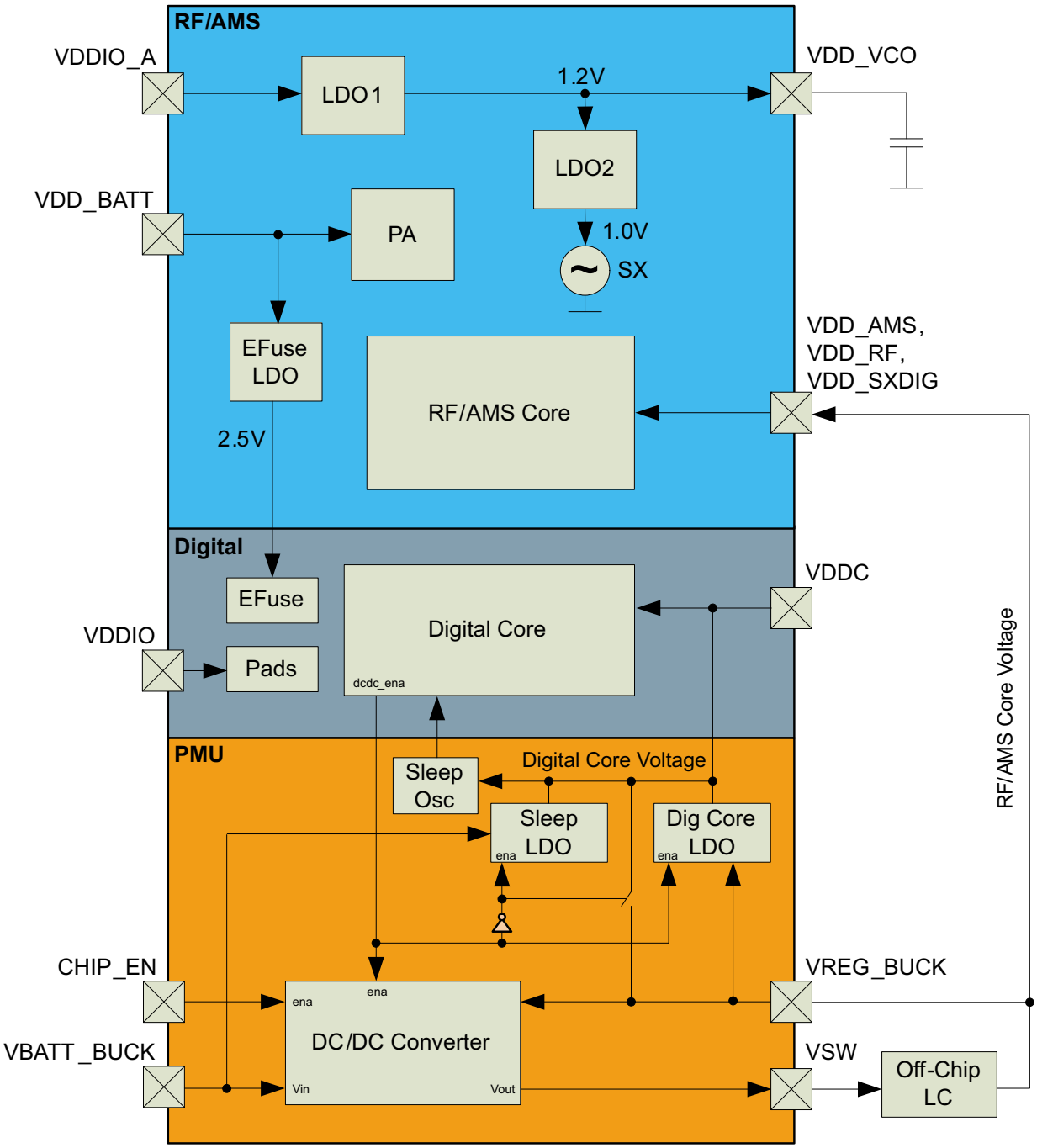
The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. Table 5-1 shows the typical values for the digital and RF/AMS core voltages. The PA and EFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

The power connections in Figure 5-1 provide a conceptual framework for understanding the ATWINC1500A power architecture. Refer to the reference design in Section Section 10., “Reference Design” on page 28 for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

Table 5-1. PMU Output Voltages

Parameters	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.35V
Digital Core Voltage (VDDC)	1.10V

Figure 5-1. ATWINC1500-MU Power Architecture



5.2 Power Consumption

5.2.1 Description of Device States

Atmel ATWINC1500-MU device has several Device States:

- **ON_Transmit** - Device is actively transmitting an 802.11 signal
- **ON_Receive** - Device is actively receiving an 802.11 signal
- **ON_Doze** - Device is on but is neither transmitting nor receiving
- **Power_Down** - Device is asleep with core supply off
- **Power_Off** - Device is powered off; core and I/O supply are off

5.2.2 Controlling the Device States

Table 5-2 shows how to switch between the device states using the following:

- **CHIP_EN** - Device pin (pin #23) used to enable DC/DC Converter
- **VDDIO** - I/O supply voltage from external supply

Table 5-2. ATWINC1500-MU Device State Control

Device State	CHIP_EN	VDDIO	Remark	Power Consumption	
				I_{VBATT}	I_{VDDIO}
ON_Transmit	VDDIO	On	Transmitting(1)	230mA	29mA
ON_Receive	VDDIO	On	Receiving	68mA	29mA
ON_Doze	VDDIO	On	Idle(2)	280µA	<10µA
Power_Down	GND	On		<0.5µA	<0.2µA
Power_Off	GND	GND		0	0

Note: 1. The output power is 18dBm
2. The device is Idle in ON_Doze state during Passive Scan waiting for the Beacon Signal

5.2.3 Restrictions for Power_Off State

When ATWINC1500A is in the Device State Power_Off, there is no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the ATWINC1500A pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

5.3 Power-Up Sequence

The power-up sequence for ATWINC1500A is shown in Figure 5-2 on page 11. The timing parameters are provided in Table 5-3 on page 11.

Figure 5-2. Power-up Sequence

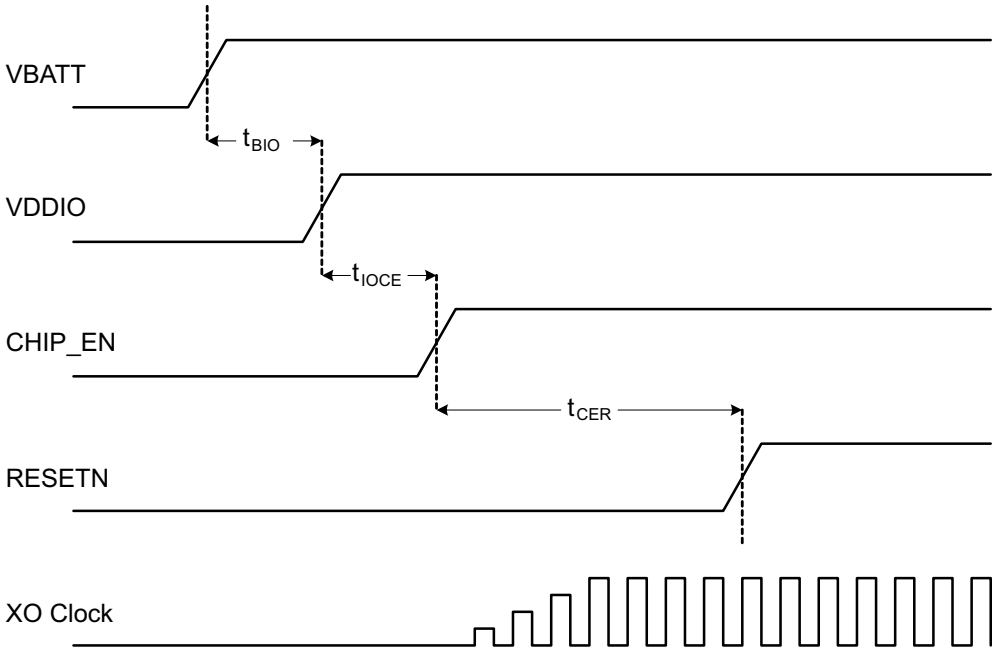


Table 5-3. Power-up Sequence Timing

Parameter	Min	Max	Units	Description	Notes
t_{BIO}	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together.
t_{IOCE}	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_{CER}	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.

6. CPU and Memory Subsystem

6.1 Processor

ATWINC1500A has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and

MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

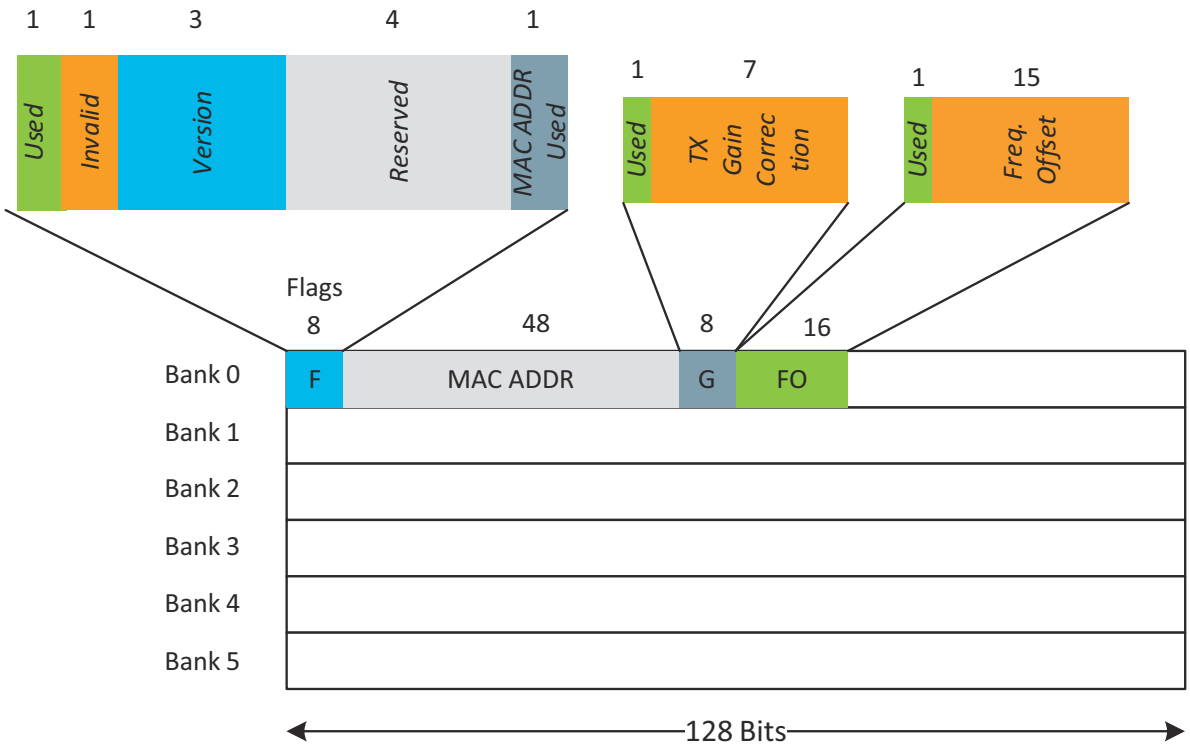
6.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 128KB instruction RAM and a 64KB data RAM. ATWINC1500A also has 4Mb of flash memory, which can be used for system software. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

6.3 Non-Volatile Memory (EFuse)

ATWINC1500A has 768 bits of non-volatile EFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The EFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 6-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating MAC address. Refer to ATWINC1500A Programming Guide for the EFuse programming instructions.

Figure 6-1. EFuse Bit Map



7. Clocking

7.1 Crystal Oscillator

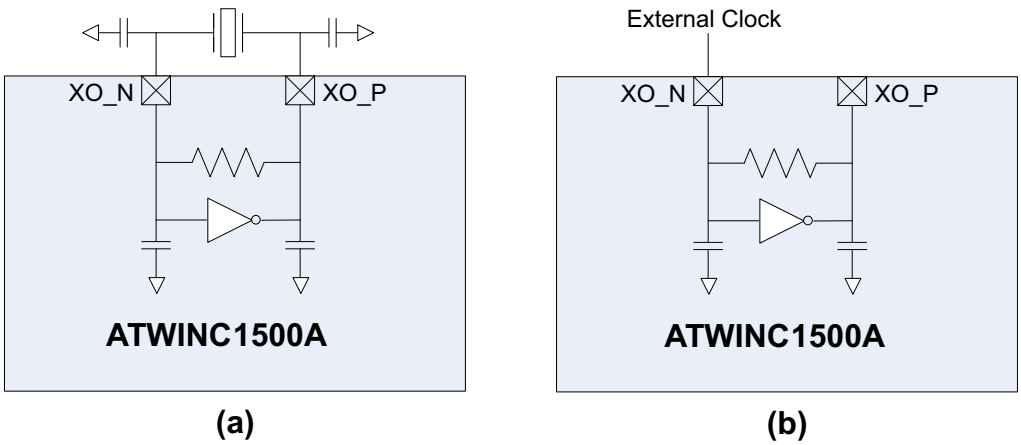
Table 7-1. ATWINC1500-MU Crystal Oscillator Parameters

Parameter	Min	Typical	Max	Units
Crystal Resonant Frequency	12	26	40	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability – Initial Offset (1)	-100		100	ppm
Stability - Temperature and Aging	-25		25	ppm

Notes: 1. Initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in Figure 7-1(a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5pF can be applied to the XO_N terminal as shown Figure 7-1(b).

Figure 7-1. ATWINC1500-MU XO Connections to Crystal



(a) the crystal oscillator is used, and (b) the crystal oscillator is bypassed

Table 7-2. ATWINC1500-MU Bypass Clock Specification

Parameter	Min	Max	Units	Comments
Oscillator frequency	12	32	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.5	1.2	Vpp	Must be AC coupled
Stability - Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

7.2 Low Power Oscillator

ATWINC1500A has an internally-generated 32kHz clock to provide timing information for various sleep functions. Alternatively, ATWINC1500A allows for an external 32kHz clock to be used for this purpose, which is provided through Pin 24 (RTC_CLK). Software selects whether the internal clock or external clock is used.

The internal low-power clock is ring-oscillator based and has accuracy within 10,000ppm. When using the internal low-power clock, the advance walk-up time in beacon monitoring mode has to be increased by about 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, walk-up time has to be increased by 1ms.

For any application targeting very low power consumption, an external 32kHz RTC clock should be used.

8. WLAN Subsystem

The WLAN subsystem is composed by the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

8.1 MAC

8.1.1 Features

The Atmel ATWINC1500-MU IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/HCCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

8.1.2 Description

The ATWINC1500A MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a

programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

8.2 PHY

8.2.1 Features

The Atmel ATWINC1500-MU IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

8.2.2 Description

The ATWINC1500A WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

8.3 Radio

8.3.1 Receiver Performance

Table 8-1. ATWINC1500-MU Receiver Performance

Parameter	Description	Min	Typical	Max	Unit
Frequency		2.412		2.484	MHz
Sensitivity 802.11b	1Mbps DSS		-98		dBm
	2Mbps DSS		-94		dBm
	5.5Mbps DSS		-92		dBm
	11Mbps DSS		-88		dBm
Sensitivity 802.11g	6Mbps OFDM		-90		dBm
	9Mbps OFDM		-89		dBm
	12Mbps OFDM		-88		dBm
	18Mbps OFDM		-85		dBm
	24Mbps OFDM		-83		dBm
	36Mbps OFDM		-80		dBm
	48Mbps OFDM		-76		dBm
	54Mbps OFDM		-74		dBm
Sensitivity 802.11n (BW = 20MHz)	MCS 0		-89		dBm
	MCS 1		-87		dBm
	MCS 2		-85		dBm
	MCS 3		-82		dBm
	MCS 4		-77		dBm
	MCS 5		-74		dBm
	MCS 6		-72		dBm
	MCS 7		-71		dBm
Maximum Receive Signal Level	1-11Mbps DSS	-10	0		dBm
	6-54Mbps OFDM	-10	0		dBm
	MCS 0 - 7	-10	0		dBm

Table 8-1. ATWINC1500-MU Receiver Performance (Continued)

Parameter	Description	Min	Typical	Max	Unit
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		dB
	6Mbps OFDM (25MHz offset)		40		dB
	54Mbps OFDM (25MHz offset)		25		dB
	MCS 0 - 20MHz BW (25MHz offset)		40		dB
	MCS 7 - 20MHz BW (25MHz offset)		20		dB
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		dBm
	880-915MHz GSM		-10		dBm
	1710-1785MHz GSM		-15		dBm
	1850-1910MHz GSM		-15		dBm
	1850-1910MHz WCDMA		-24		dBm
	1920-1980MHz WCDMA		-24		dBm

8.3.2 Transmitter Performance

Table 8-2. ATWINC1500-MU Transmitter Performance

Parameter	Description	Min	Typical	Max	Unit
Frequency		2.412		2.484	MHz
Output Power	802.11b DSSS 1Mbps		20.6(1)		dBm
	802.11b DSSS 11Mbps		20.6(1)		dBm
	802.11g OFDM 6Mbps		20.5(1)		dBm
	802.11g OFDM 54Mbps		17.8		dBm
	802.11n HT20 MCS 0		18.8(1)		dBm
	802.11n HT20 MCS 7		15.3(1)		dBm
Tx Power Accuracy			±1.5(2)		dB
Carrier Suppression			30.0		dBc

Table 8-2. ATWINC1500-MU Transmitter Performance (Continued)

Parameter	Description	Min	Typical	Max	Unit
Out of Band Transmit Power	76-108		-125		dBm/Hz
	776-794		-125		dBm/Hz
	869-960		-125		dBm/Hz
	925-960		-125		dBm/Hz
	1570-1580		-125		dBm/Hz
	1805-1880		-125		dBm/Hz
	1930-1990		-125		dBm/Hz
	2110-2170		-125		dBm/Hz
Harmonic Output Power	2^{nd}		-33		dBm/MHz
	3^{rd}		-38		dBm/MHz

Note: 1. Measured at 802.11 spec compliant EVM / Spectral Mask.
2. Without calibration.

9. External Interfaces

ATWINC1500A external interfaces include I²C Slave for control, SPI Slave and SDIO Slave for control and data transfer, I²C Master for external EEPROM, UART for debug, control, and data transfer, General Purpose Input / Output (GPIO) pins, and a Wi-Fi / Bluetooth coexistence interface. With the exception of the SPI Slave and SDIO Slave host interfaces, which are selected using the dedicated SDIO_SPI_CFG pin, the other interfaces can be assigned to various pins by programming the corresponding pin muxing control register for each pin to a specific value between 0 and 6.The default values of these registers are 0, which is GPIO mode. The summary of the available interfaces and their corresponding pin mux settings is shown in Table 9-1. For specific programming instructions refer to ATWINC1500A Programming Guide.

Table 9-1. Pin-Mux Matrix of External Interfaces

Pin name	Mux 0	Mux 1	Mux 2	Mux 3	Mux 4	Mux 6
GPIOO/HOST_WAKE	GPIO_0	I_HOST_WAKEUP		O_UART_TXD	IO_12C_MASTER_SCL	IO_COE
GPIO2/IRQN	GPIO_2	O_IRQN		I_UART_RXD		IO_COE
SD_DAT3	GPIO_7	IO_SD_DAT3		O_UART_TXD		IO_COE
SD_DAT2/SPI_RXD		IO_SD_DAT2	I_SPI_RXD			
SD_DAT1/SPI_SSN		IO_SD_DAT1	IO_SPI_SSN			
SD_DAT0/SPI_TXD		IO_SD_DAT0	O_SPI_TXD			
SD_CMD/SPI_SCK		IO_SD_CMD	IO_SPI_SCK			
SD_CLK	GPIO_8	I_SD_CLK		I_UART_RXD		IO_COE
GPIO/RTC_CLK	GPIO_1	I_RTC_CLK		I_UART_RXD	IO_12C_MASTER_SDA	IO_COE
GPIO15	GPIO_15					
GPIO16	GPIO_16		IO_12C_MASTER_SCL			
GPIO18	GPIO_18					
12C_SCL		IO_12C_SCL		I_RTC_CLK	IO_12C_MASTER_SCL	IO_COE
12C_SDA		IO_12C_SDA			IO_12C_MASTER_SDA	IO_COE

9.1 I²C Slave Interface

Description

The I²C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA, Pin 33) and a serial clock (SCL, Pin 32). It responds to the seven bit address value 0x60. The ATWINC1500A I²C supports I²C bus Version 2.1 - 2000 and can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”.

9.1.1 I²C Timing

The I²C slave timing is provided in Figure 9-1 and in Table 9-2 on page 20.

Figure 9-1. ATWINC1500-MU I²C Slave Timing Diagram

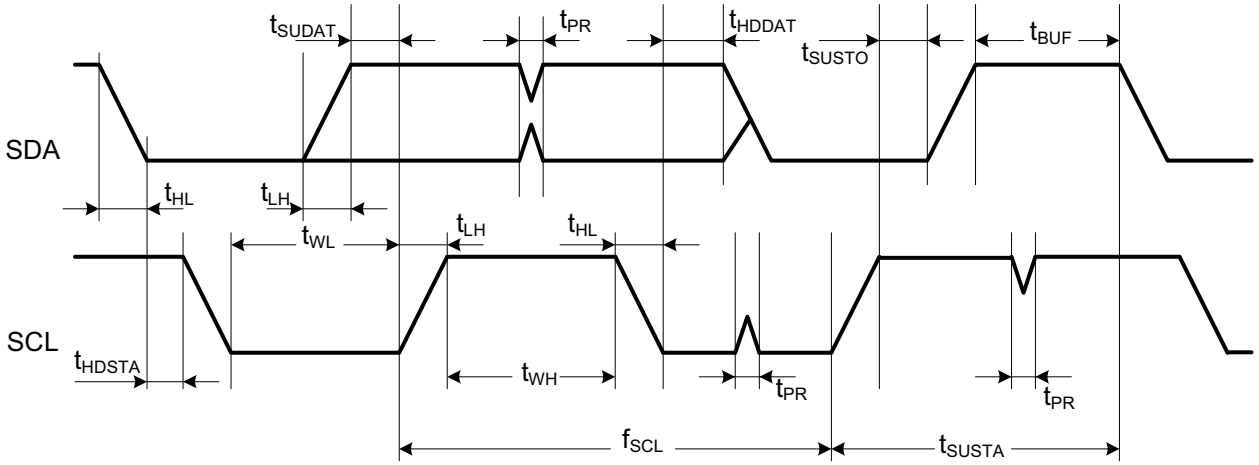


Table 9-2. ATWINC1500-MU I²C Slave Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL clock frequency	f_{SCL}	0	400	kHz	
SCL low pulse width	t_{WL}	1.3		µs	
SCL high pulse width	t_{WH}	0.6		µs	
SCL, SDA fall time	t_{HL}		300	ns	
SCL, SDA rise time	t_{LH}		300	ns	This is dictated by external components
START setup time	t_{SUSTA}	0.6		µs	
START hold time	t_{HDSTA}	0.6		µs	
SDA setup Time	t_{SUDAT}	100		ns	
SDA hold time	t_{HDDAT}	0		ns	Slave and Master default
		40		ns	Master programming option
STOP setup time	t_{SUSTO}	0.6		µs	
Bus free time between STOP and START	t_{BUF}	1.3		µs	
Glitch pulse reject	t_{PR}	0	50	ns	

9.2 I²C Master Interface

Description

ATWINC1500A provides an I²C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I²C Master is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA can be configured on one of the following pins: GPIO1 (pin 24) or I2C_SDA (pin 33). SCL can be configured on one of the following pins: GPIO0 (pin 10) or I2C_SCL (pin 32). For more specific instructions refer to ATWINC1500A Programming Guide.

The I²C Master interface supports three speeds:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The timing diagram of the I²C Master interface is the same as that of the I²C Slave interface (see Figure 9-1 on page 20). The timing parameters of I²C Master are shown in Table 9-3.

Table 9-3. ATWINC1500-MU I²C Master Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		High speed mode		Units
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL low pulse width	t_{WL}	4.7		1.3		1.16		µs
SCL high pulse width	t_{WH}	4		0.6		0.06		µs
SCL fall time	t_{HLSCL}		300		300	10	40	ns
SDA fall time	t_{HLSDA}		300		300	10	80	ns
SCL rise time	t_{LHSCL}		1000		300	10	40	ns
SDA rise time	t_{LHSDA}		1000		300	10	80	ns
START setup time	t_{SUSTA}	4.7		0.6		0.16		µs
START hold time	t_{HDSTA}	4		0.6		0.16		µs
SDA setup Time	t_{SUDAT}	250		100		10		ns
SDA hold time	t_{HDDAT}	5		40		0	70	ns
STOP setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus free time between STOP and START	t_{BUF}	4.7		1.3				µs
Glitch pulse reject	t_{PR}			0	50			ns

9.3 SPI Slave Interface

9.3.1 Description

ATWINC1500A provides a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown inTable 9-4. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 9-4. ATWINC1500-MU SPI Slave Interface Pin Mapping

Pin #	SPI Function
9	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
18	SCK: Serial Clock
13	RXD: Serial Data Receive (MOSI)
17	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions refer to ATWINC1500A Programming Guide.

9.3.2 SPI Slave modes

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 9-5 and inTable 9-2 on page 20. The red lines in Figure 9-2 on page 23 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 9-5. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

9.3.3 SPI Timing

The SPI timing is provided in Figure 9-3 and in Table on page 24

Figure 9-2. SPI Slave Clock Polarity and Clock Phase Timing

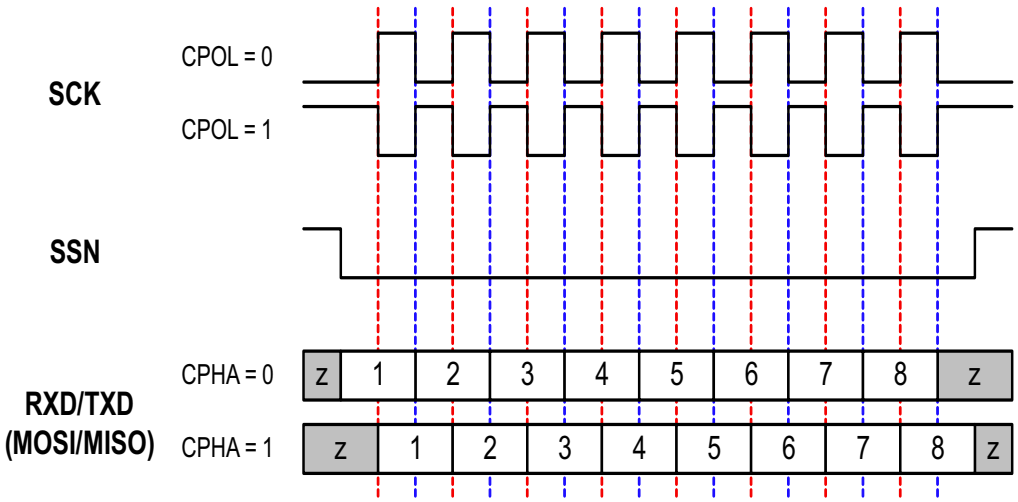


Figure 9-3. ATWINC1500-MU SPI Timing Diagram

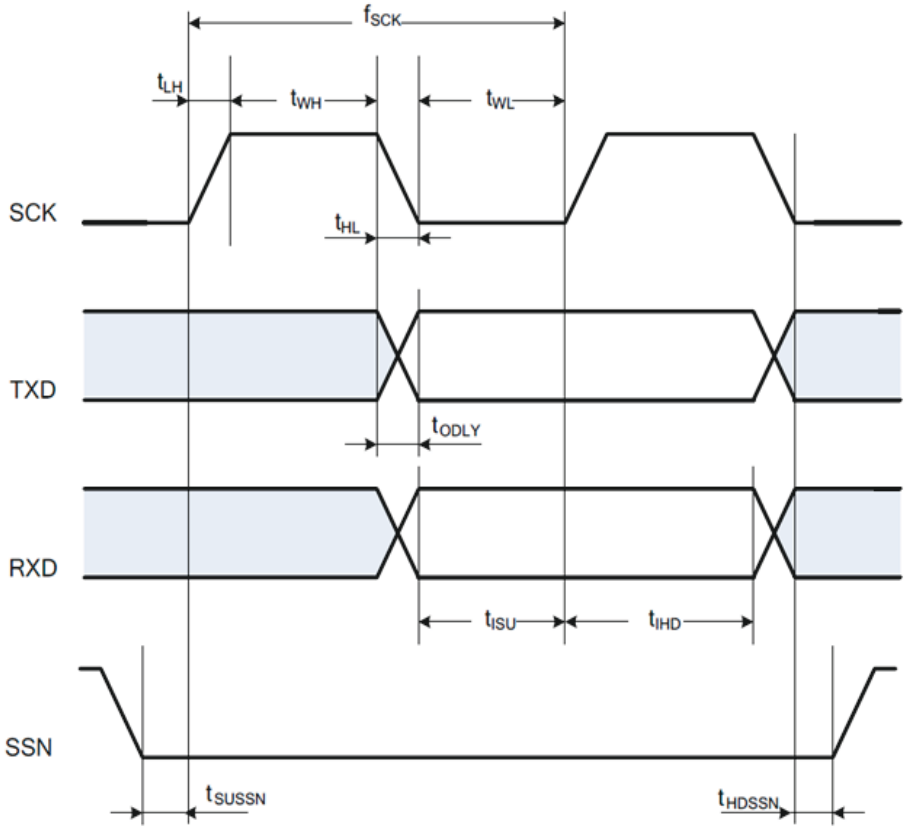


Table 9-6. ATWINC1500-MU SPI Slave Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock input frequency	f_{SCK}		48	MHz
Clock low pulse width	t_{WL}	15		ns
Clock high pulse width	t_{WH}	15		ns
Clock rise time	t_{LH}		10	ns
Clock fall time	t_{HL}		10	ns
Input setup time	t_{ISU}	5		ns
Input hold time	t_{IHD}	5		ns
Output Delay	t_{ODLY}	0	20	ns
Slave select setup time	t_{SUSSN}	5		ns
Slave select hold time	t_{HDSSN}	5		ns

9.4 SDIO Slave Interface

The SD memory card communication is based on an advanced 9-pin interface (Clock, Command, 4 Data and 3 Power lines) designed to operate at maximum operating frequency of 50MHz.

9.4.1 Features

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 and 50MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to Direct read/write (IO52) and Extended read/write (IO53) transactions
- Supports Suspend/Resume operation

9.4.2 Description

The ATWINC1500A SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWINC1500A for data DMA. To use this interface, pin 9 (SDIO_SPI_CFG) must be grounded. The SDIO Slave pins are mapped as shown in Table 9-7.

Table 9-7. ATWINC1500-MU SDIO Interface Pin Mapping

Pin #	SPI Function
9	CFG: Must be tied to ground
12	DAT3: Data 3
13	DAT2: Data 2
16	DAT1: Data 1

Table 9-7. ATWINC1500-MU SDIO Interface Pin Mapping (Continued)

Pin #	SPI Function
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card will identify itself as an SDIO device. The host software will obtain the card information in a tuple (linked list) format and determine if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

9.4.3 SDIO Timing

The SDIO Slave interface timing is provided in Figure 9-4 on page 25 and Table 9-8 on page 25

Figure 9-4. ATWINC1500-MU SDIO Timing Diagram

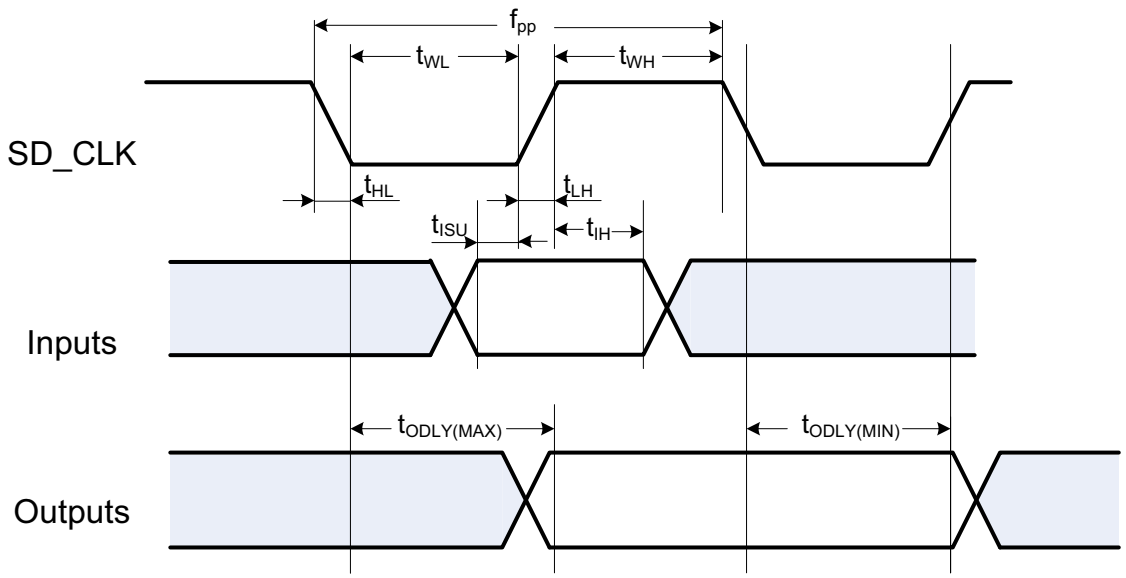


Table 9-8. ATWINC1500-MU SDIO Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock input frequency	f_{pp}	0	50	MHz
Clock low pulse width	t_{WL}	10		ns
Clock high pulse width	t_{WH}	10		ns
Clock rise time	t_{LH}		10	ns
Clock fall time	t_{HL}		10	ns
Input setup time	t_{ISU}	5		ns
Input hold time	t_{IH}	5		ns
Output Delay	t_{ODLY}	0	14	ns

9.5 UART

ATWINC1500A has a Universal Asynchronous Receiver/Transmitter (UART) interface for serial communication. It is intended primarily for debugging, and it can also be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where ATWINC1500A operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface, where RXD can be enabled on one of four alternative pins and TXD can be enabled on one of three alternative pins by programming their corresponding pin mux control registers to 3 (see Table 9-1 on page 19).

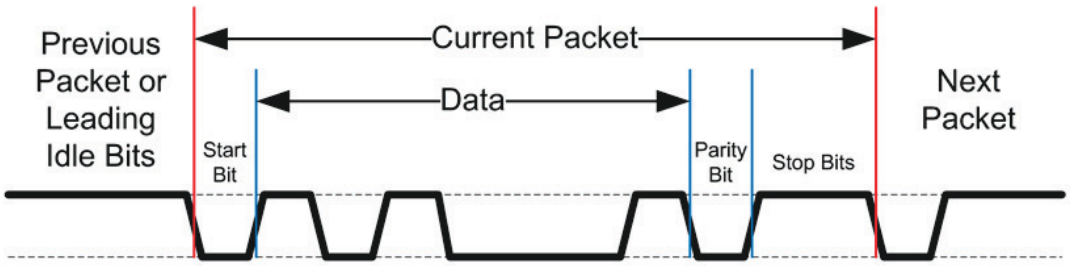
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and 3 fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz / 8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has Rx and Tx FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both Rx and Tx direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 9-5 on page 26. This example shows 7-bit data (0x45), odd parity, and two stop bits.

For more specific instructions refer to ATWINC1500A Programming Guide.

Figure 9-5. Example of UART Rx or Tx



9.6 Wi-Fi / Bluetooth Coexistence

ATWINC1500A supports 2-wire, 3-wire, and 4-wire WiFi/Bluetooth Coexistence signaling, conforming to the IEEE 802.15.2-2003 standard, Part 15.2. The type of coexistence interface used (2-, 3-, or 4-wire) is chosen to be compatible with the specific Bluetooth device used in a given application. Table 9-9 on page 27 shows a usage example of the 2-wire interface using the GPIO0/HOST_WAKE and GPIO1/RTC_CLK pins; 3-wire interface using the GPIO0/HOST_WAKE, GPIO1/RTC_CLK, and SD_DAT3 pins; and 4-wire interface using the GPIO0/HOST_WAKE, GPIO1/RTC_CLK, SD_DAT3, and SD_CLK pins. For more specific instructions on configuring Coexistence refer to ATWINC1500A Programming Guide.

Table 9-9. ATWINC1500-MU Coexistence Pins

Pin Name	Pin #	2-wire	3-wire	4-wire
GPIO0/HOST_WAKE	10	Used	Used	Used
GPIO1/RTC_CLK	24	Used	Used	Used
SD_DAT3	12	Not used	Used	Used
SD_CLK	19	Not used	Not used	Used

9.7 GPIOs

Eight General Purpose Input / Output (GPIO) pins, labeled GPIO0, GPIO1, GPIO2, GPIO7, GPIO8, GPIO15, GPIO16, and GPIO18, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are only available when the host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, six GPIOs are available. For more specific usage instructions refer to ATWINC1500A Programming Guide.

10. Reference Design

The reference design schematic for Atmel ATWINC1500A-MU is shown in Figure 10-1 on page 29.

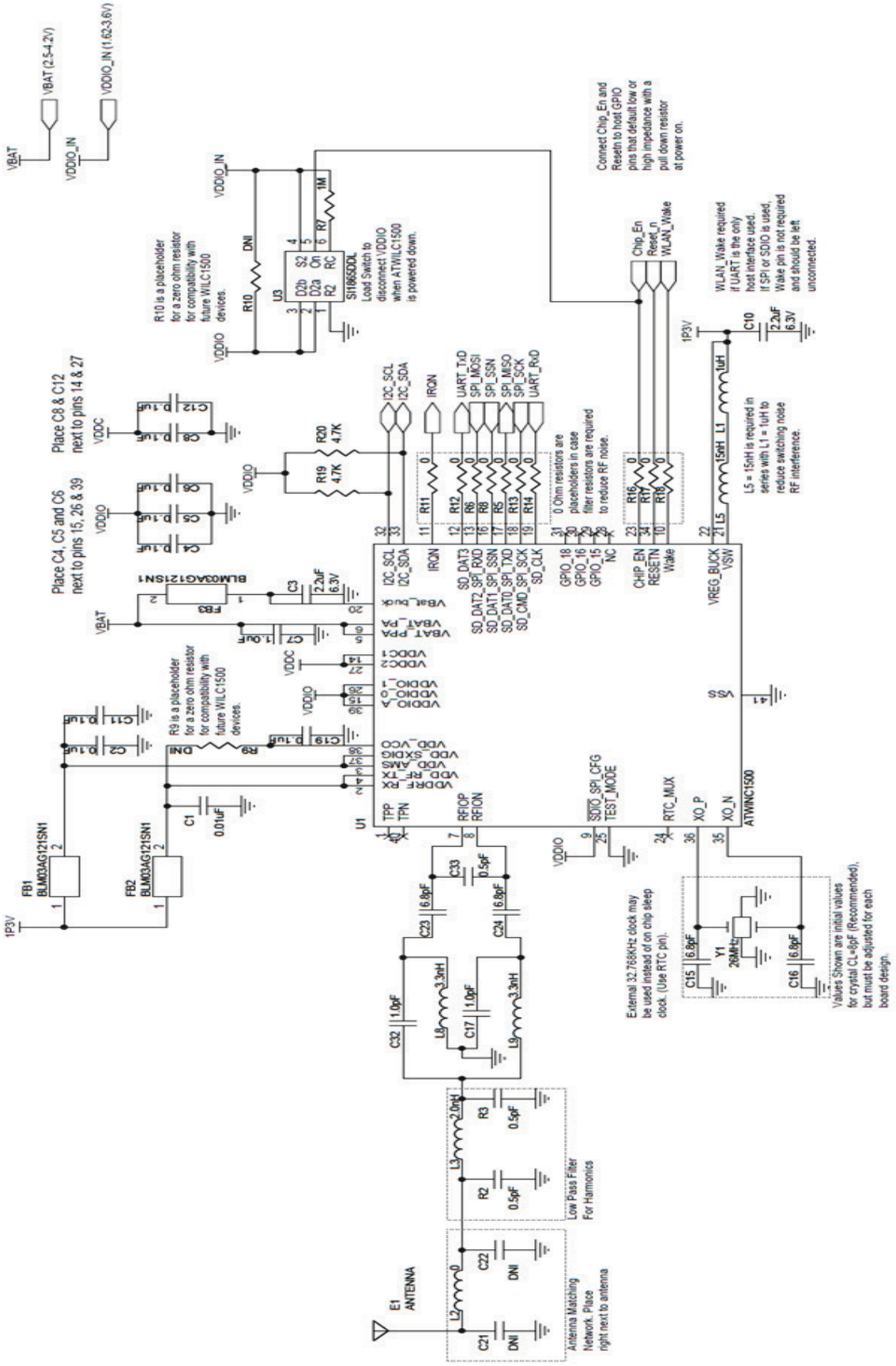
RFIOP and RFION pins must be AC coupled. It is recommended that balun be located right next to the pins – if this is not possible, RFIOP and RFION should be routed as 50Ω differential pair to the balun.

It is recommended to use a load switch for VDDIO to achieve lower power consumption. In the absence of the load switch, when the CHIP_EN pin is low, the I/Os controlling the internal flash memory become high impedance, so the inputs to the flash float causing a large leakage current on the VDDIO supply. When the load switch is used, it is controlled by the CHIP_EN pin: when CHIP_EN is high, the load switch is turned on; when CHIP_EN is low, the load switch is open and VDDIO is disconnected from the chip.

When the VDDIO supply to ATWINC1500A is disconnected, it is important that none of the pins to the chip be driven or pulled high – they should either be set to a low level or high impedance state. If VDDIO is disconnected from the external power supply and a high level is driven onto any pad of the device, the device will be powered up through the diode, which is built into the pad for ESD protection. This means that if any external pull-up resistors are attached to any pins they should be disconnected from the supply when CHIP_EN is low and VDDIO supply is disconnected.

ATWINC1500A provides programmable pull-up resistors on various pins (see Table 4-1 on page 6). The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the device is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100KΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current would be approximately 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float. Refer to ATWINC1500A Programming Guide for information on enabling/disabling the programmable pull-up resistors.

Figure 10-1. Atmel ATWINC1500A-MU Reference Schematic



11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDC	Core Supply Voltage	-0.3	1.5	V
VDDIO	I/O supply voltage	-0.3	5.0	V
VBATT	Battery supply voltage	-0.3	5.0	V
V_{IN} (1)	Digital input voltage	-0.3	VDDIO	V
V_{AIN} (2)	Analog input voltage	-0.3	1.5	V
V_{ESDHBM} (3)	ESD human body model	-1000, -2000	+1000, +2000	V
T_A	Storage temperature	-65	150	°C
	Junction temperature		125	°C
	RF input power max		23	dBm

Notes:
1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, VDD_VCO
3. For V_{ESDHBM}, each pin is classified as Class1 or Class2.
   - The Class1 pins include all the pins (both analog and digital).
   - Class2 are all digital pins only.
   - V_{ESDHBM} is +/-1kV for Class1 pins. V_{ESDHBM} is +/-2kV for Class2 pins.

11.2 Recommended Operating Conditions

Table 11-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
$VDDIO_L$	I/O supply voltage low range	1.62	1.80	2.00	V
$VDDIO_M$	I/O supply voltage mid range (1)	2.00	2.50	3.00	V
$VDDIO_H$	I/O supply voltage high range	3.00	3.30	3.60	V
VBATT	Battery supply voltage (2)	2.50 (3)	3.60	4.20	V
	Operating temperature	-30		85	°C

Note:
1. I/O supply voltage is applied to the following pins: VDDIO_A, VDDIO
2. Battery supply voltage is applied to following pins: VDD_BATT_PPA, VDD_BATT_PA, VBATT_BUCK
3. The Atmel ATWINC1500-MU is functional across this range of voltages; however, optimal RF performance is guaranteed for VBATT in the range 3.0V < VBATT < 4.2V.
4. Refer to Section 5.1, “Power Architecture” for the details of power connections

11.3 DC Characteristics

The Table 11-3 provides the DC characteristics for the digital pads.

Table 11-3. Recommended Operating Conditions

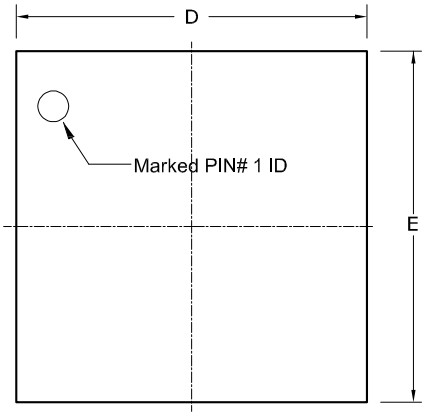
VDDIO	Condition	Min	Max	Unit
$VDDIO_L$	Input low voltage V_{IL}	-0.30	0.60	V
	Input high voltage V_{IH}	VDDIO-0.60	VDDIO+0.30	V
	Output low voltage V_{OL}		0.45	V
	Output high voltage V_{OH}	VDDIO-0.50		V
$VDDIO_M$	Input low voltage V_{IL}	-0.30	0.63	V
	Input high voltage V_{IH}	VDDIO-0.60	VDDIO+0.30	V
	Output low voltage V_{OL}		0.45	V
	Output high voltage V_{OH}	VDDIO-0.50		V
$VDDIO_H$	Input low voltage V_{IL}	-0.30	0.65	V
	Input high voltage V_{IH}	VDDIO-0.60	VDDIO+0.30 (up to 3.60)	V
	Output low voltage V_{OL}		0.45	V
	Output high voltage V_{OH}	VDDIO-0.50		V
All	Output loading		20	pF
All	Digital input load		6	pF

12. Package Drawing

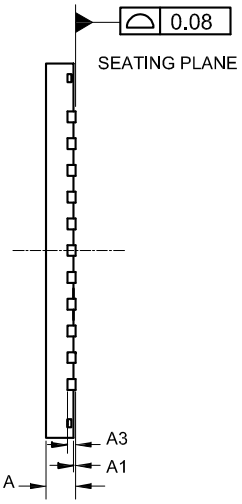
12.1 40QFN 5x5

Figure 12-1. 40QFN Package Drawing

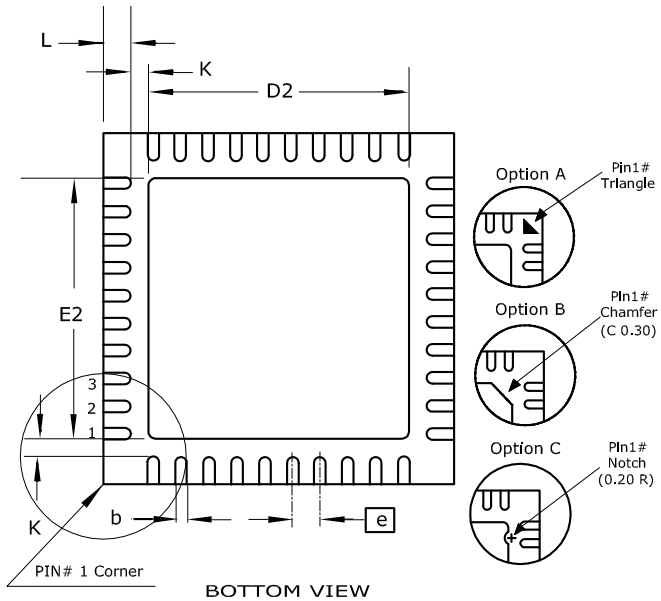
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	-----	0.90
A1	0.00	-----	0.05
A2	-----	0.65	0.70
A3		0.20 REF	
b	0.15	0.2	0.25
D		5.00 bsc	
D2	3.60	3.70	3.80
E		5.00 bsc	
E2	3.60	3.70	3.80
K	0.20	----	----
L	0.35	0.40	0.45
e		0.40 bsc	
R	0.075	-----	----
n		40	

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-1 for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

30/07/2014

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	QFN, 40 Lds - 0.40mm Pitch, 5x5x0.80mm Body size Quad Flat Package (Punched) (QFN)			A

13. Technical Support and Resources

For technical support and other resources visit: http://www.atmel.com/design-support

14. Revision History

14.1 42353C – 01/2015

1.	Datasheet status changed from “Preliminary” to “Complete”
2.	Updated “Ordering Information” on page 3
3.	Major editing updates

14.2 42353B – 11/2014

1.	Major document update, new sections added, replaced text in most sections, new and updated drawings.

14.3 42353A – 09/2014

1.	Initial document release

Table of Contents

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