

XMC4500 Satellite-kit: General Purpose Motor Drive Kit

Part Number: KIT_XMC4X_MOT_GPDLV_001



Features

- Seamless connection to CPU board via ACT Satellite Connector
- 3 phase low voltage half-bridge inverter using Infineon's N-channel
- OptiMOS™3 power transistors
- Gate Driver IC (6ED003L02-F2) with over-current detection circuit (ITRIP)
- Current measurement by using single or triple shunts (amplified)
- Single side assembly of all parts
- Position sensing via
 - Inductive resolver interface using delta-sigma modulator and pattern generator for resolver excitation
 - Hall sensor interface
- Power jack for external 24V supply
- Power supply generation:
 - Switch mode power supply for 5V power generation
 - Low drop voltage regulators (15 V) for MOSFET gate driver and resolver excitation
 - Low drop voltage regulators (3.3V) for logic
- Maximum DC-link current: 7.5 A, nominal DC-link current 5 A
- Single side assembly of all parts
- 3 LEDs indicating power (15 Volt, 5 Volt, 3.3 Volt)

PLEASE SEE THE FOLLOWING PAGES FOR USERS MANUAL

Hexagon Application Kit

For XMC4000 Family

MOT_GPDLV-V2

General Purpose Motor Drive Card

Board User's Manual

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Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 1.0, 2012-09-21	Initial release

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Introduction

This document describes the features and hardware details of the General Purpose Motor Drive Card (MOT_GPDLV-V2) designed to work with Infineon's CPU boards of the XMC4000 family. This board is a member of Infineon's Hexagon Application Kits.

1 Overview

The MOT_GPDLV-V2 board is an application expansion satellite card of the Hexagon Application Kits. The satellite card along with a CPU board (e.g. CPU_45A-V2 board) demonstrates the motor control capabilities of XMC4000 family. The main use case for this satellite card is proofing software algorithms and methods for motor control. The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1.1 Key Features

The MOT_GPDLV-V2 satellite card is equipped with following features

- Seamless connection to the CPU board (e.g. CPU_45A-V2) via the ACT satellite connector
- 3 phase low voltage half-bridge inverter using Infineon's N-channel OptiMOS™3 power transistors
- Gate Driver IC (6ED003L02-F2) with over-current detection circuit (ITRIP)
- Current measurement by using single or triple shunts (amplified)
- Position sensing via
 - Inductive resolver interface using delta-sigma modulator and pattern generator for resolver excitation
 - Quadrature encoder interface for both single ended and differential signals
 - Hall sensor interface
- Input voltage range: 24 V +/-20%
- Power supply
 - Switch mode power supply for 5V power generation
 - Low drop voltage regulators (15 V) for MOSFET gate driver and resolver excitation
 - Low drop voltage regulators (3.3V) for logic
- Maximum DC-link current: 7.5 A, nominal DC-link current 5 A

1.2 Block Diagram

Figure 1 shows the block diagram of the MOT_GPDLV-V2 satellite card. There are following building blocks:

- Connectors to CPU Board, power supply, motor and position interfaces
- Analog signal measurement
- Position sensing

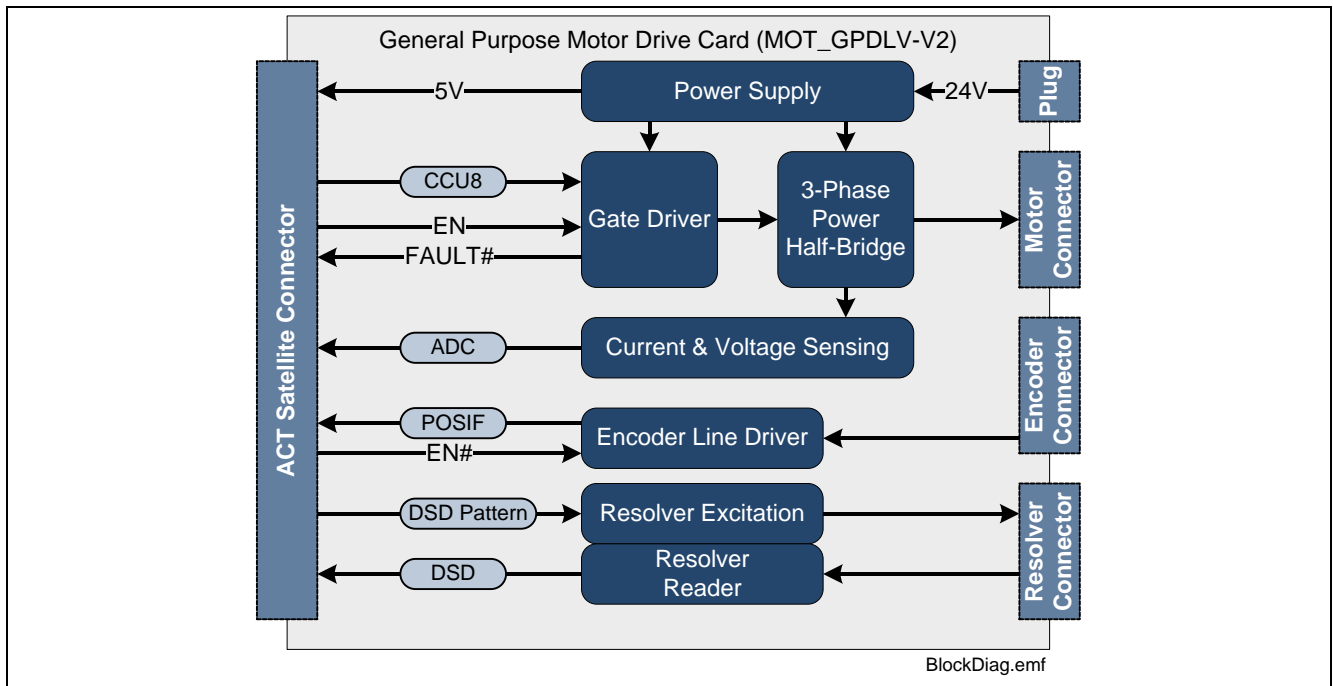


Figure 1 Block Diagram of the General Purpose Motor Drive Card

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

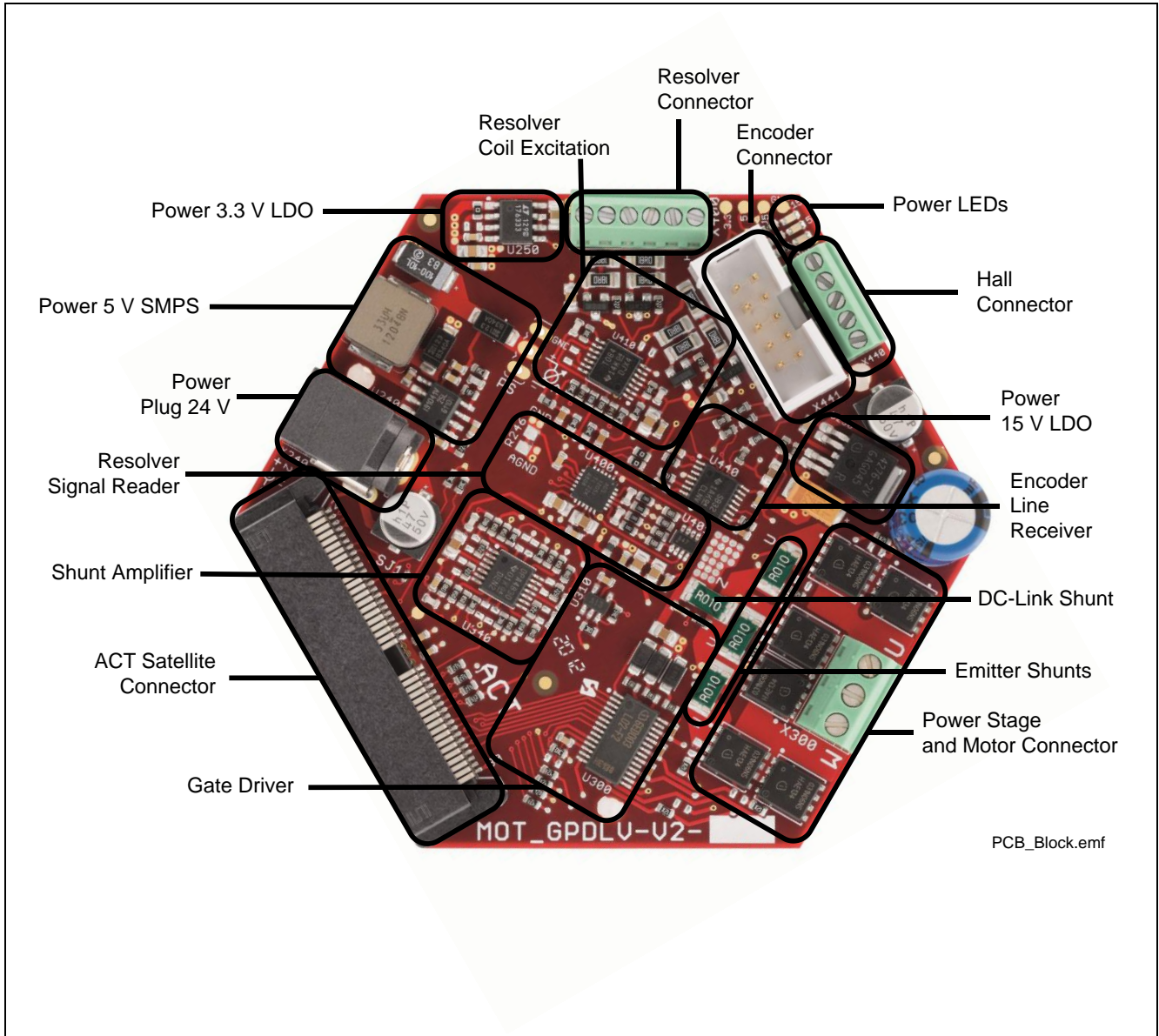


Figure 2 General Purpose Motor Drive Card

2.1 Power Supply

The General Purpose Motor Drive Card must be supplied by an external 24 Volt DC power supply connected to its power jack X240. The power to be delivered by the external power supply depends on the overall load mainly defined by the power consumption of the motor. The power supply unit (24V / 2A) delivered with the motor control kit is sufficient to drive the enclosed motor as well as other satellite cards connected to the CPU board. The power supply concept is shown in Figure 3.

A diode protects the power supply units and the circuit if more than one power supply is connected to the system via other satellite cards or via the CPU board (USB). The General Purpose Motor Drive Card is able to supply all other boards with 5V (VDD5) via the ACT satellite connector.

An on-board DC-DC converter (U240) steps down the 24 V input voltage from the power jack to 5 V (VDD5). The input voltage VDD24 must be 24 V +/-20%. The 5 Volt supply for analog circuits VDDA5 is derived from VDD5 filtered by a low pass. A LDO voltage regulator generates 3.3 V (VDD3.3) out of VDD5 and another voltage regulator generates 15 V (VDD15) power supply out of the 24 V input voltage.

Three power LEDs indicate the presence of the generated supply voltages.

Table 1 Power LED

LED	Power Rail	Voltage	Note
V210	VDD5	5.0 V	Must always be "ON"
V211	VDD3.3	3.3 V	Must always be "ON"
V212	VDD15	15.0V	Must always be "ON"

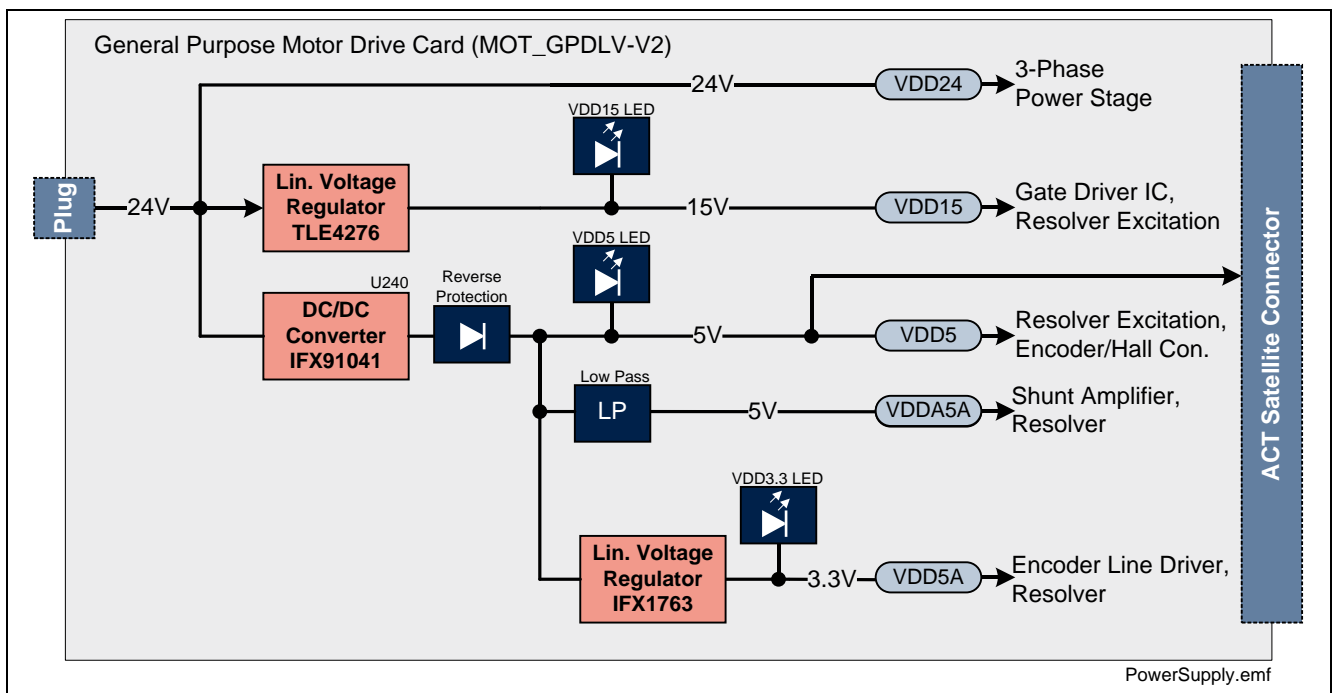


Figure 3 Block Diagram of the Power Circuit

Table 2 shows the connection of the power rails to the ACT satellite connector.

Table 2 Power rail connection to the ACT Satellite Connector

Pin No.	Power rail	Description
43,44,45,46	VDD5	5 V
1,2,79,80	GND	Ground

2.2 Satellite Connector

The satellite connector of the General Purpose Motor Drive Card is the interface to the CPU board e.g. CPU_45A-V2. Take care to connect the General Purpose Motor Drive Card always to the corresponding ACT satellite connector of the CPU board only as shown in Figure 4.

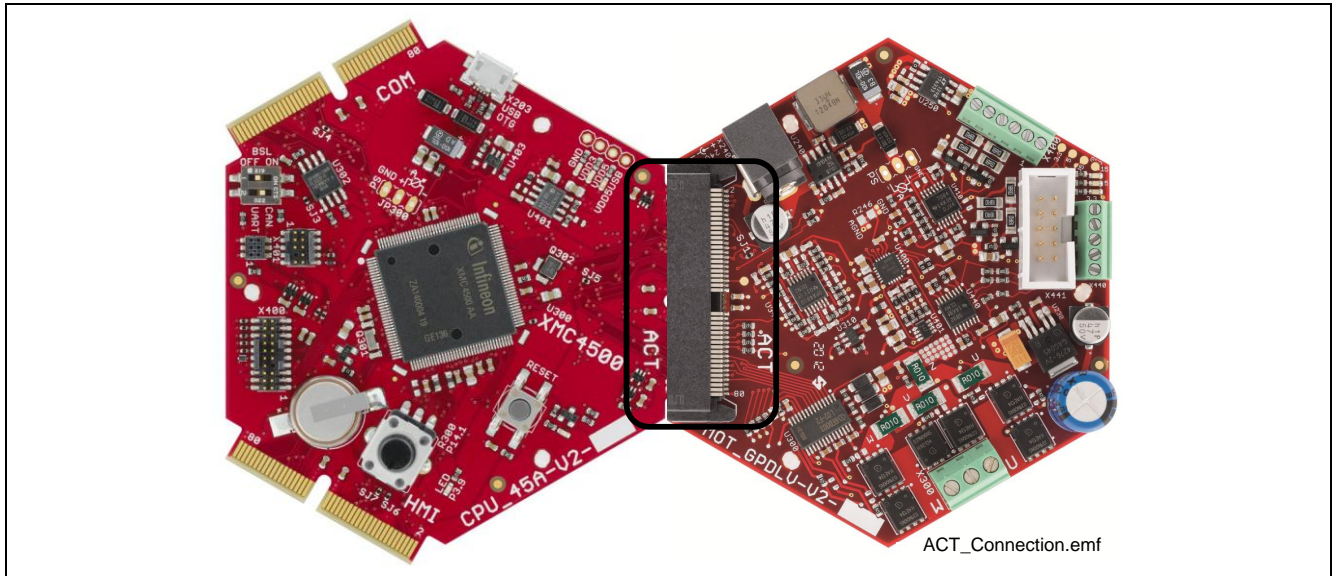


Figure 4 Connection to the CPU Board

The signal mapping details of the ACT satellite connector and the General Purpose Motor Drive Card are provided in Figure 5. The inner rows show the general function of the 80 pins of the ACT connector, which is common for all ACT satellites cards. The outer rows show the signals of the General Purpose Motor Drive Card.

The General Purpose Motor Drive Card provides 5 functional groups of signals (marked by color code) at its pins of the satellite connector:

- The encoder signals (ENCA, ENCB, ENCI): pin 4, 6 and 8
- Resolver signals (PWMN/P, MCLK, MCOS, MSIN): pin 9, 11, 13, 14, 15, 16
- Control and TRAP signals (FAULT#, ENPOW, ENENC#): pin 25, 26, 30
- Voltage and current measurement signals: (UU, UV, UW, UZ, AMP_IW...) located from pin 49 to 60
- PWM signals for the 3-Phase power stage (HIN1#, LIN1#, HIN2 ...): pin 64, 66, 68,70, 72, 74

MOT_GPDLV-V2	Function	ACT		Function	MOT_GPDLV-V2	
		Function	Pin	Function		
GND	GND	GND	2	GND	GND	44
nc	ENCA	PIF0IN1	4	PIF0IN1	VDD5	45
nc	ENCB	PIF0IN2	6	PIF0IN2	VDD5	46
nc	ENCI	PIF0IN3	8	PIF0IN3	AREF	47
nc	nc	DSDIN0	10	DSDIN0	DACL/ADCO	48
PWMN	nc	DSDIN1	11	DSDIN1	DAC2/DACREF	49
PWMP	nc	DSDIN2	12	DSDIN2	ADC3/ORC0	50
MCLK	MCOS	DSDIN3	13	DSDIN3	ADC4/ORC1	51
MCLK	MSIN	RSVD	14	RSVD	ADC5/ORC2	52
nc	nc	CC_IN3	15	CC_IN3	ADC7	53
nc	nc	CC_IN4	16	CC_IN4	ADC9	54
nc	nc	CC_IN5	17	CC_IN5	ADCL1	55
FAULT#	ENPOW	CC_IN1	18	CC_IN1	ADCL2	56
nc	nc	CC_IN2	19	CC_IN2	ADCL3	57
nc	nc	ENA_A	20	ENA_A	PWMB0_H	58
nc	nc	ENA_B	21	ENA_B	PWMB0_L	59
nc	nc	ENA_X	22	ENA_X	PWMA0_H	60
nc	nc	SPL_MTR	23	SPL_MTR	PWMA0_L	61
nc	nc	SPL_MRS	24	SPL_MRS	PWMA1_H	62
nc	nc	SPL_SCLK	25	SPL_SCLK	PWMA1_L	63
nc	nc	I2C_SCL	26	I2C_SCL	PWMA2_H	64
nc	nc	GPIO	27	GPIO	PWMA2_L	65
nc	nc	RESET	28	RESET	PWMB1_L	66
VDD5	VDD5	ACT_GPI00	29	ACT_GPI00	PWMB1_H	67
VDD5	VDD5	ACT_GPI01	30	ACT_GPI01	PWMB2_H	68
VDD5	VDD5	ACT_GPI02	31	ACT_GPI02	PWMB2_L	69
VDD5	VDD5	ACT_GPI03	32	ACT_GPI03	PWMX0	70
VDD5	VDD5	ACT_GPI04	33	ACT_GPI04	PWMX1	71
VDD5	VDD5	ACT_GPI05	34	ACT_GPI05	PWMX2	72
VDD5	VDD5	ACT_GPI06	35	ACT_GPI06	PWMX3	73
VDD5	VDD5	ACT_GPI07	36	ACT_GPI07	GND	74
VDD5	VDD5	ACT_GPI08	37	ACT_GPI08	GND	75
VDD5	VDD5	ACT_GPI09	38	ACT_GPI09	GND	76
VDD5	VDD5	ACT_GPI10	39	ACT_GPI10	GND	77
VDD5	VDD5	ACT_GPI11	40	ACT_GPI11	GND	78
VDD5	VDD5	ACT_GPI12	41	ACT_GPI12	GND	79
VDD5	VDD5	ACT_GPI13	42	ACT_GPI13	GND	80
VDD5	VDD5	ACT_GPI14	43	ACT_GPI14	GND	80
VDD5	VDD5	ACT_GPI15	44	ACT_GPI15	GND	80
VDD5	VDD5	ACT_GPI16	45	ACT_GPI16	GND	80
VDD5	VDD5	ACT_GPI17	46	ACT_GPI17	GND	80
VDD5	VDD5	ACT_GPI18	47	ACT_GPI18	GND	80
VDD5	VDD5	ACT_GPI19	48	ACT_GPI19	GND	80
VDD5	VDD5	ACT_GPI20	49	ACT_GPI20	GND	80
VDD5	VDD5	ACT_GPI21	50	ACT_GPI21	GND	80
VDD5	VDD5	ACT_GPI22	51	ACT_GPI22	GND	80
VDD5	VDD5	ACT_GPI23	52	ACT_GPI23	GND	80
VDD5	VDD5	ACT_GPI24	53	ACT_GPI24	GND	80
VDD5	VDD5	ACT_GPI25	54	ACT_GPI25	GND	80
VDD5	VDD5	ACT_GPI26	55	ACT_GPI26	GND	80
VDD5	VDD5	ACT_GPI27	56	ACT_GPI27	GND	80
VDD5	VDD5	ACT_GPI28	57	ACT_GPI28	GND	80
VDD5	VDD5	ACT_GPI29	58	ACT_GPI29	GND	80
VDD5	VDD5	ACT_GPI30	59	ACT_GPI30	GND	80
VDD5	VDD5	ACT_GPI31	60	ACT_GPI31	GND	80
VDD5	VDD5	ACT_GPI32	61	ACT_GPI32	GND	80
VDD5	VDD5	ACT_GPI33	62	ACT_GPI33	GND	80
VDD5	VDD5	ACT_GPI34	63	ACT_GPI34	GND	80
VDD5	VDD5	ACT_GPI35	64	ACT_GPI35	GND	80
VDD5	VDD5	ACT_GPI36	65	ACT_GPI36	GND	80
VDD5	VDD5	ACT_GPI37	66	ACT_GPI37	GND	80
VDD5	VDD5	ACT_GPI38	67	ACT_GPI38	GND	80
VDD5	VDD5	ACT_GPI39	68	ACT_GPI39	GND	80
VDD5	VDD5	ACT_GPI40	69	ACT_GPI40	GND	80
VDD5	VDD5	ACT_GPI41	70	ACT_GPI41	GND	80
VDD5	VDD5	ACT_GPI42	71	ACT_GPI42	GND	80
VDD5	VDD5	ACT_GPI43	72	ACT_GPI43	GND	80
VDD5	VDD5	ACT_GPI44	73	ACT_GPI44	GND	80
VDD5	VDD5	ACT_GPI45	74	ACT_GPI45	GND	80
VDD5	VDD5	ACT_GPI46	75	ACT_GPI46	GND	80
VDD5	VDD5	ACT_GPI47	76	ACT_GPI47	GND	80
VDD5	VDD5	ACT_GPI48	77	ACT_GPI48	GND	80
VDD5	VDD5	ACT_GPI49	78	ACT_GPI49	GND	80
VDD5	VDD5	ACT_GPI50	79	ACT_GPI50	GND	80
VDD5	VDD5	ACT_GPI51	80	ACT_GPI51	GND	80

Figure 5 Pin Mapping on ACT Satellite Connector

Figure 6 is an extended view of the signal mapping between the General Purpose Motor Drive Card (MOT_GPDLV-V2) and the “XMC4500 CPU Board General Purpose” (CPU_45A-V2). It shows in details which pin of the XMC4500 is mapped to which signal on the motor drive card.

MOT_GPDLV-V2		CPU_45A-V2		Satellite Connector		CPU_45A-V2		MOT_GPDLV-V2	
Function	XMC Pin	XMC Function	XMC Pin	Pin	Function	XMC Function	XMC Pin	Function	XMC Pin
GND	VSS	GND	VSS	1	GND	GND	VSS	GND	VSS
nc	nc	nc	nc	2	P1F0IN1	P1F0_IN0A	P1.3	ENCA	P1.3
nc	nc	nc	nc	3	P1F1IN1	P1F0_IN1A	P1.2	ENCB	P1.2
nc	nc	nc	nc	4	P1F0IN2	P1F0_IN2A	P1.1	ENCI	P1.1
PWMN	P1.0	DSD_PWMN	P0.8(2)	5	P1F1IN2	DSD_DIN0A	P2.6	nc	nc
PWMP	P5.1	DSD_PWMP	P2.6	6	PWMN	DSD_DIN1	P1.6	MCOS	P1.6
MCLK	P1.7	DSD_MCLK2A	P1.6	7	PWMP	DSD_DIN2	P6.5 (3)	MSIN	P6.5 (3)
MCLK	P3.4	DSD_MCLK3B	P6.5 (3)	8	DSDCLK0	DSD_DIN3	nc	nc	nc
nc	nc	nc	nc	9	DSDCLK1	RSVD	CCU43_IN0A	P4.6	nc
nc	nc	nc	nc	10	RSVD	CC_IN0	CCU43_IN1A	P4.5	nc
nc	P4.3	CCU43_IN3A	P4.6	11	CC_IN3	CC_IN1	CCU43_IN2A	P4.4	nc
nc	P5.2	CCU81_IN1B	P4.5	12	CC_IN4	CC_IN2	CCU43_IN2C	P2.13	ENPOW
nc	P5.4	CCU81_IN3B	P4.4	13	CC_IN5	ENA_A	CCU43_IN3C	P2.12	nc
nc	P0.7 (1)	CCU80_IN0A	P2.13	14	TRAP_A	ENA_B	CCU430UT1	P6.4	ENENC#
nc	P5.0	CCU81_IN0A/1A/2A/3A	P2.12	15	TRAP_B	ENA_X	U0C1_DOUT0	P3.13	nc
nc	P4.7	CCU43_IN0C	P2.12	16	TRAP_X	ENA_X	U0C1_DX0B	P2.5	nc
nc	P3.11	U0C1_SELO2	P3.13	17	TRAP_X	SPL_MSTR	U0C1_SCLKOUT	P3.0	nc
nc	P3.8	U0C1_SELO3	P3.0	18	SPL_CSA0	SPL_MRST	U1C0_SCLKOUT	P5.8	nc
nc	nc	nc	nc	19	SPL_CSA1	SPL_SCLK	V1C0_SCLKOUT	P0.6	nc
nc	P2.14	U1C0_DX0D/DOUT0	P5.8	20	SPL_CSA2	I2C_SCL	nc	nc	nc
nc	P15.4	P15.4 Input	nc	21	I2C_SDA	ACT_GPI01	nc	nc	nc
nc	P4.2	P4.2	nc	22	ACT_GPI00	RESET	nc	nc	nc
VDD5	VDD5	nc	nc	23	ACT_GPI00	RESET#	nc	nc	nc
VDD5	VDD5	VDD5	VDD5	24	VDD5	VDD5	VDD5	VDD5	VDD5
nc	VAGND	AGND	VDD5	25	VDD5	VDD5	VDD5	VDD5	VDD5
AMP_IW	P14.9	VADC_61CH1	VDD5	26	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P14.6	VADC_60CH6	AGND	27	VDD5	VDD5	VDD5	VDD5	VDD5
AMP_IU	P14.7	VADC_60CH7	DAC0/ADC1	28	VDD5	VDD5	VDD5	VDD5	VDD5
UZ	P14.0	VADC_60CH0	ADC3/ORC0	29	VDD5	VDD5	VDD5	VDD5	VDD5
AMP_IV	P14.5	VADC_62CH1	ADC5/ORC2	30	VDD5	VDD5	VDD5	VDD5	VDD5
AMP_IZ	P15.14	VADC_63CH6	ADC7	31	VDD5	VDD5	VDD5	VDD5	VDD5
UZ	P15.15	VADC_63CH7	ADC9	32	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P1.15	CCU81_OUT00	ADC11	33	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P1.12	CCU81_OUT01	ADC13	34	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P1.14	CCU81_OUT10	PWMB0_H	35	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P1.11	CCU81_OUT11	PWMB0_L	36	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P1.13	CCU81_OUT20	PWMB1_H	37	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P1.10	CCU81_OUT21	PWMB1_L	38	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P6.0 (3)	CCU81_OUT31	PWMB2_H	39	VDD5	VDD5	VDD5	VDD5	VDD5
nc	P6.1 (3)	CCU81_OUT30	PWMB2_L	40	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	41	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	42	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	43	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	44	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	45	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	46	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	47	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	48	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	49	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	50	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	51	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	52	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	53	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	54	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	55	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	56	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	57	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	58	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	59	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	60	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	61	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	62	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	63	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	64	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	65	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	66	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	67	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	68	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	69	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	70	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	71	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	72	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	73	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	74	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	75	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	76	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	77	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	78	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	79	VDD5	VDD5	VDD5	VDD5	VDD5
GND	VSS	GND	VSS	80	VDD5	VDD5	VDD5	VDD5	VDD5

Figure 6 Pin Mapping to XMC4500 on CPU Board CPU_45A-V2

2.3 Gate Driver and Power Stage

The power stage consists of three half-bridges using Infineon's N-channel OptiMOS™ power transistors. They are selected for a safe operation area with huge headroom, hence no cooling is needed when using at nominal current of 5 Ampere.

The gate driver (6ED003L02-F2) is Infineon's full bridge driver in SOI-technology offering an excellent ruggedness on transient voltages. The external bootstrap circuitry has been dimensioned according to the formula (see Infineon application note AN-EICEDRIVER-6EDL04-1):

$$C_{BS} = \frac{i_{QBS} \cdot t_P + Q_G}{\Delta V_{BS}} \cdot 1.2$$

$$\frac{C_{BS} \cdot \Delta V_{BS}}{1.2} = i_{QBS} \cdot t_P + Q_G$$

$$(0.833 \cdot C_{BS} \cdot \Delta V_{BS}) - Q_G = i_{QBS} \cdot t_P$$

$$t_P = \frac{(0.833 \cdot C_{BS} \cdot \Delta V_{BS}) - Q_G}{i_{QBS}}$$

With

C_{BS} : Bootstrap Capacity (1 uF)

i_{QBS} : highside driver quiescent current (max. 100 uA)

Q_G : Gate charge (max. 130 nC)

ΔV_{BS} : max. allowed voltage drop at the bootstrap capacitor (5 V)

Factor 1.2: 20% margin for capacitor

the minimum switching period t_p is 40 ms:

$$t_p = \frac{(0.833 \cdot 1 \mu F \cdot 5 V) - 130 \text{ nC}}{100 \mu A}$$

$$t_p = 40 \text{ ms}$$

The gate driver offers several protection features like under-voltage lockout, signal interlocking of every phase to prevent cross-conduction and overcurrent detection.

In an error situation a FAULT# signal is generated and must be handled by the microcontroller. The FAULT# signal changes to low state if an over-current condition has been detected by the ITRIP circuit. The ITRIP current level is measured as the amplified voltage drop over the DC-link shunt (see Figure 7). The minimum input voltage level to trigger an over-current event is specified at 380 mV. With an amplifier gain of $1 + (40.2/10) = 5.02$ and a DC-Link shunt with 10 mΩ the ITRIP will be triggered at a DC-Link current higher than 7.57 A:

$$I = U / R,$$

$$I = (0.38 \text{ V} / 5.02) / 10 \text{ m}\Omega,$$

$$I = 7.57 \text{ A}.$$

The overcurrent condition must be present for longer than about 100 us ($3 \cdot RC$ time constant of the RC filter R322, C310) in order to trigger the ITRIP. This shall protect the PCB traces and the components in the high current path.

The microcontroller must provide the PWM signals (LIN1/2/3#, HIN1/2/3#) for the high-side and low-side switches. The PWM signals must be generated low-active.

The gate driver must be enabled via signal ENPOW.

A phase current measurement is provided via shunt resistors

- a) single shunt (10 mΩ) in the DC-link path and/or
- b) triple shunt (10 mΩ) in the low-side path

The resistance of the shunts limits the system behavior and may not fit to the low-ohmic power transistors. This is intended as the main purpose of this board is to proof SW algorithms and methods over a wide range.

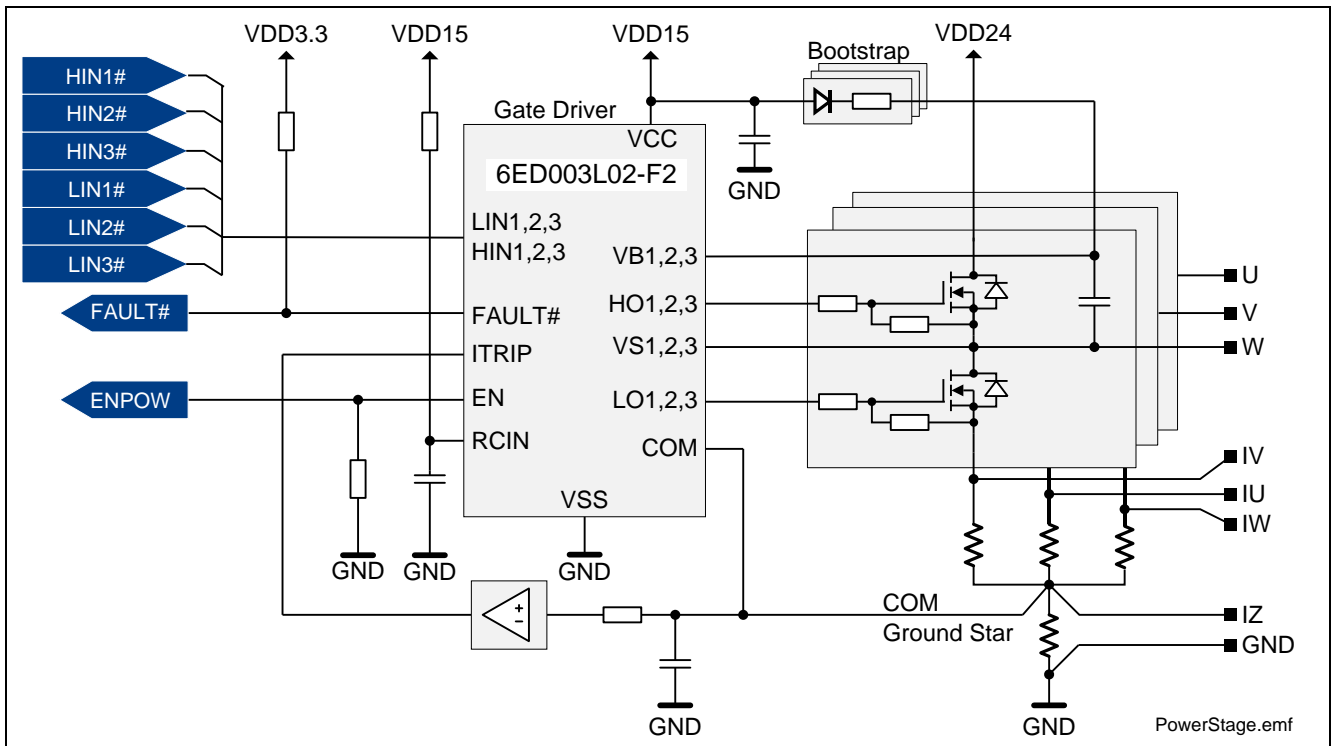


Figure 7 Block Diagram of the Gate Driver and the Power Stage

Table 3 shows the connection of the Gate Driver signals to the ACT satellite connector.

Table 3 Gate Driver signals connection to the ACT Satellite Connector

Pin No.	Signal Name	Description
25	FAULT#	this signal indicates over-current and under-voltage (low-active)
26	ENPOW	High level enables the power stage (high-active)
64	HIN1#	High-side logic input 1 (low-active)
66	LIN1#	Low-side logic input 1 (low-active)
68	HIN2#	High-side logic input 2 (low-active)
70	LIN2#	Low-side logic input 2 (low-active)
72	HIN3#	High-side logic input 3 (low-active)
74	LIN3#	Low-side logic input 3 (low-active)

2.4 Voltage and Current Measurements

The phase current measurement is illustrated on the left side of Figure 8; the right side shows the voltage divider for the voltage measurement.

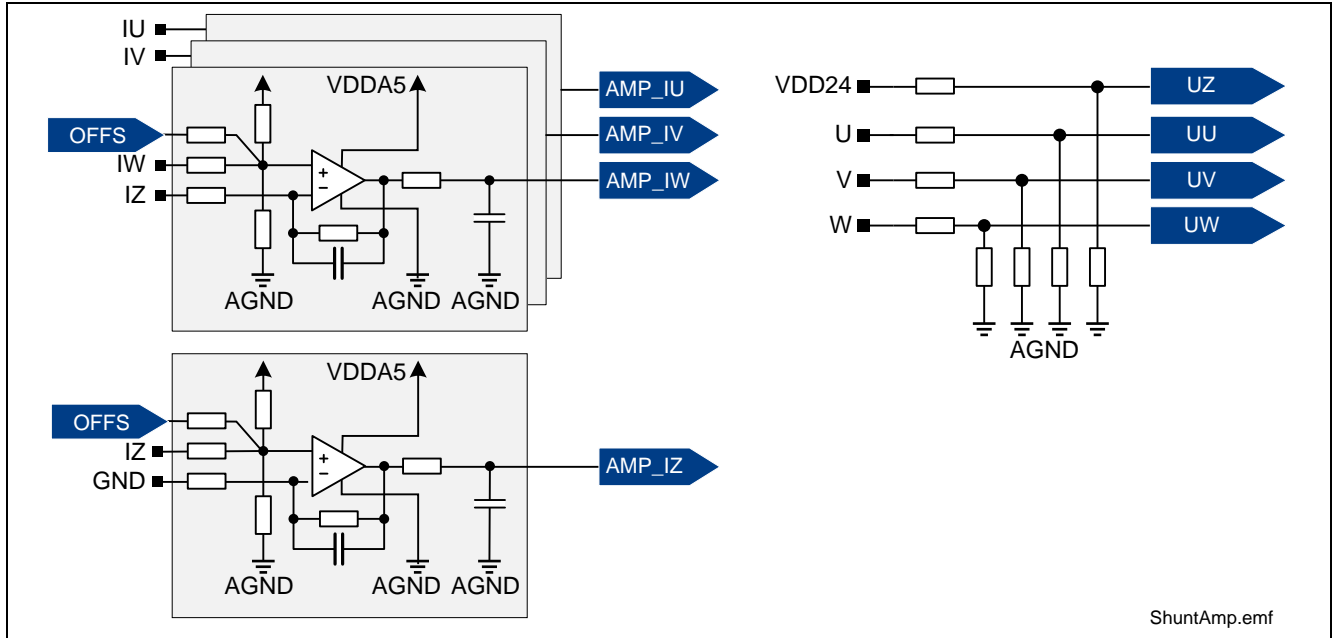


Figure 8 Measurement of Voltages and Currents

2.4.1 Phase Current Measurement

The current measurement can be done via a single shunt (signal IZ) in the DC-link path or via triple shunts (IU, IV, IW) in the emitter path. In both cases the measurement is dimensioned for the following requirements:

Motor power range up to 120W which leads to a nominal DC-link current of about 5 Ampere and a maximum phase peak current of about 20 Ampere. The phase current range is 75 mA to 20 A.

A shunt resistance of 10 mΩ leads to 0.75 mV voltage drop @ 75 mA and 200 mV voltage drop @ 20 A. This voltage is amplified by a non-inverting amplifier. The output of the operational amplifier (AMP_IU, AMP_IV, AMP_IW, AMP_IZ) is available at the ACT Satellite Connector and connected to ADC input channels of the XMC4000 microcontroller.

The gain of the operational amplifier is set to 21 ($G = 1 + (R1 / R2)$), which leads to an output voltage of 15.75 mV @ 75 mA and 4.20 V @ 20A.

The XMC4000 offers a DAC output which is used as DC offset generator for the OpAmps (signal OFFS). The DAC voltage must be adjusted to a voltage level of about 1.2 V in order to get 0 V at the output of the OpAmps when there is no current flow through the shunts. Alternatively the offset can be generated by a resistive voltage divider.

2.4.2 Phase Voltage Measurement

The phase voltage is directly measured using resistive dividers at the phases (signals UZ, UU, UV, and UW). The divider is dimensioned to divide the measured voltage UZ, UU, UV, UW by factor 10.21. The formula to calculate the phase voltage U_{PHx} from the measured voltage U_x is:

$$U_{PHx} = 10.21 * U_x$$

Table 4 summarizes all voltage signals and current signals available at the ACT satellite connector.

Table 4 Voltage and Current signals at the ACT Satellite Connector

Pin No.	Signal Name	Description
50	OFFS	Offset voltage input required for the shunt amplifier

Table 4 Voltage and Current signals at the ACT Satellite Connector

Pin No.	Signal Name	Description
53	AMP_IU	Amplified shunt voltage output representing the current of phase U
57	AMP_IV	Amplified shunt voltage output representing the current of phase V
49	AMP_IW	Amplified shunt voltage output representing the current of phase W
59	AMP_IZ	Amplified shunt voltage output representing the DC-link current
56	UU	Divided voltage output of phase U (divided by 10.21)
52	UV	Divided voltage output of phase V (divided by 10.21)
60	UW	Divided voltage output of phase W (divided by 10.21)
55, 58, 61	UZ	Divided DC-link output voltage (divided by 10.21)

2.5 Resolver Interface

For rotor position detection a resolver can be used. The three coils of the resolver must be connected to the connector X400 as shown in Figure 9.

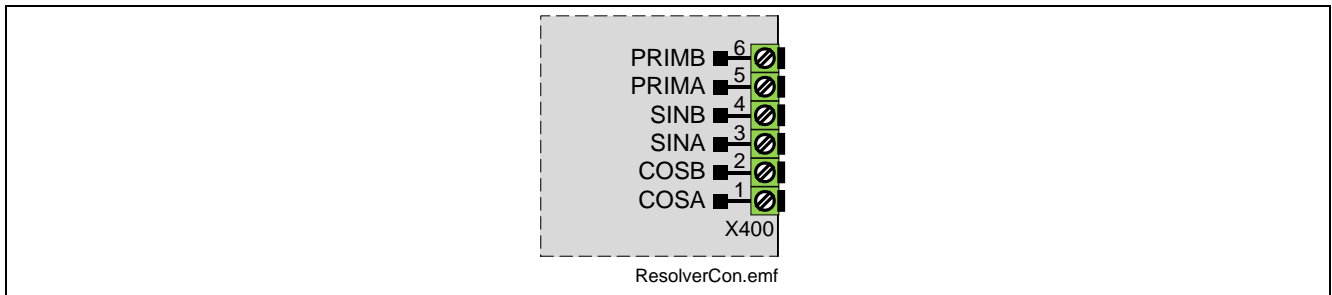


Figure 9 Connection Scheme of the Resolver Connector

The XMC4000 devices use an on-chip pattern generator for the excitation of the primary coil and a decimation filter to read the SIN/COS feedback measured by a delta-sigma modulator.

The primary coil excitation is done via the microcontroller signals PWMP/PWMN which is a digital data stream with a selectable clock rate in the MHz range. These signals are integrated, amplified and fed to the primary coil of the resolver as shown in Figure 10.

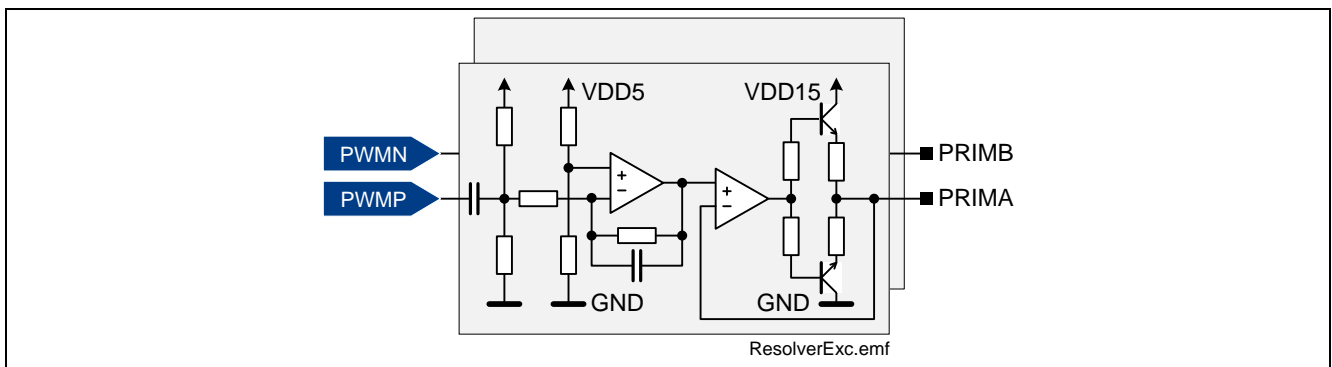


Figure 10 Resolver Excitation Circuit

The feedback signals (SINA/B and COSA/B) of the secondary coils are fed to a delta-sigma modulator ADS1205 which has an internal clock and generates the SIN/COS serial data stream on the signals MSIN/MCOS. It also provides the modulator clock MCLK. The circuit is shown in Figure 11.

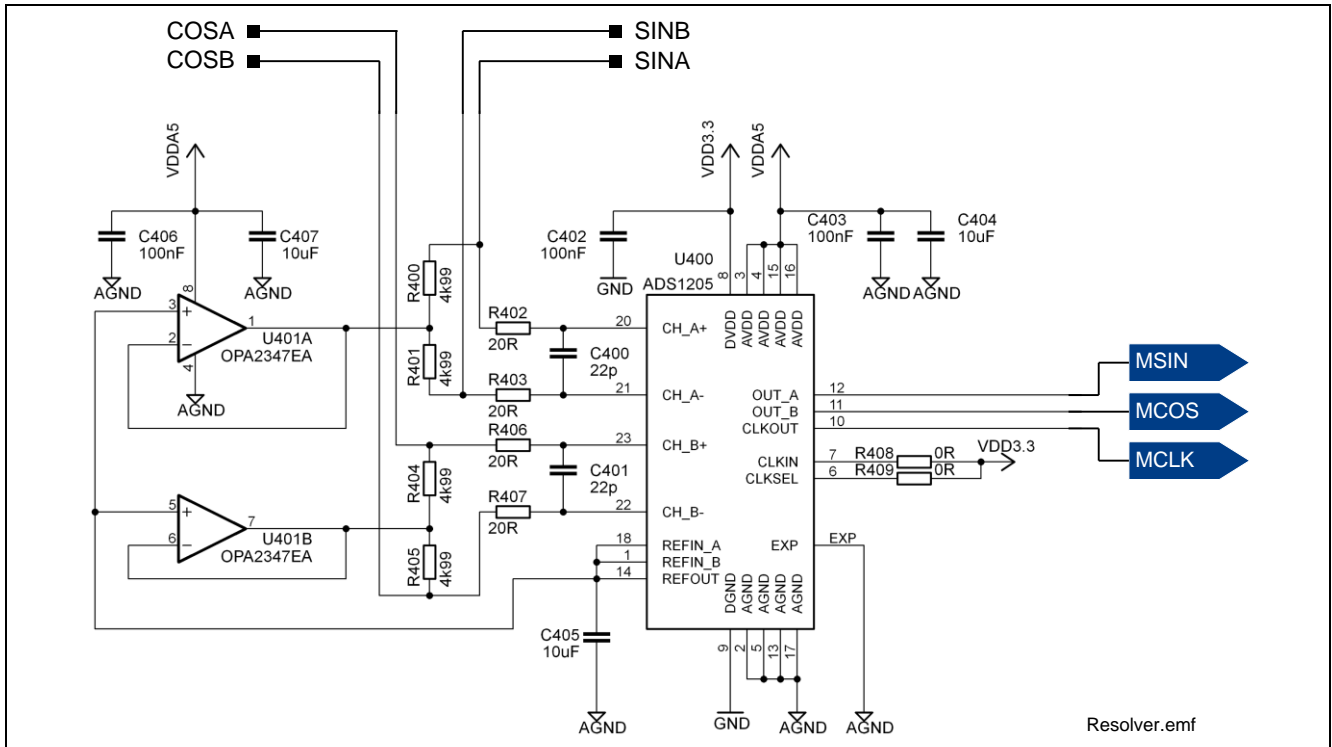


Figure 11 Resolver Modulator Circuit

Table 5 summarizes all signals of the resolver which are connected to the ACT satellite connector.

Table 5 Resolver signals at the ACT Satellite Connector

Pin No.	Signal Name	Description
9	PWMN	Excitation input signal (inverted)
11	PWMP	Excitation input signal
14	MCOS	COS signal output of the delta sigma modulator
16	MSIN	SIN signal output of the delta sigma modulator
15, 13	MCLK	Clock output of the delta sigma modulator

2.6 Encoder and Hall Interface

A quadrature encoder can be used for detecting the actual rotor position. There are single-ended and differential encoders, the board supports both types. For the differential types an encoder line receiver is required as the microcontroller needs single ended signals.

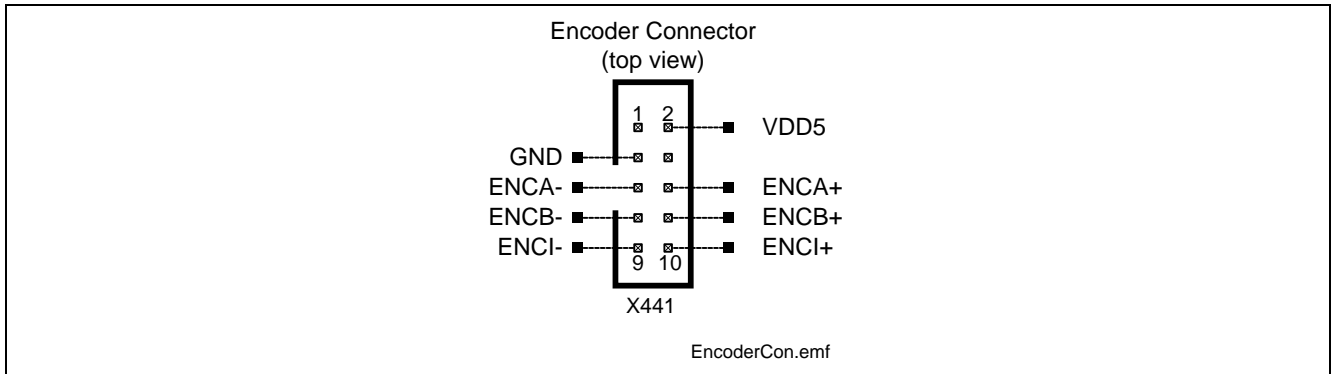


Figure 12 Encoder Connector for differential encoder signals

The differential signals from the encoder (ENCA+/-, ENCB+/-, ENCI+/-) must be connected to the 10-pin encoder connector X441 (Figure 13). The receiver must be enabled by the signal ENENC# (set to "0").

In case of using a single ended encoder or a hall sensor the signals must be applied to the connector X440 and the encoder line receiver must be disabled by setting the signal ENENC# to high level (default).

The parallel operation of both a differential encoder and a hall sensor is possible by adapting the resistor values shown in Figure 13. The pull-up resistors value must be changed to 4.7 k Ω , the serial resistors must be set to 680 Ω . This will ensure appropriate signal levels for the encoder signals ENCx in all use cases and limits the current to about 5 mA.

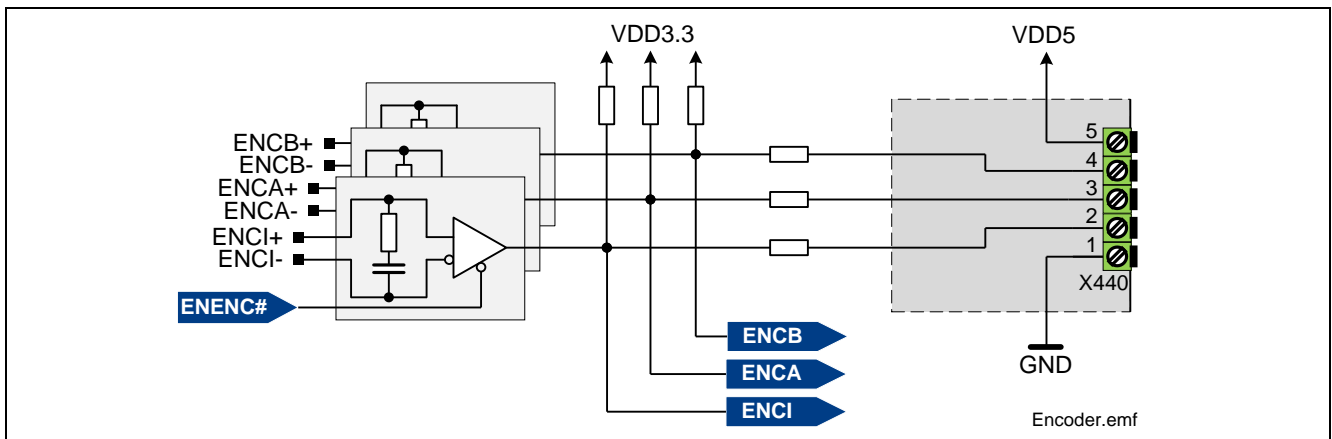


Figure 13 Encoder Line Receiver (differential signals) and hall interface

Figure 6 shows the connection of the encoder/hall signals available at the ACT satellite connector.

Table 6 Encoder / hall signals at the ACT Satellite Connector

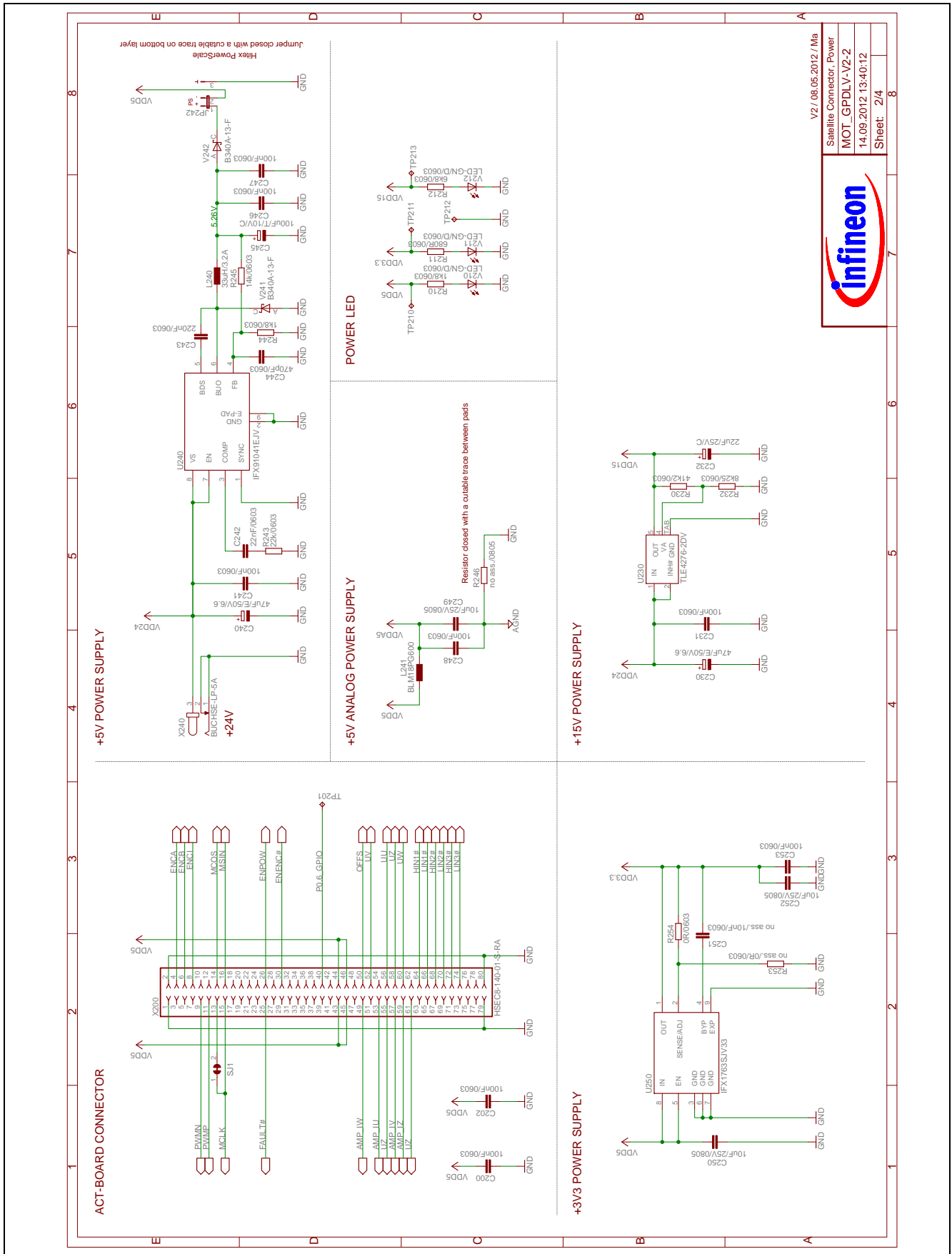
Pin No.	Signal Name	Description
30	ENCEN#	enable signal for the encoder line receiver (active low)
4	ENCA	Encoder channel A
6	ENCB	Encoder channel B
8	ENCI	Encoder channel I

3 Production Data

3.1 Schematics

This chapter contains the schematics for the General Purpose Motor Drive Card (MOT_GPDLV-V2):

- Figure 14: Satellite Connector, Power Supply
- Figure 15: Gate Driver, Power Stage, Shunt Amplifier, Motor Connector
- Figure 16: Resolver, Encoder, Hall Connector



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Satellite Connector, Power
MOT_GPDLV-V2-2
14.09.2012 13:40:12
Sheet: 2/4

Figure 14 Satellite Connector, Power Supply

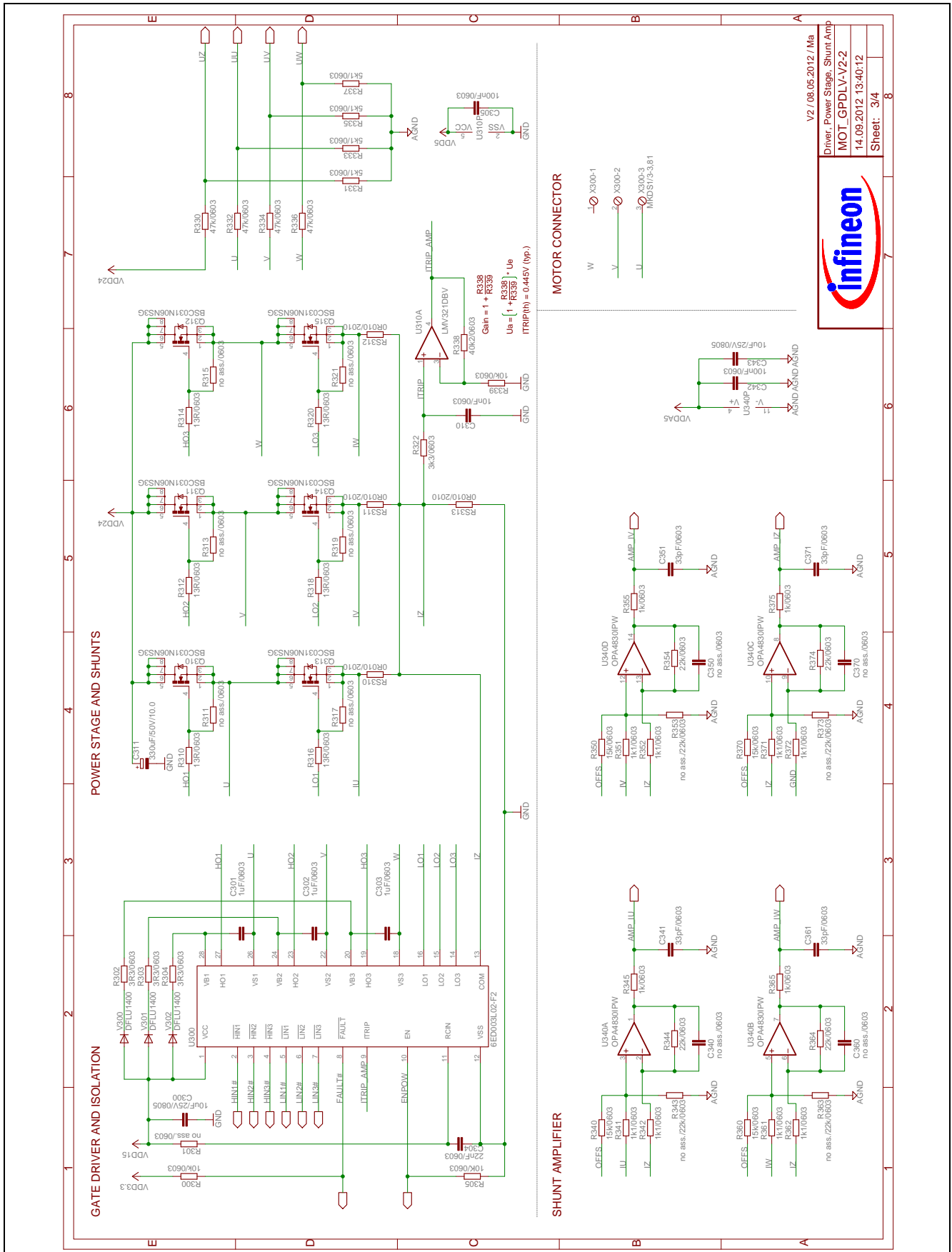
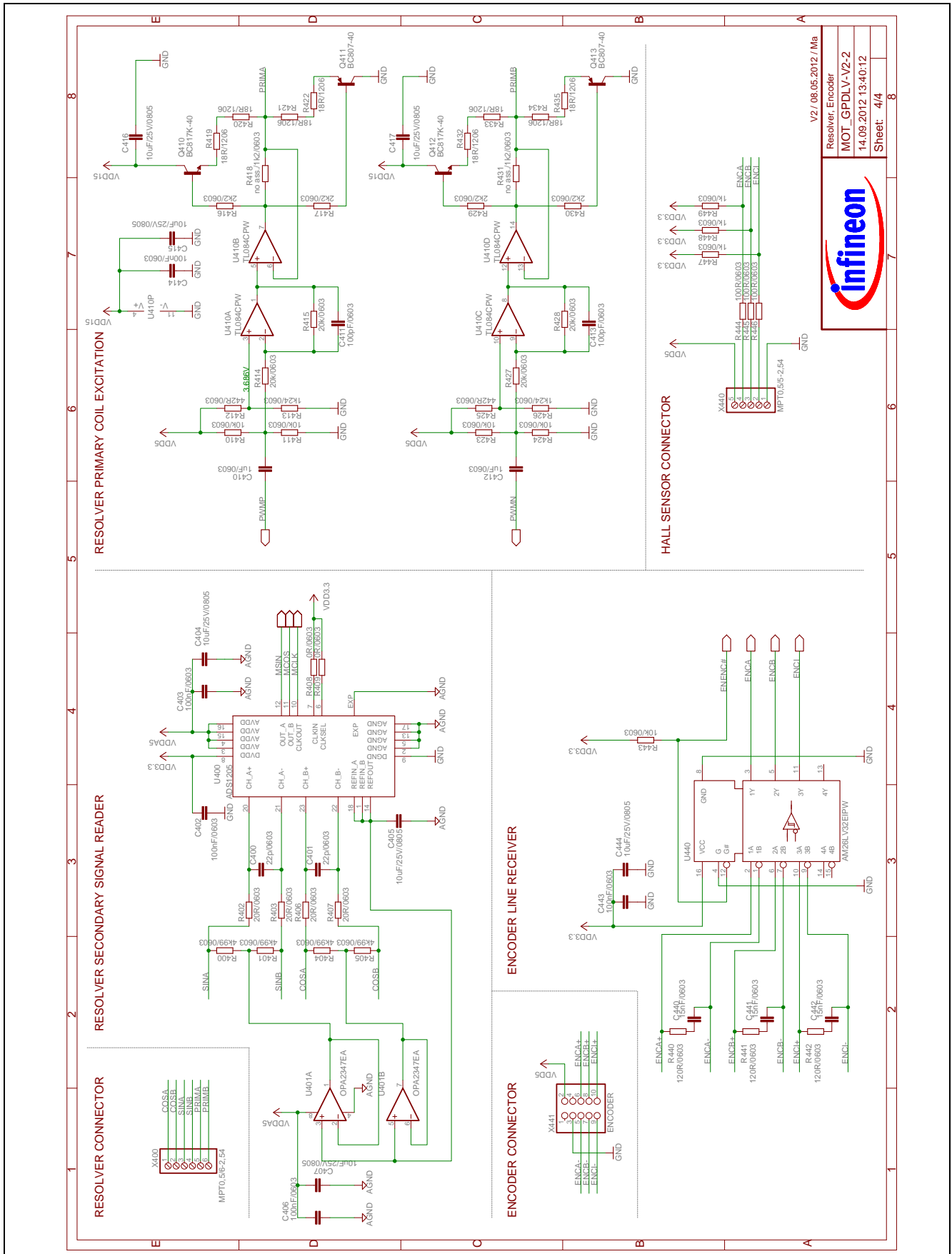


Figure 15 Gate Driver, Power Stage, Shunt Amplifier, Motor Connector



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Resolver, Encoder
MOT_GPDLV-V2-2
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Figure 16 Resolver, Encoder, Hall Connector

3.2 Components Placement and Geometry

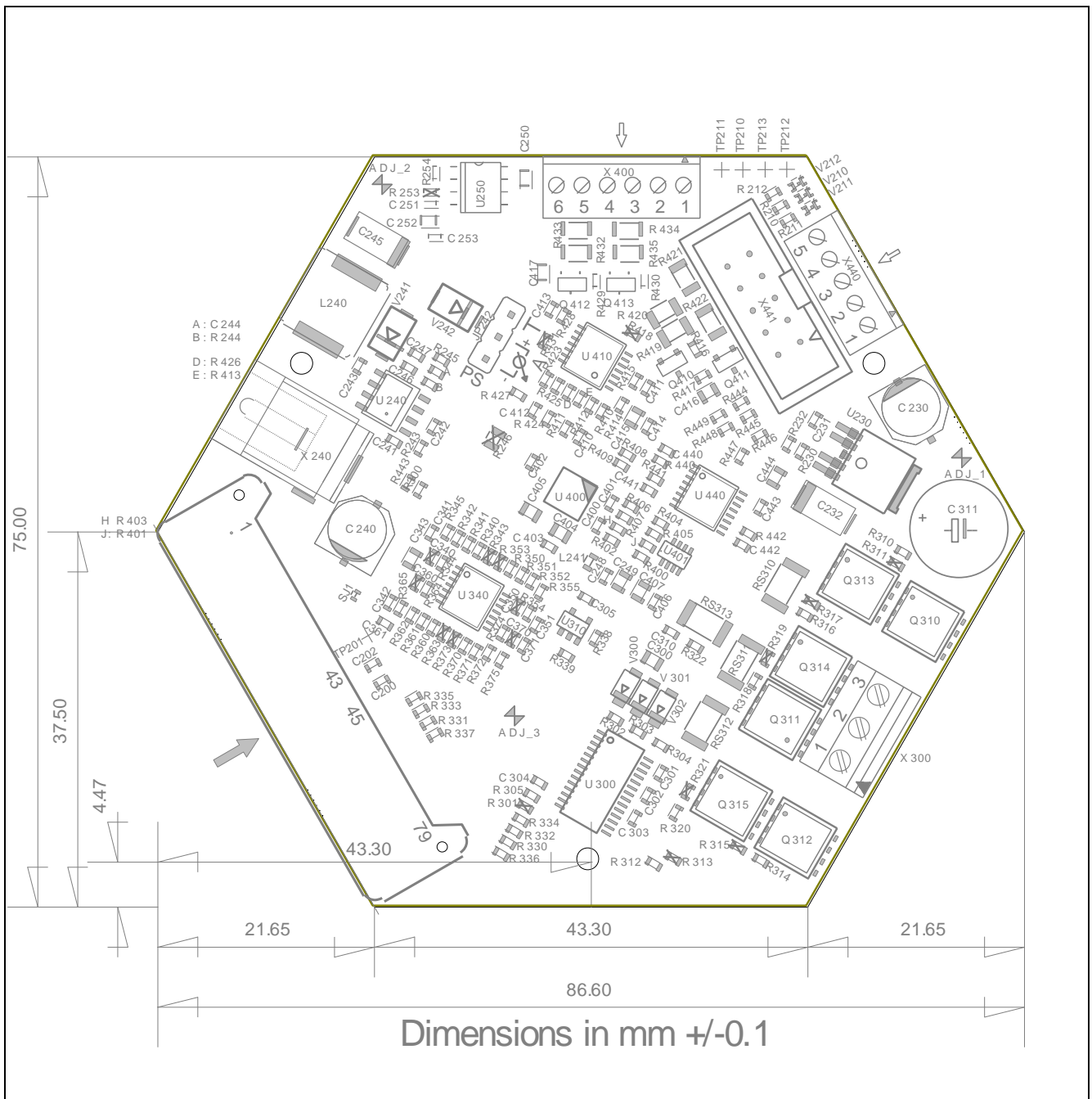


Figure 17 Components Placement and Geometry

3.3 List of Material

The list of material is valid for a certain assembly version for the General Purpose Motor Drive Card. This version is stated in the header of the Table 7. The assembly version number can be identified by the board identification code printed on the PCB. The last digit field "002" of the board identification codes "MOT_GPDLV-V2-002" is representing the assembly version. If there is no assembly version number printed on the PCB (white empty field) than the PCB has the assembly version number 1.

The only difference between both assembly version 1 and 2 is the value of the resistor R322. In version 1 it is 100 kΩ, whereas in assembly version 2 R322 is 3.3 kΩ.

Table 7 List of Material for General Purpose Motor Drive Card (MOT_GPDLV-V2-002)

Sl. No.	Qty	Value	Device	Reference Designator
1	3	0R/0603	Resistor	R254, R408, R409
2	4	0R010/2010	Shunt	RS310, RS311, RS312, RS313
3	7	1k/0603	Resistor	R345, R355, R365, R375, R447, R448, R449
4	8	1k1/0603	Resistor	R341, R342, R351, R352, R361, R362, R371, R372
5	2	1k8/0603	Resistor	R210, R244
6	2	1k24/0603	Resistor	R413, R426
7	5	1uF/0603	Capacitor	C301, C302, C303, C410, C412
8	4	2k2/0603	Resistor	R416, R417, R429, R430
9	3	3R3/0603	Resistor	R302, R303, R304
10	1	3k3/0603	Resistor	R322
11	4	4k99/0603	Resistor	R400, R401, R404, R405
12	4	5k1/0603	Resistor	R331, R333, R335, R337
13	1	6ED003L02-F2	Gate Driver 6ED003L02-F2	U300
14	1	6k8/0603	Resistor	R212
15	1	8k25/0603	Resistor	R232
16	8	10k/0603	Resistor	R300, R305, R339, R410, R411, R423, R424, R443
17	1	10nF/0603	Capacitor	C310
18	12	10uF/25V/0805	Capacitor	C249, C250, C252, C300, C343, C404, C405, C407, C415, C416, C417, C444
19	6	13R/0603	Resistor	R310, R312, R314, R316, R318, R320
20	1	14k/0603	Resistor	R245
21	4	15k/0603	Resistor	R340, R350, R360, R370
22	3	15nF/0603	Capacitor	C440, C441, C442
23	8	18R/1206	Resistor	R419, R420, R421, R422, R432, R433, R434, R435
24	4	20R/0603	Resistor	R402, R403, R406, R407
25	4	20k/0603	Resistor	R414, R415, R427, R428
26	5	22k/0603	Resistor	R243, R344, R354, R364, R374
27	2	22nF/0603	Capacitor	C242, C304
28	2	22p/0603	Capacitor	C400, C401
29	1	22uF/25V/C	Capacitor unipolar	C232
30	4	33pF/0603	Capacitor	C341, C351, C361, C371
31	1	33uH/3.2A	Inductor IHLP-3232DZ-11	L240

Table 7 List of Material for General Purpose Motor Drive Card (MOT_GPDLV-V2-002)

Sl. No.	Qty	Value	Device	Reference Designator
32	1	40k2/0603	Resistor	R338
33	1	41k2/0603	Resistor	R230
34	4	47k/0603	Resistor	R330, R332, R334, R336
35	2	47uF/E/50V/6.6	Capacitor unipolar	C230, C240
36	3	100R/0603	Resistor	R444, R445, R446
37	15	100nF/0603	Capacitor	C200, C202, C231, C241, C246, C247, C248, C253, C305, C342, C402, C403, C406, C414, C443
38	2	100pF/0603	Capacitor	C411, C413
39	1	100uF/T/10V/C	Capacitor unipolar	C245
40	3	120R/0603	Resistor	R440, R441, R442
41	1	220nF/0603	Capacitor	C243
42	1	330uF/50V/10.0	Capacitor unipolar	C311
43	2	442R/0603	Resistor	R412, R425
44	1	470pF/0603	Capacitor	C244
45	1	680R/0603	Resistor	R211
46	1	ADS1205	Delta-Sigma Modulator	U400
47	1	AM26LV32EIPW	Differential Line Receiver	U440
48	2	B340A-13-F	Schottky Diode	V241, V242
49	2	BC807-40	Transistor	Q411, Q413
50	2	BC817K-40	Transistor	Q410, Q412
51	1	BLM18PG600	Inductor	L241
52	6	BSC031N06NS3G	Infineon OptiMOS3 Power-Transistor	Q310, Q311, Q312, Q313, Q314, Q315
53	1	BUCHSE-LP-5A	Power Plug	X240
54	3	DFLU1400	Diode	V300, V301, V302
55	1	ENCODER	Connector	X441
56	3	FIDUCIAL	FIDUCIAL	ADJ_1, ADJ_2, ADJ_3
57	1	HSEC8-140-01-S-RA	SAMTEC 80-pin connetor	X200
58	1	IFX1763SJV33	Voltage Regulator	U250
59	1	IFX91041EJV	Voltage Regulator	U240
60	3	LED-GN/D/0603	LED green	V210, V211, V212
61	1	LMV321DBV	OpAmp	U310
62	1	MKDS1/3-3,81	PHOENIX Connector	X300
63	1	MPT0,5/5-2,54	PHOENIX Connector	X440
64	1	MPT0,5/6-2,54	PHOENIX Connector	X400
65	1	OPA2347EA	OpAmp	U401
66	1	OPA4830IPW	OpAmp	U340
67	1	TL084CPW	OpAmp	U410
68	1	TLE4276-2DV	Voltage Regulator	U230
69	1	no ass./0R/0603	Resistor	R253
70	2	no ass./1k2/0603	Resistor	R418, R431

Table 7 List of Material for General Purpose Motor Drive Card (MOT_GPDLV-V2-002)

Sl. No.	Qty	Value	Device	Reference Designator
71	1	no ass./10nF/0603	Capacitor	C251
72	4	no ass./22k/0603	Resistor	R343, R353, R363, R373
73	4	no ass./0603	Capacitor	C340, C350, C360, C370
74	7	no ass./0603	Resistor	R301, R311, R313, R315, R317, R319, R321
75	1	no ass./0805	Resistor	R246
76	1	3-pin header	PowerScale Connector	JP242
77	1	0402	Solder Jumper	SJ1
78	5	no assembly	SMD Pads	TP201, TP210, TP211, TP212, TP213

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