S12VR Hardware Design Guidelines

by: Carlos Aceff

1   Introduction

This document lists the required external components and shows how they should be connected to use the MC9S12VR family of S12 MagniV microcontrollers in any application. It also lists recommended external components that can be used to extend the use cases of the MCU. Finally, it provides a printed-circuit board (PCB) design recommendation section, with layout and routing recommendations that should increment immunity against electromagnetic coupling and reduce electromagnetic emissions.

2   Hardware Design Guidelines

2.1   Voltage regulator

For VSUP, connect a 10 µF electrolytic capacitor in parallel with a 220 nF X7R ceramic capacitor to remove battery ripples. Additionally, the VSUP line needs to be protected against reverse battery conditions (using a diode, for example).

Contents

Another capacitor can also be added as a charge tank to provide power when losing battery. The value of this capacitor depends on the tasks and the amount of time required to shut down the MCU.

The voltage regulator has the following outputs: VDDX1 and VDDX2. These pins are the 5 V power supply for the I/O drivers and need to be externally connected between them.

VDDX1 and VDDX2 should be connected to the following external capacitors:
1. For loop stability and critical to the voltage regulator's proper operation, a 10 µF tantalum capacitor is required. This capacitor can be replaced by a 4.7 µF X7R ceramic capacitor.
2. 220 nF X7R ceramic capacitors can help to protect against spikes created by switching loaded pads. These must be connected to VDDX1, VDDX2, and VDDA
3. To reduce RF emissions, increasing the quality of the supply, a pair of 10 nF in parallel with a 1 nF capacitor must be added in the net.

NOTE
In general, these capacitors must be placed as close as possible to the IC to reduce RF transmission.

Additionally, the VDDA must be externally connected on the board to VDDX1/VDDX2. VSSA must also be externally connected to the same ground as VSSX1/VSSX2 and VSS.

VSENSE can be connected directly to the battery line (without reverse battery protections) because the pin itself is already protected. However, a serial resistor of 10 KΩ is required to protect the device from fast transients.
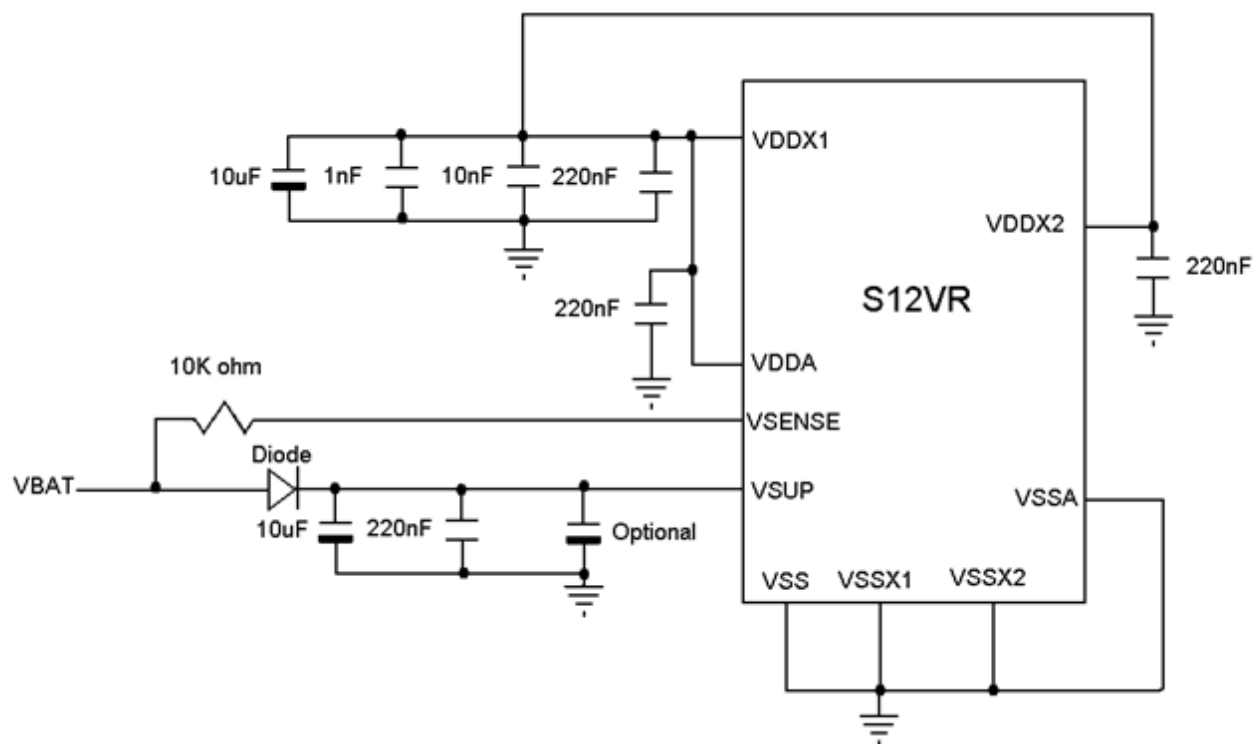
Figure 1. Voltage regulator

2.2 Reset circuit

The reset line is a bi-directional line. It can be used in either of the following ways:

- External circuits can initiate an MCU reset by pulling down this line.
- The MCU can initiate a reset to trigger external resets.

When the MCU initiates an external reset due to a COP or clock monitor reset, it is important that the line not be externally pulled low for more than 24 μs after reset is pulled low. The CPU will otherwise fetch the external pin RESET vector address (0xFFFE) instead of the corresponding COP or clock monitor reset vector address.

To accommodate a debounce capacitor in the reset line, a diode (for example the BAV10) can be added to the circuit. The diode keeps the capacitor charged for the period of time that the MCU pulls low the reset line during a COP or clock monitor reset event; thus, the correct reset vector address will be fetched. See Figure 2.
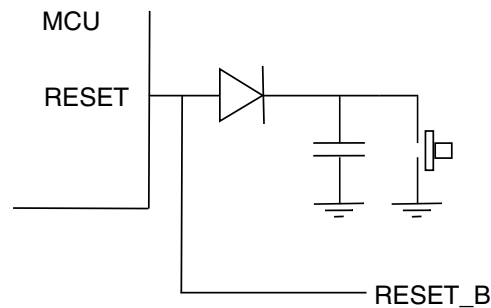
Figure 2. Reset circuit

No external pullup resistor is required at the reset line since the MCU already includes a 5KΩ resistor.

2.3 BKGD, test, interrupt pins, and unused pins

The BKGD line needs an external pullup resistor in the range of 4.7 KΩ to 10 KΩ. 10 pF capacitors can be connected to this pin to filter the signal. However, it is not recommended to use larger values since it can affect the slew rate of the signal used to program the MCU.

The TEST line is used only in Freescale factory tests. In any actual application it must be connected to ground.

Used interrupt pins should have a corresponding internal pullup or pulldown resistor configured to prevent wrong interrupt detections. If the interrupt occurs with a low edge or low level, then it must have a pullup configured; otherwise, the pulldown should be configured. Common modules with interrupt capable pins are the Keyboard Interrupt (KBI), Timer (TIM) modules, and the IRQ and XIRQ pins.

Unused digital pins need to have the internal pullup or pulldown resistors configured. This will assure a known state at all times.

If High Side Drivers are unused, connect VSUPHS to a reverse battery protected reference and leave the unused HSX disconnected.

If the Low Side Drivers are not used, connect LSGND to ground and leave the unused LSX disconnected.

If the LINPHY is not used, connect the LGND to ground and leave the corresponding LIN terminal floating.

2.4 Analog-to-digital module, high-voltage inputs

To keep the maximum error in 10-bit resolution less than 1/2LSD (2.5mV) at the maximum leakage current, the maximum source resistance should be 1 KΩ.

High-voltage inputs need an external resistor of 10 KΩ to protect the device from fast transients and to achieve the specified pin input divider ratios when used in analog mode.

2.5   High-side drivers, low-side drivers, and EVDD

The VSUPHS high-side driver power pin must be connected to a reverse battery protected line, typically through a diode. This pin can be directly connected to the VSUP pin, which should also be protected by a diode.
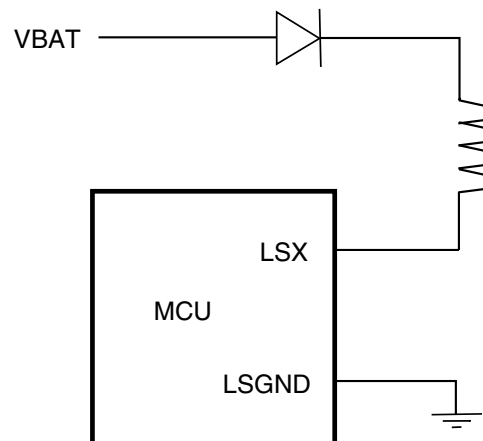
> **NOTE**
> The nominal current high-side drivers can operate is 50 mA, so the resistive load must consider that specification.

> **NOTE**
> On mask set 2N05E, high-side drivers cannot drive capacitive loads. Doing so could activate the overcurrent shutdown circuitry. Mask set 0N59H includes an overcurrent fault mask logic. This can mask faults that last less than 10 µs after the High Side Driver is activated, thus masking the overcurrent associated with small capacitors connected at the pin.

Low-side drivers drive coils up to 450m Henries (H) at a 10 kHz frequency; a reverse battery protection is required. Thus, the other end of the coil can be connected to the VSUP pin, which should also be protected by a diode. Pin LSGND must be connected to the same ground as the voltage regulator.

See Figure 3 for a connection example.

Figure 3. Low-side driver recommended circuit

> **NOTE**
> These devices do not drive capacitive loads; doing so could activate the overcurrent shutdown circuitry.

The EVDD does not require external devices other than the load to drive (20 mA at 5 V).

2.6   LINPHY

When configured as a master, a 1 KΩ pullup resistor must be added to this line. When configured as a slave, no external pullup resistor is required, since the module comes with a configurable pullup slave resistor. It is also recommended to have a 0.22 nF X7R capacitor connected between LIN and LGND. This value may need to be reduced if the total LIN bus capacitance exceeds the maximum allowed overall bus capacitance (10 nF), or if the maximum LIN time constant in the overall system exceeds 5 µs.
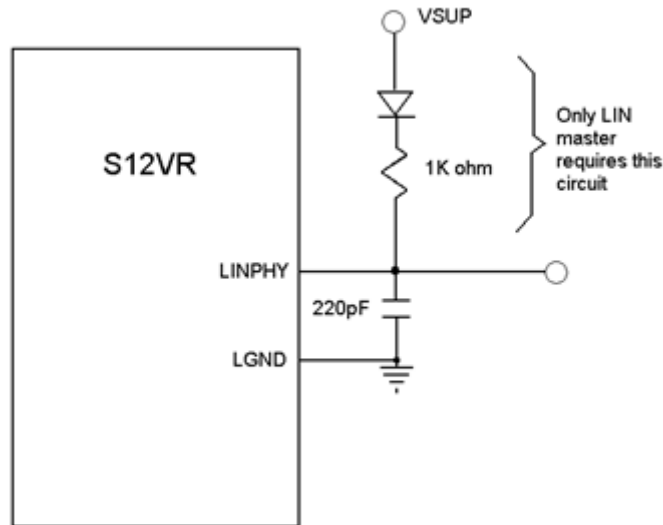
Figure 4. LINPHY components

3 PCB Design Recommendations

3.1 General layout considerations

To help the MCU dissipate heat (lowering the thermal resistance and allowing lower junction operating temperatures), it is recommended to leave a square of copper pour connected to ground on the same face on which the MCU is mounted. Use this copper pour to connect all the return to ground pins.

To increment the EMC immunity, place a plane covering the complete area of the board and connected to ground below the layer on which the MCU is mounted. This plane will also help to dissipate heat.
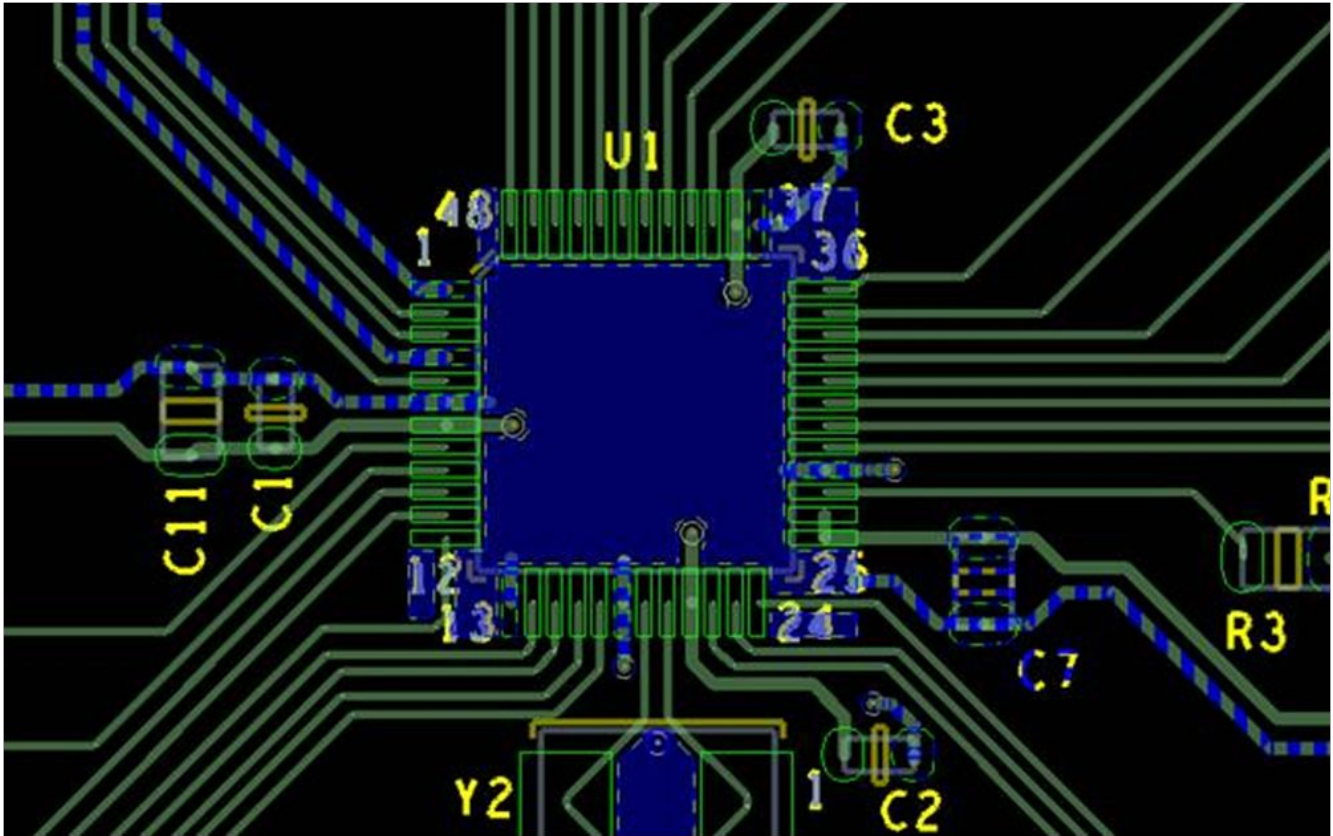
In the figure above, the blue region is a copper pour placed below the MCU (U1). Note that the MCU is powered through pin 25 and that the copper pour is used as the MCU's return to ground.

3.2   External oscillator layout

To reduce the electromagnetic emissions, place the crystal and associated capacitors close to the MCU. To increase the immunity against electromagnetic coupling, follow a pattern similar to the one shown in the figure below. In this pattern, the crystal/resonator is placed close to the MCU and the associated capacitors are placed close to the crystal/resonator. A copper pour (labeled "Plane A" in the figure) is added to separate the crystal/resonator circuits traces from other copper pours or traces where electromagnetic coupling could occur. Since the VSS pin (pin 18) is the return to GND coming from the core and the external oscillator circuitry, it is recommended to use this pin to reference the copper pour ("Plane A" in the figure).
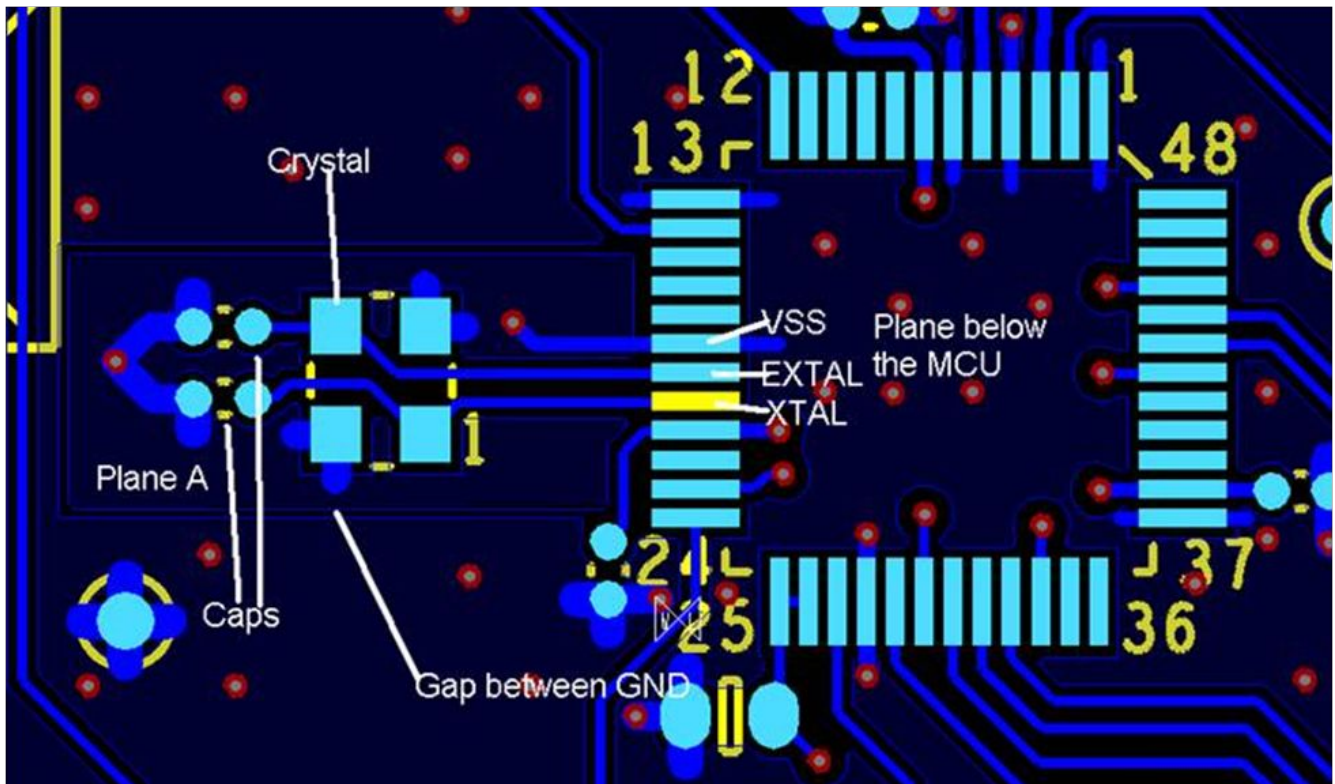
To further isolate this circuit from other traces or copper pours on other layers, it is recommended to add another copper pour to the layer below the one on which the crystal/circuit is placed. This copper pour will be referenced to VSS by the use of two vias: one directly connected to the VSS pin and the other connected close to the capacitors' return to GND.

S12VR Hardware Design Guidelines, Rev 1, 10/2013

3.3   Voltage regulator component layout

To reduce electromagnetic emissions, place 220 nF capacitors (in the smallest package available) close to the following pins: VSUP (pin 25), VDDX1 (pin 7), VDDX2 (pin 21), and VDDA (pin 38).

The VDDX1, VDDX2, and VDDA pins need to be shorted between them; to make the length of these traces short, they should be routed below the MCU using an internal layer. To allow the collection of all MCU grounds, avoid cutting the copper pour right below the MCU; use internal layers to route traces below the MCU.
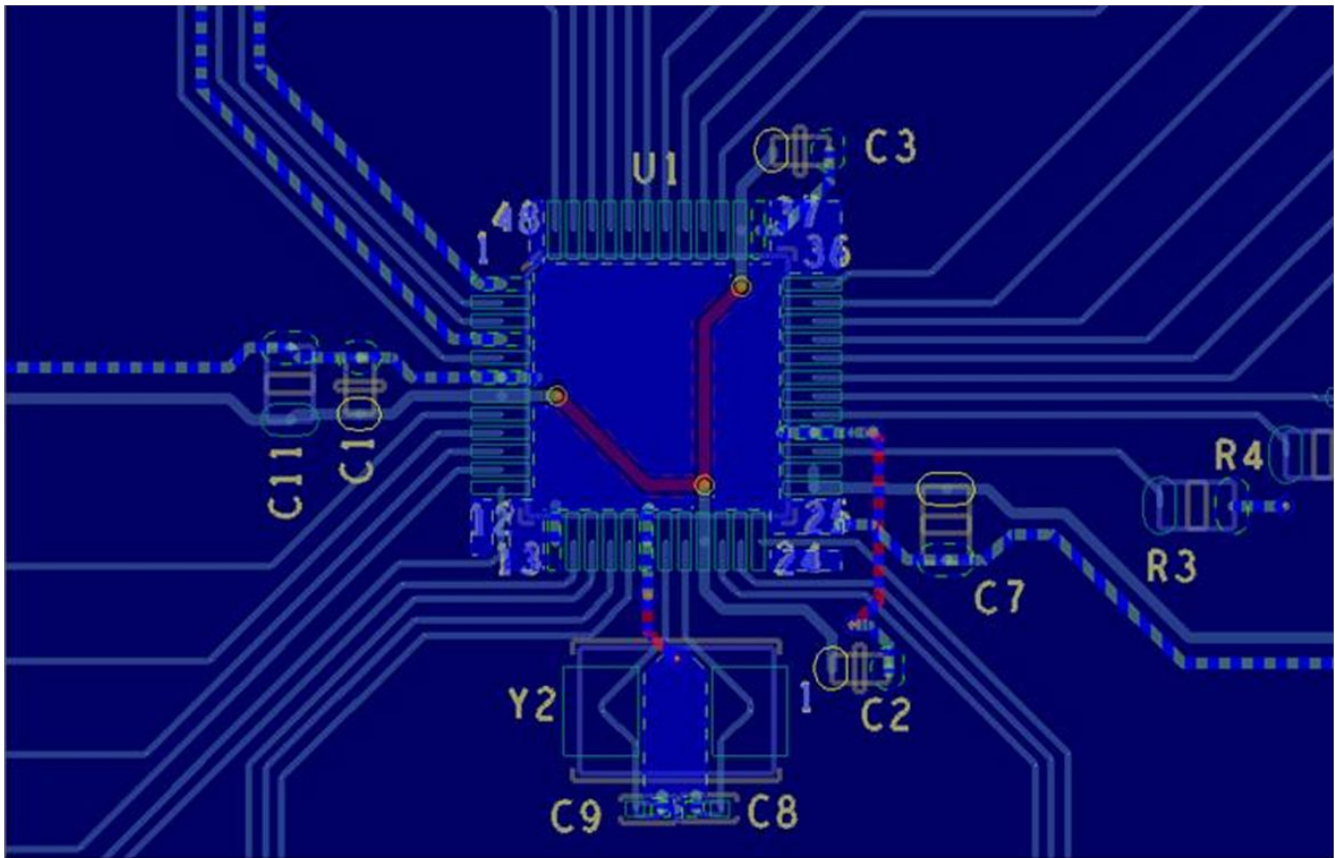
The figure above shows 220nF capacitors C7, C2, C1, and C3 placed close to the MCU. The return to ground of capacitor C2 (pin VSSX2) is connected using two vias. However, if mounting on both faces is allowed, mount this capacitor on the face opposite the MCU and closer to the pins where it should be connected. The solid red lines in the figure show the traces required to short the 5V voltage regulator outputs and VDDA. These traces are routed one layer below where the MCU is placed.

4   Conclusion

In addition to several external components that must be connected to the MCU, some recommended components can extend its use cases. These components are listed in the different sections of this document.

Also, proper layout and routing can help to increase the immunity of the system and reduce its emissions.

5 References

Freescale Semiconductor, *MC9S12VR Family Reference Manual* (MC9S12VRRMV2), http://www.freescale.com/magniv

6 Revision history

Revision number	Date	Description of changes
0	03/2013	Initial version.
1	10/2013	- Reset circuit : removed external pullup resistor from figure and revised text to indicate that no external pullup is required on the reset line. Changed wording in second paragraph to "The CPU will otherwise fetch the external pin RESET vector address (0xFFFE) instead of the corresponding COP or clock monitor reset vector address" (was "The MCU will otherwise trigger the external pin RESET exception instead of . . ."). Added sentence to third paragraph: "The diode keeps the capacitor charged for the period of time that the MCU pulls low the reset line during a COP or clock monitor reset event; thus, the correct reset vector address will be fetched." - BKGD, test, interrupt pins, and unused pins : removed "An external resistor in the range of 4.7 to 10 k ohm is recommended to pull up or pull down interrupt pins" from the third paragraph and changed wording of the fourth paragraph to "Unused digital pins need to have the internal pullup or pulldown resistors configured. This will assure a known state at all times" (was "Unused digital pins need pull up or down resistors so the current consumed by them can be decreased by setting the pin low or high.. EXTAL and XTAL come after reset with pull downs and must be connected to GND if not used"). Changed wording in the sixth paragraph to "If the Low Side Drivers are not used, connect LSGND to ground and leave the unused LSX disconnected" (was "If the Low Side Drivers are not used, connect LSGND to ground and leave the corresponding low side driver connected"). - Analog-to-digital module, high-voltage inputs : changed wording in first paragraph to "To keep the maximum error in 10-bit resolution less than 1/2 LSD (2.5 mV) at the maximum leakage current, the maximum source resistance should be 1KΩ" (was "To protect the analog inputs from disruptive input currents (maximum +/-2.5 mA), these lines must be protected by a serial resistor of 1 KΩ∀). - High-side drivers, low-side drivers, and EVDD : replaced "Its nominal operation is from 7 V to 18 V1" with "This pin can be directly connected to VSUP pin which should be protected also by a diode" and revised note about mask set 0N59H. Changed wording of first note to "The nominal current high-side drivers can operate is 50 mA, so the resistive load must consider that specification" (was "The maximum current high-side drivers can operate is 50 mA, so the resistive load must consider that specification"). Changed wording of second note to "associated with small capacitors connected at the pin" (was "small capacitance at the pin"). Changed wording in second paragraph to "Low-side drivers can drive coils up to 450m Henries (H) at 10KHz frequency; a reverse battery protection is required. Thus the other end of the coil can be connected to VSUP pin which should also be protected by a diode" (was "Low-side drivers drive coils up to LPLS0/1 Henries (H) at a 10 kHz frequency; a diode is recommended. Pin LSGND must be connected to the same ground as the voltage regulator"). - Voltage regulator : changed wording in third paragraph to "These pins are the 5 V power supply for the I/O drivers and need to be externally connected between them" (was "These pins are the 5 V power supply for the I/O drivers and are internally connected by metal"). In capacitor list, changed "wet chemical capacitor" in the first list item to "tantalum capacitor." Added sentence: "This capacitor can be replaced by a 4.7 µF X7R ceramic capacitor." - Editorial changes and improvements throughout.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support