PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD/13/7945
Dated 18 Jun 2013

Capacity expansion, for the product housed in TO-220 package at the Nantong Fujitsu Microelectronics (China) Subcontractor plant

Table 1. Change Implementation Schedule

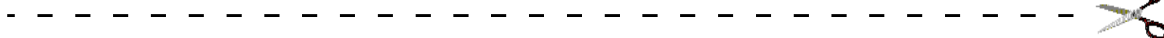
Forecasted implementation date for change	10-Sep-2013
Forecasted availability date of samples for customer	11-Jun-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Jun-2013
Estimated date of changed product first shipment	17-Sep-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Assembly additional location
Reason for change	To improve service to ST Customers
Description of the change	To respond the ever increasing demand for the products housed in TO-220 package, ST is glad to announce the expansion of capacity at Nantong Fujitsu Microelectronics (China) Subcontractor factory, For the complete list of the part numbers affected by this change, please refer to the attached Products List
Change Product Identification	will be ensured by the first two digits of the traceability code ("GF")
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt Please sign and return to STMicroelectronics Sales Office	**PCN IPD/13/7945** **Dated 18 Jun 2013**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

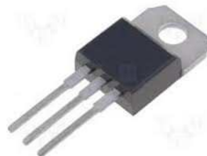
Name	Function
Giuffrida, Antonino	Marketing Manager
Martelli, Nunzio	Product Manager
Vitali, Gian Luigi	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

IPD Group

Assembly and Testing capacity expansion, for the product housed in TO-220 package,
at the Nantong Fujitsu Microelectronics (China) Subcontractor plant.

Packages typology



WHAT:

To respond the ever increasing demand for the products housed in TO-220 package,
ST is glad to announce the expansion of capacity at Nantong Fujitsu Microelectronics (China) Subcontractor factory,
For the complete list of the part numbers affected by this change, please refer to the attached Products List

Samples, are available right now upon request for immediate customer qualification, while the full availability of products will be granted from wk 22 2013 onwards,

WHY:

- To improve service to ST Customers

HOW:

By expanding capacity according the ST quality and reliability standard.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant product's datasheets.
There are as well no modifications in the packing modes nor in the standard delivery quantities either it may affect ST's Customers assembly methods.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests.Please refer to Appendix 1 for all the details.

WHEN:

Production start and first shipments will occur as indicated in the table below.

Affected Product Types	Samples	1st Shipment
PowerMOSFET	**Now**	**Wk22**
Power Bipolar	**Now**	**Wk22**
Thyristor &Triac	**Now**	**Wk22**
Rectifier	**Now**	**Wk22**

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled in the Nantong Fujitsu Microelectronics Subcontractor factory, will be ensured by the first two digits of the traceability code ("GF") .

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Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Reliability Report

Assembly and Testing capacity expansion, for the product housed in TO-220 package, at the NFME (China)Subcontractor plant.

General Information	
Product Lines:	ED7K / EZ66
Product Families:	Power MOSFET
P/Ns:	STP140NF75 (ED7K) STP10NK60Z (EZ66)
Product Group:	IMS - IPD
Product division:	Power Transistor Division
Package:	TO-220
Silicon Process techn.:	PowerMOSFET - StripFET™

Locations	
Wafer Diffusion Plants:	*ED7K: Global Foundries* *EZ66: AngMoKio (SINGAPORE)*
EWS Plants:	*ED7K: Global Foundries* *EZ66: AngMoKio (SINGAPORE)*
Assembly plant:	*NFME CHINA*
Reliability Lab:	*IMS-IPD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	May 2013	8	C. Cappello	G.Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the TO-220 package graded Molding Compound manufactured in the NFME (China) Subcontractor assy plant.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STP140NF75 LINE: ED7K PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*Global Foundries (Singapore)*
Technology	Power MOSFET - StripFET™
Die finishing back side	Ti/Ni/Ag
Die size	4610 x 6350 μm^2
Metal	Al/Si/Cu
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Global Foundries (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	NFME (China)
Package description	TO-220
Molding compound	HF Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 15 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	NFME (China)
Tester	TESEC

D.U.T.: STP10NK60Z LINE: EZ66 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*AngMoKio (Singapore)*
Technology	Power MOSFET - StripFET™
Die finishing back side	Ti/Ni/Au
Die size	4950 x 3810 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*AngMoKio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	NFME (China)
Package description	TO-220
Molding compound	HF Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	NFME (China)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STP140NF75	ED7K	Power MOSFET
2	STP10NK60Z	EZ66	Power MOSFET

5.2 Reliability test plan summary

Lot. 1 - D.U.T.: STP140NF75 LINE: ED7K PACKAGE: TO-220

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 1
HTRB	N	JESD22 A-108	T.A.=175°C Vdss=60V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 20V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 175°C	77	168 H 500 H 1000 H	0/77
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=50V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77
TF	N	Mil-Std 750D Method 1037	ΔTc=105°C	77	5 Kcy 10 Kcy	0/77

Lot. 2 - D.U.T.: STP10NK60Z LINE: EZ66 PACKAGE: TO-220

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 2
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77
TF	N	Mil-Std 750D Method 1037	ΔTc=105°C	77	5 Kcy 10 Kcy	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Qualification of
Rectifiers in TO-220AB package: Additional Assembly and Test Location in China

General Information	
Product Line	Rectifiers (BU78)
Product Description	Bipolar, Turboswitch and Power Schottky in TO-220AB package: Additional assembly and test location in China
Product Group	IPD
Product division	ASD & IPAD
Package	TO-220AB (3 leads)
Maturity level step	Qualified

Locations	
Wafer fab	STM Singapore STM Tours (France)
Assembly plant	Subcontractor (China)
Reliability Lab	STM Tours (France)

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	18-Feb-2013	9	I. BALLON	First issue Qualification of Rectifiers (Bipolar, Turboswitch and Power Schottky in TO-220AB package: Additional assembly and test location in China

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP 2614	Reliability requirements for product qualification
0061692	Reliability tests and criteria for qualifications
FMEA	8419012
RER	1242001

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
PCT	Pressure Pot 2 bars
THB	Temperature Humidity Bias
IOLT	Intermittent Operational Life
RSH	Resistance to Solder Heat
SD	Solderability

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify new subcontractor for TO-220AB (3 leads) package for Rectifiers devices

The product series currently involved in this qualification are listed below.

Product sub-Family	Commercial product
Rectifiers	STPSxxxCT STTHxxxCT

Specific devices not expressly listed in the above table are included in this change.

The reliability methodology used follows the JESD47-E: « Stress Test Driven Qualification Methodology ».
The following reliability tests ensuing are:

- HTRB to evaluate the risk of contamination.
- THB to verify there is no apparition of corrosion and risk of moisture penetration.
- TC,RSH and IOLT to ensure the mechanical robustness of the products.
- Solderability to verify good wettability on leads

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

- Rectifiers (Bipolar, Turboswitch, Power Schottky) in TO-220AB (3 leads) package: Additional assembly and test location in China.

4.2 Construction note

	Rectifiers (STPSxxxCT-STTHxxxCT) in TO-220AB package
Wafer/Die fab. information	
Wafer fab manufacturing location	STMicroelectronics Singapore STMicroelectronics Tours (France)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	STMicroelectronics Singapore STMicroelectronics Tours (France)
Assembly information	
Assembly site	Subcontractor (China)
Package description	TO-220AB (3leads)
Molding compound	Epoxy resin
Lead finishing process	Electroplating
Lead finishing material	Matte Tin (Sn 100%)
Final testing information	
Testing location	Subcontractor (China)

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Product	Back End	Package	Product Family
1	STTH16L06CT	Subcontractor (China)	TO-220AB (3 leads)	Turboswitch
2	STTH2002CT			Bipolar
3	STPS40M100CT			Power Schottky
4	STPS40SM100CT			
5				

5.2 Test plan and results summary

Die Oriented Tests

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1	Lot 2				
HTRB	N	JESD22 A-108	Tj, Vr = 0.8xVrrm	154	168 H	0/77	0/77				
					500 H	0/77	0/77				
					1000 H	0/77	0/77				

Package Oriented Tests

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						Note
						Lot 3						
THB	N	JESD22 A-101	Ta = 85°C, RH = 85%, Vr = 0.8xVrrm or 100V max	25	168 H	0/25						
					500 H	0/25						
					1000 H	0/25						
				SS	Steps	Failure/SS						Note
						Lot 3	Lot 5					
TC	N	JESD22 A-104	Ta = -65°C to 150°C 2 cycles/hour	50	100 cy	0/25	0/25					
					500 cy	0/25	0/25					
				SS	Steps	Failure/SS						Note
						Lot 2						
PCT	N	JESD22 A-102	121°C, RH=100%, P=2 bars	77	96hrs	0/77						
				SS	Steps	Failure/SS						Note
						Lot 3						
IOLT	N	MIL-STD 750 Method 1037	Delta Tc=85°C, Pon=3.5min Poff=3.5min	25	8572cy	0/25						
						Failure/SS						Note
						Lot 5						
RSH	N	JESD22B-106	2 dipping at 260°C 10s On / 15s Off	12		0/12						
				SS	Steps	Failure/SS						Note
						Lot 4	Lot 5					
SD	N	J-STD-002	245°C SnAgCu bath Dry aging	20	Visual inspection	0/10	0/10					
			245°C SnAgCu bath Wet aging	20	Visual inspection	0/10	0/10					
						Lot 4	Lot 5					
			220°C SnPb bath Dry aging	20	Visual inspection	0/10	0/10					
			220°C SnPb bath Wet aging	20	Visual inspection	0/10	0/10					

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

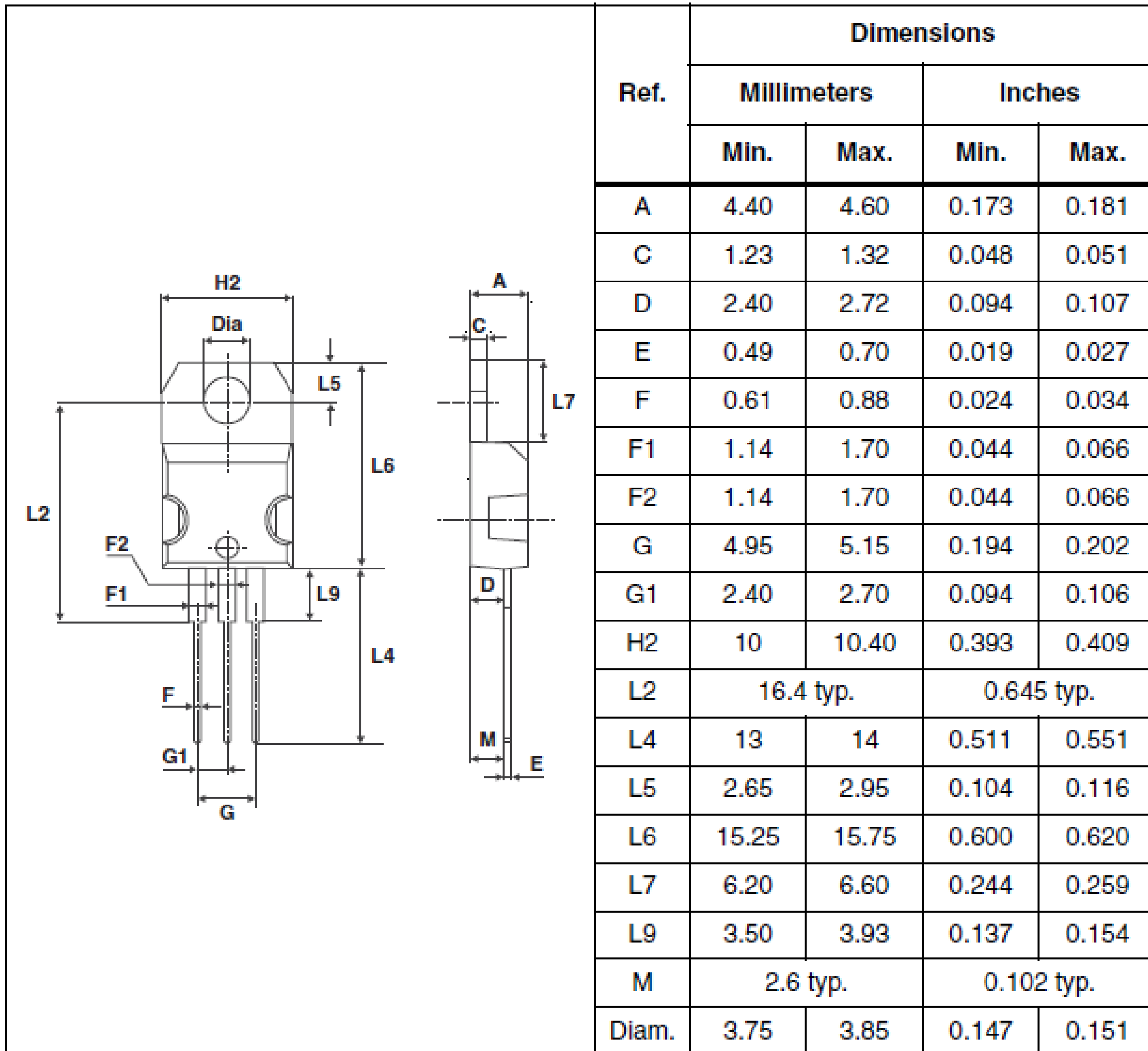
Package	Pin connection
TO-220AB	A1 (1) A2 (3) K (2) K A A K

6.1.2 Bonding diagram

Package	Bonding diagrams
TO-220AB	3 2 1

6.1.3 Package outline/Mechanical data

- **TO-220AB (3 leads)**



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
C	1.23	1.32	0.048	0.051
D	2.40	2.72	0.094	0.107
E	0.49	0.70	0.019	0.027
F	0.61	0.88	0.024	0.034
F1	1.14	1.70	0.044	0.066
F2	1.14	1.70	0.044	0.066
G	4.95	5.15	0.194	0.202
G1	2.40	2.70	0.094	0.106
H2	10	10.40	0.393	0.409
L2	16.4 typ.		0.645 typ.	
L4	13	14	0.511	0.551
L5	2.65	2.95	0.104	0.116
L6	15.25	15.75	0.600	0.620
L7	6.20	6.60	0.244	0.259
L9	3.50	3.93	0.137	0.154
M	2.6 typ.		0.102 typ.	
Diam.	3.75	3.85	0.147	0.151

6.2 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PCT Pressure Pot	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors), followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.

Test name	Description	Purpose
RSH	The device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.
SD	The device is aged in a wet and dry bath of solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish. .	To test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder

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