

TVS Diode

Transient Voltage Suppressor Diodes

ESD3V3XU1BL

Bi-directional Ultra Low Capacitance ESD / Transient Protection Diode

ESD3V3XU1BL

Data Sheet

Revision 1.3, 2013-09-11
Final

Edition 2013-09-11

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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Revision History: Revision 1.2, 2013-02-06

Page or Item	Subjects (major changes since previous revision)
Revision 1.3, 2013-09-11	
5-6	Updated of Table 2-1 , Table 2-2 , Table 2-3 and Table 2-4

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Last Trademarks Update 2010-10-26

1 Bi-directional Ultra Low Capacitance ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection of high speed data lines exceeding
 - IEC61000-4-2 (ESD): ± 20 kV (air / contact)
 - IEC61000-4-4 (EFT): ± 2.5 kV / ± 50 A (5/50 ns)
 - IEC61000-4-5 (surge): ± 3 A (8/20 μ s)
- Maximum working voltage: $V_{RWM} = \pm 3.6$ V
- Ultra low capacitance $C_L = 0.20$ pF (typical) at $f = 1$ GHz
- Very low clamping voltage: $V_{CL} = 14$ V at $I_{TLP} = 16$ A (typical) according to TLP [1]
- Very low dynamic resistance: $R_{DYN} = 0.45$ Ω (typical)
- Pb-free and halogen-free package (RoHS compliant)



1.2 Application Examples

- USB 3.0, Firewire, DVI, HDMI, S-ATA, DisplayPort, Thunderbolt
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

1.3 Product Description

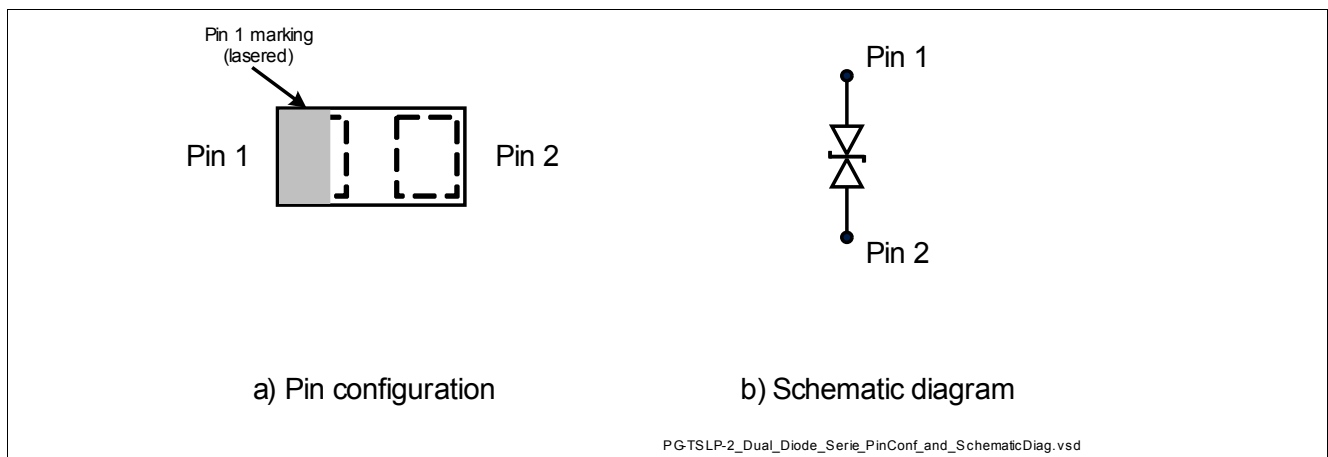


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD3V3XU1BL	TSLP-2-17	1 line, bi-directional	X2

2 Characteristics

Table 2-1 Maximum Rating at $T_A = 25\text{ °C}$, unless otherwise specified ¹⁾

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge ²⁾	V_{ESD}	–	–	20	kV
Peak pulse current ($t_p = 8/20\text{ }\mu\text{s}$) ³⁾	I_{PP}	–	–	3	A
Peak pulse power $t_p = 8/20\text{ }\mu\text{s}$ ³⁾	P_{PK}	–	–	36	W
Operating temperature range	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) Device is electrically symmetrical

2) V_{ESD} according to IEC61000-4-2 ($R = 330\text{ }\Omega$, $C = 150\text{ pF}$ discharge network)

3) I_{PP} according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component.

2.1 Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

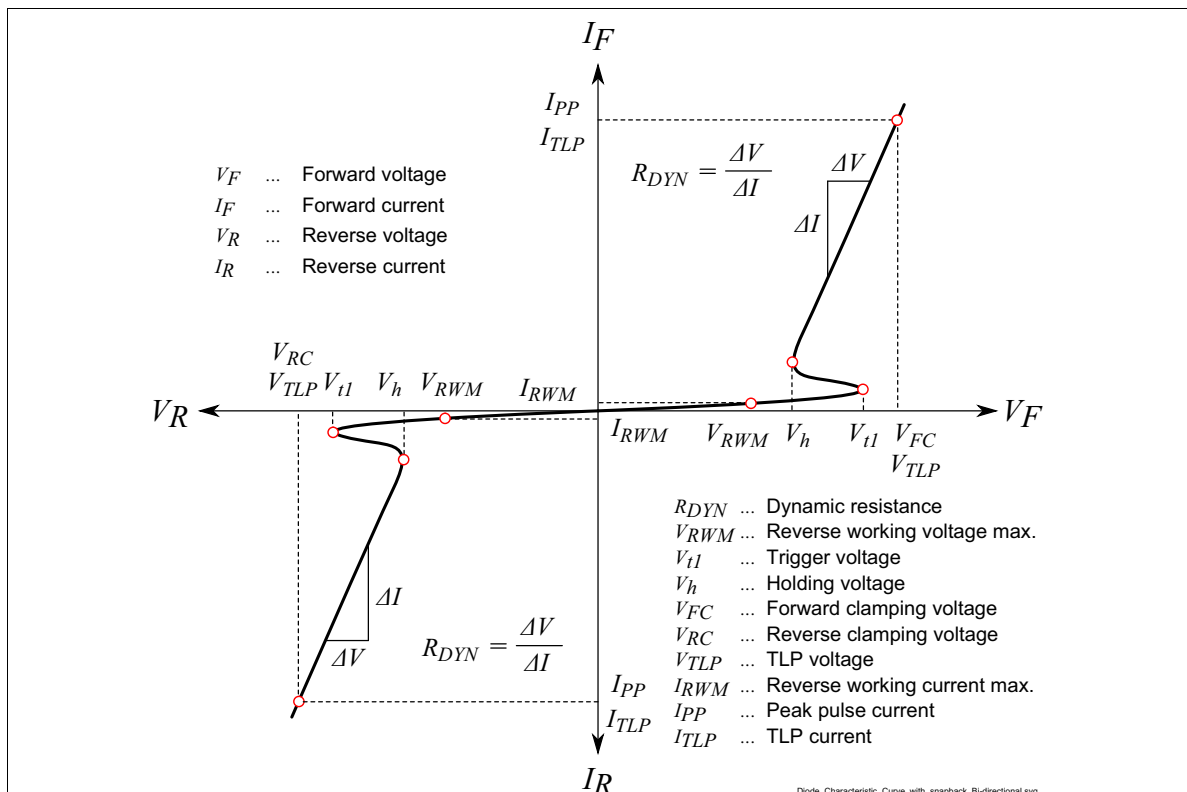


Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-3.6	–	3.6	V	
Reverse current	I_R	–	1	50	nA	$V_R = 3.3\text{ V}$
Trigger voltage	V_{t1}	5	–	–	V	
Holding voltage	V_h	4	4.6	–	V	$I_R = 10\text{ mA}$

1) Device is electrically symmetrical

Table 2-3 AC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.22	0.35	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		–	0.20	–		$V_R = 0\text{ V}, f = 1\text{ GHz}$
Series inductance	L_S	–	0.4	–	nH	

Table 2-4 ESD and Surge Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ²⁾	V_{CL}	–	14	–	V	$I_{TLP} = 16\text{ A}$
		–	20	–		$I_{TLP} = 30\text{ A}$
Clamping voltage ³⁾		–	12	–		$V_{ESD} = 8\text{ kV}$
		–	18	–		$V_{ESD} = 15\text{ kV}$
Clamping voltage ⁴⁾		–	8	–		$I_{PP} = 3\text{ A}$
Dynamic resistance ²⁾	R_{DYN}	–	0.45	–	Ω	
Dynamic resistance ⁴⁾		–	1	–		

1) Device is electrically symmetrical

2) ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitive Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$ and V_{TLP} averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristic between $I_{TLP1} = 5\text{ A}$ and $I_{TLP2} = 40\text{ A}$. Please refer to Application Note AN210[1].

3) V_{ESD} according to IEC61000-4-2, V_{CL} at 30 ns ($R = 330\ \Omega$, $C = 150\text{ pF}$ discharge network)

4) I_{PP} according to IEC61000-4-5 ($t_p = 8/20\ \mu\text{s}$)

3 Typical Characteristics

At $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

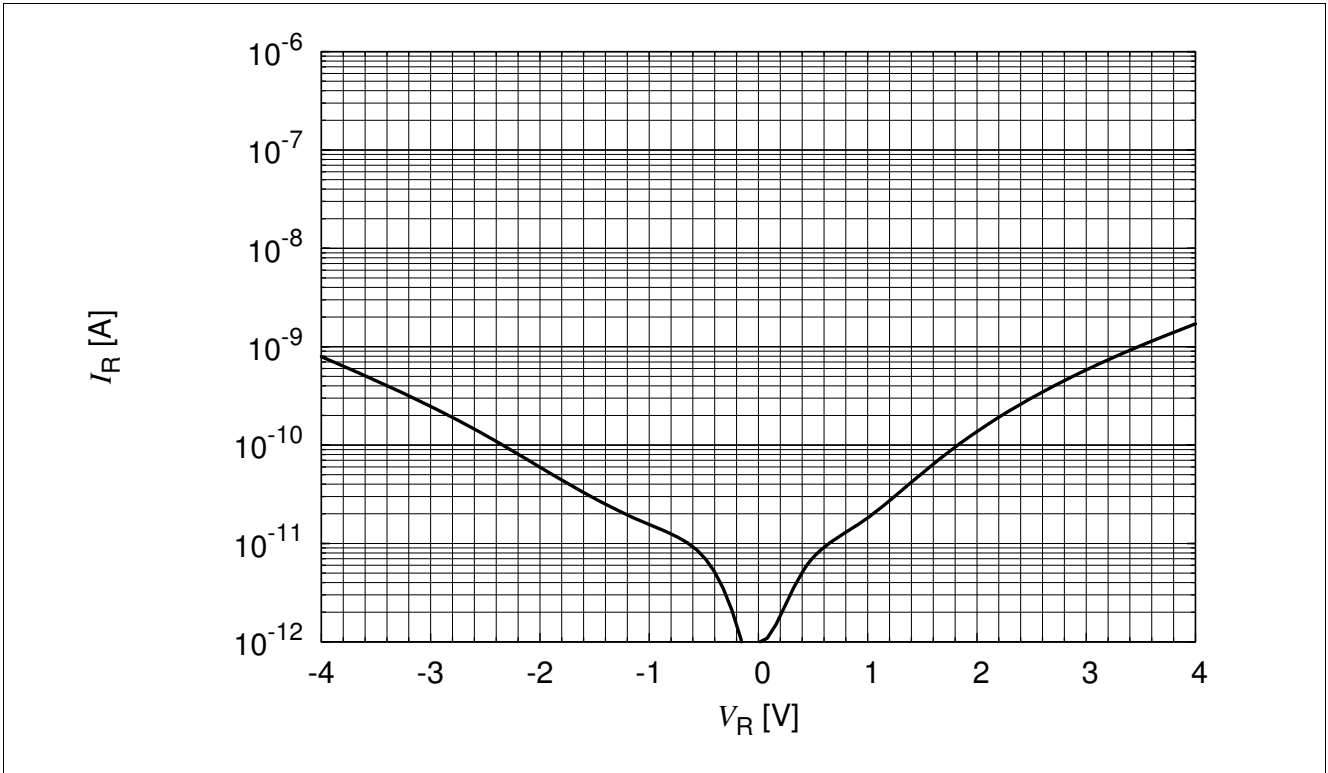


Figure 3-1 Reverse current $I_R = f(V_R)$

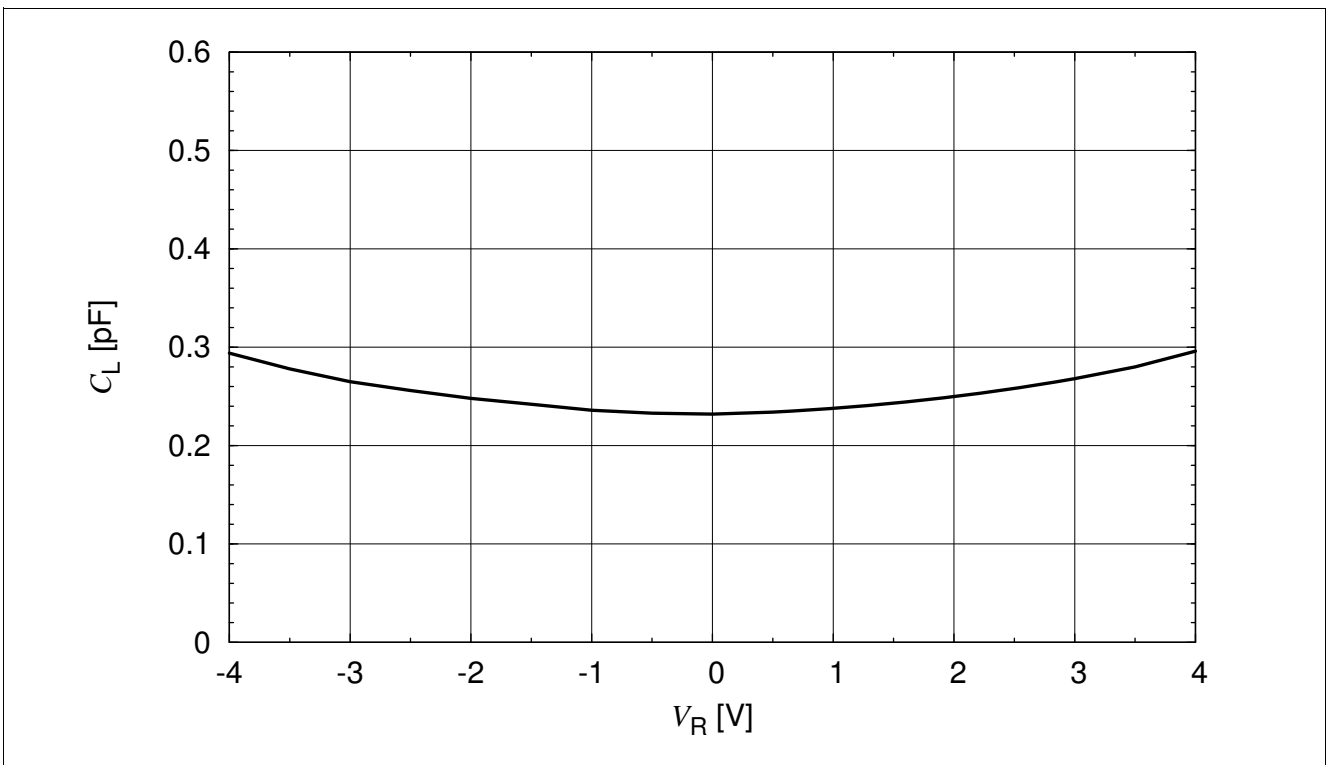


Figure 3-2 Line capacitance $C_L = f(V_R), f = 1\text{ MHz}$

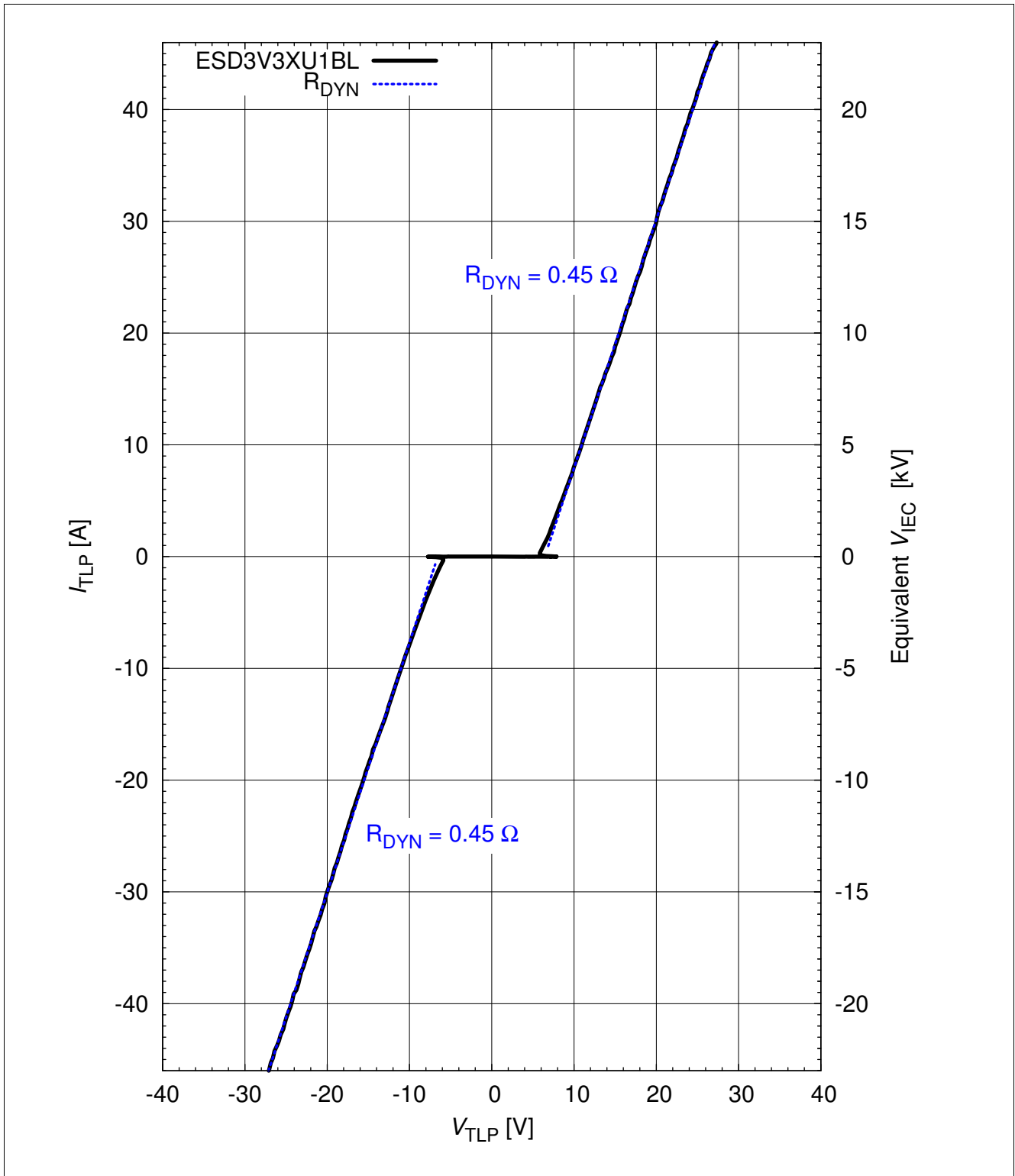


Figure 3-3 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$, I_{TLP} and V_{TLP} averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 5 \text{ A}$ and $I_{TLP2} = 40 \text{ A}$. Please refer to Application Note AN210[1]

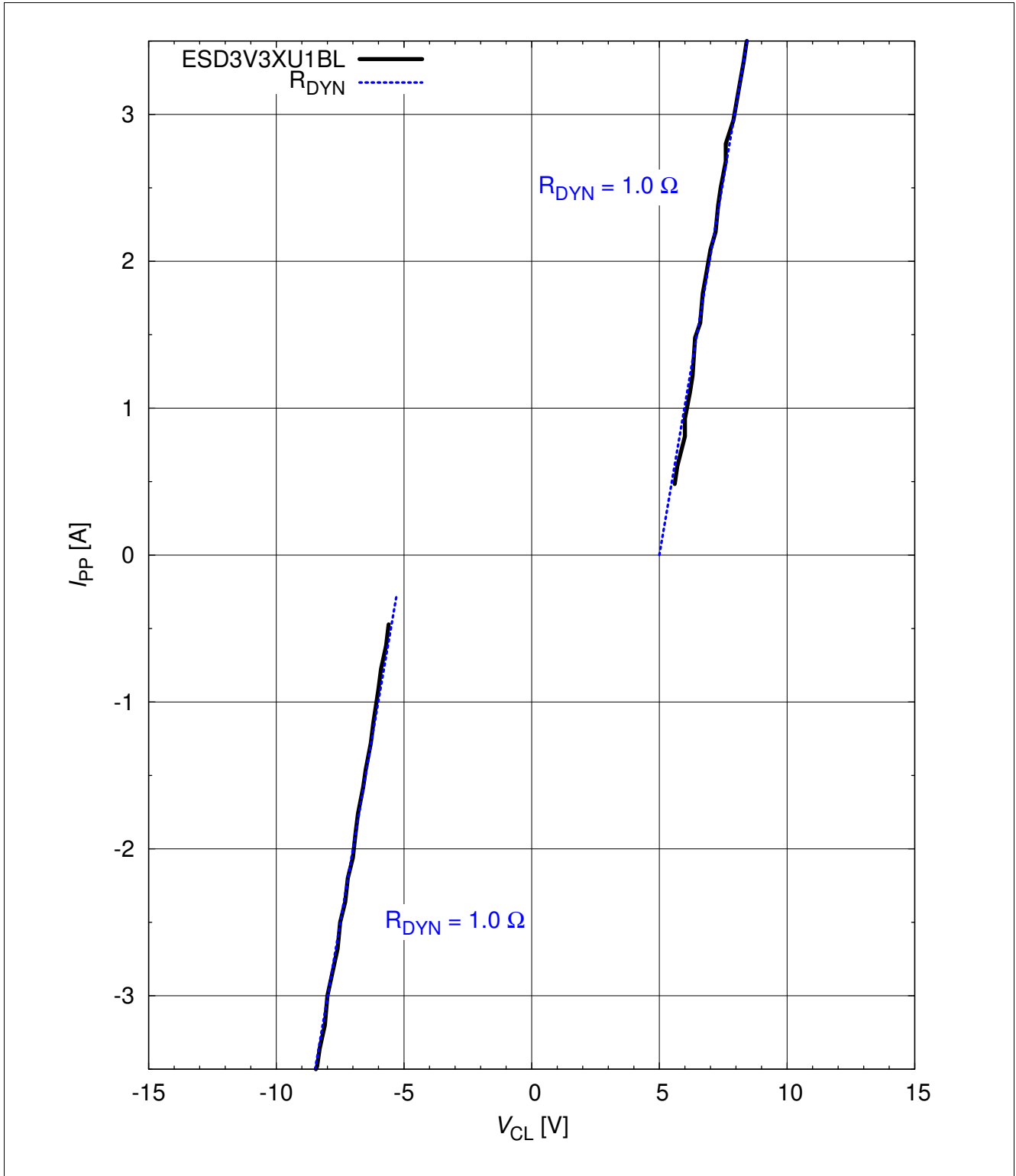


Figure 3-4 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

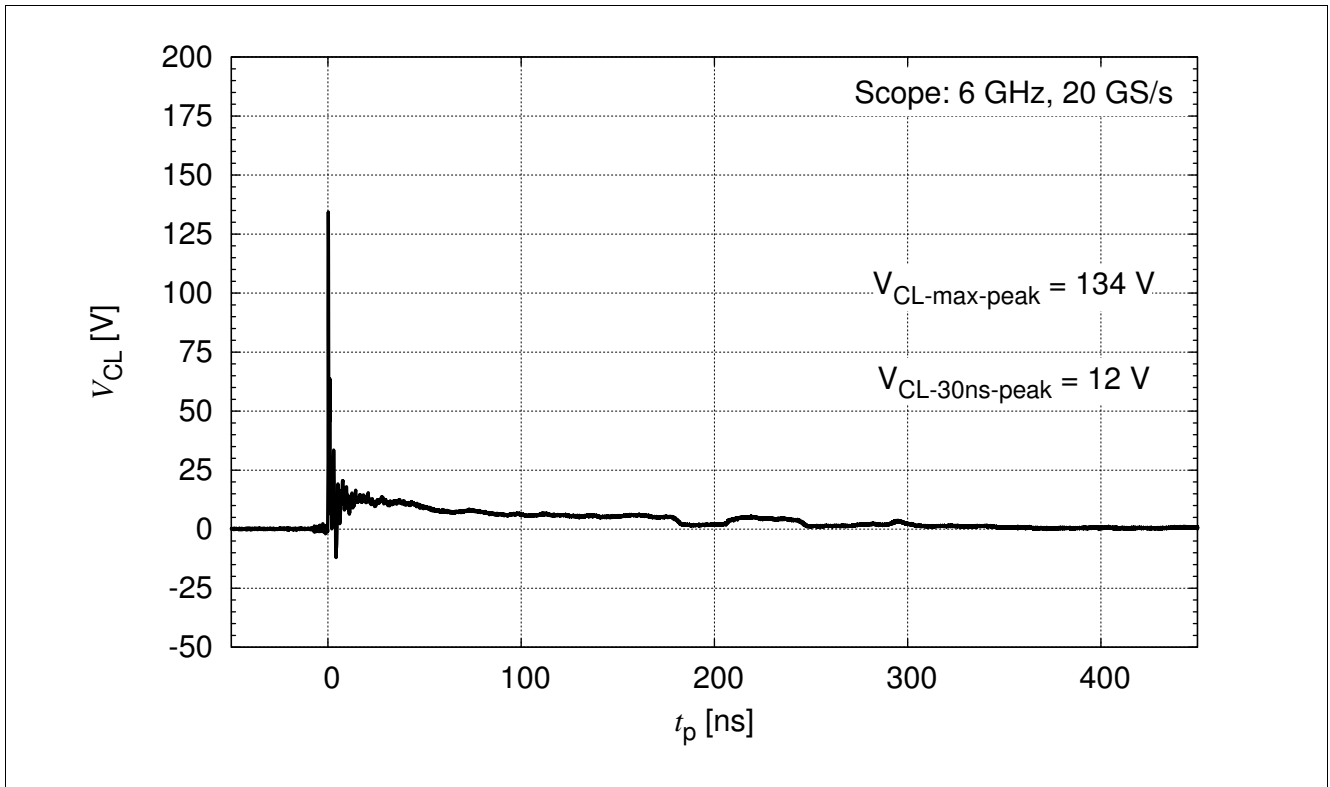


Figure 3-5 Clamping voltage at +8 kV discharge according IEC61000-4-2 ($R = 330 \Omega$, $C = 150 \text{ pF}$)

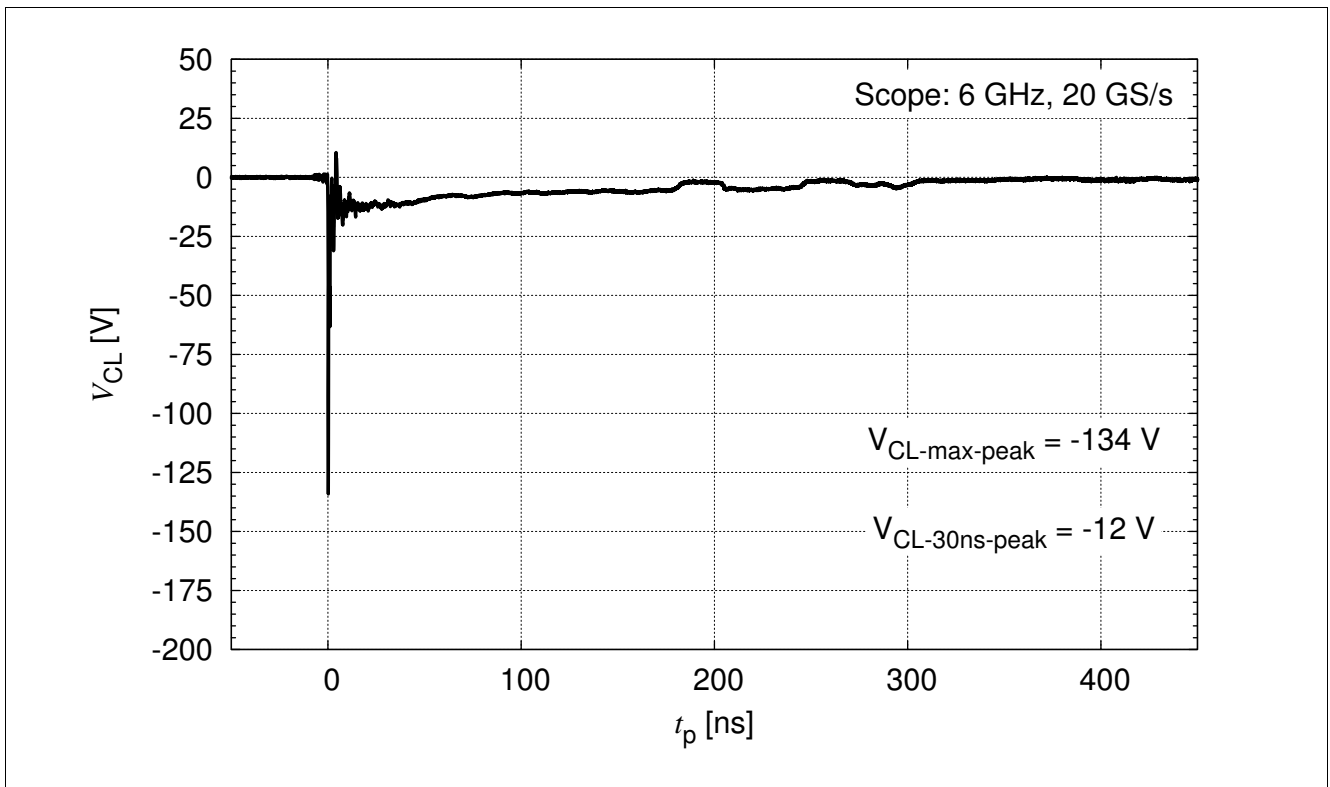


Figure 3-6 Clamping voltage at -8 kV discharge according IEC61000-4-2 ($R = 330 \Omega$, $C = 150 \text{ pF}$)

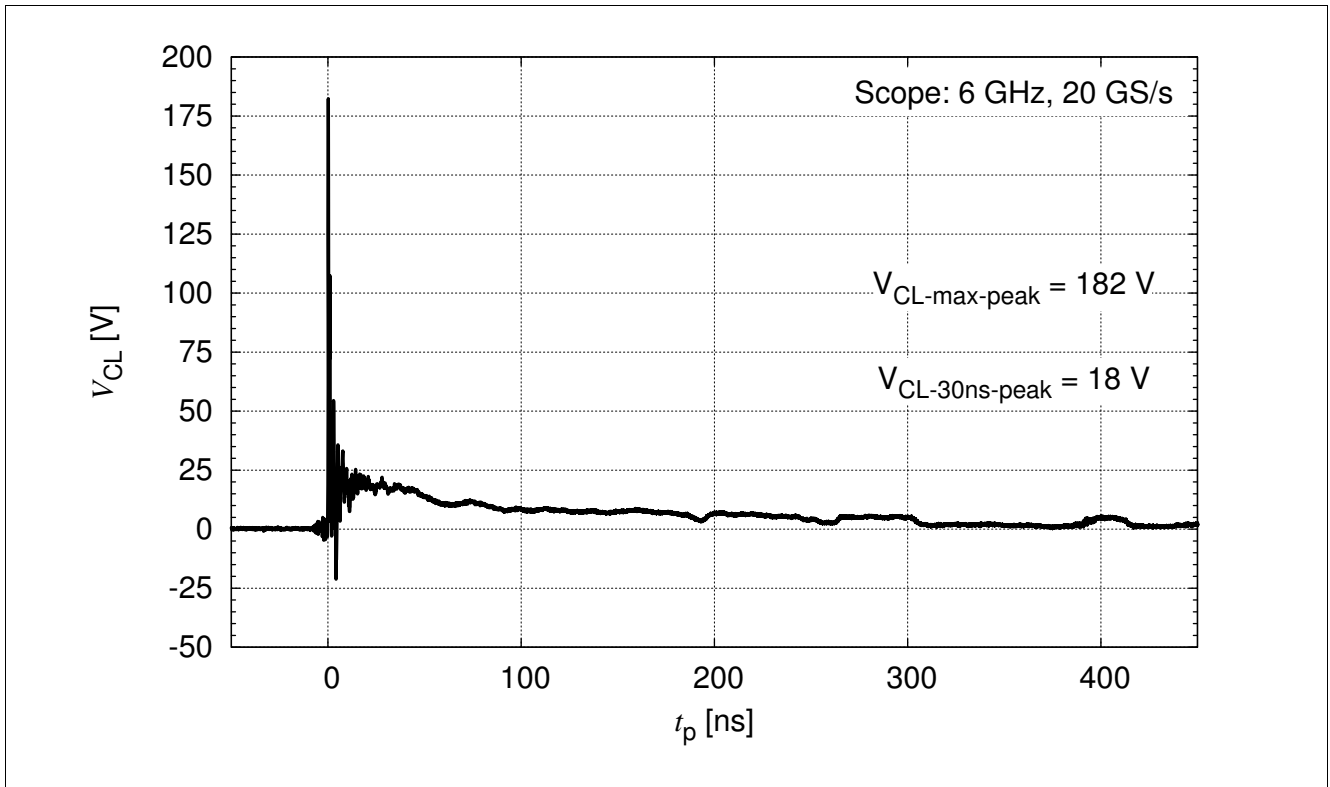


Figure 3-7 Clamping voltage at +15 kV discharge according IEC61000-4-2 ($R = 330 \text{ Ohm}$, $C = 150 \text{ pF}$)

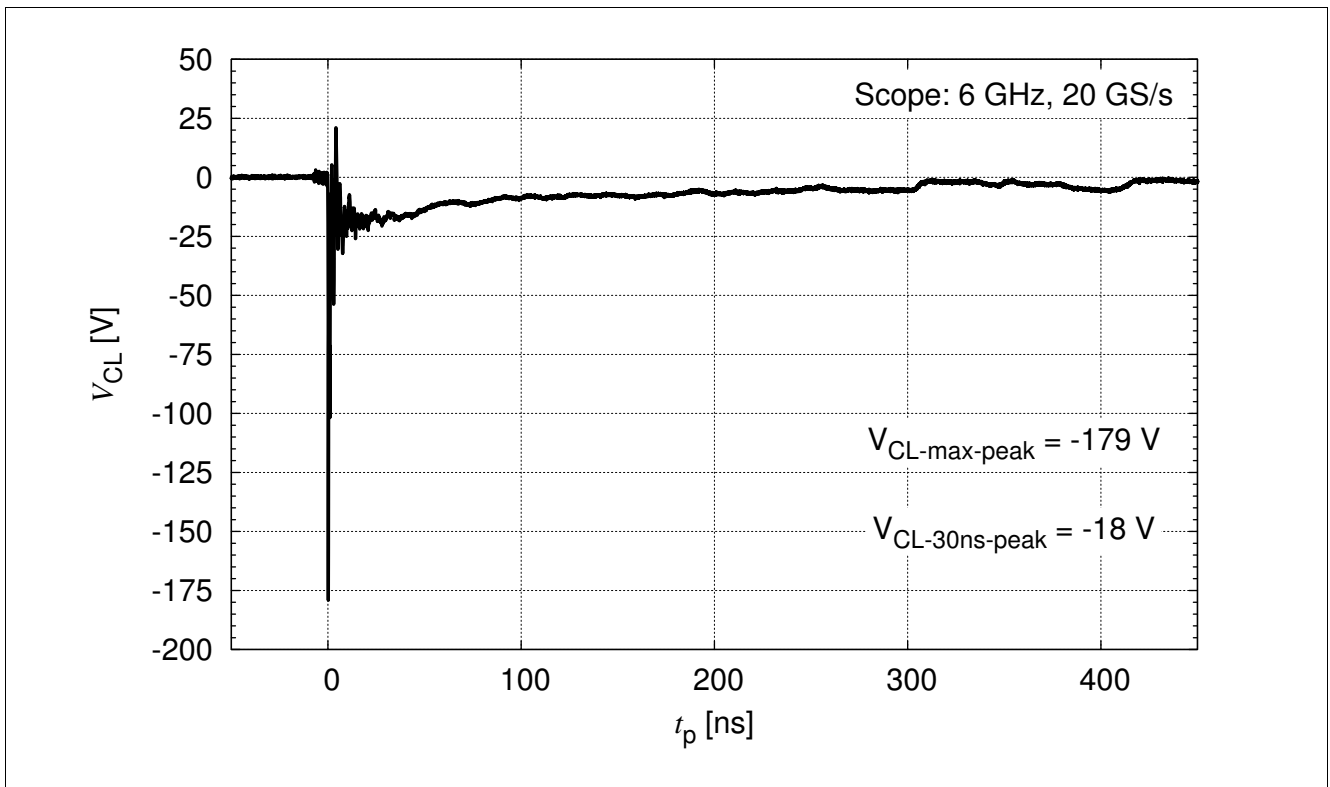


Figure 3-8 Clamping voltage at -15 kV discharge according IEC61000-4-2 ($R = 330 \text{ } \Omega$, $C = 150 \text{ pF}$)

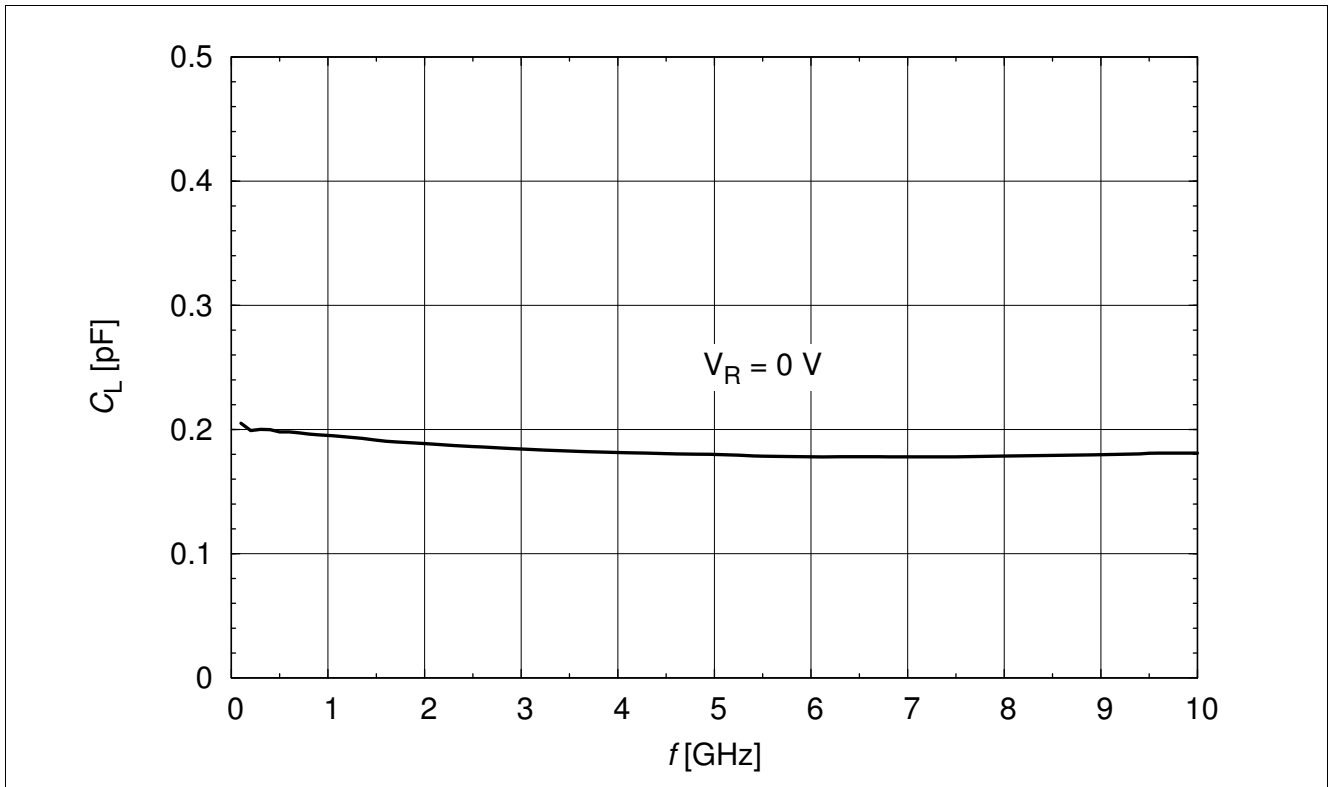


Figure 3-9 Line capacitance: $C_L = f(f)$, $V_R = 0\text{ V}$

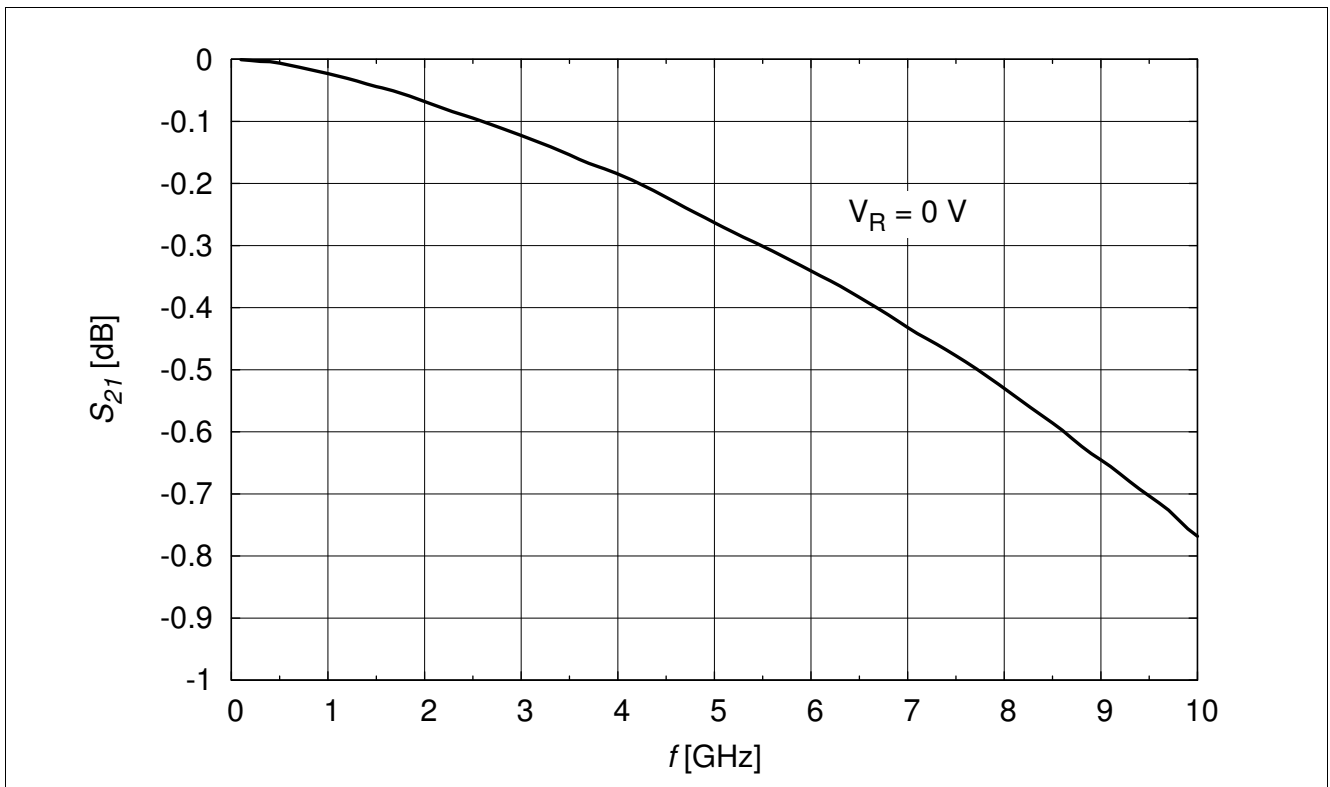


Figure 3-10 Insertion loss: $S_{21} = f(f)$, $V_R = 0\text{ V}$

4 Package Information

4.1 TSLP-2-17[2]

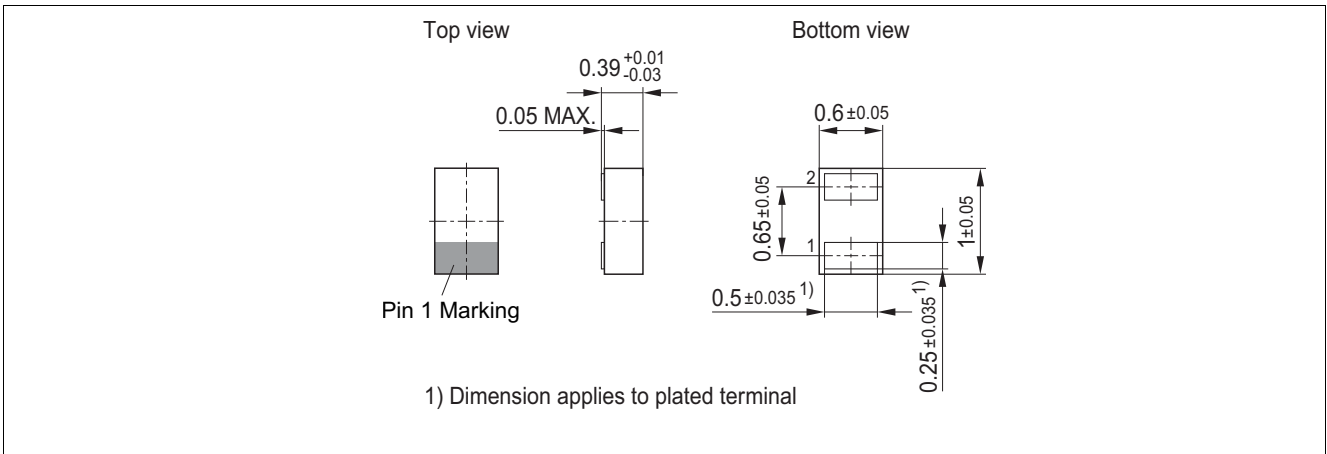


Figure 4-1 TSLP-2-17 Package outline (dimension in mm)

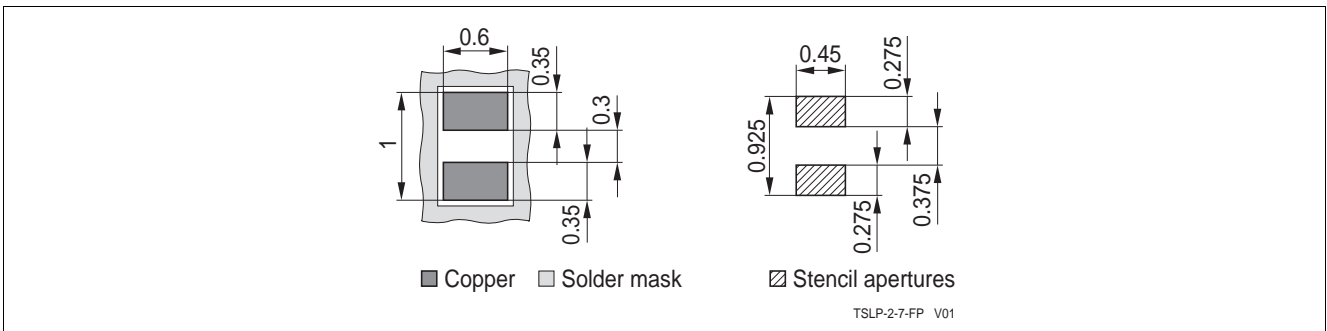


Figure 4-2 TSLP-2-17 Footprint (dimension in mm)

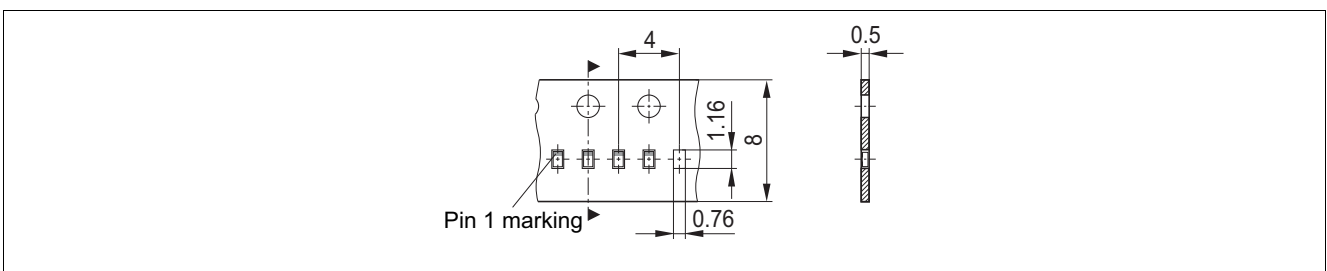


Figure 4-3 TSLP-2-17 Packing (dimension in mm)

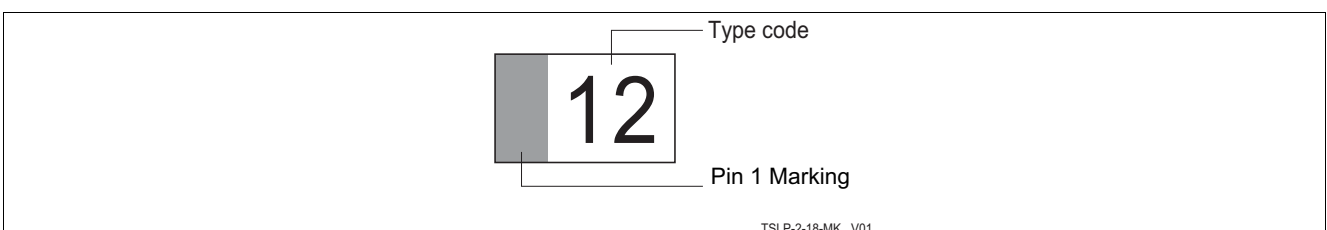


Figure 4-4 TSLP-2-17 Marking (example)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

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