

# AN11051

Pin FMEA for HEF4000 family

Rev. 2 — 15 July 2015

Application note

## Document information

Info	Content
<b>Keywords</b>	FMEA, HEF4000, CMOS, wide operating supply range (3 V to 15 V)
<b>Abstract</b>	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of the NXP Semiconductors' HEF4000 family under typical failure situations



## Revision history

Rev	Date	Description
v 1.0	20110428	initial version
v. 2.0	20150715	<a href="#">Table 4</a> : Added pin V <sub>EE</sub>

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## 1. Introduction

Though the HEF4000 series is one of the oldest CMOS logic families around, it is still frequently used in new designs because of its ease of design-in, wide operating supply range (3 V to 15 V), excellent noise immunity, and low power consumption. All of the standard functions are available, plus more specialized functions such as IEEE bus interfaces and PLL frequency synthesizers.

## 2. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of the NXP Semiconductor AUP family under typical failure situations such as a short-circuit to  $V_{DD}$  or  $V_{SS}$  or to a neighboring pin, or if a pin is left open.

Some HEF4000 family devices have special functions, that can have different behaviors. A failure is classified according to its effect on the HEF4000 device and the functionality of the application; see [Table 1](#).

**Table 1. Classification of failure effects**

Class	Failure effect
A	damage to device affects application functionality
B	no damage to device may affect application functionality
C	no damage to device no affect to application functionality

**Table 2. FMEA matrix for pin short-circuit to  $V_{DD}$**

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined HIGH, no damage, no leakage, no output level change
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes
$V_{SS}$	B	short-circuits and high currents can damage device, will affect functionality

**Table 3. FMEA matrix for pin short-circuit to  $V_{SS}$**

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined LOW, no damage, no leakage, no output level change
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes
$V_{DD}$	B	no damage to device, will affect functionality

**Table 4. FMEA matrix for pin left open**

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage, may affect functionality
Output	C	normal operating condition, no damage, no leakage
$V_{SS}$ ; $V_{EE}$	B	undefined operating condition, no damage, increases leakage, will affect functionality
$V_{DD}$	B	undefined operating condition, no damage, increases leakage (only for I/O types), will affect functionality

**Table 5. FMEA matrix for pin short-circuits between neighboring pins**

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage
	B	if inputs have different voltage levels: leakage increases, will affect functionality
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality
	C	if input and output have same voltage levels, no damage, no leakage
Input to $V_{SS}$	-	see <a href="#">Table 3</a>
Input to $V_{DD}$	-	see <a href="#">Table 2</a>
Output to output	C	if outputs have same voltage levels, no damage, no leakage
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality
Output to input	-	same effect as 'input to output' condition
Output to $V_{SS}$	-	see <a href="#">Table 3</a>
Output to $V_{DD}$	-	see <a href="#">Table 2</a>
$V_{SS}$ to $V_{DD}$	-	not applicable, these pins are not neighbors

### 3. Abbreviations

**Table 6. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
FMEA	Failure Modes and Effects Analysis
PLL	Phase-Locked Loop

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## 5. Contents

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1	<b>Introduction</b> .....	<b>3</b>
2	<b>Pin FMEA</b> .....	<b>3</b>
3	<b>Abbreviations</b> .....	<b>4</b>
4	<b>Legal information</b> .....	<b>5</b>
4.1	Definitions .....	5
4.2	Disclaimers .....	5
4.3	Trademarks.....	5
5	<b>Contents</b> .....	<b>6</b>

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