Entry Level Tool II

Reference Manual

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Version : 1.0.3

Date : October 7, 2005

MPD_ELT2_RM0_103

About this Manual

Introduction

This manual provides component details about the Entry Level Tool - II board.

Table below shows the ELT II Reference Manual revision history.

Version	Date	Description
1.0.3	October 2005	Change layout format
01.02	June 2005	Corrected few figures and typos
01.01	June 2005	Corrected Typos and Fonts
01.00	May 2005	First Publication of the Reference Manual

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Ctrl + N to open to the Go To Page dialog box.
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- Thumbnail icons, which provide miniature preview of each page, provides a link to the pages.
- numerous links shown in Navy Blue colour allow you to jump to related information.

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Typographic Conventions

The ELT II reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: **General Description, Block Diagram**
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: ***Figure 1-1. Entry Level Tool-II Block Diagram, Table 2-1. MAX II Device Features***
1., 2., 3.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
• ■	Bullets are used in a list of items when the sequence of items is not important.
	The hand points to special information that requires special attention
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with theprocedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

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1. Introduction

The ***Entry Level Tool - II*** is a **MAX II** CPLD (EPM240/570) based board, which serves as the basic tool for understanding and experimenting with Programmable Logic Devices, namely the MAX II Family, and hence the name Entry Level Tool - II or ELT-II for short. The ELT-II Board helps in understanding the basic Programmable Logic Design flow in the simplest manner. This board contains a number of user IOs for easy access and experimentation.

General Description

The Entry Level Tool - II provides a hardware platform for designing and developing simple and low-end systems based on Altera MAX II Devices. The Entry Level Tool - II Board features a MAX II EPM240T100Cx device with 240 Logic Elements (LEs) and 8,192 bits of User Flash Memory (UFM). The board also supports vertical migration with the EPM570T100Cx device with 570 Logic Elements (LEs) and 8,192 bits of User Flash Memory (UFM) for larger design support.

The board comes preprogramming with the *ELT II Board Diagnostic System*, which can be used to verify the boards functionality. The programming files for the *ELT II Board Diagnostic System* are also supplied with the board to verify the board's functionality at any time.

Features

- Based on MAX II CPLD EPM240T100Cx
- 41 General Purpose IOs (+5V tolerant) available on the standard Santa Cruz short expansion footprint
- 10 CPLD clock selection option available through jumper selection along with the dual crystal support on the board, making the clock selection choices 10x2 = 20 (2 Hz upto 230.4 Khz)
- 4-Digit scanning 7-Segment LED Display Interface
- 8x2 On-Off Push Button switches shared with IO headers, giving flexibility of additional 16 general purpose IOs (+5V tolerant)
- 4x4 Momentary Push Button Switch Matrix and 8 LEDs shared and configured through 4 Jumper selection options to use them in any of the possible available combinations

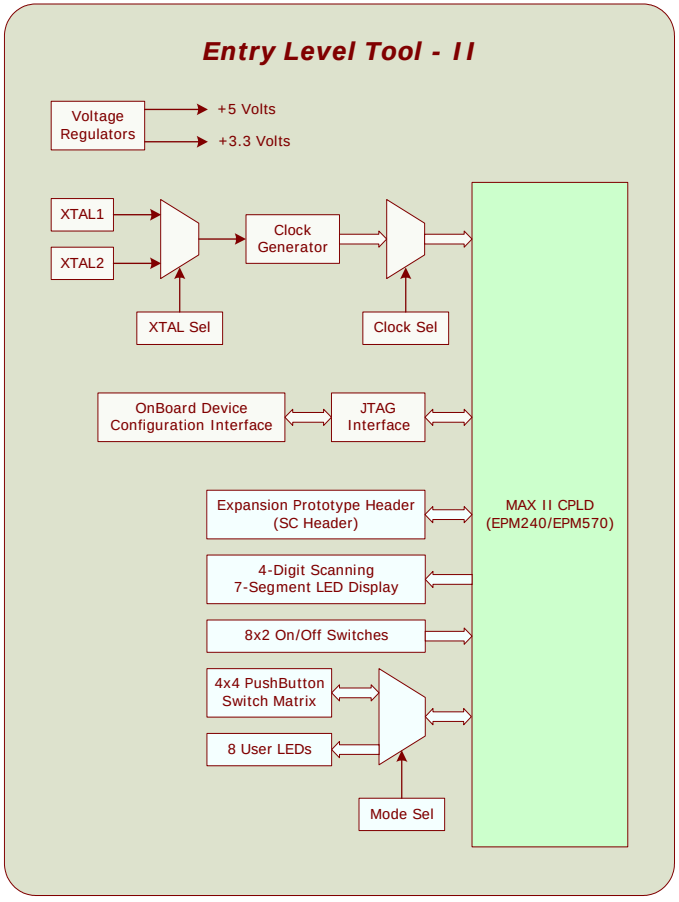
- On Board logic for MAX II configuration (Quartus II Compatible)
- On Board Power Supply for smooth operation of the board
- On Board Global System Reset circuitry
- Migration support from EPM240T100Cx to EPM570T100Cx devices for higher density support for larger designs

The ELT II board is manufactured and assembled by making use of Pb-free processes and hence it is designated as an ECO Friendly Board.

Block Diagram

Figure 1-1. shows the Block Diagram of the ELT - II Board.

Figure 1-1. Entry Level Tool - II Block Diagram



Fundamentally both versions (EPM240 and EPM570) are the same except for the following difference, otherwise all the functionality and IO pin mapping remains the same.

The 100-Pin TQFP package of the EPM570 has only 76 IOs while the 100-Pin TQFP package of the EPM240 has 80 IOs. Hence the ELT - II Board with EPM240 has all the features mentioned in this document, where as the ELT - II Board with EPM570 lacks some peripherals since the EPM570 has 4 less IOs compared to the EPM240 device.

The peripheral difference between the EPM240 and EPM570 versions of the Entry Level Tool - II board is mentioned in the Table 1-1 below:

Table 1-1. Peripheral difference between EPM240 and EPM570 versions of ELT II

Sr. No.	Peripheral	EPM240 Version	EPM570 Version
1.	User LEDs	8	4 (Lower Part)
2.	Push Button Switch Matrix	4x4	2x2 (Lower Part)

All the other peripherals and the Pin Mapping of the Peripherals with the MAX II device remains the same in both the versions.

2. Board Components

Board Layout

This section contains a brief overview of the important components on the Entry Level Tool - II. Figure 2-1. below shows the top view of the ELT - II Board.

Figure 2-1. ELT - II Top View

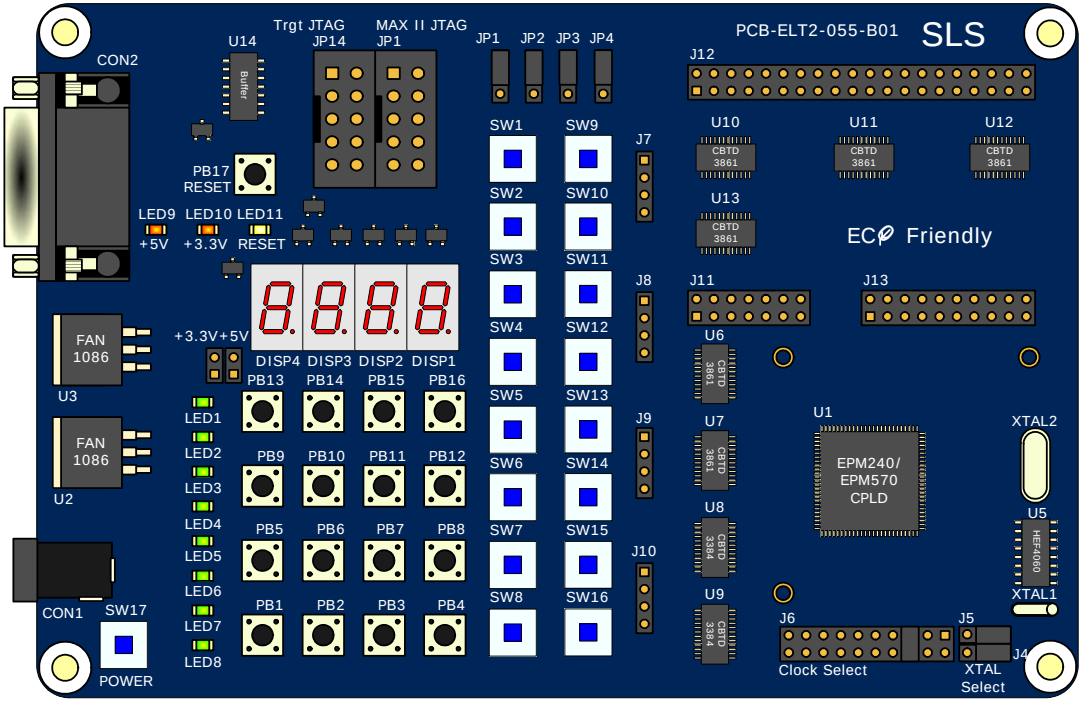
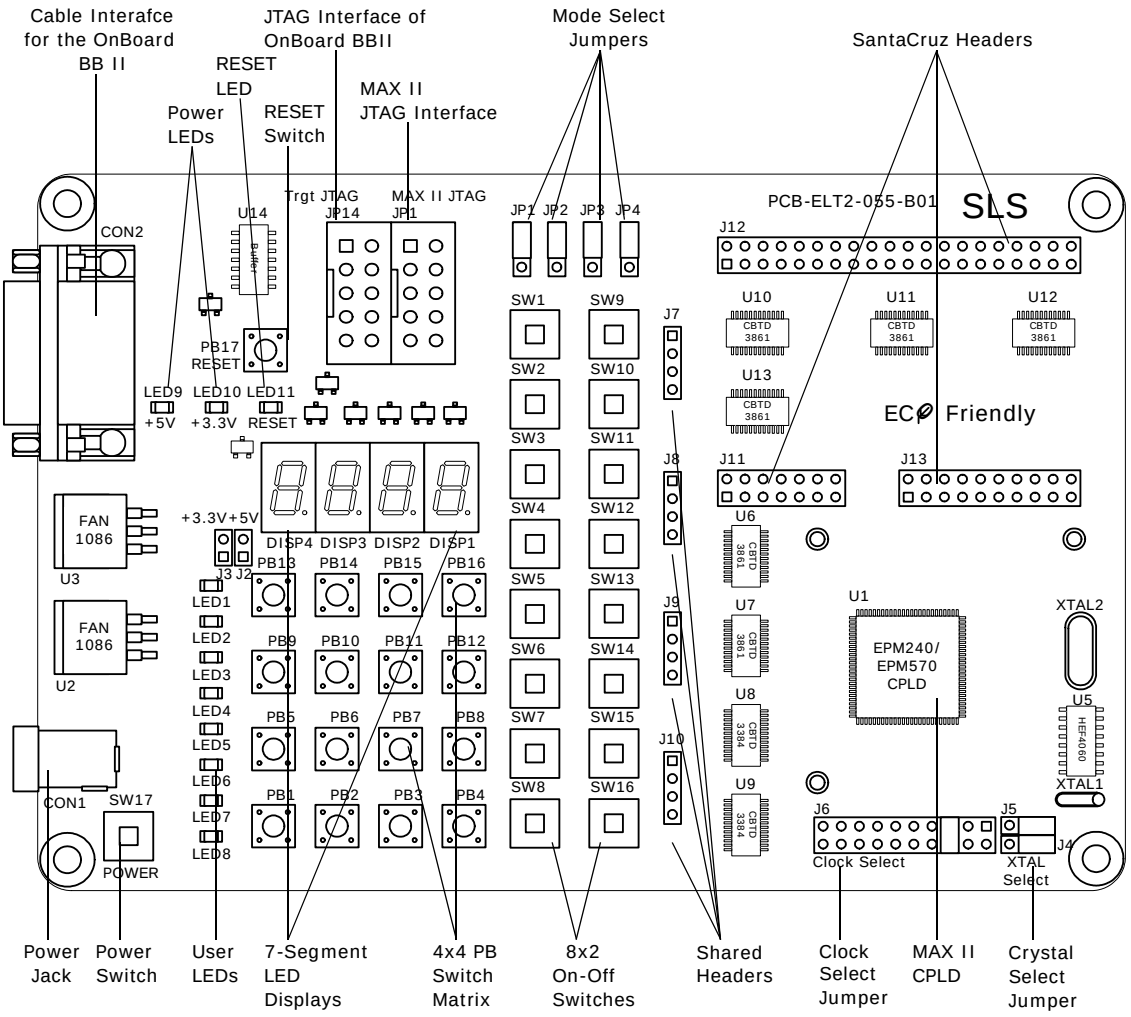


Figure 2-2. Below shows the Components on the Entry Level Tool - II Board.

Figure 2-2. Entry Level Tool - II Board Components



The MAX II Device

U1 is a MAX II device in a 100-Pin TQFP package. The board is basically designed around EPM240T100Cx device. But it supports upward migration with the EPM570T100Cx devices as well (For larger design support) with few modifications made at the assembly level. The board supports EPM570 devices at the cost of 4 General Purpose IOs, whose details are mentioned in the following sections. Figure 2-3. below shows the MAX II device.

Figure 2-3. MAX II Device

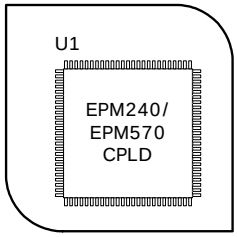


Table 2-1 shown below lists the MAX II device features.

Table 2-1. MAX II Device Features

Feature	EPM240	EPM570
LEs	240	570
Equivalent MacroCell Range	128 to 240	240 to 570
UFM Size (Bits)	8,192	8,192
Maximum User IO Pins	80	76(1)

Note: to Table 2-1:

(1) User IO Pins for the EPM570 Device is for the 100-Pin TQFP package used on the ELT II Board.

The development board provides two methods for configuring the MAX II device using the Quartus II software running on a host computer:

1. The designer can configure the device directly using an Altera download cable connected to the MAX II JTAG Header (J1).
2. The designer can configure the device using the on board JTAG configuration interface using the custom interface provided by SLS.

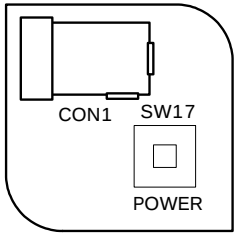
See the section 3 for more details. See the Altera MAX II literature page for MAX II related documentation at www.altera.com including MAX II pin out documents.

The MAX II Device operates entirely from 3.3 Volts (Both VccInt and VccIO).

Power-Supply Circuitry

The Entry Level Tool - II runs from a 6.5V, unregulated, center-positive input power supply (fed through Power Jack CON1). On-board circuitry generates 5 Volts and 3.3 Volts regulated power levels. The **SW17** is a power switch, which controls the unregulated power input to the on-board power supply circuitry.
Figure 2-4. below shows the Power switch and the Power jack on the ELT II Board.

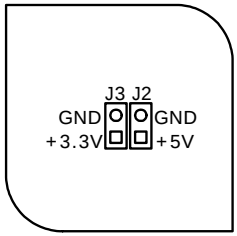
Figure 2-4. Power Switch and Power Jack



- The 5 Volts supply is present on pin 2 of **J11** (SantaCruz Headers) for use by any device plugged into the SantaCruz Short Expansion Connector.
- The 3.3 Volts supply is used as the power source for all the MAX II device IO pins (VccIO) and device core (VccInt). The 3.3 Volts supply is also available to the SantaCruz Short Expansion Connector.

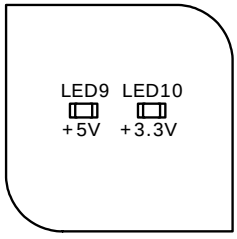
The 5 Volts supply is coming on the **J2** header and the 3.3 Volts supply is coming on the **J3** header as test point signals, as shown in the Figure 2-5. below:

Figure 2-5. Test Point Headers



The ELT II Board also contains a +5 Volts Supply OK indicator (**LED9**) and a +3.3 Volts Supply OK indicator (**LED10**) as shown in the Figure 2-6. below:

Figure 2-6. Power LEDs



Reset Circuitry

The Entry Level Tool - II Board contains a dedicated circuitry to perform the Global RESET function. The Push Button Switch **PB17** acts as the Global RESET switch. When this switch is pressed, an active LOW (Logic “0”) RESET signal is generated to the MAX II CPLD. The ELT - II board also has a reset indicator LED (**LED11**) as shown in the Figure 2-7. below:

Figure 2-7. RESET Switch and LED

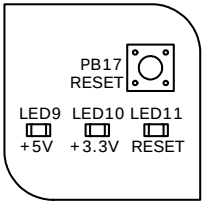


Table 2-2 shown below gives the Pin mapping of the reset signal.

Table 2-2. Mapping of Reset Signal

Sr. No.	Signal	CPLD Pin
1.	RESET_n(1)	U1.44

Note: to Table 2-2:

(1) _n indicates Active Low polarity of the RESET signal.

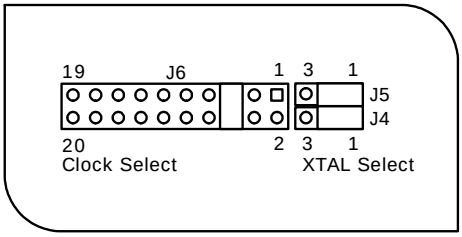
Clock Circuitry

The Entry Level Tool - II Board includes a number of clock options for the designer to aid the development of variety of systems. The clock network drives the MAX II device and the clock/osc pins on the SantaCruz Expansion Connector.

The Clock Circuitry of the ELT II Board gives the designer two options to configure the input clock to the MAX II CPLD as shown in the Figure 2-8. below:

1. Crystal Select
2. Clock Select

Figure 2-8. ELT II Clock Configuration



The clock circuitry of the Entry Level Tool - II board, basically, makes use of two crystals - 3.6864 MHz and 32.768 KHz. The crystal for the clock generator can be selected by making use of jumpers **J4** and **J5** as shown in the Table 2-3 below:

Table 2-3. Crystal Selection Option

Sr. No.	To Select Crystal	Jumper Setting
1.	32.768 KHz	Short J4.2-J4.1 and Short J5.2-J5.1
2.	3.6864 MHz	Short J4.2-J4.3 and Short J5.2-J5.3

The selected crystal is connected to the 14-stage Binary Counter and divider circuit, which generates 10 clock outputs, out of which, any one can be selected and connected to the CPLD as CPLD Clock input using jumper **J6** as shown in the Table 2-4 below:

Table 2-4. Clock Selection Option

Sr. No.	Jumper Setting	Available Clock Option using	
		32.768 KHz	3.6864 MHz
1.	Short J6.1 and J6.2	2.048 KHz	230.4 KHz
2.	Short J6.3 and J6.4	1.024 KHz	115.2 KHz
3.	Short J6.5 and J6.6	512 Hz	57.6 KHz
4.	Short J6.7 and J6.8	256 Hz	28.8 KHz
5.	Short J6.9 and J6.10	128 Hz	14.4 KHz
6.	Short J6.11 and J6.12	64 Hz	7.2 KHz

Table 2-4. Clock Selection Option			
Sr. No.	Jumper Setting	Available Clock Option using	
		32.768 KHz	3.6864 MHz
7.	Short J6.13 and J6.14	32 Hz	3.6 KHz
8.	Short J6.15 and J6.16	8 Hz	900 Hz
9.	Short J6.17 and J6.18	4 Hz	450 Hz
10.	Short J6.19 and J6.20	2 Hz	225 Hz

Thus a total of 20 clock options available to the designer to develop any type of MAX II based system.

The Clock distribution of the Entry Level Tool - II Board is as follows:

1. A buffered Crystal frequency is directly fed to the *Proto Osc In* pin (Pin **J13.9**) of the SantaCruz Headers, i.e., the selected crystal frequency (32.768 KHz or 3.6864 MHz) is directly available on the **J13.9** Pin.
2. The selected crystal frequency drives the CPLD (Pin **U1.14**) and the *Proto Clk In* pin (Pin **J13.11**) of the SantaCruz Headers, i.e., the selected clock frequency (controlled by the selected crystal frequency) is available on these Pins.
3. A user clock (*Proto Clk Out*) coming from the SantaCruz Header pin (**J13.13**) is fed to the CPLD clock pin (**U1.64**).

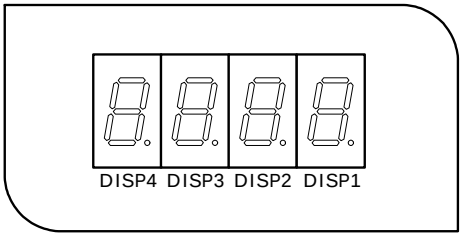
The mapping of the Clock signals with the MAX II device is shown in the Table 2-5 below:

Table 2-5. Mapping of the Clock Signals		
Sr. No.	Clock	CPLD Pin
1.	CPLD Clk In	U1.14
2.	Proto Clk Out	U1.64

7-Segment LED Displays

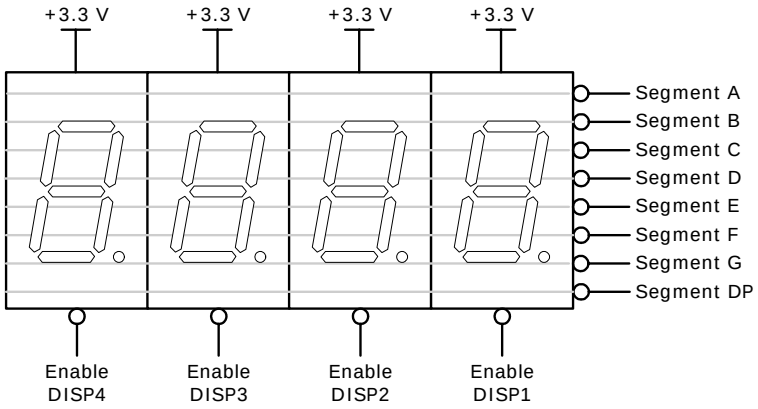
The Entry Level Tool - II Board incorporates four Common Anode 7-Segment LED displays in scanning fashion, i.e., at a time only one display is being driven using this interface to conserve power and device IO pins. Figure 2-9. below shows the 7-Segment LED Displays on the ELT II Board.

Figure 2-9. 7-Segment LED Displays



The Symbolic representation of the 7-Segment LED Displays is shown in the Figure 2-10. below:

Figure 2-10. Symbolic Representation of the 7-Segment LED Interface



As shown in the Figure 2-10. , to glow a particular segment, the corresponding segment line must be driven LOW (Logic “0”) as the 7-segment LED displays used on the ELT II board are of Common Anode type. Since the 7-segment LED displays are interfaced in scanning fashion, all the segment lines of all the 7-segment LED displays are shared (common) and each display has an active LOW (Logic “0”) Enable input. Hence, to display a particular digit on a display, the respective data must be written on the segment lines and the corresponding display must be enabled using this interface, e.g., to display 8 on Display4, the 7-segment code of 8 must be

written on the *segment lines* and *Enable DISP4* must be asserted for the period of scanning time duration and so on.

Figure 2-11. below shows the segment identification for the Common Anode 7-Segment LED display on the Entry Level Tool - II Board.

Figure 2-11. Segment Identification

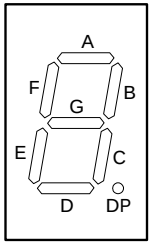


Table 2-6 shown below gives the mapping of 7-Segment LED display interface with the MAX II chip.

Table 2-6. Mapping of 7-Segment LED Displays

Sr. No.	Signal Name	CPLD Pin
1.	Segment A	U1.33
2.	Segment B	U1.34
3.	Segment C	U1.35
4.	Segment D	U1.42
5.	Segment E	U1.41
6.	Segment F	U1.36
7.	Segment G	U1.38
8.	Segment DP	U1.40
9.	Enable DISP1	U1.30
10.	Enable DISP2	U1.29
11.	Enable DISP3	U1.28
12.	Enable DISP4	U1.27

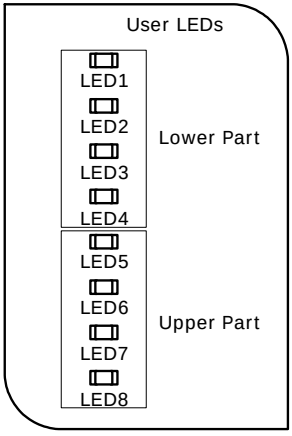
User LEDs

The Entry Level Tool - II provides 8 user LEDs connected to the MAX II device. These LEDs are shared with the Push Button Switch Matrix. The LEDs and the Push Button Switch Matrix can be individually enabled or disabled in parts by a jumper selection option.

For more details about the Push Button Switch Matrix and using shared configuration, see the "Push Button Switch Matrix" section of this manual.

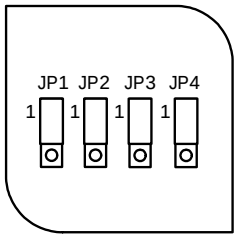
Figure 2-12. Below shows the user LED configuration of the ELT II Board.

Figure 2-12. User LEDs



The LEDs on the ELT - II board are divided in two parts: Lower and Upper, each a group of 4 LEDs as shown in the figure above. Each part can be individually enabled or disable by using a jumper selection option (**JP2** and **JP4**) as shown in the Figure 2-13. below thus giving flexibility to the designer to use the LEDs as a group of 4 LEDs (Upper or Lower) or a group of 8 LEDs.

Figure 2-13. LED/PB Matrix Jumper Selection Options



All the LEDs are connected in Common Anode configuration, and hence a logic LOW (Logic “0”) must be driven on the LED pin to turn ON the corresponding LED. The LED will turn on only if the respective LED part (Lower or Upper) is enabled. Disabling an LED part physically isolates the LED part from the CPLD pins. Table 2-7 below gives the jumper selection option for enabling/disabling LED parts.

Table 2-7. LED Jumper Selection Options

Sr. No.	Function	Jumper Setting
1.	Enable LED Lower Part	Short JP2.2 and JP2.1
2.	Disable LED Lower Part	Short JP2.2 and JP2.3
3.	Enable LED Upper Part	Short JP4.2 and JP4.1
4.	Disable LED Upper Part	Short JP4.2 and JP4.3

It should be noted that if no jumper pins are shorted, then by default all the LEDs are **disabled**.

For the mapping of the LED pins with the MAX II device, refer to the Table 2-9, “Mapping of LEDs and PB Matrix,” on page 21.

It should be noted that in the ELT - II Board incorporating EPM570, the upper LED part (LED5 to LED8) is not available and hence no jumper selection option (JP4) is in effect for the same.

Push Button Switch Matrix

The Entry Level Tool - II provides a 4x4 (momentary contact) Push Button (PB) Switch Matrix connected to the MAX II device. This Push Button Switch Matrix is shared with the LEDs. The Push Button Switch Matrix and the LEDs can be individually enabled or disabled in parts by a jumper selection option.

For more details about the user LEDs, see the "On-Off Push Button Switches" section of this manual.

Figure 2-14. Below shows the 4x4 Push Button Switch Matrix configuration of the ELT II Board. As shown in the figure below, the Push Button Switch Matrix on the ELT - II board is divided in two parts: Lower and Upper, each representing a 2x2 Matrix as shown in the figure below. Each part can be individually enabled or disable by using a jumper selection option (JP1 and JP3) as shown in the Figure 2-14. thus giving flexibility to the designer to use the PB Matrix as 2x2 PB Matrix (Lower or Upper) or combined 4x4 PB Matrix.

Figure 2-14. Push Button Switch Matrix

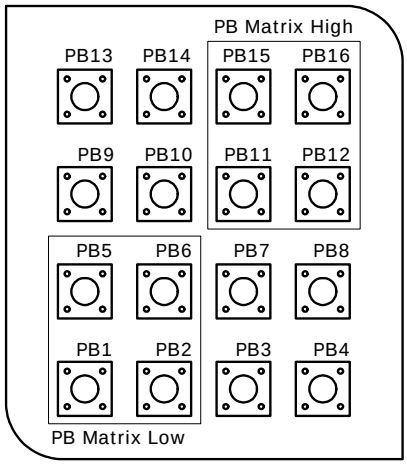


Figure 2-15. Symbolic representation of the Matrix KeyBoard

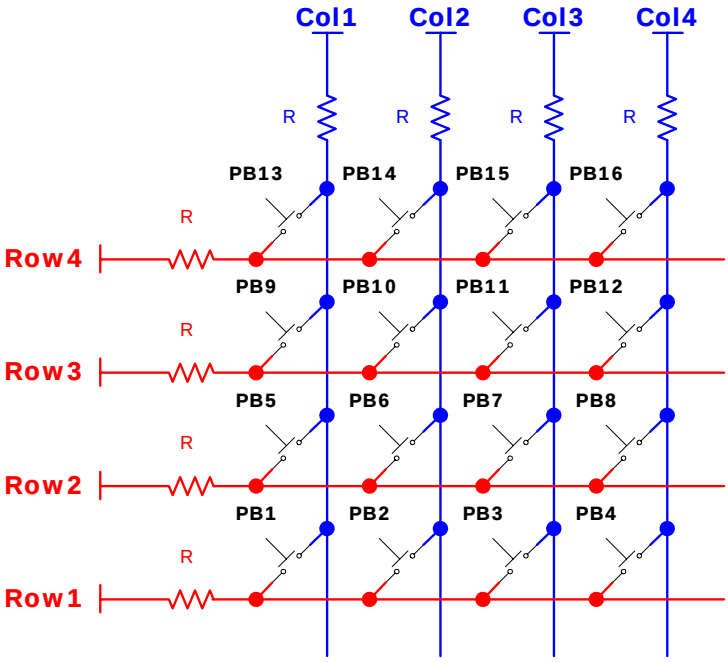


Figure 2-15. above shows the Symbolic representation of the Push Button Matrix KeyBoard. The following Figure 2-16. and Figure 2-17. shows the Symbolic representation of the Push button Switch Matrix KeyBoard with individual parts (Lower and Upper) Enabled using the Jumper setting. However, it is important to note that disabling a PB Matrix part physically isolates the PB Matrix part from the CPLD pins. When both the parts are enabled, the PB matrix becomes 4x4 Switch Matrix.

Figure 2-16. Symbolic representation of Lower PB Matrix

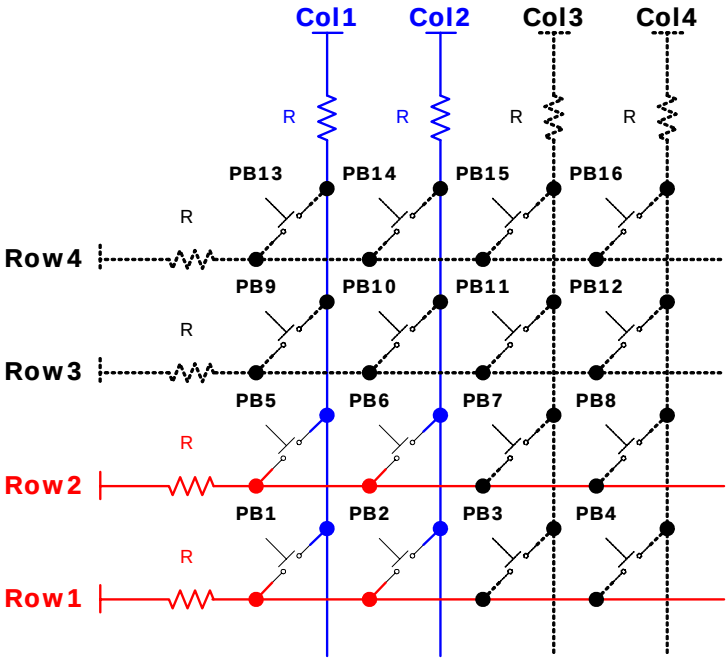


Figure 2-17. Symbolic representation of Upper PB Matrix

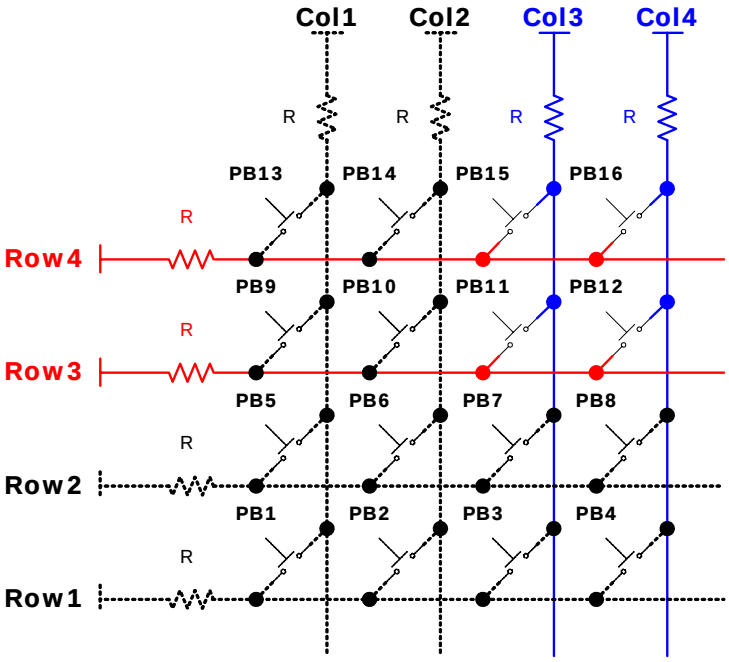


Table 2-8 below gives the jumper selection option for enabling/disabling Push Button Switch Matrix parts.

Table 2-8. PB Switch Matrix Jumper Selection Options

Sr. No.	Function	Jumper Setting
1.	Enable PB Matrix Lower Part	Short JP1.2 and JP1.1
2.	Disable PB Matrix Lower Part	Short JP1.2 and JP1.3
3.	Enable PB Matrix Upper Part	Short JP3.2 and JP3.1
4.	Disable PB Matrix Upper Part	Short JP3.2 and JP3.3

It should be noted that if no jumper pins are shorted, then by default all the Push Button matrix parts are **disabled**.

Table 2-9 shown below gives the pin mapping of the LED and PB Matrix with the MAX II device.

Table 2-9. Mapping of LEDs and PB Matrix

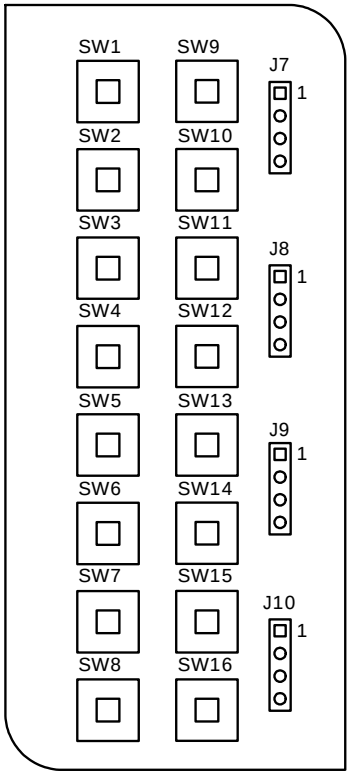
Sr. No.	Peripheral (LEDs)	Shared peripheral (PB Matrix)	CPLD Pin
1.	LED1	PB_Matrix_Col1	U1.48
2.	LED2	PB_Matrix_Col2	U1.49
3.	LED3	PB_Matrix_Row1	U1.43
4.	LED4	PB_Matrix_Row2	U1.47
5.	LED5	PB_Matrix_Col3	U1.37
6.	LED6	PB_Matrix_Col4	U1.39
7.	LED7	PB_Matrix_Row3	U1.90
8.	LED8	PB_Matrix_Row4	U1.88

It should be noted that in the ELT - II Board incorporating EPM570, the upper PB Matrix part (Row3-4 and Col3-4) is not available and hence only lower PB Matrix is available (comprising of Row1-2 and Col1-2). This implies that no jumper selection option (JP3) is in effect for the same.

On-Off Push Button Switches

The Entry Level Tool - II Board supports 8x2 On-Off Push Button switches (**SW1** to **SW16**), which can be used as general purpose user inputs. In OFF (IDLE) state, the CPLD pin is pulled high through a Pull-Up resistor. When the Push Button switch is turned ON (Pushed Downward), the CPLD pin sees logic LOW (Logic “0”) level. Figure 2-18. below shows the On-Off Push Button Switches.

Figure 2-18. On-Off Push Button Switches



These 16 inputs are shared with IO headers (**J7** to **J10** as shown in the figure above), giving flexibility of additional 16 general purpose, +5V tolerant IOs to the designer. To use these headers as general purpose inputs/outputs, the designer must ensure that the switches are in IDLE (OFF) state to ensure that the Push Button Switch doesn't accidently drive the shared IO line LOW (Logic "0").

Table 2-10 shown below gives the pin mapping of the On-Off Push Button switches and shared headers with the MAX II device.

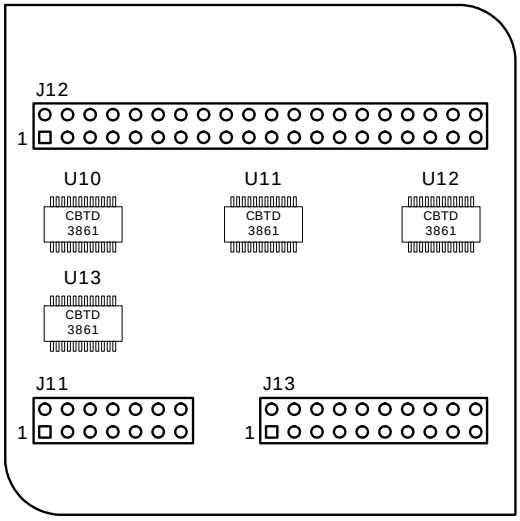
Table 2-10. Mapping of On-Off Switch and Shared Headers

Sr. No.	Peripheral (On-Off Switch)	Shared Peripheral (IO Headers)	CPLD Pin
1.	SW1	J7.1	U1.2
2.	SW2	J7.2	U1.3
3.	SW3	J8.1	U1.6
4.	SW4	J8.2	U1.7
5.	SW5	J9.1	U1.15
6.	SW6	J9.2	U1.16
7.	SW7	J10.1	U1.19
8.	SW8	J10.2	U1.20
9.	SW9	J7.3	U1.4
10.	SW10	J7.4	U1.5
11.	SW11	J8.3	U1.8
12.	SW12	J8.4	U1.12
13.	SW13	J9.3	U1.17
14.	SW14	J9.4	U1.18
15.	SW15	J10.3	U1.21
16.	SW16	J10.4	U1.26

Expansion Prototype Connector

Headers **J11**, **J12** and **J13** collectively form the standard-footprint, mechanically-stable connection, called Santa Cruz Short Expansion Connector, that can be used (for example) as an interface to a special-function daughter card as shown in the Figure 2-19. below:

Figure 2-19. Expansion Prototype Connector



Note: to Figure 2-19. :

The expansion prototype connector interface includes:

- 41 pins for prototyping. All 41 IO pins connect to user IO pins on the MAX II device. Each signal passes through permanently enabled analog switches to protect the MAX II device from +5 V logic levels.
- A copy of the on-board oscillator output (buffered selected XTAL frequency 32.768 KHz/3.6864 MHz).
- A copy of the MAX II CPLD system clock frequency.
- An active LOW (Logic “0”) system RESET signal.
- Five regulated +3.3 Volts power-supply pins.
- One regulated +5 Volts power-supply pin.
- Numerous ground connections.

The output logic level on the expansion prototype connector is 3.3 Volts.

Table 2-11 shown below give the pin mapping of the Expansion Prototype Connector **J11** with the MAX II device.

Table 2-11. Mapping of Expansion Prototype Connector J11

Sr. No.	Signal	Peripheral	CPLD Pin
1.	GND	J11.1	-
2.	+5 V	J11.2	-
3.	NC	J11.3	-
4.	Proto IO 31	J11.4	U1.100
5.	Proto IO 32	J11.5	U1.99
6.	Proto IO 33	J11.6	U1.98
7.	Proto IO 34	J11.7	U1.97
8.	Proto IO 35	J11.8	U1.96
9.	Proto IO 36	J11.9	U1.95
10.	Proto IO 37	J11.10	U1.92
11.	Proto IO 38	J11.11	U1.91
12.	Proto IO 39	J11.12	U1.89
13.	Proto IO 40	J11.13	U1.87
14.	Proto IO 41	J11.14	U1.1

Table 2-12 shown below give the pin mapping of the Expansion Prototype Connector **J12** with the MAX II device.

Table 2-12. Mapping of Expansion Prototype Connector J12

Sr. No.	Signal	Peripheral	CPLD Pin
1.	RESET	J12.1	-
2.	GND	J12.2	-
3.	Proto IO 1	J12.3	U1.86
4.	Proto IO 2	J12.4	U1.85
5.	Proto IO 3	J12.5	U1.84
6.	Proto IO 4	J12.6	U1.83
7.	Proto IO 5	J12.7	U1.82
8.	Proto IO 6	J12.8	U1.81
9.	Proto IO 7	J12.9	U1.78
10.	Proto IO 8	J12.10	U1.77
11.	Proto IO 9	J12.11	U1.76
12.	Proto IO 10	J12.12	U1.75
13.	Proto IO 11	J12.13	U1.74
14.	Proto IO 12	J12.14	U1.73
15.	Proto IO 13	J12.15	U1.72
16.	Proto IO 14	J12.16	U1.71
17.	Proto IO 15	J12.17	U1.70
18.	Proto IO 16	J12.18	U1.69
19.	GND	J12.19	-
20.	NC	J12.20	-
21.	Proto IO 17	J12.21	U1.68
22.	GND	J12.22	-
23.	Proto IO 18	J12.23	U1.67
24.	GND	J12.24	-
25.	Proto IO 19	J12.25	U1.66
26.	GND	J12.26	-

Table 2-12. Mapping of Expansion Prototype Connector J12

Sr. No.	Signal	Peripheral	CPLD Pin
27.	Proto IO 20	J12.27	U1.62
28.	Proto IO 21	J12.28	U1.61
29.	Proto IO 22	J12.29	U1.58
30.	GND	J12.30	-
31.	Proto IO 23	J12.31	U1.57
32.	Proto IO 24	J12.32	U1.56
33.	Proto IO 25	J12.33	U1.55
34.	NC	J12.34	-
35.	Proto IO 26	J12.35	U1.54
36.	Proto IO 27	J12.36	U1.53
37.	Proto IO 28	J12.37	U1.52
38.	Proto IO 29	J12.38	U1.51
39.	Proto IO 30	J12.39	U1.50
40.	GND	J12.40	-

Table 2-13 shown below give the pin mapping of the Expansion Prototype Connector **J13** with the MAX II device.

Table 2-13. Mapping of Expansion Prototype Connector J13

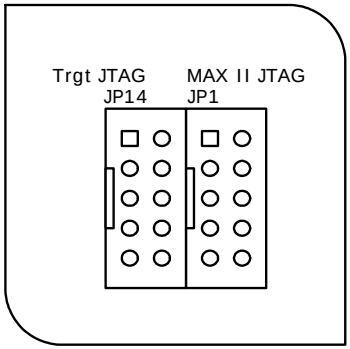
Sr. No.	Signal	Peripheral	CPLD Pin
1.	V Unregulated	J13.1	-
2.	GND	J13.2	-
3.	NC	J13.3	-
4.	GND	J13.4	-
5.	3.3 V	J13.5	-
6.	GND	J13.6	-
7.	3.3 V	J13.7	-
8.	GND	J13.8	-
9.	Proto Osc In	J13.9	-
10.	GND	J13.10	-
11.	Proto Clk In	J13.11	-
12.	GND	J13.12	-
13.	Proto Clk Out	J13.13	-
14.	GND	J13.14	-
15.	3.3 V	J13.15	-
16.	GND	J13.16	-
17.	3.3 V	J13.17	-
18.	GND	J13.18	-
19.	3.3 V	J13.19	-
20.	GND	J13.20	-

3. MAX II Device Configuration

Configuration Interface

The Entry Level Tool - II supports two methods for configuring the MAX II device. The ELT - II board contains the standard 10-pin JTAG Header (**JP1**) for configuring the on-board MAX II device as shown in the Figure 3-1. below:

Figure 3-1. JTAG Header

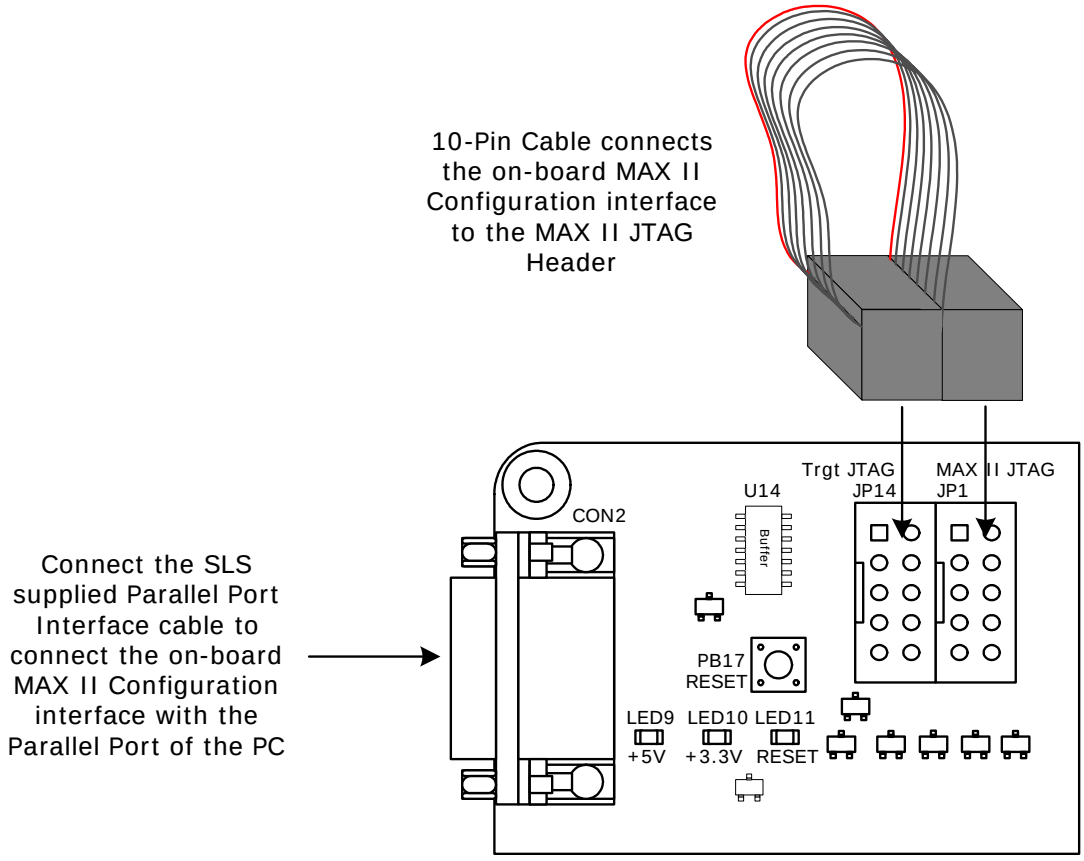


The MAX II device can be configured using any of the two available options as mentioned below:

1. **Using standard JTAG Interface:** The **JP1** header connects to the JTAG pins (TMS, TCK, TDI, TDO) of the MAX II device (**U1**). Altera Quartus II software can directly configure the MAX II device via an Altera provided download cable connected to **JP1** Header.
2. **Using on-board Programming Interface:** The ELT - II Board incorporates on-board interface to configure the MAX II device. To use the on-board interface, the board requires only parallel port connectivity. The Quartus II software automatically detects the interface as a Byte Blaster II connected on the parallel port and configures the MAX II device.

Figure 3-2. below shows the connection details for using the on-board MAX II Configuration interface:

Figure 3-2. Using on-board MAX II Configuration interface



As shown in the figure above, connect the SLS supplied Parallel Port cable to the **CON2** connector on the Entry Level Tool - II Board, to get the PC connectivity. Use 10-Pin Cable supplied to connect **JP14** with the **JP1** to connect the on-board MAX II Configuration interface with the MAX II JTAG interface. Now the on-board device configuration interface is ready to be used with the Quartus II software to configure the MAX II device.

References

1. ***MAX II Device HandBook*** - Altera Corporation - http:\\www.altera.com (For MAX II related information)