

HSMC E-Gasket Board

(HSMC to Santa Cruz Adapter)

Reference Manual



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Introduction

This manual provides information about the HSMC E-Gasket Board.

Table below shows the revision history of HSMC E-Gasket board reference manual.

Version	Date	Description
1.4	April 2008	Changed the HSMC connector pin nos according to Altera ASP part from the Samtec QTH part
1.3	March 2008	Changed Pin description of J1.180.
1.2	December 2007	Third release: - Made corrections in Figure 2.4: DP Bank1, Figure 2.5: DP Bank 2, Figure 2.6: DP Bank 3. - Added Power supply section.
1.1	November 2007	Second publication: - Changed Block Diagram & Board Components figures - Added Document part number and Product code
1.0	July 2007	First Publication of the HSMC E-Gasket Board Reference Manual

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Shift + Ctrl + N to open to the Go To Page dialog box.
- Bookmarks serve as an additional table of contents.
- Thumbnail icons, which provide miniature preview of each page, provide a link to the pages.
- Numerous links shown in Navy Blue color allow you to jump to related information.

How to Contact SLS

For the most up-to-date information about SLS products, go to the SLS worldwide website at <http://www.slscorp.com>. For additional information about SLS products, consult the source shown below.

Information Type	E-mail
Product literature services, SLS literature services, Non-technical customer services, Technical support.	support@slscorp.com

Typographic Conventions

The HSMC E-Gasket board reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: Board Components .
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: <i>Figure 2-1. Front View of HSMC E-Gasket Board</i>
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
•	Bullets are used in a list of items when the sequence of items is not important.
	The hand points to special information that requires special attention
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.



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HSMC (High Speed Mezzanine Card) is new Altera standard for board expansion interface. The purpose of this interface is to map signals to a common connector interface to allow for new multi-gigahertz differential signaling, slower single-ended signaling as well as power and ground.

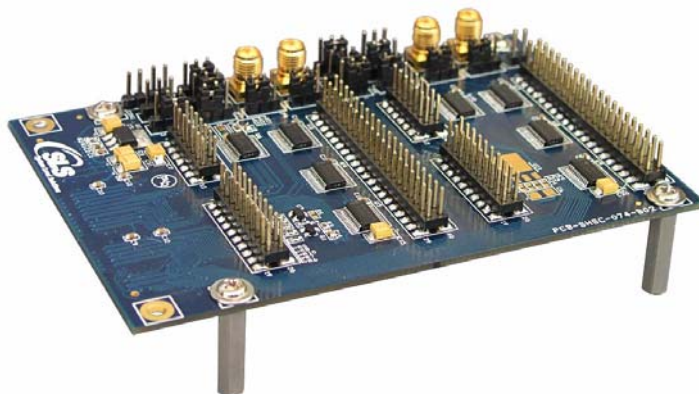
In order to use Altera standard Santa Cruz snap on boards with HSMC interface, we have come up with HSMC to Santa Cruz interface adapter, here after referred as “**HSMC E-Gasket Board**” (A board act as an interface between the HSMC expansion connector and the Santa Cruz snap on board).The HSMC E-Gasket board contains default level shifting circuitry supporting 3.3V compatible level shifting for the Santa Cruz daughter cards with input protection up to +5V.



Refer to the supplied documentation on CD for using HSMC E-Gasket with HSMC Host board having different IO standard, which is not 3.3V compatible.

[Figure 1-1](#), shows the HSMC E-Gasket board angle view.

Figure 1-1. HSMC E-Gasket Board Angle View



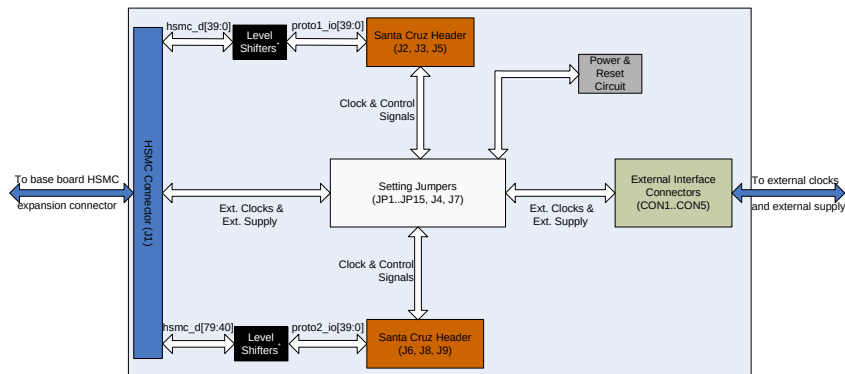
Block Diagram

The HSMC E-Gasket board includes following components:

- Santa Cruz Headers (M): J2, J3, J5 (SC1) and J6, J8, J9 (SC2)
- HSMC Connector (F): J1
- Jumpers for SC1: JP2, JP3, JP4, JP5, JP6, JP7, JP8 and J4
- Jumpers for SC2: JP9, JP10, JP11, JP12, JP13, JP14, JP15 and J7
- SMA Connectors: CON2, CON3, CON4, CON5
- External Supply Connector: CON1
- Jumper for External Supply: JP1

[Figure 1-2](#). below shows block diagram of the HSMC E-Gasket.

Figure 1-2. HSMC E-Gasket Board Block Diagram



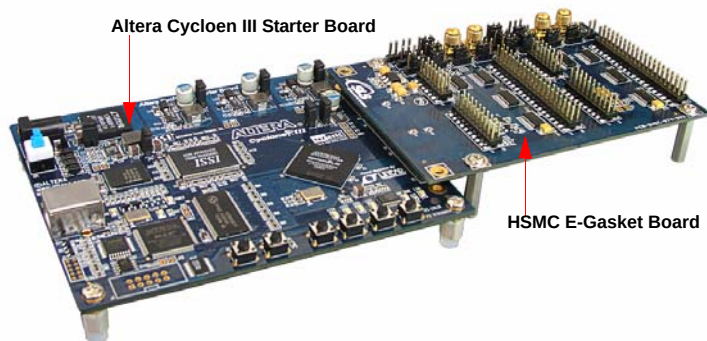
Note: * The default level shifting circuitry supports 3.3V compatible level shifting for the Santa Cruz daughter cards with input protection up to +5V.

Next Chapter explains overview of all the board components.

Example Usage

HSMC Interface Header (J1) of the HSMC E-Gasket Board is connected to HSMC Interface Socket (J1) of Altera Cyclone III Starter Board as shown in [Figure 1-3](#).

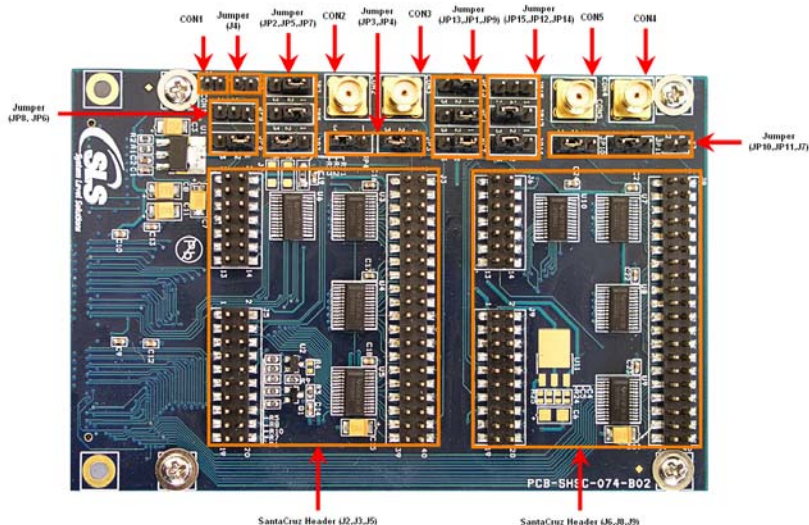
Figure 1-3. Connection of HSMC E-Gasket Board with Altera Cyclone III Starter Board



2. Board Components

This section contains brief overview of the components on the HSMC E-Gasket. [Figure 2-1](#), below shows the components on the top view of the HSMC E-Gasket Board.

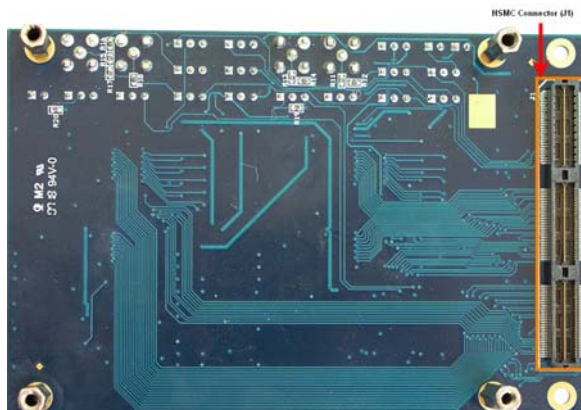
Figure 2-1. Top View of the HSMC E-Gasket Board



HSMC Connector

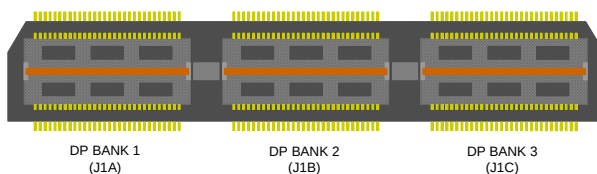
The HSMC E-Gasket Board provides HSMC interface on the back side of the board. See [Figure 2-2](#).

Figure 2-2. Back View of the HSMC E-Gasket Board



The [Figure 2-3](#). below shows zoom view of HSMC interface. It is divided into three DP bank for easy understanding.

Figure 2-3. Zoom View of the HSMC Interface



[Figure 2-4](#). , [Figure 2-5](#). , [Figure 2-6](#). shows the pin description of DP Bank 1(J1A), DP Bank 2(J1B), DP Bank 3(J1C).

Figure 2-4. DP Bank 1- J1A

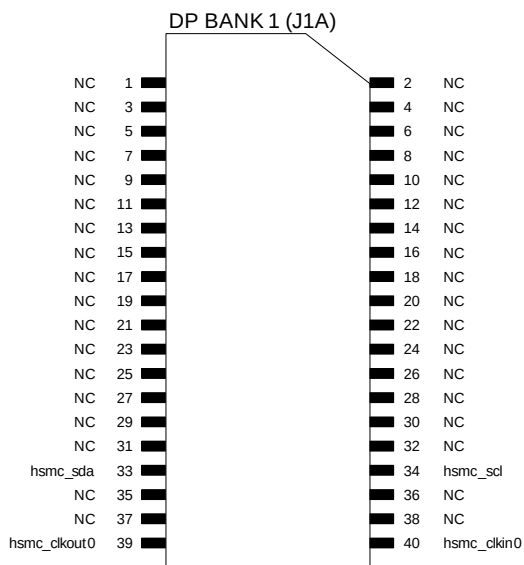


Figure 2-5. DP Bank 2 - J1B

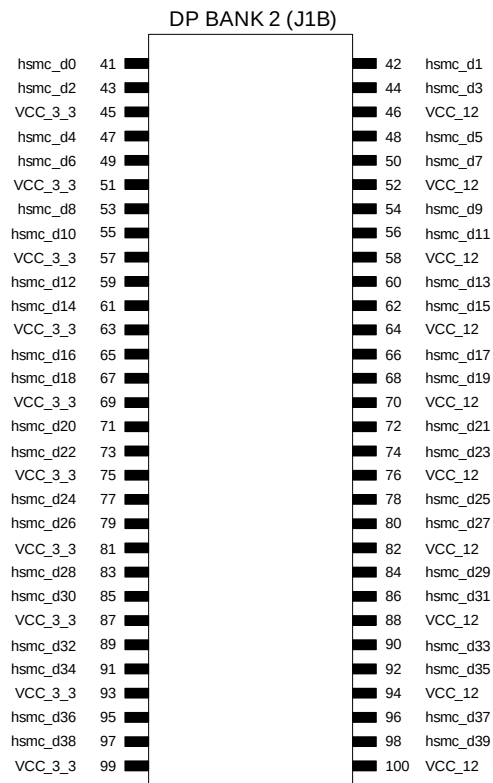


Figure 2-6. DP Bank 3 - J1C

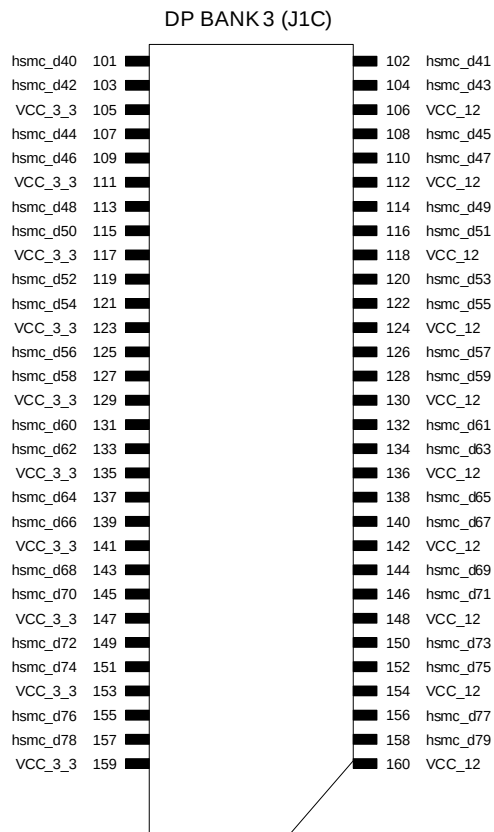


Table 2-1 lists HSMC interface connector (J1) pin mapping for Santa Cruz headers & jumpers settings.

<i>Table 2-1. HSMC Interface Connector (J1) Pin Mapping</i>			
HSMC Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J1.33	hsmc_sda	JP3.1 ¹ , JP10.1 ¹	hsmc_sda
J1.34	hsmc_scl	JP6.1 ¹ , JP13.1, ¹ JP5.3 ¹ , JP6.3 ¹	hsmc_scl
J1.39	hsmc_clkout0	JP12.3 ¹ , JP13.3 ¹	hsmc_clkout0
J1.40	hsmc_clkin0	JP7.3 ¹ , JP14.3 ¹	hsmc_clkin0
J1.41	hsmc_d0	J3.3	proto1_io0
J1.42	hsmc_d1	J3.4	proto1_io1
J1.43	hsmc_d2	J3.5	proto1_io2
J1.44	hsmc_d3	J3.6	proto1_io3
J1.47	hsmc_d4	J3.7	proto1_io4
J1.48	hsmc_d5	J3.8	proto1_io5
J1.49	hsmc_d6	J3.9	proto1_io6
J1.50	hsmc_d7	J3.10	proto1_io7
J1.53	hsmc_d8	J3.11	proto1_io8
J1.54	hsmc_d9	J3.12	proto1_io9
J1.55	hsmc_d10	J3.13	proto1_io10
J1.56	hsmc_d11	J3.14	proto1_io11
J1.59	hsmc_d12	J3.15	proto1_io12
J1.60	hsmc_d13	J3.16	proto1_io13
J1.61	hsmc_d14	J3.17	proto1_io14
J1.62	hsmc_d15	J3.18	proto1_io15
J1.65	hsmc_d16	J3.21	proto1_io16
J1.66	hsmc_d17	J3.23	proto1_io17
J1.67	hsmc_d18	J3.25	proto1_io18

Table 2-1. HSMC Interface Connector (J1) Pin Mapping

HSMC Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J1.68	hsmc_d19	J3.27	proto1_io19
J1.71	hsmc_d20	J3.28	proto1_io20
J1.72	hsmc_d21	J3.29	proto1_io21
J1.73	hsmc_d22	J3.31	proto1_io22
J1.74	hsmc_d23	J3.32	proto1_io23
J1.77	hsmc_d24	J3.33	proto1_io24
J1.78	hsmc_d25	J3.35	proto1_io25
J1.79	hsmc_d26	J3.36	proto1_io26
J1.80	hsmc_d27	J3.37	proto1_io27
J1.83	hsmc_d28	J3.39	proto1_io28
J1.84	hsmc_d29	J2.4	proto1_io29
J1.85	hsmc_d30	J2.5	proto1_io30
J1.86	hsmc_d31	J2.6	proto1_io31
J1.89	hsmc_d32	J2.7	proto1_io32
J1.90	hsmc_d33	J2.8	proto1_io33
J1.91	hsmc_d34	J2.9	proto1_io34
J1.92	hsmc_d35	J2.10	proto1_io35
J1.95	hsmc_d36	J2.11	proto1_io36
J1.96	hsmc_d37	J2.12	proto1_io37
J1.97	hsmc_d38	J2.13	proto1_io38
J1.98	hsmc_d39	J2.14	proto1_io39
J1.101	hsmc_d40	J8.3	proto2_io0
J1.102	hsmc_d41	J8.4	proto2_io1
J1.103	hsmc_d42	J8.5	proto2_io2
J1.104	hsmc_d43	J8.6	proto2_io3
J1.107	hsmc_d44	J8.7	proto2_io4

Table 2-1. HSMC Interface Connector (J1) Pin Mapping

HSMC Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J1.108	hsmc_d45	J8.8	proto2_io5
J1.109	hsmc_d46	J8.9	proto2_io6
J1.110	hsmc_d47	J8.10	proto2_io7
J1.113	hsmc_d48	J8.11	proto2_io8
J1.114	hsmc_d49	J8.12	proto2_io9
J1.115	hsmc_d50	J8.13	proto2_io10
J1.116	hsmc_d51	J8.14	proto2_io11
J1.119	hsmc_d52	J8.15	proto2_io12
J1.120	hsmc_d53	J8.16	proto2_io13
J1.121	hsmc_d54	J8.17	proto2_io14
J1.122	hsmc_d55	J8.18	proto2_io15
J1.125	hsmc_d56	J8.21	proto2_io16
J1.126	hsmc_d57	J8.23	proto2_io17
J1.127	hsmc_d58	J8.25	proto2_io18
J1.128	hsmc_d59	J8.27	proto2_io19
J1.131	hsmc_d60	J8.28	proto2_io20
J1.132	hsmc_d61	J8.29	proto2_io21
J1.133	hsmc_d62	J8.31	proto2_io22
J1.134	hsmc_d63	J8.32	proto2_io23
J1.137	hsmc_d64	J8.33	proto2_io24
J1.138	hsmc_d65	J8.35	proto2_io25
J1.139	hsmc_d66	J8.36	proto2_io26
J1.140	hsmc_d67	J8.37	proto2_io27
J1.143	hsmc_d68	J8.39	proto2_io28
J1.144	hsmc_d69	J6.4	proto2_io29
J1.145	hsmc_d70	J6.5	proto2_io30

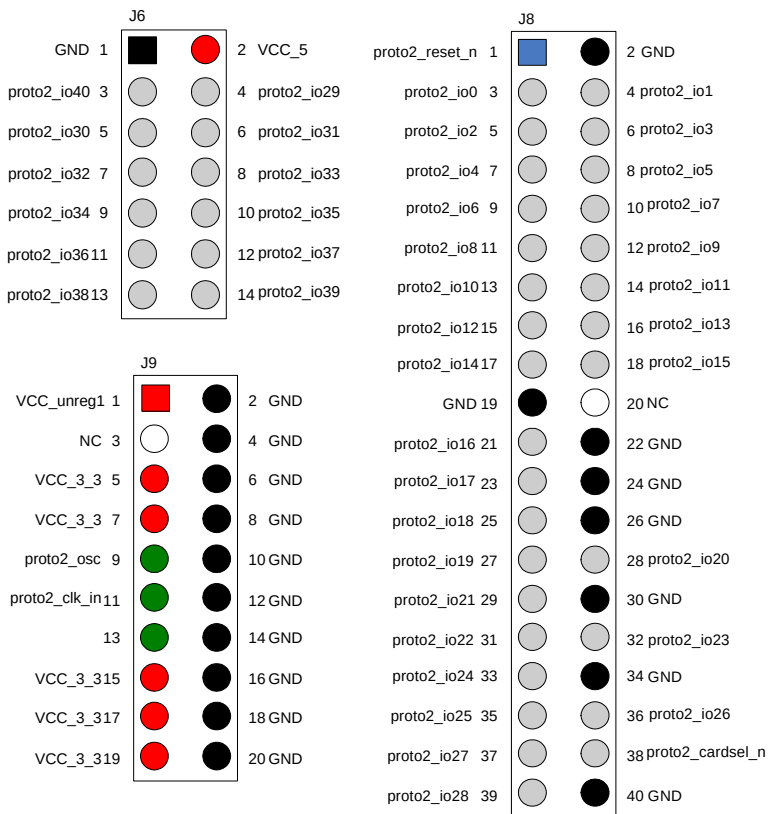
Table 2-1. HSMC Interface Connector (J1) Pin Mapping

HSMC Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J1.146	hsmc_d71	J6.6	proto2_io31
J1.149	hsmc_d72	J6.7	proto2_io32
J1.150	hsmc_d73	J6.8	proto2_io33
J1.151	hsmc_d74	J6.9	proto2_io34
J1.152	hsmc_d75	J6.10	proto2_io35
J1.155	hsmc_d76	J6.11	proto2_io36
J1.156	hsmc_d77	J6.12	proto2_io37
J1.157	hsmc_d78	J6.13	proto2_io38
J1.158	hsmc_d79	J6.14	proto2_io39
J1.160	PSNTn	GND	-
Note: (1) These pins are mapped to jumpers and have multiple input mapping. Refer to Jumpers for Santa Cruz Header1 and Jumpers for Santa Cruz Header 2 section for the mapping details of these pins.			

Santa Cruz Headers

The HSMC E-Gasket Board provides Santa Cruz interface as shown in [Figure 2-1](#). Any short Santa Cruz compatible snap on board can be snapped on to Santa Cruz headers of the HSMC E-Gasket. The [Figure 2-7](#), shows the Santa Cruz Header, SC2 pin description.

Figure 2-7. Santa Cruz Headers (M) - J6, J8, J9



The Figure 2-7. shows the Santa Cruz Header, SC1 pin description.

Figure 2-8. Santa Cruz Headers (M) - J2, J3, J5

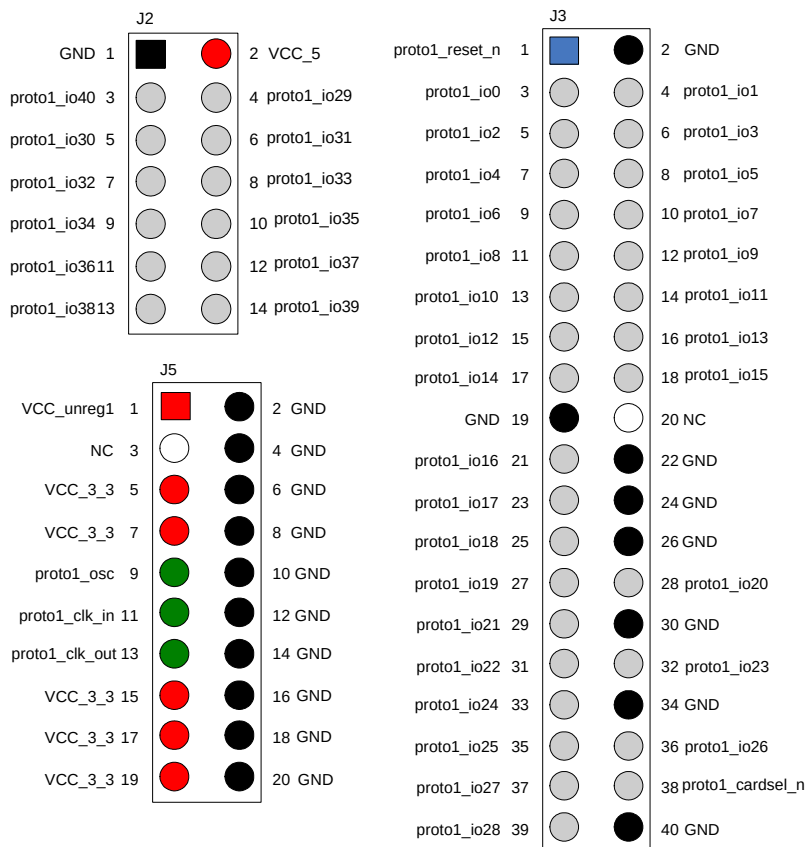


Table 2-2 lists Santa Cruz header (J2) pin mapping for the HSMC interface connector (J1) and jumpers settings.

Table 2-2. Santa Cruz Header (J2) Pin Mapping

Santa Cruz Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J2.3	proto1_io40	JP8.2 ¹	proto1_io40
J2.4	proto1_io29	J1.84	hsmc_d29
J2.5	proto1_io30	J1.85	hsmc_d30
J2.6	proto1_io31	J1.86	hsmc_d31
J2.7	proto1_io32	J1.89	hsmc_d32
J2.8	proto1_io33	J1.90	hsmc_d33
J2.9	proto1_io34	J1.91	hsmc_d34
J2.10	proto1_io35	J1.92	hsmc_d35
J2.11	proto1_io36	J1.95	hsmc_d36
J2.12	proto1_io37	J1.96	hsmc_d37
J2.13	proto1_io38	J1.97	hsmc_d38
J2.14	proto1_io39	J1.98	hsmc_d39

Note:

- (1) These pins are mapped to jumpers and have multiple input mapping. Refer to [Jumpers for Santa Cruz Header1](#) section for the mapping details of these pins.

Table 2-3 lists Santa Cruz header (J3) pin mapping for the HSMC interface connector and jumpers settings.

<i>Table 2-3. Santa Cruz Header (J3) Pin Mapping</i>			
Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J3.1	proto1_reset_n	JP3.2 ¹	proto1_reset_n
J3.3	proto1_io0	J1.41	hsmc_d0
J3.4	proto1_io1	J1.42	hsmc_d1
J3.5	proto1_io2	J1.43	hsmc_d2
J3.6	proto1_io3	J1.44	hsmc_d3
J3.7	proto1_io4	J1.47	hsmc_d4
J3.8	proto1_io5	J1.48	hsmc_d5
J3.9	proto1_io6	J1.49	hsmc_d6
J3.10	proto1_io7	J1.50	hsmc_d7
J3.11	proto1_io8	J1.53	hsmc_d8
J3.12	proto1_io9	J1.54	hsmc_d9
J3.13	proto1_io10	J1.55	hsmc_d10
J3.14	proto1_io11	J1.56	hsmc_d11
J3.15	proto1_io12	J1.59	hsmc_d12
J3.16	proto1_io13	J1.60	hsmc_d13
J3.17	proto1_io14	J1.61	hsmc_d14
J3.18	proto1_io15	J1.62	hsmc_d15
J3.21	proto1_io16	J1.65	hsmc_d16
J3.23	proto1_io17	J1.66	hsmc_d17
J3.25	proto1_io18	J1.67	hsmc_d18
J3.27	proto1_io19	J1.68	hsmc_d19
J3.28	proto1_io20	J1.71	hsmc_d20
J3.29	proto1_io21	J1.72	hsmc_d21

Table 2-3. Santa Cruz Header (J3) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J3.31	proto1_io22	J1.73	hsmc_d22
J3.32	proto1_io23	J1.74	hsmc_d23
J3.33	proto1_io24	J1.77	hsmc_d24
J3.35	proto1_io25	J1.78	hsmc_d25
J3.36	proto1_io26	J1.79	hsmc_d26
J3.37	proto1_io27	J1.80	hsmc_d27
J3.38	proto1_cardsel_n	JP4.2 ¹	proto1_cardsel_n
J3.39	proto1_io28	J1.83	hsmc_d28

Note:

- (1) These pins are mapped to jumpers and have multiple input mapping. Refer to [Jumpers for Santa Cruz Header1](#) section for the mapping details of these pins.

[Table 2-4](#) lists Santa Cruz header (J5) pin mapping for the HSMC interface connector and jumpers settings.

Table 2-4. Santa Cruz Header (J5) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J5.1	VCC_unreg1	JP2.2 ¹	VCC_unreg1
J5.9	proto1_osc	JP5.2 ¹	proto1_osc
J5.11	proto1_clk_in	JP6.2 ¹	proto1_clk_in
J5.13	proto1_clk_out	JP7.2 ¹	proto1_clk_out

Note:

- (1) These pins are mapped to jumpers and have multiple input mapping. Refer to [Jumpers for Santa Cruz Header1](#) section for the mapping details of these pins.

Table 2-5 lists Santa Cruz header (J6) pin mapping for the HSMC interface connector and jumpers settings.

Table 2-5. Santa Cruz Header (J6) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J6.3	proto2_io40	JP15.2 ¹	proto2_io40
J6.4	proto2_io29	J1.144	hsmc_d69
J6.5	proto2_io30	J1.145	hsmc_d70
J6.6	proto2_io31	J1.146	hsmc_d71
J6.7	proto2_io32	J1.149	hsmc_d72
J6.8	proto2_io33	J1.150	hsmc_d73
J6.9	proto2_io34	J1.151	hsmc_d74
J6.10	proto2_io35	J1.152	hsmc_d75
J6.11	proto2_io36	J1.155	hsmc_d76
J6.12	proto2_io37	J1.156	hsmc_d77
J6.13	proto2_io38	J1.157	hsmc_d78
J6.14	proto2_io39	J1.158	hsmc_d79
Note: (1) These pins are mapped to jumpers and have multiple input mapping. Refer to Jumpers for Santa Cruz Header 2 section for the mapping details of these pins.			

Table 2-6 lists Santa Cruz header (J8) pin mapping for the HSMC interface connector and jumpers settings.

Table 2-6. Santa Cruz Header (J8) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J8.1	proto2_reset_n	JP10.2 ¹	proto2_reset_n
J8.3	proto2_io0	J1.101	hsmc_d40
J8.4	proto2_io1	J1.102	hsmc_d41
J8.5	proto2_io2	J1.103	hsmc_d42
J8.6	proto2_io3	J1.104	hsmc_d43
J8.7	proto2_io4	J1.107	hsmc_d44
J8.8	proto2_io5	J1.108	hsmc_d45
J8.9	proto2_io6	J1.109	hsmc_d46
J8.10	proto2_io7	J1.110	hsmc_d47
J8.11	proto2_io8	J1.113	hsmc_d48
J8.12	proto2_io9	J1.114	hsmc_d49
J8.13	proto2_io10	J1.115	hsmc_d50
J8.14	proto2_io11	J1.116	hsmc_d51
J8.15	proto2_io12	J1.119	hsmc_d52
J8.16	proto2_io13	J1.120	hsmc_d53
J8.17	proto2_io14	J1.121	hsmc_d54
J8.18	proto2_io15	J1.122	hsmc_d55
J8.21	proto2_io16	J1.125	hsmc_d56
J8.23	proto2_io17	J1.126	hsmc_d57
J8.25	proto2_io18	J1.127	hsmc_d58
J8.27	proto2_io19	J1.128	hsmc_d59
J8.28	proto2_io20	J1.131	hsmc_d60

Table 2-6. Santa Cruz Header (J8) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J8.29	proto2_io21	J1.132	hsmc_d61
J8.31	proto2_io22	J1.133	hsmc_d62
J8.32	proto2_io23	J1.134	hsmc_d63
J8.33	proto2_io24	J1.137	hsmc_d64
J8.35	proto2_io25	J1.138	hsmc_d65
J8.36	proto2_io26	J1.139	hsmc_d66
J8.37	proto2_io27	J1.140	hsmc_d67
J8.38	proto2_cardsel_n	JP11.2 ¹	proto1_cardsel_n
J8.39	proto2_io28	J1.143	hsmc_d68
Note: (1) These pins are mapped to jumpers and have multiple input mapping. Refer to Jumpers for Santa Cruz Header 2 section for the mapping details of these pins.			

[Table 2-7](#) lists Santa Cruz header (J9) pin mapping for the HSMC interface connector and jumpers settings.

Table 2-7. Santa Cruz Header (J9) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J9.1	VCC_unreg2	JP9.2 ¹	VCC_unreg2
J9.9	proto2_osc	JP12.2 ¹	proto2_osc
J9.11	proto2_clk_in	JP13.2 ¹	proto2_clk_in

Table 2-7. Santa Cruz Header (J9) Pin Mapping

Santa Cruz Header Pin Number	Signal Name	Mapped Pin Number	Mapped Signal Name
J9.13	proto2_clk_out	JP14.2 ¹	proto2_clk_out
Note: (1) These pins are mapped to jumpers and have multiple input mapping. Refer to Jumpers for Santa Cruz Header 2 section for the mapping details of these pins.			

Connectors

The board provides different connectors for external supply and external clock interface.

CON1

This connector provides external power supply. [Table 2-8](#) shows the Connector CON1 pin mapping.

Table 2-8. Connector (CON1) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
CON1.1	VCC_ext	JP1.3
CON1.2	GND	-
Note: (1) External Supply input to +5V regulator and Vunreg on the Santa Cruz Headers (Jumper Option)		

CON2

This SMA connector provides optional external clock input (sma_clk0) for proto1_osc. For settings CON2, refer [Table 2-12, Jumper \(JP5\) Pin Mapping](#).

CON3

This SMA connector provides optional external clock output (sma_clk1) for proto1_clk_out. For setting CON3, refer [Table 2-14, Jumper \(JP7\) Pin Mapping](#).

Jumpers for Santa Cruz Header1

CON4

This SMA connector provides optional external clock input (sma_clk2) for proto2_osc. For settings CON4, refer [Table 2-20, Jumper \(JP12\) Pin Mapping](#).

CON5

This SMA connector provides optional external clock output (sma_clk3) for proto2_clk_out. For settings CON5, refer [Table 2-22, Jumper \(JP14\) Pin Mapping](#).

The HSMC E-Gasket Board has different jumpers for settings for Santa Cruz Header 1 (J2, J3, J5).

JP2

[Table 2-9](#) shows the pin mapping of jumper JP2.

<i>Table 2-9. Jumper (JP2) Pin Mapping</i>		
Pin Number	Signal Name	Mapped Pin No.
JP2.1	VCC_5	U1.2
JP2.2	VCC_unreg1	J5.1
JP2.3	VCC_in	U1.3
Note:		
(1) Short pins 2 and 1 to power +5V at Vunreg of SC Header 1 (Default).		
(2) Short pins 2 and 3 to power the input power of +5V regulator at Vunreg of SC Header 1.		

JP3

[Table 2-10](#) shows the pin mapping of jumper JP3.

<i>Table 2-10. Jumper (JP3) Pin Mapping</i>		
Pin Number	Signal Name	Mapped Pin No.
JP3.1	hsmc_sda	JP8.1, J1.33
JP3.2	protol_reset_n	J3.1

Table 2-10. Jumper (JP3) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP3.3	por_n1	U2.2
Note: (1) Short pins 2 and 1 to use hsmc_sda as proto1_reset_n signal. (2) Short pins 2 and 3 to use por_n1 as proto1_reset_n signal (Default)		

JP4

Table 2-11 shows the pin mapping of jumper JP4.

Table 2-11. Jumper (JP4) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP4.1	VCC_3.3	-
JP4.2	proto1_cardsel_n	J3.38
JP4.3	GND	-
Note: (1) Short pins 2 and 1 to drive the SC Header 1 proto1_cardsel_n HIGH. (2) Short pins 2 and 3 to permanently enable the SC Header 1 proto1_cardsel_n (Default).		

JP5

Table 2-12 shows the pin mapping of jumper JP5.

Table 2-12. Jumper (JP5) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP5.1	sma_clk0	CON2
JP5.2	proto1_osc	J5.9

Table 2-12. Jumper (JP5) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP5.3	hsmc_clkout0	JP6.3, J1.39
Note: (1) Short pins 2 and 1 to use sma_clk0 as proto1_osc for SC Header 1 (Default). (2) Short pins 2 and 3 to use hsmc_clkout0 as proto1_osc for SC Header 1.		

JP6

Table 2-13 shows the pin mapping of jumper JP6.

Table 2-13. Jumper (JP6) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP6.1	hsmc_scl	JP13.1, J1.34
JP6.2	proto1_clk_in	J5.11
JP6.3	hsmc_clkout0	J5.3, J1.39
Note: (1) Short pins 2 and 1 to use hsmc_scl as proto1_clk_in for SC Header 1. (2) Short pins 2 and 3 to use hsmc_clkout0 as proto1_clk_in for SC Header 1 (Default).		

JP7

Table 2-14 shows the pin mapping of jumper JP7.

Table 2-14. Jumper (JP7) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP7.1	sma_clk1	CON3
JP7.2	proto1_clk_out	J5.13

Table 2-14. Jumper (JP7) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP7.3	hsmc_clkln0	JP14.3, J1.40
Note: (1) Short pins 2 and 1 to use sma_clk1 as proto1_clk_out for SC Header1 (2) Short pins 2 and 3 to use hsmc_clkln0 as proto1_clk_out for SC Header 1 (Default).		

JP8

Table 2-15 shows the pin mapping of jumper JP8.

Table 2-15. Jumper (JP8) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
JP8.1	hsmc_sda	JP3.1, J1.33
JP8.2	proto1_io40	J2.3
JP8.3	p1_io40	J4.1
Note: (1) Short pins 2 and 1 to use hsmc_sda as SC Header 1 proto1_io40 signal (Default) (2) Short pins 2 and 3 to use p1_io40 signal as SC Header 1 proto1_io40 signal.		

J4

Table 2-16 shows the pin mapping of jumper J4.

Table 2-16. Jumper (J4) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
J4.1	p1_io40	JP8.3
J4.2	GND	-
Note: (1) External IO input header for the input to jumper option for the SC Header1 IO40		

Jumpers for Santa Cruz Header 2

The section below explains jumper settings for Santa Cruz Header 2 (J6, J8, J9).

JP9

Table 2-17 shows the pin mapping of jumper JP9.

<i>Table 2-17. Jumper (JP9) Pin Mapping</i>		
Pin Number	Signal Name	Mapped Pin No.
JP9.1	VCC_5	U1.2
JP9.2	VCC_unreg2	J9.1
JP9.3	VCC_in	U1.3
Note: (1) Short pins 2 and 1 to power VCC_5 at VCC_unreg2 of SC Header 2 (Default). (2) Short pins 2 and 3 to power the input power of +5V regulator at Vunreg of SC Header 2.		

JP10

Table 2-18 shows the pin mapping of jumper JP10.

<i>Table 2-18. Jumper (JP10) Pin Mapping</i>		
Pin Number	Signal Name	Mapped Pin No.
JP10.1	hsmc_sda	JP15.1, J1.33
JP10.2	proto2_reset_n	J8.1
JP10.3	por_n2	U2.2
Note: (1) Short pins 2 and 1 to use hsmc_sda as SC Header 2 proto2_reset_n signal. (2) Short pins 2 and 3 to use por_n2 signal as SC Header 2 proto2_reset_n signal (Default).		

JP11

Table 2-19 shows the pin mapping of jumper JP11.

Table 2-19. Jumper (JP11) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
JP11.1	NC	-
JP11.2	proto2_cardsel_n	J8.38
JP11.3	GND	-
Note: (1) Short pins 2 and 1 to drive the SC Header 2 proto2_cardsel_n HIGH. (2) Short pins 2 and 3 to permanently enable the SC Header 2 proto2_cardsel_n signal (Default).		

JP12

Table 2-20 shows the pin mapping of jumper JP12.

Table 2-20. Jumper (JP12) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
JP12.1	sma_clk2	CON4
JP12.2	proto2_osc	J9.9
JP12.3	hsmc_clkout0	JP13.3, J1.39
Note: (1) Short pins 2 and 1 to use SMA_CLK2 as PROTO2_OSC for SC Header 2 (Default). (2) Short pins 2 and 3 to use HSMC_CLKOUT0 as PROTO2_OSC for SC Header 2.		

JP13

Table 2-21 shows the pin mapping of jumper JP13.

Table 2-21. Jumper (JP13) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
JP13.1	hsmc_scl	J1.34
JP13.2	proto2_clk_in	J9.11
JP13.3	hsmc_clkout0	JP12.3, J1.39
Note: (1) Short pins 2 and 1 to use HSMC_SCL as PROTO2_CLK_IN for SC Header 2 (Default). (2) Short pins 2 and 3 to use HSMC_CLKOUT0 as PROTO2_CLK_IN for SC Header 2.		

JP14

Table 2-22 shows the pin mapping of jumper JP14.

Table 2-22. Jumper (JP14) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
JP14.1	sma_clk3	CON5
JP14.2	proto2_clk_out	J9.13
JP14.3	hsmc_clkkin0	JP7.3, J1.40
Note: (1) Short pins 2 and 1 to use SMA_CLK3 as PROTO2_CLK_OUT for SC Header 2 (Default). (2) Short pins 2 and 3 to use HSMC_CLKIN0 as PROTO2_CLK_OUT for SC Header 2.		

JP15

Table 2-23 shows the pin mapping of jumper JP15.

Table 2-23. Jumper (JP15) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
JP15.1	hsmc_sda	JP10.1, J1.33
JP15.2	proto2_io40	J6.3
JP15.3	p2_io40	J7.1
Note: (1) Short pins 2 and 1 to use HSMC_SDA as SC Header 2 PROTO2_IO40 signal. (2) Short pins 2 and 3 to use P2_IO40 signal as SC Header 2 PROTO2_IO40 signal (Default).		

J7

Table 2-24 shows the pin mapping of jumper J7.

Table 2-24. Jumper (J7) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
J7.1	p2_io40	JP15.3
J7.2	GND	-
Note: (1) External IO input header for the input to jumper option for the SC Header2 IO40		

Jumper for CON1

The section below explains jumper settings for External Power Supply (CON1).

JP1

Table 2-25 shows the pin mapping of jumper JP1.

Table 2-25. Jumper (JP1) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
JP1.1	VCC_12	From HSMC Connector
JP1.2	VCC_in	JP9.3, JP2.3, U1.3
JP1.3	VCC_ext	CON1.1
Note: (1) Short pins 2 and 1 to use +12V supply from HSMC to generate +5V output for SC Headers (Default) (2) Short pins 2 and 3 to use external voltage input from power headers to generate +5V output for SC Headers		

Power Supply & Reset Circuitry

The section below explains power supply regulators and power on reset circuitry.

3-Terminal Adjustable Regulator (U1)

U1 is adjustable 3-terminal positive voltage regulator. It regulates 5V supply at output with input configured through Jumper JP1 (Either 12V from HSMC connector or an external supply). Table 2-25 shows the pin mapping of 3-Terminal Adjustable Regulator (U1).

Table 2-26. 3-Terminal Adjustable Regulator (U1) Pin Mapping		
Pin Number	Signal Name	Mapped Pin No.
1	ADJ	-
2	Vout	VCC_5
3	Vin	JP1.2 ¹
4	TAB_Vout	VCC_5
Note: (1) Select input to this regulator through jumper JP1.		

3-Pin Supply Voltage Supervisor (U2)

U2 is 3-terminal Supply Voltage Supervisor, used to provide Power On Reset(POR) signal to Santa Cruz headers. [Table 2-27](#) shows the pin mapping of 3-pin supply voltage supervisor.

Table 2-27. 3-Pin Supply Voltage Supervisor (U2) Pin Mapping

Pin Number	Signal Name	Mapped Pin No.
1	GND	-
2	RESET#	JP3.3, JP10.3 ¹
3	Vdd	VCC_3_3
Note: (1) RESET# is not directly mapped to JP3.3(POR_N1) and JP10.3(POR_N2), there is one PNP amplifier in between		