



Kinetis K63F Sub-Family Data Sheet

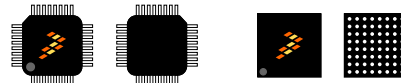
120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

The K63 product family members are optimized for cost-sensitive applications requiring low-power, USB/Ethernet connectivity, up to 256 KB of embedded SRAM and the need for extensive tamper protection, such as Electronic Point of Sales. These devices share the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- Run power consumption down to 250 μ A/MHz. Static power consumption down to 5.8 μ A with full state retention and 5 μ s wakeup. Lowest Static mode down to 339 nA
- DryIce Tamper Detection with active/passive pin, temperature, clock, supply voltage monitoring
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO Vreg, with USB device crystal-less operation
- 10/100 Mbit/s Ethernet MAC with MII and RMII interfaces

MK63FN1M0VLQ12
MK63FN1M0VMD12



144 LQFP
20 x 20 x 1.6 mm Pitch
0.5 mm

144 MAPBGA
13 x 13 x 1.46 mm
Pitch 1 mm

Performance

- Up to 120 MHz ARM® Cortex®-M4 core with DSP instructions and floating point unit

Memories and memory interfaces

- Up to 1 MB program flash memory and 256 KB RAM
- FlexBus external bus interface

System peripherals

- Multiple low-power modes, low-leakage wake-up unit
- Memory protection unit with multi-master protection
- 16-channel DMA controller
- External watchdog monitor and software watchdog

Security and integrity modules

- Hardware CRC module
- Tamper detect and secure storage
- Hardware random-number generator
- Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- 128-bit unique identification (ID) number per chip

Analog modules

- Two 16-bit SAR ADCs
- Two 12-bit DACs
- Three analog comparators (CMP)
- Voltage reference

Communication interfaces

- Ethernet controller with MII and RMII interface
- USB full-/low-speed On-the-Go controller
- Controller Area Network (CAN) module
- Three SPI modules
- Three I2C modules. Support for up to 1 Mbit/s
- Six UART modules
- Secure Digital Host Controller (SDHC)
- I2S module

Timers

- Two 8-channel Flex-Timers (PWM/Motor control)
- Two 2-channel FlexTimers (PWM/Quad decoder)
- IEEE 1588 timers
- 32-bit PITs and 16-bit low-power timers
- Real-time clock
- Programmable delay block

Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- PLL, FLL, and multiple internal oscillators
- 48 MHz Internal Reference Clock (IRC48M)

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Ordering Information ¹

| Part Number | Memory | | Maximum number of I/O's |
|----------------|--------|-----------|-------------------------|
| | Flash | SRAM (KB) | |
| MK63FN1M0VLQ12 | 1 MB | 256 | 100 |
| MK63FN1M0VMD12 | 1 MB | 256 | 95 |

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

| Type | Description | Resource |
|------------------|--|--|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | K60PB ¹ |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | K63P144M120SF5RM ¹ |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | K63P144M120SF5 ¹ |
| Package drawing | Package dimensions are provided in package drawings. | <ul style="list-style-type: none"> • LQFP 144-pin: 98ASS23177W¹ • MAPBGA 144-pin: 98ASA00222D¹ |

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

Kinetis K63 Family

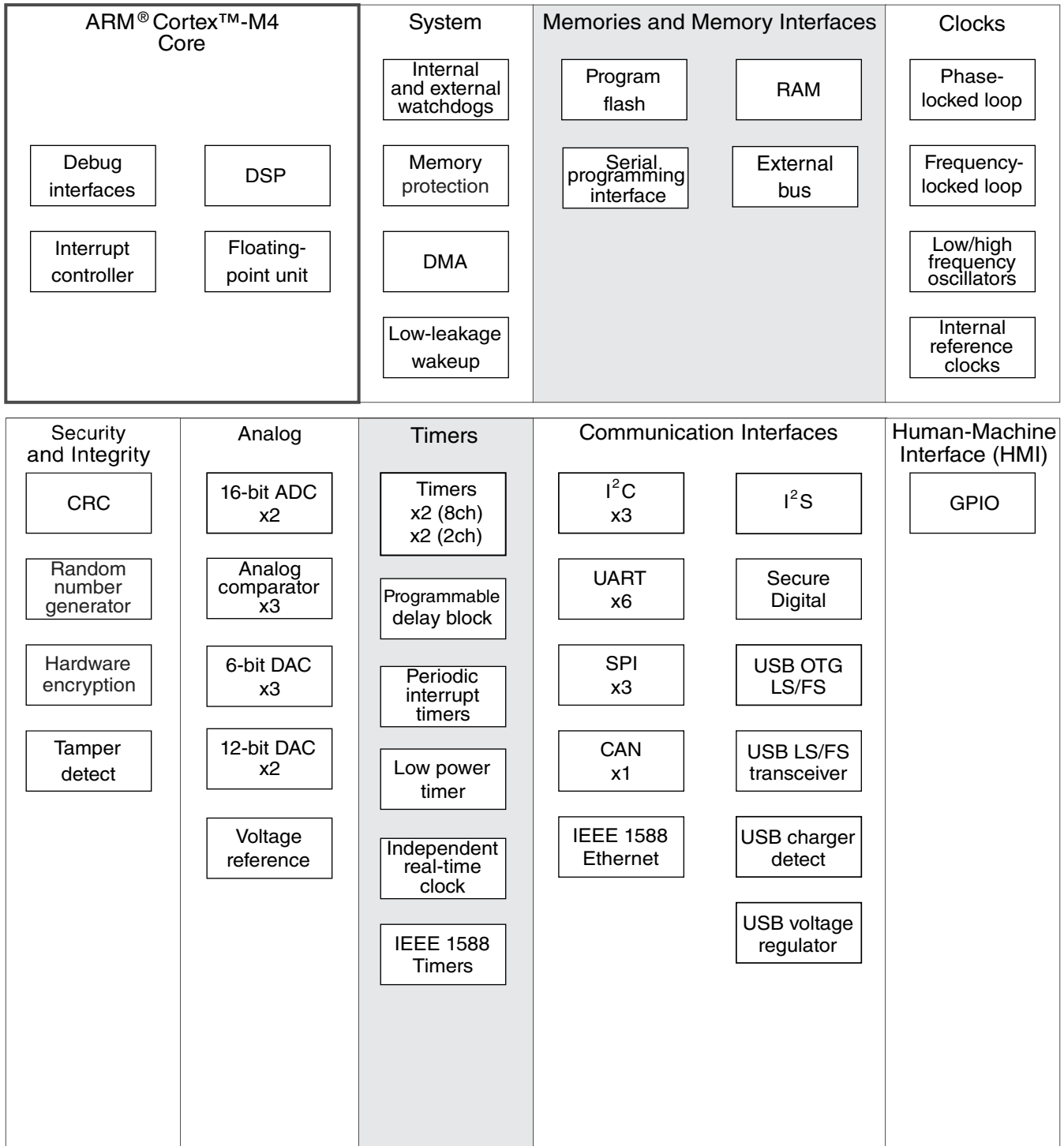


Figure 1. K63 block diagram

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1 Ratings

1.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |
| | Solder temperature, leaded | — | 245 | | |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

General

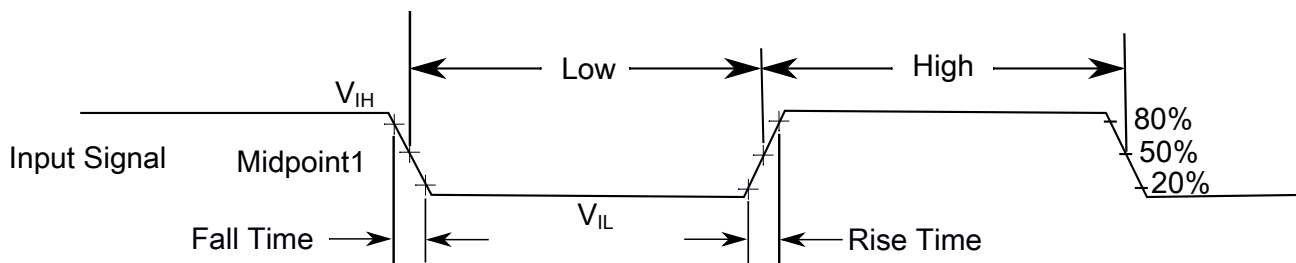
| Symbol | Description | Min. | Max. | Unit |
|----------------|--|----------------|----------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 185 | mA |
| V_{DIO} | Digital input voltage (except RESET, EXTAL, and XTAL) | -0.3 | 5.5 | V |
| V_{AIO} | Analog ¹ , RESET, EXTAL, and XTAL input voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_D | Maximum current single pin limit (applies to all digital pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |
| V_{USB0_DP} | USB0_DP input voltage | -0.3 | 3.63 | V |
| V_{USB0_DM} | USB0_DM input voltage | -0.3 | 3.63 | V |
| V_{REGIN} | USB regulator input | -0.3 | 6.0 | V |
| V_{BAT} | RTC battery supply voltage | -0.3 | 3.8 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------------------------|--|---|---|--------|-------|
| V _{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V _{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| V _{DD} – V _{DDA} | V _{DD} -to-V _{DDA} differential voltage | -0.1 | 0.1 | V | |
| V _{SS} – V _{SSA} | V _{SS} -to-V _{SSA} differential voltage | -0.1 | 0.1 | V | |
| V _{BAT} | RTC battery supply voltage | 1.71 | 3.6 | V | |
| V _{IH} | Input high voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V | 0.7 × V _{DD} 0.75 × V _{DD} | — — | V V | |
| V _{IL} | Input low voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V | — — | 0.35 × V _{DD} 0.3 × V _{DD} | V V | |
| V _{HYS} | Input hysteresis | 0.06 × V _{DD} | — | V | |
| I _{CDIO} | Digital pin (except Tamper pins) negative DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V | -5 | — | mA | 1 |
| I _{CAIO} | Analog ² , EXTAL, and XTAL pin DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection) | -5 — | — +5 | mA | 3 |
| I _{Cont} | Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection • Positive current injection | -25 — | — +25 | mA | |
| V _{ODPU} | Open drain pullup voltage level | V _{DD} | V _{DD} | V | 4 |
| V _{RAM} | V _{DD} voltage required to retain RAM | 1.2 | — | V | |
| V _{RFVBAT} | V _{BAT} voltage required to retain the VBAT register file | V _{POR_VBAT} | — | V | |

- All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is less than V_{DIO_MIN}, a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} (=V_{SS}-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{CDIO}|$.
- Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
- All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{CAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{CAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
- Open drain outputs must be pulled to V_{DD}.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|---|------|------|------|------|-------|
| V _{POR} | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| V _{LVDH} | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| V _{LVW1H} | Low-voltage warning thresholds — high range | | | | | 1 |
| | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| V _{LVW2H} | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| V _{LVW3H} | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| V _{LVW4H} | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| V _{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | 80 | — | mV | |
| V _{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| V _{LVW1L} | Low-voltage warning thresholds — low range | | | | | 1 |
| | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| V _{LVW2L} | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| V _{LVW3L} | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| V _{LVW4L} | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| V _{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | 60 | — | mV | |
| V _{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| t _{LPO} | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | μs | |

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|------|------|------|------|-------|
| V _{POR_VBAT} | Falling VBAT supply POR detect voltage | 0.8 | 1.1 | 1.5 | V | |

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------------|---|------|------|------|-------|
| V _{OH} | Output high voltage — high drive strength | | | | |

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-----------------|-------|---------------|-------|
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -8\text{mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$ | $V_{DD} - 0.5$ | — | V | |
| | Output high voltage — low drive strength | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$ | $V_{DD} - 0.5$ | — | V | |
| | | $V_{DD} - 0.5$ | — | V | |
| I_{OHT} | Output high current total for all ports | — | 100 | mA | |
| V_{OH_Tamper} | Output high voltage — high drive strength | $V_{BAT} - 0.5$ | — | V | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OH} = -10\text{mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$ | $V_{BAT} - 0.5$ | — | V | |
| | Output high voltage — low drive strength | $V_{BAT} - 0.5$ | — | V | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OH} = -2\text{mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$ | $V_{BAT} - 0.5$ | — | V | |
| I_{OH_Tamper} | Output high current total for Tamper pins | — | 100 | mA | |
| V_{OL} | Output low voltage — high drive strength | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{mA}$ | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{mA}$ | — | 0.5 | V | |
| | | — | 0.5 | V | |
| I_{OLT} | Output low current total for all ports | — | 100 | mA | |
| V_{OL_Tamper} | Output low voltage — high drive strength | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OL} = 10\text{mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OL} = 3\text{mA}$ | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OL} = 2\text{mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{mA}$ | — | 0.5 | V | |
| | | — | 0.5 | V | |
| I_{OL_Tamper} | Output low current total for Tamper pins | — | 100 | mA | |
| I_{IN} | Input leakage current (per pin) for full temperature range | — | 1 | μA | 1 |
| I_{IN} | Input leakage current (per pin) at 25°C | — | 0.025 | μA | 1 |
| I_{IN_Tamper} | Input leakage current (per Tamper pin) for full temperature range | — | 1 | μA | |
| I_{IN_Tamper} | Input leakage current (per Tamper pin) at 25°C | — | 0.025 | μA | |
| I_{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 0.25 | μA | |
| I_{OZ_Tamper} | Hi-Z (off-state) leakage current (per Tamper pin) | — | 0.25 | μA | |

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------------|--|------|------|------|-------|
| R _{PU} | Internal pullup resistors (except Tamper pins) | 20 | 50 | kΩ | 2 |
| R _{PD} | Internal pulldown resistors (except Tamper pins) | 20 | 50 | kΩ | 3 |

1. Measured at V_{DD}=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}
3. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLS_X→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|------|------|------|-------|
| t _{POR} | After a POR event, amount of time from the point V _{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | 300 | μs | |
| | • VLLS0 → RUN | — | 156 | μs | |
| | • VLLS1 → RUN | — | 156 | μs | |
| | • VLLS2 → RUN | — | 78 | μs | |
| | • VLLS3 → RUN | — | 78 | μs | |
| | • LLS → RUN | — | 4.8 | μs | |
| | • VLPS → RUN | — | 4.5 | μs | |
| | • STOP → RUN | — | 4.5 | μs | |

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------------|---|------|-------|----------|------|-------|
| I _{DDA} | Analog supply current | — | — | See note | mA | 1 |
| I _{DD_RUN} | Run mode current — all peripheral clocks disabled, code executing from flash | — | 31.1 | 36.65 | mA | 2 |
| | | — | 31 | 36.75 | mA | |
| I _{DD_RUN} | Run mode current — all peripheral clocks enabled, code executing from flash | — | 42.7 | 48.35 | mA | 3, 4 |
| | | — | 40 | 41.60 | mA | |
| | | — | 48.33 | 51.50 | mA | |
| I _{DD_WAIT} | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled | — | 17.9 | — | mA | 2 |
| I _{DD_WAIT} | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 6.9 | — | mA | 5 |
| I _{DD_VLPR} | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 1.0 | — | mA | 6 |
| I _{DD_VLPR} | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | 1.7 | — | mA | 7 |
| I _{DD_VLPW} | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | 0.678 | — | mA | 8 |
| I _{DD_STOP} | Stop mode current at 3.0 V | — | 0.49 | 0.67 | mA | |
| | | — | 1.18 | 2.11 | mA | |
| | | — | 3.0 | 5.74 | mA | |
| I _{DD_VLPS} | Very-low-power stop mode current at 3.0 V | — | 57 | 139.31 | μA | |
| | | — | 291 | 679.33 | μA | |
| | | — | 927.3 | 1869.85 | μA | |
| I _{DD_LLS} | Low leakage stop mode current at 3.0 V | — | 5.8 | 10.48 | μA | 9 |
| | | — | 26.7 | 47.99 | μA | |

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|---|------|-------|--------|------|-------|
| | <ul style="list-style-type: none"> • @ 70°C • @ 105°C | — | 114.9 | 196.49 | μA | |
| I _{DD_VLLS3} | Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 4.4 | 5.54 | μA | |
| | | — | 21 | 36.46 | μA | |
| | | — | 90.2 | 150.17 | μA | |
| I _{DD_VLLS2} | Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 2.1 | 2.34 | μA | |
| | | — | 6.84 | 10.36 | μA | |
| | | — | 29.4 | 46.74 | μA | |
| I _{DD_VLLS1} | Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 0.817 | 0.86 | μA | |
| | | — | 3.97 | 5.77 | μA | |
| | | — | 21.3 | 33.99 | μA | |
| I _{DD_VLLS0} | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 0.520 | 0.60 | μA | |
| | | — | 3.67 | 5.52 | μA | |
| | | — | 21.2 | 33.68 | μA | |
| I _{DD_VLLS0} | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 0.339 | 0.412 | μA | |
| | | — | 3.36 | 4.2 | μA | |
| | | — | 20.3 | 29.9 | μA | |
| I _{DD_VBAT} | Average current with RTC and 32 kHz disabled <ul style="list-style-type: none"> • @ 1.8 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C • @ 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 0.16 | 0.19 | μA | |
| | | — | 0.55 | 0.72 | μA | |
| | | — | 2.5 | 3.68 | μA | |
| | | — | 0.18 | 0.21 | μA | |
| | | — | 0.66 | 0.86 | μA | |
| | | — | 2.92 | 4.30 | μA | |
| I _{DD_VBAT} | Average current when CPU is not accessing RTC registers | | | | | 10 |

Table 6. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|--|------|------|------|------|-------|
| | <ul style="list-style-type: none"> • @ 1.8 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C • @ 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C | — | 0.59 | 0.70 | μA | |
| | | — | 1.0 | 1.30 | μA | |
| | | — | 3.0 | 4.42 | μA | |
| | | — | 0.71 | 0.84 | μA | |
| | | — | 1.22 | 1.59 | μA | |
| | | — | 3.5 | 5.15 | μA | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus, 30 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus clock, 30 MHz Flexbus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 256 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

Table 7. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|----------------------------|---|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| I _{IREFSTEN4MHZ} | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | μA |
| I _{IREFSTEN32KHZ} | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | μA |
| I _{EREFSTEN4MHZ} | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |
| I _{EREFSTEN32KHZ} | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. | | | | | | | |
| VLLS1 | | 440 | 490 | 540 | 560 | 570 | 580 | |

Table continues on the next page...

Table 7. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | VLLS3 | 440 | 490 | 540 | 560 | 570 | 580 | nA |
| | LLS | 490 | 490 | 540 | 560 | 570 | 680 | |
| | VLPS | 510 | 560 | 560 | 560 | 610 | 680 | |
| | STOP | 510 | 560 | 560 | 560 | 610 | 680 | |
| I _{48MIRC} | 48 Mhz internal reference clock | 350 | 350 | 350 | 350 | 350 | 350 | μA |
| I _{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | μA |
| I _{RTC} | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 432 | 357 | 388 | 475 | 532 | 810 | nA |
| I _{UART} | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | μA |
| | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | |
| | OSCCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| I _{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | μA |
| I _{ADC} | ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 42 | 42 | 42 | 42 | 42 | 42 | μA |

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

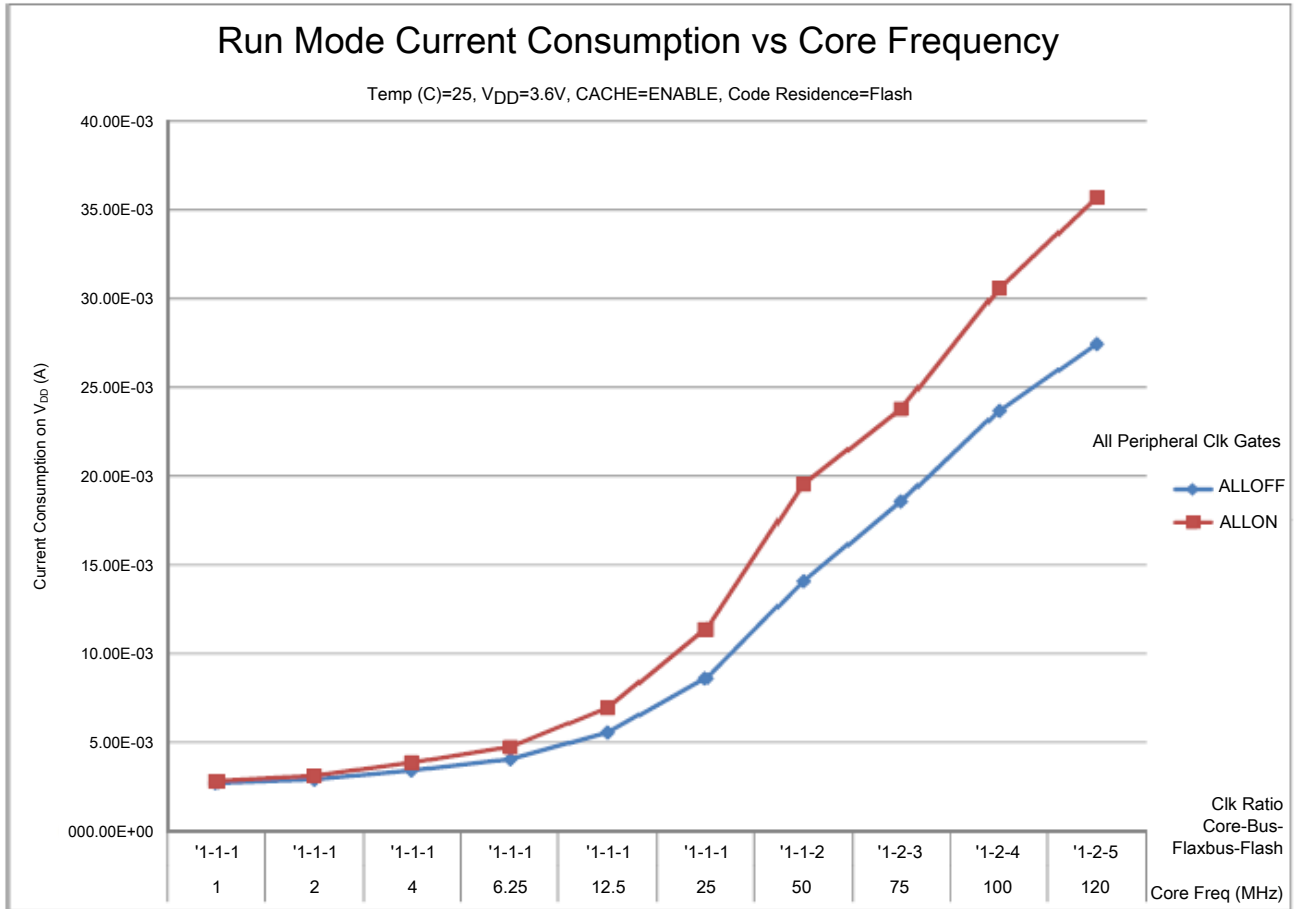


Figure 3. Run mode supply current vs. core frequency

General

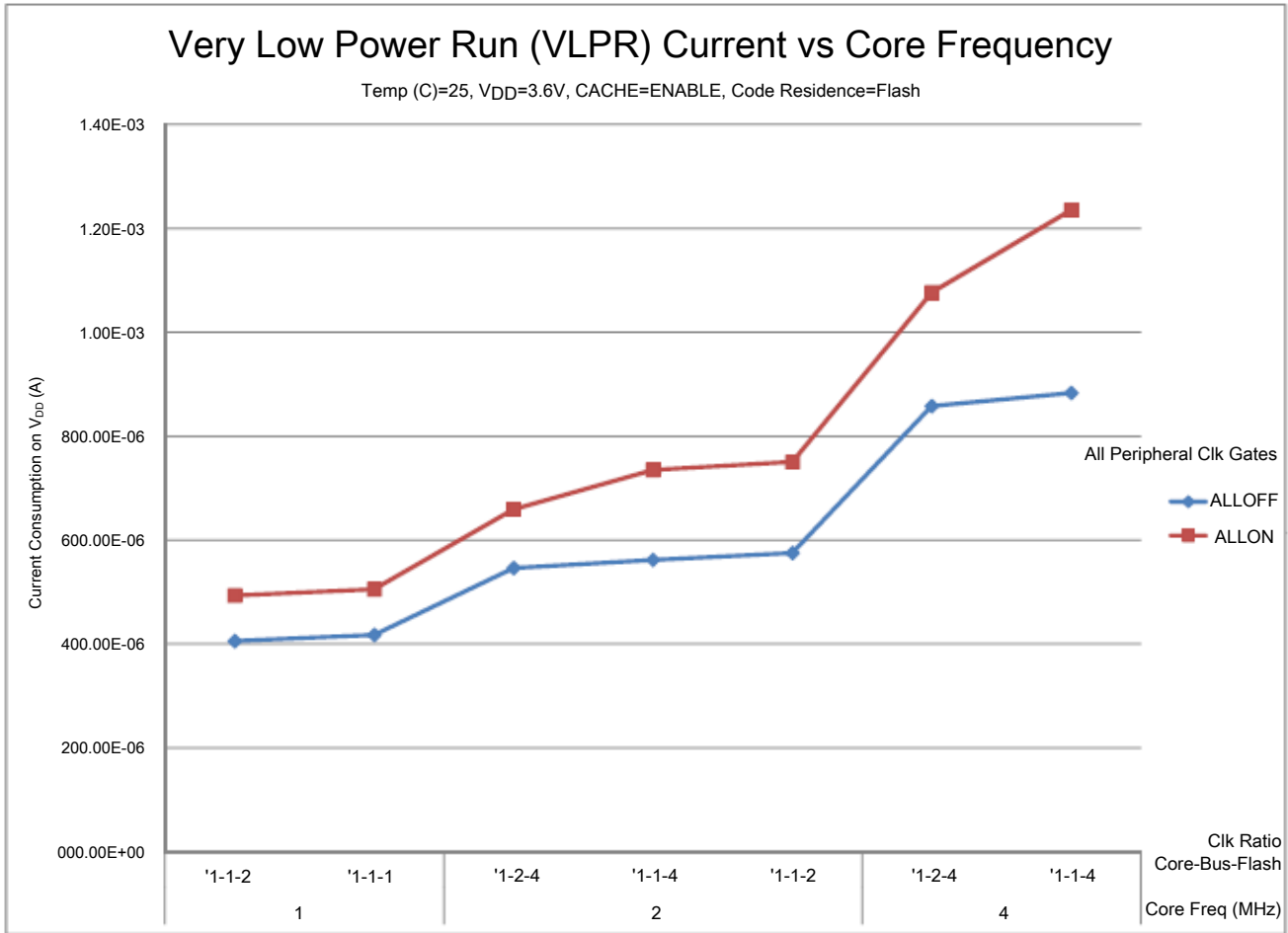


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|----------|------|-------|
| | | | 144 LQFP | | |
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 16 | dBμV | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 22 | dBμV | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 21 | dBμV | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 16 | dBμV | |
| V _{RE_IEC} | IEC level | 0.15–1000 | L | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and*

Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 96\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|-------------|---------------------------------|------|------|------|
| C_{IN_A} | Input capacitance: analog pins | — | 7 | pF |
| C_{IN_D} | Input capacitance: digital pins | — | 7 | pF |

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------------|--|------|------|------|-------|
| Normal run mode | | | | | |
| f_{SYS} | System and core clock | — | 120 | MHz | |
| | System and core clock when Full Speed USB in operation | 20 | — | MHz | |
| f_{ENET} | System and core clock when ethernet in operation | | | MHz | |
| | • 10 Mbps | 5 | — | | |
| | • 100 Mbps | 50 | — | | |
| f_{BUS} | Bus clock | — | 60 | MHz | |
| FB_CLK | FlexBus clock | — | 50 | MHz | |
| f_{FLASH} | Flash clock | — | 25 | MHz | |

Table continues on the next page...

Table 10. Device clock specifications (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|----------------------------|----------------------------------|------|------|------|-------|
| f _{LPTMR} | LPTMR clock | — | 25 | MHz | |
| VLPR mode ¹ | | | | | |
| f _{SYS} | System and core clock | — | 4 | MHz | |
| f _{BUS} | Bus clock | — | 4 | MHz | |
| FB_CLK | FlexBus clock | — | 4 | MHz | |
| f _{FLASH} | Flash clock | — | 0.8 | MHz | |
| f _{ERCLK} | External reference clock | — | 16 | MHz | |
| f _{LPTMR_pin} | LPTMR clock | — | 25 | MHz | |
| f _{LPTMR_ERCLK} | LPTMR external reference clock | — | 16 | MHz | |
| f _{FlexCAN_ERCLK} | FlexCAN external reference clock | — | 8 | MHz | |
| f _{I2S_MCLK} | I2S master clock | — | 12.5 | MHz | |
| f _{I2S_BCLK} | I2S bit clock | — | 4 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, IEEE 1588 timer, timers, and I²C signals.

Table 11. General switching specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|------|------|------------------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path | 100 | — | ns | 3 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 50 | — | ns | 3 |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns | 3 |
| | Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion | 2 | — | Bus clock cycles | |
| | Port rise and fall time (high drive strength) - 3 V | | | | 4 |
| | <ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled | — | 8 | ns | |
| | | — | 6 | ns | |
| | | — | 18 | ns | |

Table continues on the next page...

Table 11. General switching specifications (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|---|------|------|------|-------|
| | <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ | — | 12 | ns | |
| | Port rise and fall time (high drive strength) - 5 V <ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ | — | 6 | ns | 4 |
| | | — | 4 | ns | |
| | | — | 24 | ns | |
| | | — | 14 | ns | |
| | Port rise and fall time (low drive strength) - 3 V <ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ | — | 12 | ns | 5 |
| | | — | 6 | ns | |
| | | — | 24 | ns | |
| | | — | 16 | ns | |
| | Port rise and fall time (low drive strength) - 5 V <ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ | — | 17 | ns | 5 |
| | | — | 10 | ns | |
| | | — | 36 | ns | |
| | | — | 20 | ns | |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 25 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit |
|----------------|----------------------------------|------|------|------|
| T _J | Die junction temperature | -40 | 125 | °C |
| T _A | Ambient temperature ¹ | -40 | 105 | °C |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

$$T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$$

2.4.2 Thermal attributes

Table 13. Thermal attributes

| Board type | Symbol | Description | 144 LQFP | 144 MAPBGA | Unit | Notes |
|-------------------|-------------------|--|----------|------------|------|-------|
| Single-layer (1s) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 51 | 38.1 | °C/W | 1 |
| Four-layer (2s2p) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 43 | 21.6 | °C/W | 1 |
| Single-layer (1s) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 42 | 30.8 | °C/W | 1 |
| Four-layer (2s2p) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 36 | 18 | °C/W | 1 |
| — | R _{θJB} | Thermal resistance, junction to board | 30 | 16.5 | °C/W | 2 |
| — | R _{θJC} | Thermal resistance, junction to case | 11 | 8.9 | °C/W | 3 |
| — | Ψ _{JT} | Thermal characterization parameter, junction to package top | 2 | 0.9 | °C/W | 4 |

Table 13. Thermal attributes

| Board type | Symbol | Description | 144 LQFP | 144 MAPBGA | Unit | Notes |
|------------|--------|---|----------|------------|------|-------|
| | | outside center (natural convection) | | | | |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 14. Debug trace operating behaviors

| Symbol | Description | Min. | Max. | Unit |
|-----------|--------------------------|---------------------|------|------|
| T_{cyc} | Clock period | Frequency dependent | | MHz |
| T_{wl} | Low pulse width | 2 | — | ns |
| T_{wh} | High pulse width | 2 | — | ns |
| T_r | Clock and data rise time | — | 3 | ns |
| T_f | Clock and data fall time | — | 3 | ns |
| T_s | Data setup | 1.5 | — | ns |
| T_h | Data hold | 1 | — | ns |

Peripheral operating requirements and behaviors

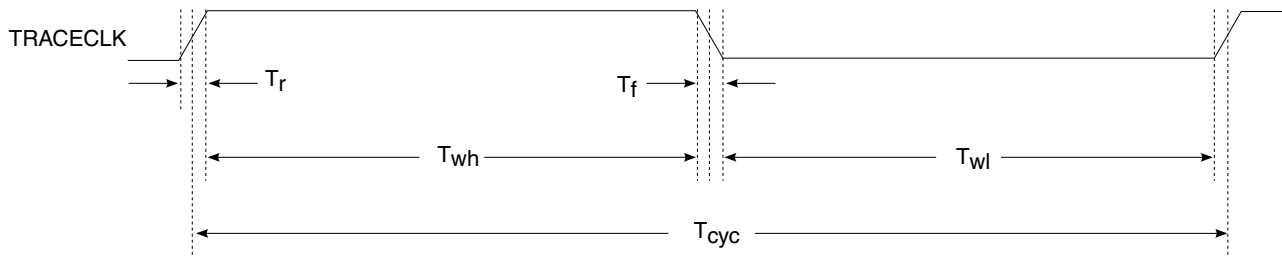


Figure 5. TRACE_CLKOUT specifications

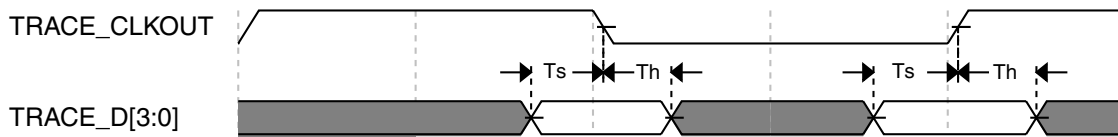


Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 15. JTAG limited voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 0 | 10 | MHz |
| | | 0 | 25 | |
| | | 0 | 50 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 50 | — | ns |
| | | 20 | — | ns |
| | | 10 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 2.6 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |

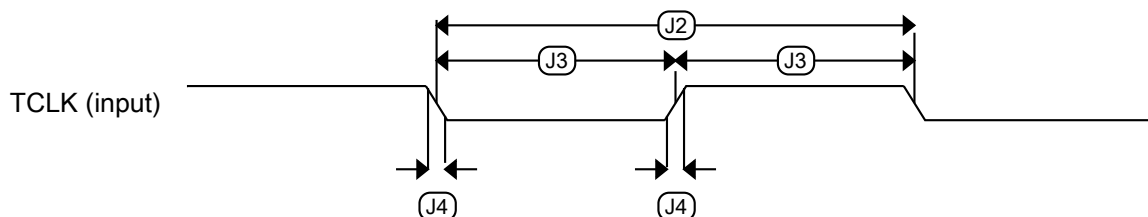
Table continues on the next page...

Table 15. JTAG limited voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------|---|------|------|------|
| J11 | TCLK low to TDO data valid | — | 17 | ns |
| J12 | TCLK low to TDO high-Z | — | 17 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

Table 16. JTAG full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------------------|----------------|----------------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 0 0 0 | 10 20 40 | MHz |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 50 25 12.5 | — — — | ns ns ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 2.9 | — | ns |
| J11 | TCLK low to TDO data valid | — | 22.1 | ns |
| J12 | TCLK low to TDO high-Z | — | 22.1 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

**Figure 7. Test clock input timing**

Peripheral operating requirements and behaviors

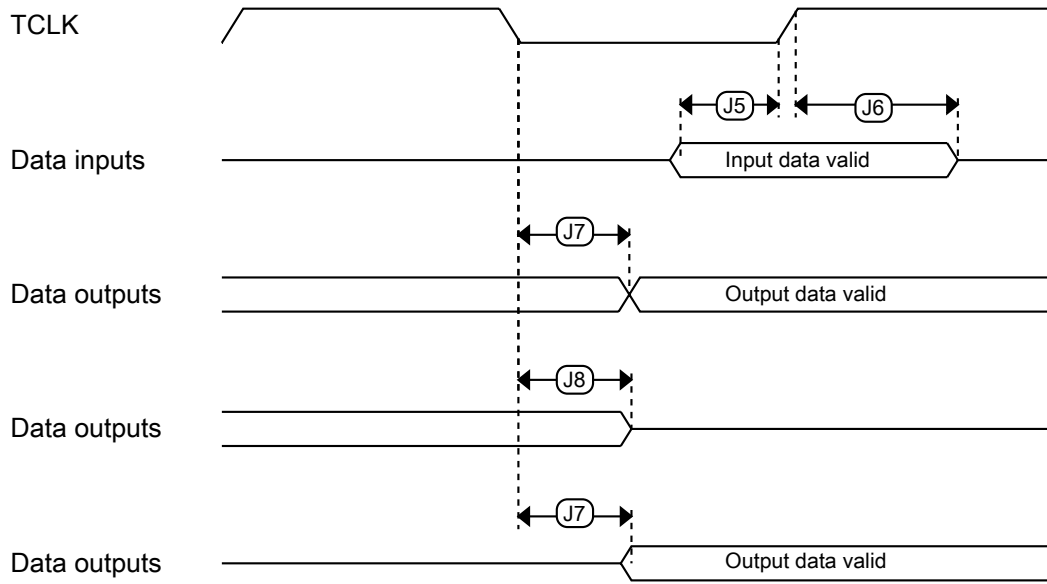


Figure 8. Boundary scan (JTAG) timing

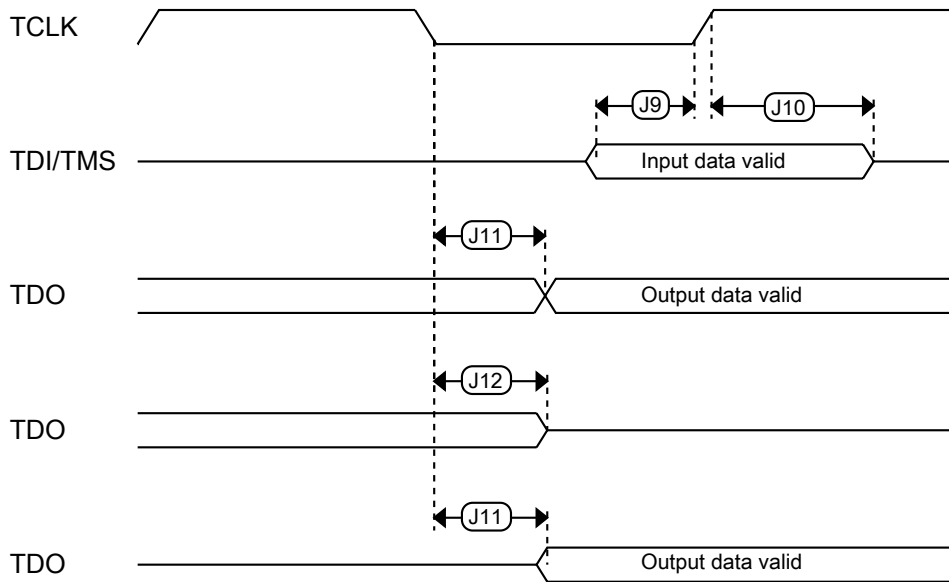
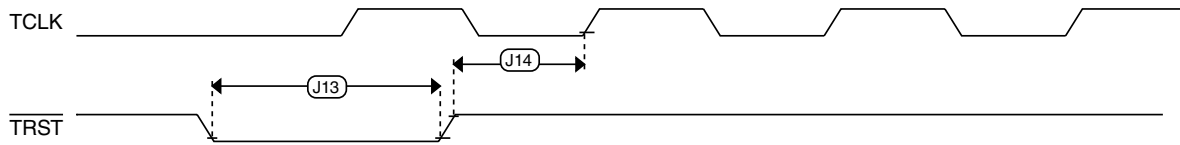


Figure 9. Test Access Port timing

Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 17. MCG specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------------------------|--|-------|-----------|-----------|--------------------|-------|
| $f_{\text{ints_ft}}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | — | 32.768 | — | kHz | |
| $f_{\text{ints_t}}$ | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | |
| I_{ints} | Internal reference (slow clock) current | — | 20 | — | μA | |
| $\Delta f_{\text{dco_res_t}}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | — | ± 0.3 | ± 0.6 | $\%f_{\text{dco}}$ | 1 |
| $\Delta f_{\text{dco_res_t}}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | — | ± 0.2 | ± 0.5 | $\%f_{\text{dco}}$ | 1 |
| $\Delta f_{\text{dco_t}}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | — | ± 0.5 | ± 2 | $\%f_{\text{dco}}$ | 1, 2 |
| $\Delta f_{\text{dco_t}}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | — | ± 0.3 | ± 1 | $\%f_{\text{dco}}$ | 1 |
| $f_{\text{intf_ft}}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | — | 4 | — | MHz | |
| $f_{\text{intf_t}}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | 3 | — | 5 | MHz | |
| I_{intf} | Internal reference (fast clock) current | — | 25 | — | μA | |

Table continues on the next page...

Table 17. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|---------------------|---|--|------------|---------|---------|-------|------|
| f_{loc_low} | Loss of external clock minimum frequency — RANGE = 00 | $(3/5) \times f_{ints_t}$ | — | — | kHz | | |
| f_{loc_high} | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | $(16/5) \times f_{ints_t}$ | — | — | kHz | | |
| FLL | | | | | | | |
| f_{fill_ref} | FLL reference frequency range | 31.25 | — | 39.0625 | kHz | | |
| f_{dco} | DCO output frequency range | Low range (DRS=00) $640 \times f_{fill_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS=01) $1280 \times f_{fill_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) $1920 \times f_{fill_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) $2560 \times f_{fill_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco_t_DMX32}$ | DCO output frequency | Low range (DRS=00) $732 \times f_{fill_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS=01) $1464 \times f_{fill_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) $2197 \times f_{fill_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) $2929 \times f_{fill_ref}$ | — | 95.98 | — | MHz | |
| J_{cyc_fill} | FLL period jitter • $f_{DCO} = 48$ MHz • $f_{DCO} = 98$ MHz | — | 180 150 | — | ps | | |
| $t_{fill_acquire}$ | FLL target frequency acquisition time | — | — | 1 | ms | 7 | |
| PLL | | | | | | | |
| f_{vco} | VCO operating frequency | 48.0 | — | 120 | MHz | | |
| I_{pll} | PLL operating current • PLL @ 96 MHz ($f_{osc_hi_1} = 8$ MHz, $f_{pll_ref} = 2$ MHz, VDIV multiplier = 48) | — | 1060 | — | μ A | 8 | |
| I_{pll} | PLL operating current • PLL @ 48 MHz ($f_{osc_hi_1} = 8$ MHz, $f_{pll_ref} = 2$ MHz, VDIV multiplier = 24) | — | 600 | — | μ A | 8 | |
| f_{pll_ref} | PLL reference frequency range | 2.0 | — | 4.0 | MHz | | |
| J_{cyc_pll} | PLL period jitter (RMS) • $f_{vco} = 48$ MHz • $f_{vco} = 120$ MHz | — | 120 | — | ps | 9 | |
| | | — | 80 | — | ps | | |
| J_{acc_pll} | PLL accumulated jitter over 1 μ s (RMS) | | | | | 9 | |

Table continues on the next page...

Table 17. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------|---|------------|------|---|------|-------|
| | <ul style="list-style-type: none"> $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 120 \text{ MHz}$ | — | 1350 | — | ps | |
| | | — | 600 | — | ps | |
| D_{lock} | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | |
| D_{unl} | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| t_{pll_lock} | Lock detector detection time | — | — | $150 \times 10^{-6} + 1075(1/f_{pll_ref})$ | s | 10 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. $2 \text{ V} \leq VDD \leq 3.6 \text{ V}$.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 18. IRC48M specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|--|------|-----------|-----------|----------------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I_{DD48M} | Supply current | — | 400 | 500 | μA | |
| f_{irc48m} | Internal reference frequency | — | 48 | — | MHz | |
| $\Delta f_{irc48m_ol_lv}$ | Open loop total deviation of IRC48M frequency at low voltage ($VDD=1.71\text{V}-1.89\text{V}$) over full temperature <ul style="list-style-type: none"> Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | 1 |
| $\Delta f_{irc48m_ol_hv}$ | Open loop total deviation of IRC48M frequency at high voltage ($VDD=1.89\text{V}-3.6\text{V}$) over full temperature <ul style="list-style-type: none"> Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | 1 |

Table continues on the next page...

Table 18. IRC48M specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|--|------|-------|-------|----------------|-------|
| $\Delta f_{irc48m_ol_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0 to 85 °C <ul style="list-style-type: none"> Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.5 | ± 1.0 | % f_{irc48m} | 1 |
| Δf_{irc48m_cl} | Closed loop total deviation of IRC48M frequency over voltage and temperature | — | — | ± 0.1 | % f_{host} | 2 |
| J_{cyc_irc48m} | Period Jitter (RMS) | — | 35 | 150 | ps | |
| $t_{irc48mst}$ | Startup time | — | 2 | 3 | μs | 3 |

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma)
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting USB_CLK_RECOVER_IRC_EN[IRC_EN]=1.

3.3.3 Oscillator electrical specifications

3.3.3.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|------|------|------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I_{DDOSC} | Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz | — | 500 | — | nA | 1 |
| I_{DDOSC} | Supply current — high-gain mode (HGO=1) <ul style="list-style-type: none"> 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz | — | 25 | — | μA | 1 |
| | | — | 400 | — | μA | |
| | | — | 500 | — | μA | |
| | | — | 2.5 | — | mA | |
| | | — | 3 | — | mA | |
| | | — | 4 | — | mA | |

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|------|----------|------|------------|-------|
| C_x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C_y | XTAL load capacitance | — | — | — | | 2, 3 |
| R_F | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | M Ω | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | M Ω | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | M Ω | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | M Ω | |
| R_S | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | k Ω | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | k Ω | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | k Ω | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | k Ω | |
| V_{pp} ⁵ | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| f_{osc_lo} | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| f_{ec_extal} | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| t_{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| t_{cst} | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.3.4 32 kHz oscillator electrical characteristics

3.3.4.1 32 kHz oscillator DC electrical specifications

Table 21. 32kHz oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------|----------------------------|------|------|------|------------|
| V_{BAT} | Supply voltage | 1.71 | — | 3.6 | V |
| R_F | Internal feedback resistor | — | 100 | — | M Ω |

Table continues on the next page...

Table 21. 32kHz oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|------------|---|------|------|------|------|
| C_{para} | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| V_{pp}^1 | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------|---|------|--------|-----------|------|-------|
| f_{osc_lo} | Oscillator crystal | — | 32.768 | — | kHz | |
| t_{start} | Crystal start-up time | — | 1000 | — | ms | 1 |
| $f_{ec_extal32}$ | Externally provided input clock frequency | — | 32.768 | — | kHz | 2 |
| $V_{ec_extal32}$ | Externally provided input clock amplitude | 700 | — | V_{BAT} | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

3.4 Memories and memory interfaces

3.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|---------|-------|
| $t_{hvpgrm8}$ | Program Phrase high-voltage time | — | 7.5 | 18 | μ s | |
| $t_{hversscr}$ | Erase Flash Sector high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk512k}$ | Erase Flash Block high-voltage time for 512 KB | — | 416 | 3616 | ms | 1 |

Peripheral operating requirements and behaviors

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|---------|-------|
| $t_{rd1blk512k}$ | Read 1s Block execution time • 512 KB program flash | — | — | 1.8 | ms | |
| $t_{rd1sec4k}$ | Read 1s Section execution time (4 KB flash) | — | — | 100 | μ s | 1 |
| t_{pgmchk} | Program Check execution time | — | — | 95 | μ s | 1 |
| t_{rdsrc} | Read Resource execution time | — | — | 40 | μ s | 1 |
| t_{pgm8} | Program Phrase execution time | — | 90 | 150 | μ s | |
| $t_{ersblk512k}$ | Erase Flash Block execution time • 512 KB program flash | — | 435 | 3700 | ms | 2 |
| t_{ersscr} | Erase Flash Sector execution time | — | 15 | 115 | ms | 2 |
| $t_{rd1alln}$ | Read 1s All Blocks execution time • Program flash only devices | — | — | 3.4 | ms | |
| t_{rdonce} | Read Once execution time | — | — | 30 | μ s | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 70 | — | μ s | |
| t_{ersall} | Erase All Blocks execution time | — | 870 | 7400 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μ s | 1 |
| t_{swap01} | Swap Control execution time • control code 0x01 | — | 200 | — | μ s | |
| t_{swap02} | • control code 0x02 | — | 70 | 150 | μ s | |
| t_{swap04} | • control code 0x04 | — | 70 | 150 | μ s | |
| t_{swap08} | • control code 0x08 | — | — | 30 | μ s | |

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| I_{DD_PGM} | Average current adder during high voltage flash programming operation | — | 3.5 | 7.5 | mA |
| I_{DD_ERS} | Average current adder during high | — | 1.5 | 4.0 | mA |

Table 25. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------------------------|------|------|------|------|
| | voltage flash erase operation | | | | |

3.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|--|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.

3.4.2 EzPort switching specifications

Table 27. EzPort switching specifications

| Num | Description | Min. | Max. | Unit |
|------|---|-------------------------------|--------------------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{\text{SYS}}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{\text{SYS}}/8$ | MHz |
| EP2 | $\overline{\text{EZP_CS}}$ negation to next EZP_CS assertion | $2 \times t_{\text{EZP_CK}}$ | — | ns |
| EP3 | $\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup) | 5 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold) | 5 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 2 | — | ns |
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 5 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid | — | 18 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0 | — | ns |
| EP9 | $\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

Peripheral operating requirements and behaviors

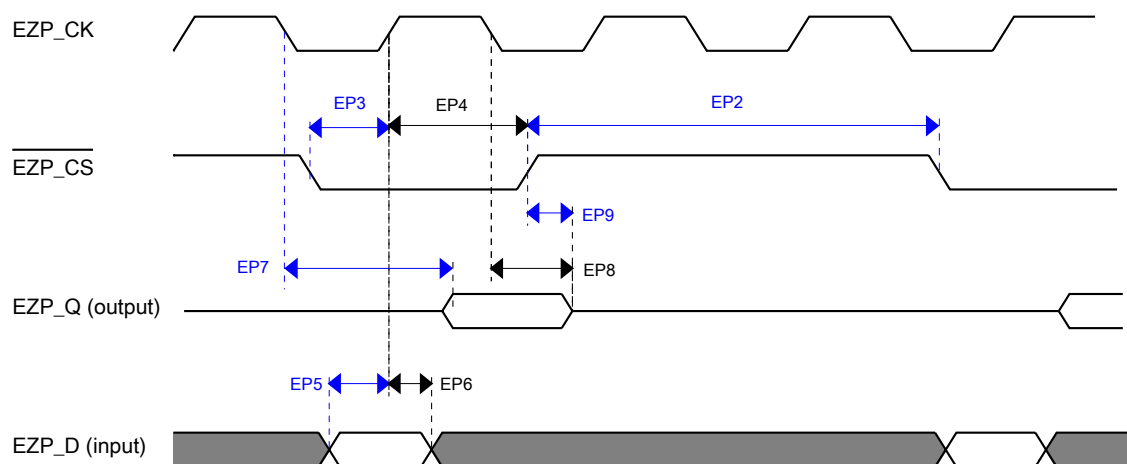


Figure 11. EzPort Timing Diagram

3.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 28. Flexbus limited voltage range switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|------|--------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 20 | — | ns | |
| FB2 | Address, data, and control output valid | — | 11.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0.5 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 8.5 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, $\overline{\text{FB_ALE}}$, and $\overline{\text{FB_TS}}$.

2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 29. Flexbus full voltage range switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|----------|--------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 1/FB_CLK | — | ns | |
| FB2 | Address, data, and control output valid | — | 13.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 15.5 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, $\overline{\text{FB_ALE}}$, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

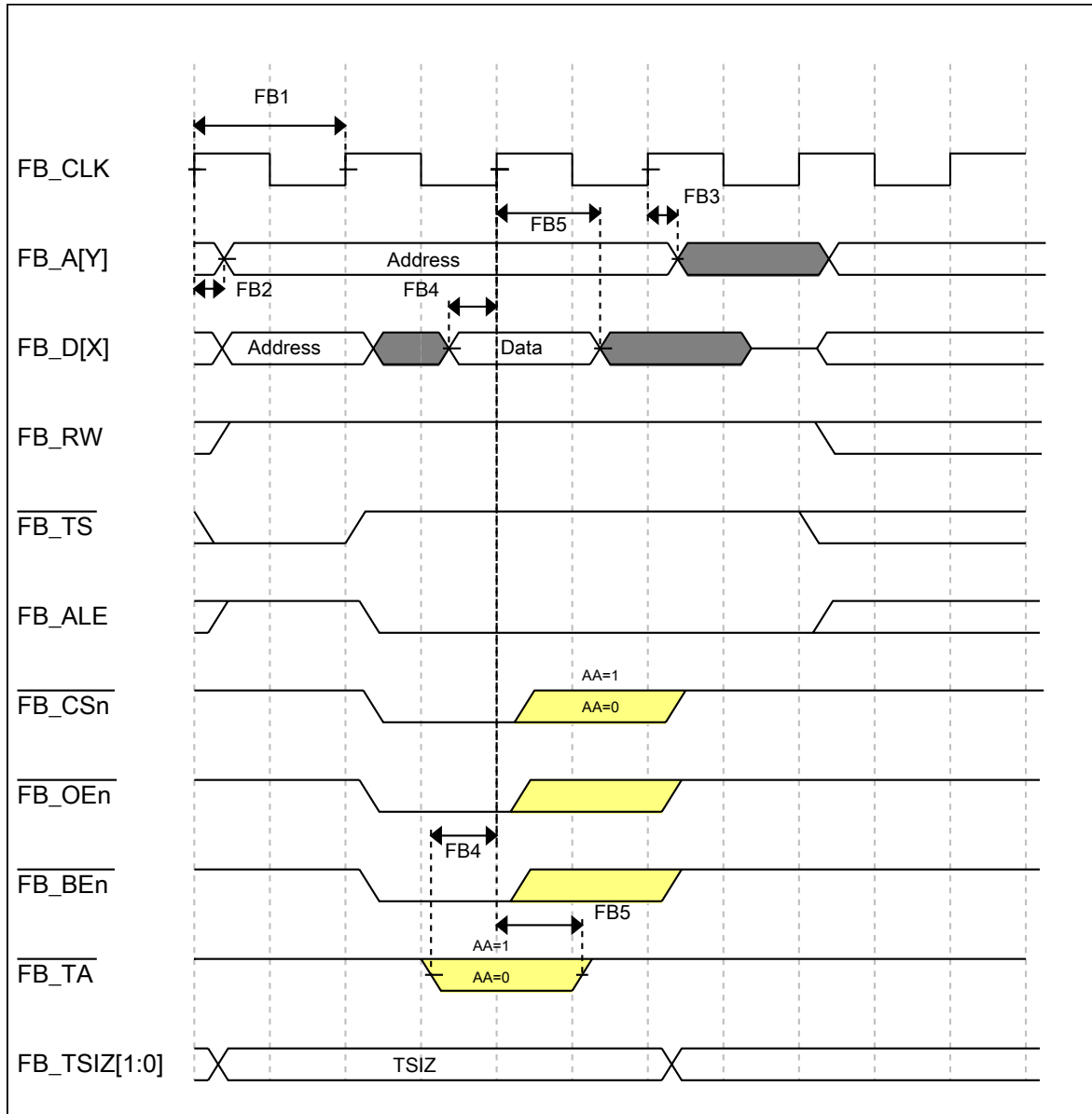


Figure 12. FlexBus read timing diagram

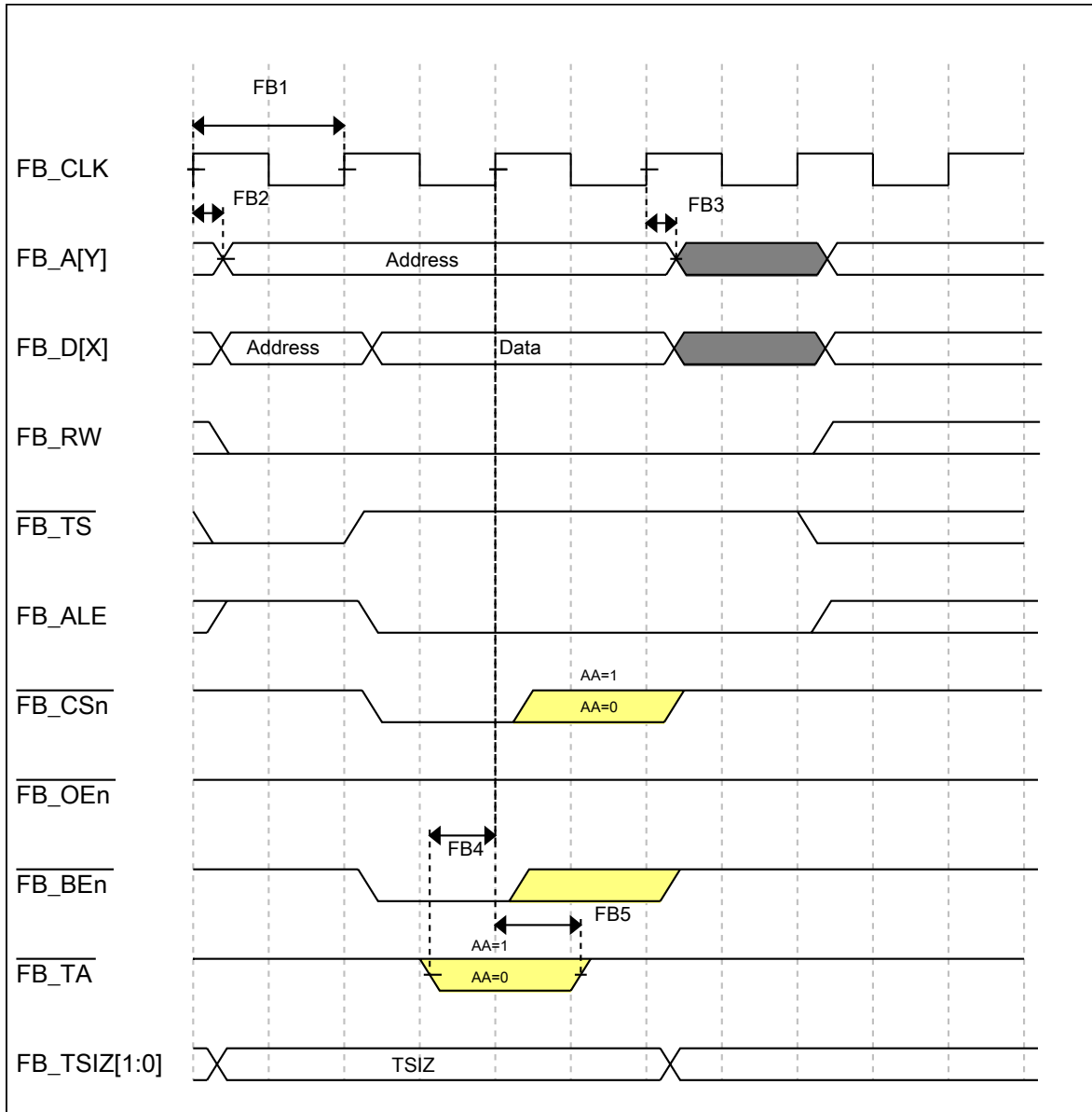


Figure 13. FlexBus write timing diagram

3.5 Security and integrity modules

3.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 30](#) and [Table 31](#) are achievable on the differential pins ADC_X_DP0, ADC_X_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 30. 16-bit ADC operating conditions

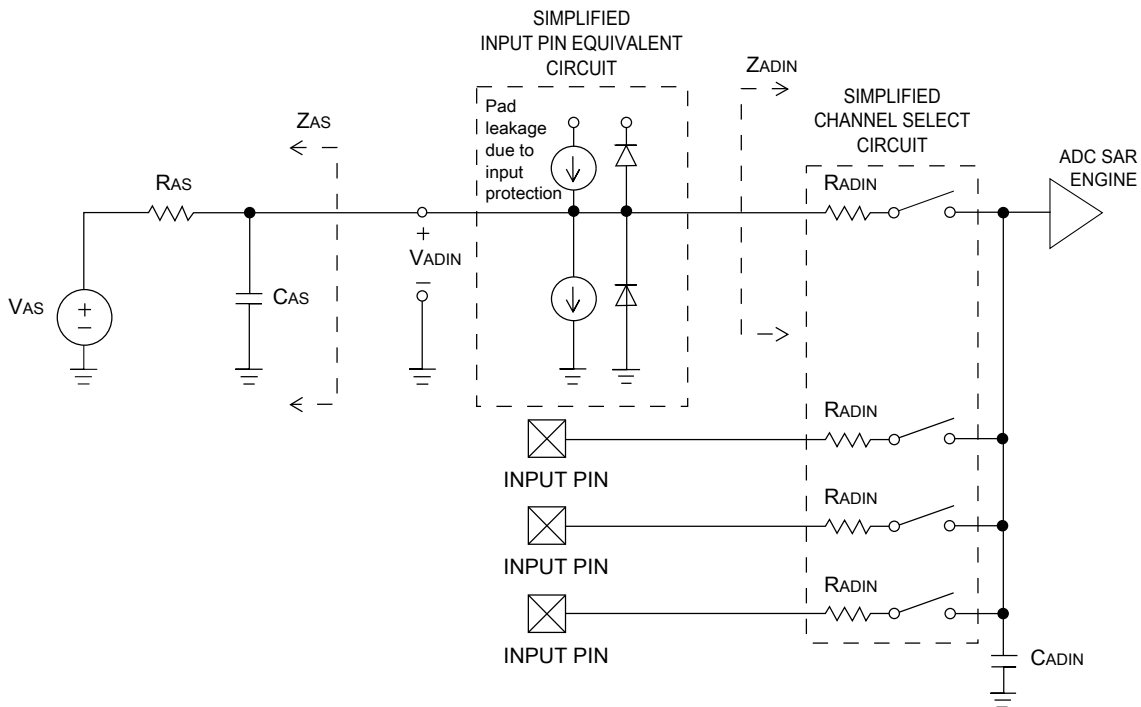
| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|-------------------------------------|---|-------------------|-------------------|-------------------|------|-------------------|
| V _{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| ΔV _{DDA} | Supply voltage | Delta to V _{DD} (V _{DD} – V _{DDA}) | -100 | 0 | +100 | mV | 2 |
| ΔV _{SSA} | Ground voltage | Delta to V _{SS} (V _{SS} – V _{SSA}) | -100 | 0 | +100 | mV | 2 |
| V _{REFH} | ADC reference voltage high | | 1.13 | V _{DDA} | V _{DDA} | V | |
| V _{REFL} | ADC reference voltage low | | V _{SSA} | V _{SSA} | V _{SSA} | V | |
| V _{ADIN} | Input voltage | | V _{REFL} | — | V _{REFH} | V | |
| C _{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes | — | 8 | 10 | pF | |
| R _{ADIN} | Input series resistance | | — | 2 | 5 | kΩ | |
| R _{AS} | Analog source resistance (external) | 13-bit / 12-bit modes f _{ADCK} < 4 MHz | — | — | 5 | kΩ | 3 |
| f _{ADCK} | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| f _{ADCK} | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| C _{rate} | ADC conversion rate | ≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | ksps | 5 |

Table continues on the next page...

Table 30. 16-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------|---------------------|--|--------|-------------------|---------|------|-------|
| C_{rate} | ADC conversion rate | 16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | ksps | 5 |

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $Temp = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8\ \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, $CFG2[ADHSC]$ must be set and $CFG1[ADLPC]$ must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

**Figure 14. ADC input impedance equivalency diagram**

3.6.1.2 16-bit ADC electrical characteristics

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

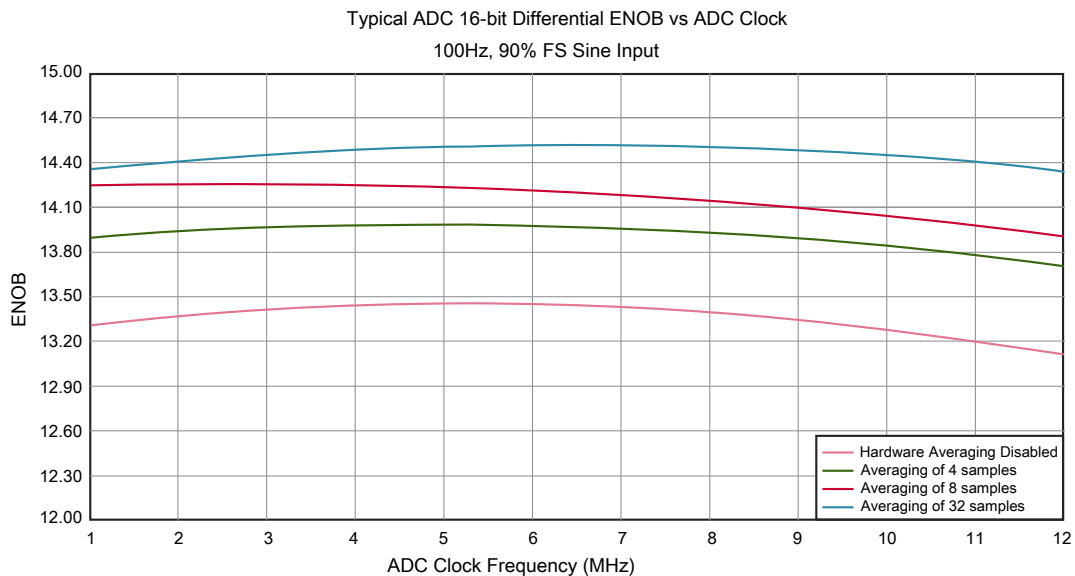
| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|---------------------------------|---|--------------------|-------------------|--------------|------------------|-----------------------------------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f_{ADACK} | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | MHz | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | MHz | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes • <12-bit modes | — — | ±4 ±1.4 | ±6.8 ±2.1 | LSB ⁴ | 5 |
| DNL | Differential non-linearity | • 12-bit modes | — | ±0.7 | -1.1 to +1.9 | LSB ⁴ | 5 |
| | | • <12-bit modes | — | ±0.2 | -0.3 to 0.5 | | |
| INL | Integral non-linearity | • 12-bit modes | — | ±1.0 | -2.7 to +1.9 | LSB ⁴ | 5 |
| | | • <12-bit modes | — | ±0.5 | -0.7 to +0.5 | | |
| E_{FS} | Full-scale error | • 12-bit modes | — | -4 | -5.4 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ |
| | | • <12-bit modes | — | -1.4 | -1.8 | | |
| E_Q | Quantization error | • 16-bit modes | — | -1 to 0 | — | LSB ⁴ | |
| | | • ≤13-bit modes | — | — | ±0.5 | | |
| ENOB | Effective number of bits | 16-bit differential mode | | | | | 6 |
| | | • Avg = 32 | 12.8 | 14.5 | — | bits | |
| | | • Avg = 4 | 11.9 | 13.8 | — | bits | |
| | | 16-bit single-ended mode | | | | | |
| • Avg = 32 | 12.2 | 13.9 | — | bits | | | |
| • Avg = 4 | 11.4 | 13.1 | — | bits | | | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode | | | | dB | 7 |
| | | • Avg = 32 | — | -94 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | — | -85 | — | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | | | | dB | 7 |
| | | • Avg = 32 | 82 | 95 | — | dB | |

Table continues on the next page...

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|--------------|---------------------|---|------------------------|-------------------|------|-------|--|
| | | 16-bit single-ended mode • Avg = 32 | 78 | 90 | | | |
| E_{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 |
| V_{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 |

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- ADC conversion clock < 3 MHz

**Figure 15. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

Peripheral operating requirements and behaviors

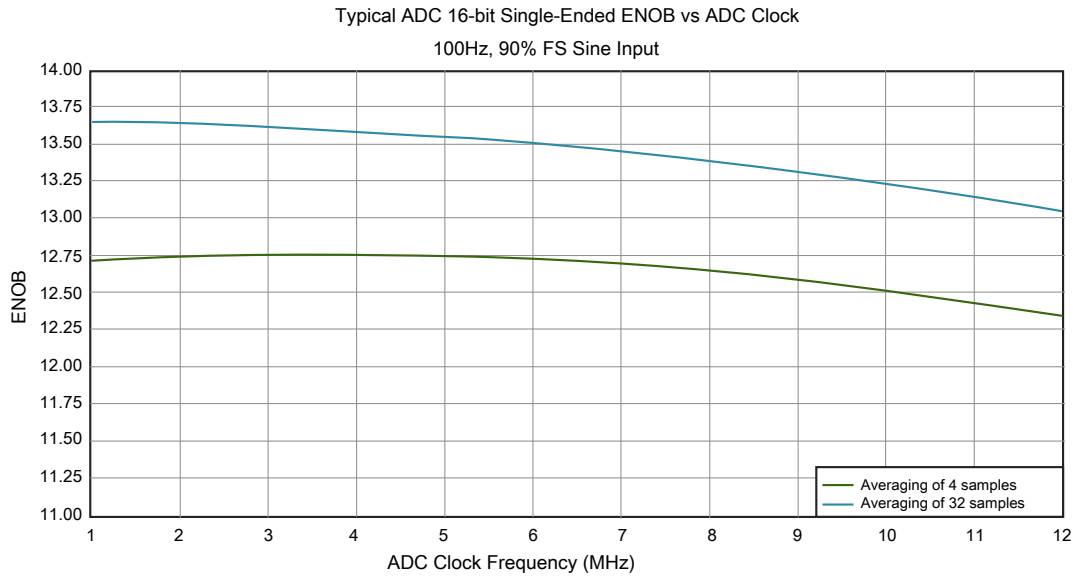


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 32. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|--|----------------|---------------------|----------|------------------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V |
| I_{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μ A |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μ A |
| V_{AIN} | Analog input voltage | $V_{SS} - 0.3$ | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V_H | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 10 20 30 | — | mV |
| V_{CMPOh} | Output high | $V_{DD} - 0.5$ | — | — | V |
| V_{CMPOl} | Output low | — | — | 0.5 | V |
| t_{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μ s |
| I_{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μ A |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

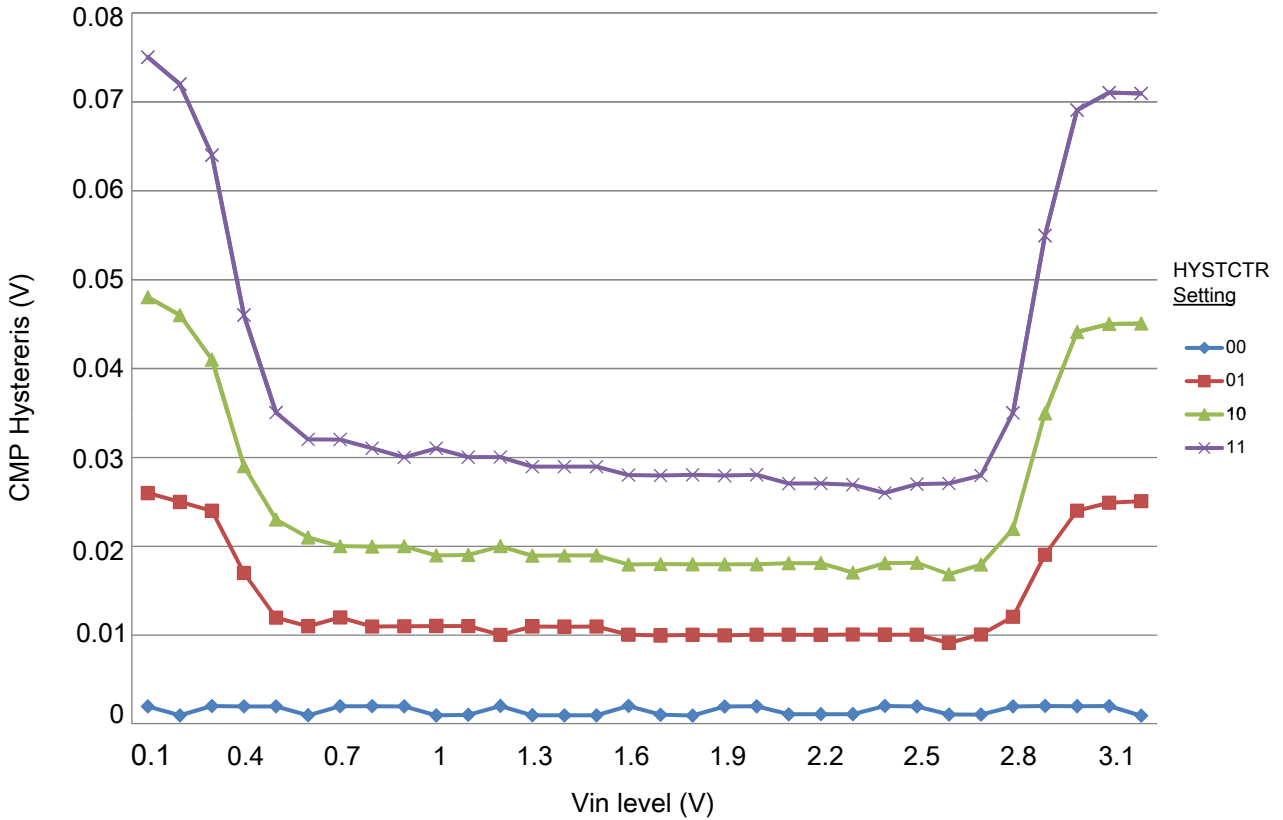


Figure 17. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

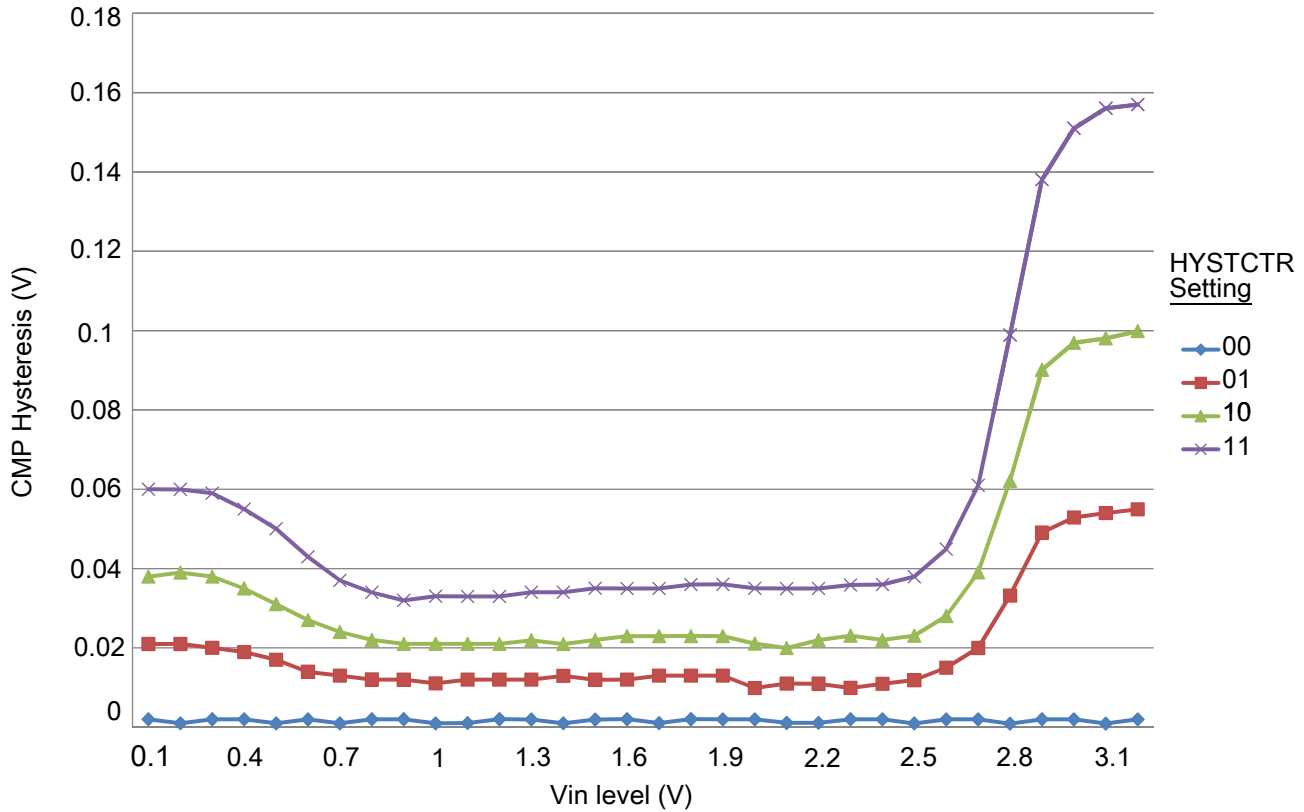


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------|-------------------------|------|------|------|-------|
| V_{DDA} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DACR} | Reference voltage | 1.13 | 3.6 | V | 1 |
| C_L | Output load capacitance | — | 100 | pF | 2 |
| I_L | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------------------|-------------|------------|-------------------------|-------|
| I_{DDA_DACLP} | Supply current — low-power mode | — | — | 150 | μA | |
| I_{DDA_DACHP} | Supply current — high-speed mode | — | — | 700 | μA | |
| t_{DACLP} | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| t_{DACHP} | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | μs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF | $V_{DACR} - 100$ | — | V_{DACR} | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ± 8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR} > 2\text{ V}$ | — | — | ± 1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$ | — | — | ± 1 | LSB | 4 |
| V_{OFFSET} | Offset error | — | ± 0.4 | ± 0.8 | %FSR | 5 |
| E_G | Gain error | — | ± 0.1 | ± 0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$ | 60 | — | 90 | dB | |
| T_{CO} | Temperature coefficient offset voltage | — | 3.7 | — | $\mu\text{V}/\text{C}$ | 6 |
| T_{GE} | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| A_C | Offset aging coefficient | — | — | 100 | $\mu\text{V}/\text{yr}$ | |
| R_{op} | Output resistance (load = 3 k Ω) | — | — | 250 | Ω | |
| SR | Slew rate -80h \rightarrow F7Fh \rightarrow 80h <ul style="list-style-type: none"> • High power (SP_{HP}) • Low power (SP_{LP}) | 1.2 0.05 | 1.7 0.12 | — — | V/ μs | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth <ul style="list-style-type: none"> • High power (SP_{HP}) • Low power (SP_{LP}) | 550 40 | — — | — — | kHz | |

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100\text{ mV}$
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100\text{ mV}$
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100\text{ mV}$ with $V_{DDA} > 2.4\text{ V}$
5. Calculated by a best fit curve from $V_{SS} + 100\text{ mV}$ to $V_{DACR} - 100\text{ mV}$

Peripheral operating requirements and behaviors

- 6. $V_{DDA} = 3.0\text{ V}$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

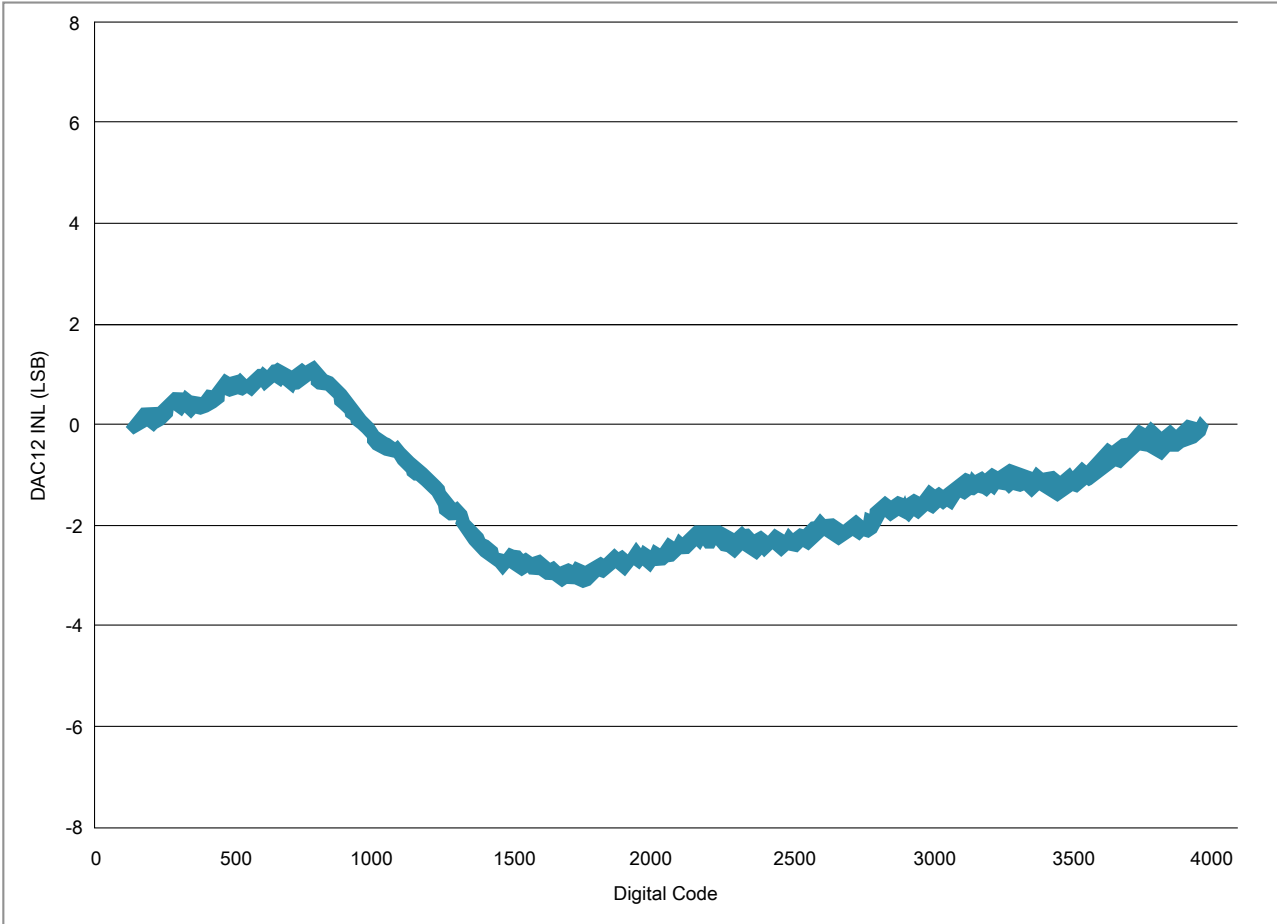


Figure 19. Typical INL error vs. digital code



Figure 20. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 35. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-------------------------|---|------|------|-------|
| V_{DDA} | Supply voltage | 1.71 | 3.6 | V | — |
| T_A | Temperature | Operating temperature range of the device | | °C | — |
| C_L | Output load capacitance | 100 | | nF | 1, 2 |

- C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
- The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 36. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------------|--|--------|-------|--------|---------|-------|
| V_{out} | Voltage reference output with factory trim at nominal V_{DDA} and temperature= 25 °C | 1.192 | 1.195 | 1.198 | V | 1 |
| V_{out} | Voltage reference output with user trim at nominal V_{DDA} and temperature= 25 °C | 1.1945 | 1.195 | 1.1955 | V | 1 |
| V_{step} | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| V_{tdrift} | Temperature drift ($V_{max} - V_{min}$ across the full temperature range) | — | 2 | 15 | mV | 1 |
| I_{bg} | Bandgap only current | — | 60 | 80 | μ A | 1 |
| I_{lp} | Low-power buffer current | — | 180 | 360 | μ A | 1 |
| I_{hp} | High-power buffer current | — | 480 | 960 | mA | 1 |
| ΔV_{LOAD} | Load regulation • current = ± 1.0 mA | — | 200 | — | μ V | 1, 2 |
| T_{stup} | Buffer startup time | — | — | 100 | μ s | — |
| $T_{chop_osc_st\ up}$ | Internal bandgap start-up delay with chop oscillator enabled | — | — | 35 | ms | — |
| V_{vdrift} | Voltage drift ($V_{max} - V_{min}$ across the full voltage range) | — | 0.5 | 2 | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 37. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| T_A | Temperature | 0 | 50 | °C | — |

Table 38. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--|-------|-------|------|-------|
| V_{out} | Voltage reference output with factory trim | 1.173 | 1.225 | V | — |

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.8.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 39. MII signal switching specifications

| Symbol | Description | Min. | Max. | Unit |
|--------|---------------------------------------|------|------|--------------|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

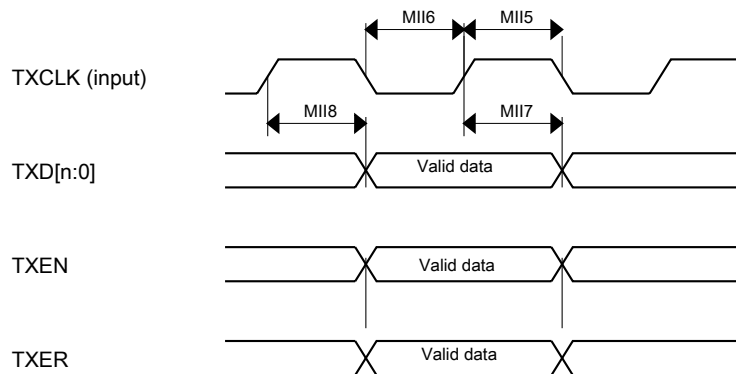


Figure 21. RMI/MII transmit signal timing diagram

Peripheral operating requirements and behaviors

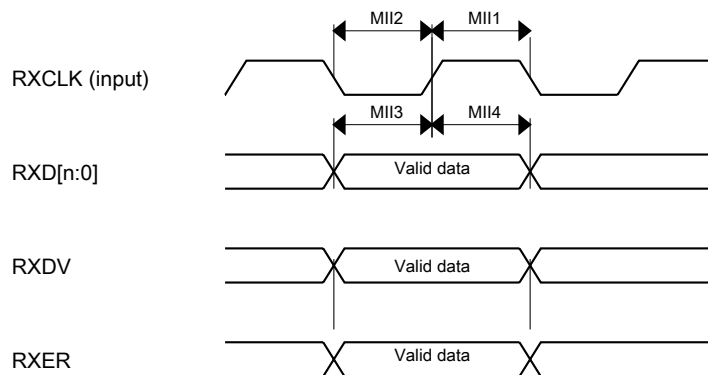


Figure 22. RMII/MII receive signal timing diagram

3.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 40. RMII signal switching specifications

| Num | Description | Min. | Max. | Unit |
|-------|---|------|------|-----------------|
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| RMII1 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| RMII2 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| RMII3 | RXD[1:0], CRS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| RMII4 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 4 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

3.8.1.3 MDIO serial management timing specifications

Table 41. MDIO serial management channel signal timing

| Num | Characteristic | Symbol | Min | Max | Unit |
|-----|----------------------------|-----------|-----|-----|-------------|
| E10 | MDC cycle time | t_{MDC} | 400 | — | ns |
| E11 | MDC pulse width | | 40 | 60 | % t_{MDC} |
| E12 | MDC to MDIO output valid | | — | 375 | ns |
| E13 | MDC to MDIO output invalid | | 25 | — | ns |
| E14 | MDIO input to MDC setup | | 10 | — | ns |
| E15 | MDIO input to MDC hold | | 0 | — | ns |

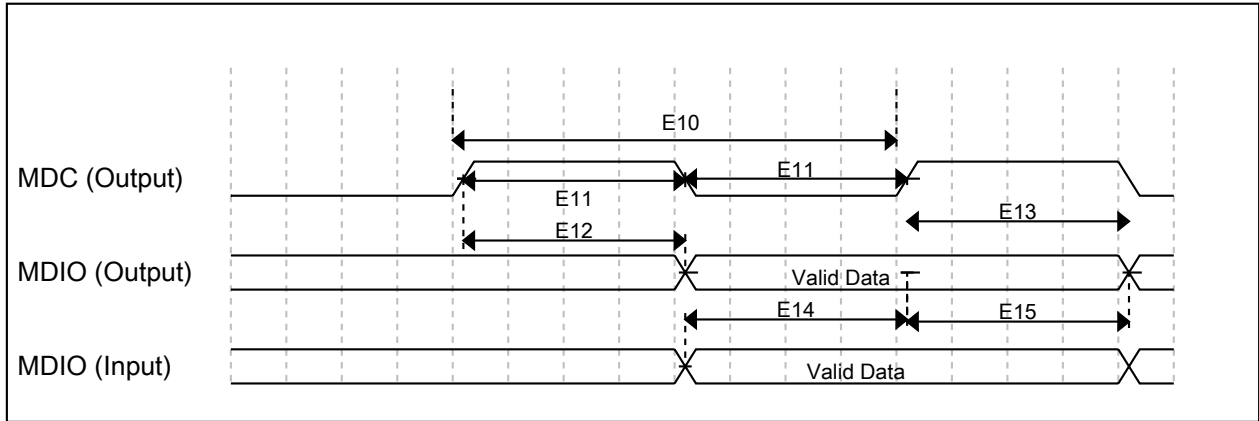


Figure 23. MDIO serial management channel timing diagram

3.8.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGPLLCLK meets the USB jitter specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter specifications for certification.

The IRC48M meets the USB jitter specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB jitter specifications for certification in Host mode operation.

3.8.3 USB DCD electrical specifications

Table 42. USB0 DCD electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------------------|---|------|------|------|---------|
| V _{DP_SRC} | USB_DP source voltage (up to 250 μ A) | 0.5 | — | 0.7 | V |
| V _{LGC} | Threshold voltage for logic high | 0.8 | — | 2.0 | V |
| I _{DP_SRC} | USB_DP source current | 7 | 10 | 13 | μ A |
| I _{DM_SINK} | USB_DM sink current | 50 | 100 | 150 | μ A |

Table continues on the next page...

Table 42. USB0 DCD electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------------------|--|-------|------|------|------|
| R _{DM_DWN} | D- pulldown resistance for data pin contact detect | 14.25 | — | 24.8 | kΩ |
| V _{DAT_REF} | Data detect voltage | 0.25 | 0.33 | 0.4 | V |

3.8.4 USB VREG electrical specifications

Table 43. USB VREG electrical specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-----------------------|---|------|-------------------|------|------|-------|
| V _{REGIN} | Input supply voltage | 2.7 | — | 5.5 | V | |
| I _{DDon} | Quiescent current — Run mode, load current equal zero, input supply (V _{REGIN}) > 3.6 V | — | 125 | 186 | μA | |
| I _{DDstby} | Quiescent current — Standby mode, load current equal zero | — | 1.1 | 10 | μA | |
| I _{DDoff} | Quiescent current — Shutdown mode <ul style="list-style-type: none"> V_{REGIN} = 5.0 V and temperature=25 °C Across operating voltage and temperature | — | 650 | — | nA | |
| | | — | — | 4 | μA | |
| I _{LOADrun} | Maximum load current — Run mode | — | — | 120 | mA | |
| I _{LOADstby} | Maximum load current — Standby mode | — | — | 1 | mA | |
| V _{Reg33out} | Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V <ul style="list-style-type: none"> Run mode Standby mode | 3 | 3.3 | 3.6 | V | |
| | | 2.1 | 2.8 | 3.6 | V | |
| V _{Reg33out} | Regulator output voltage — Input supply (V _{REGIN}) < 3.6 V, pass-through mode | 2.1 | — | 3.6 | V | 2 |
| C _{OUT} | External output capacitor | 1.76 | 2.2 | 8.16 | μF | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | mΩ | |
| I _{LIM} | Short circuit current | — | 290 | — | mA | |

1. Typical values assume V_{REGIN} = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.5 CAN switching specifications

See [General switching specifications](#).

3.8.6 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 44. Master mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------------------------------|---------------------------------|--------------------------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 30 | MHz | |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{\text{BUS}}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{\text{SCK}}/2) - 2$ | $(t_{\text{SCK}}/2) + 2$ | ns | |
| DS3 | DSPI_PCSn valid to DSPI_SCK delay | $(t_{\text{BUS}} \times 2) - 2$ | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{\text{BUS}} \times 2) - 2$ | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 15 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

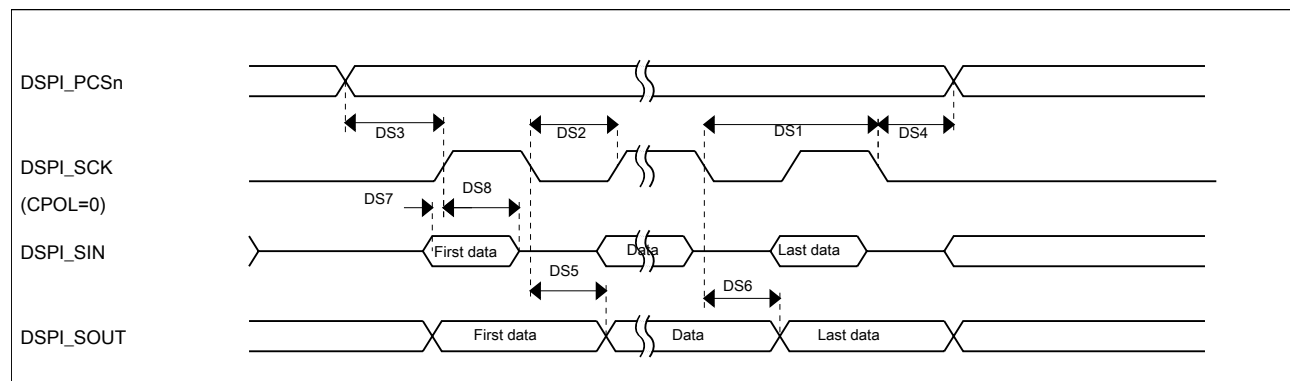


Figure 24. DSPI classic SPI timing — master mode

Table 45. Slave mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit |
|-----|------------------------|------|-----------------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 15 ¹ | MHz |

Table continues on the next page...

Table 45. Slave mode DSPI timing (limited voltage range) (continued)

| Num | Description | Min. | Max. | Unit |
|------|--|---------------------------|---------------------------|------|
| DS9 | DSPI_SCK input cycle time | 4 x t _{BUS} | — | ns |
| DS10 | DSPI_SCK input high/low time | (t _{SCK} /2) - 2 | (t _{SCK} /2) + 2 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 14 | ns |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 14 | ns |

- The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz

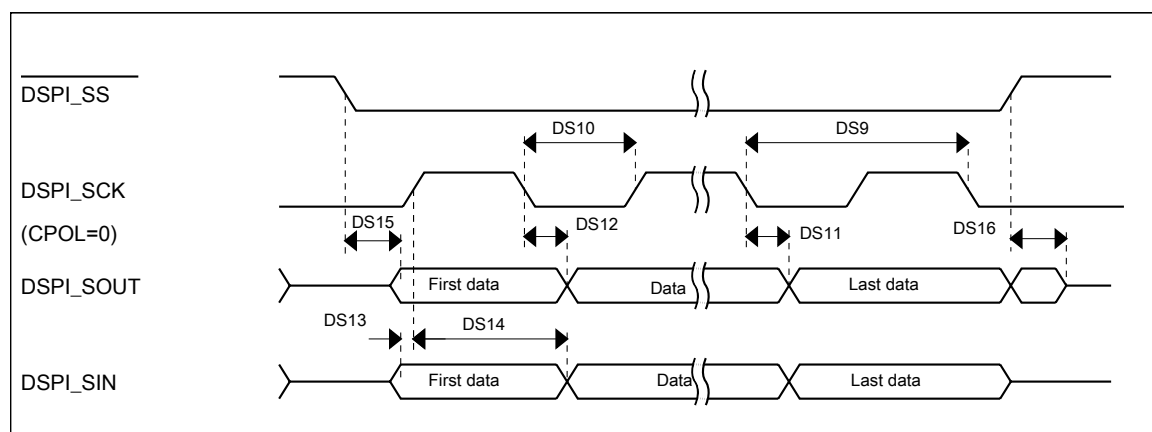


Figure 25. DSPI classic SPI timing — slave mode

3.8.7 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 46. Master mode DSPI timing (full voltage range)

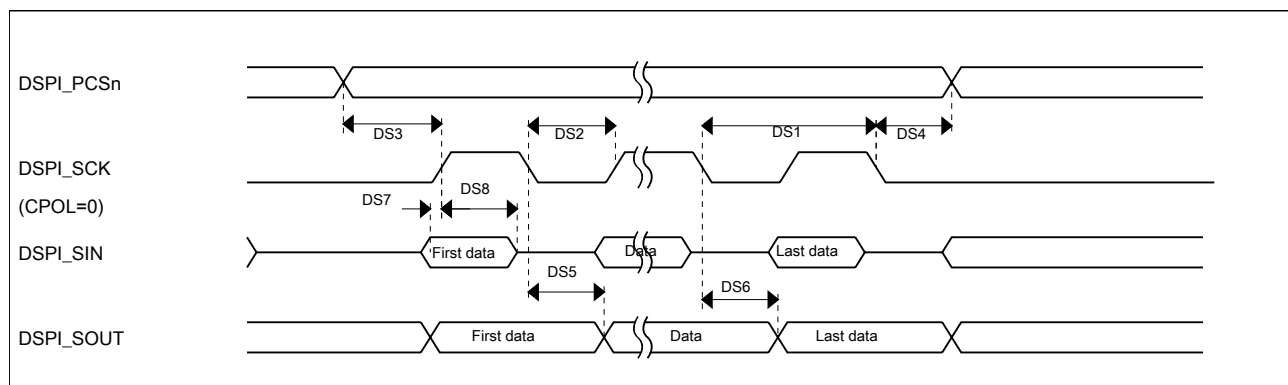
| Num | Description | Min. | Max. | Unit | Notes |
|-----|------------------------|------|------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 15 | MHz | |

Table continues on the next page...

Table 46. Master mode DSPI timing (full voltage range) (continued)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------------------------------|--------------------------|-------------------|------|-------|
| DS1 | DSPI_SCK output cycle time | $4 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK/2}) - 4$ | $(t_{SCK/2}) + 4$ | ns | |
| DS3 | DSPI_PCSn valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 4$ | — | ns | 2 |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{BUS} \times 2) - 4$ | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -4.5 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 21 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 26. DSPI classic SPI timing — master mode****Table 47. Slave mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|------|--|--------------------|-------------------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 7.5 | MHz |
| DS9 | DSPI_SCK input cycle time | $8 \times t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK/2}) - 4$ | $(t_{SCK/2}) + 4$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 23.5 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 4 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{DSPI_SS}$ active to DSPI_SOUT driven | — | 21 | ns |
| DS16 | $\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven | — | 19 | ns |

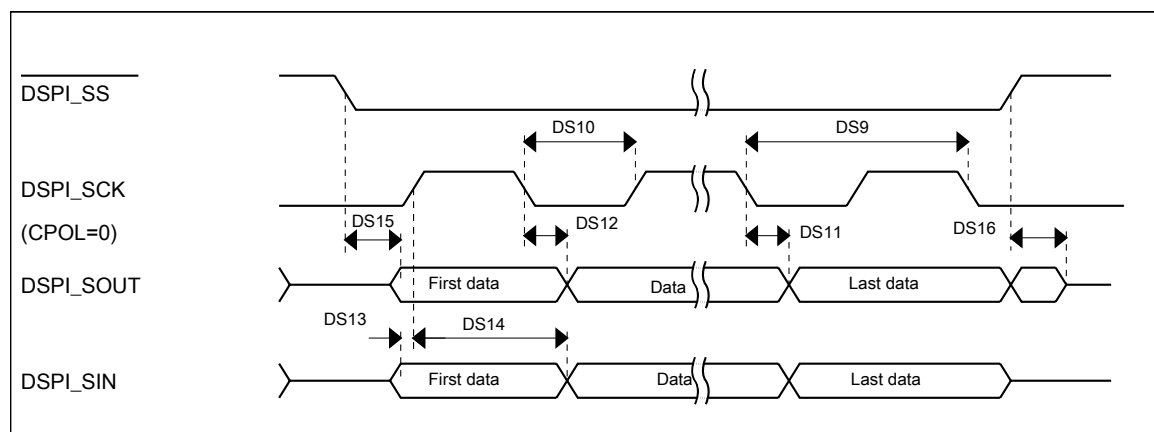


Figure 27. DSPI classic SPI timing — slave mode

3.8.8 Inter-Integrated Circuit Interface (I²C) timing

Table 48. I²C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|-----------------------|------------------|-------------------|-------------------------------------|------------------|------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f _{SCL} | 0 | 100 | 0 | 400 ¹ | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD} ; STA | 4 | — | 0.6 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 4.7 | — | 1.25 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 4 | — | 0.6 | — | μs |
| Set-up time for a repeated START condition | t _{SU} ; STA | 4.7 | — | 0.6 | — | μs |
| Data hold time for I ² C bus devices | t _{HD} ; DAT | 0 ² | 3.45 ³ | 0 ⁴ | 0.9 ² | μs |
| Data set-up time | t _{SU} ; DAT | 250 ⁵ | — | 100 ³⁶ | — | ns |
| Rise time of SDA and SCL signals | t _r | — | 1000 | 20 + 0.1C _b ⁷ | 300 | ns |
| Fall time of SDA and SCL signals | t _f | — | 300 | 20 + 0.1C _b ⁶ | 300 | ns |
| Set-up time for STOP condition | t _{SU} ; STO | 4 | — | 0.6 | — | μs |
| Bus free time between STOP and START condition | t _{BUF} | 4.7 | — | 1.3 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t _{SP} | N/A | N/A | 0 | 50 | ns |

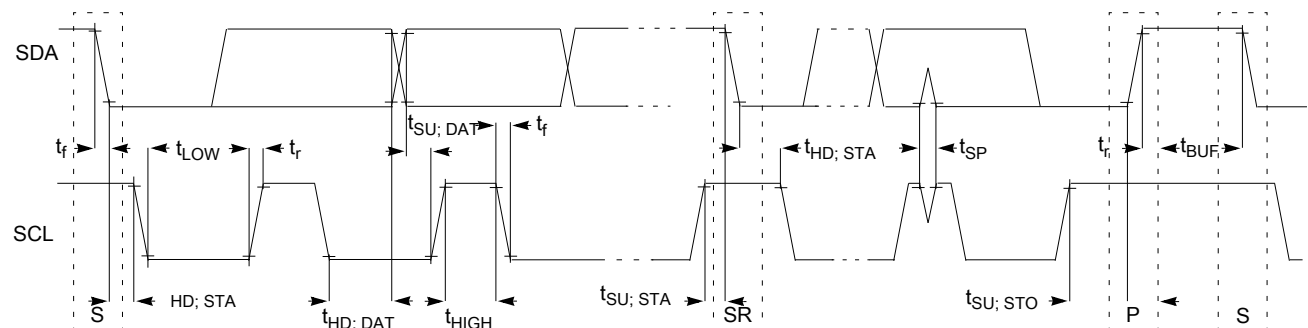
1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.

- A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{\text{SU; DAT}} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{\text{rmax}} + t_{\text{SU; DAT}} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
- C_b = total capacitance of the one bus line in pF.

Table 49. I²C 1 Mbps timing

| Characteristic | Symbol | Minimum | Maximum | Unit |
|--|----------------------|-----------------|----------------|---------------|
| SCL Clock Frequency | f_{SCL} | 0 | 1 ¹ | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{\text{HD; STA}}$ | 0.26 | — | μs |
| LOW period of the SCL clock | t_{LOW} | 0.5 | — | μs |
| HIGH period of the SCL clock | t_{HIGH} | 0.26 | — | μs |
| Set-up time for a repeated START condition | $t_{\text{SU; STA}}$ | 0.26 | — | μs |
| Data hold time for I ² C bus devices | $t_{\text{HD; DAT}}$ | 0 | — | μs |
| Data set-up time | $t_{\text{SU; DAT}}$ | 50 | — | ns |
| Rise time of SDA and SCL signals | t_r | $20 + 0.1C_b^2$ | 120 | ns |
| Fall time of SDA and SCL signals | t_f | $20 + 0.1C_b^2$ | 120 | ns |
| Set-up time for STOP condition | $t_{\text{SU; STO}}$ | 0.26 | — | μs |
| Bus free time between STOP and START condition | t_{BUF} | 0.5 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t_{SP} | 0 | 50 | ns |

- The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
- C_b = total capacitance of the one bus line in pF.

**Figure 28. Timing definition for devices on the I²C bus**

3.8.9 UART switching specifications

See [General switching specifications](#).

3.8.10 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 50. SDHC switching specifications

| Num | Symbol | Description | Min. | Max. | Unit |
|---|------------------|---|------|-------|------|
| | | Operating voltage | 1.71 | 3.6 | V |
| Card input clock | | | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed\high speed) | 0 | 25\50 | MHz |
| | fpp | Clock frequency (MMC full speed\high speed) | 0 | 20\50 | MHz |
| | f _{OD} | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | t _{WL} | Clock low time | 7 | — | ns |
| SD3 | t _{WH} | Clock high time | 7 | — | ns |
| SD4 | t _{TLH} | Clock rise time | — | 3 | ns |
| SD5 | t _{THL} | Clock fall time | — | 3 | ns |
| SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD6 | t _{OD} | SDHC output delay (output valid) | -5 | 8.3 | ns |
| SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD7 | t _{ISU} | SDHC input setup time | 5.5 | — | ns |
| SD8 | t _{IH} | SDHC input hold time | 0 | — | ns |

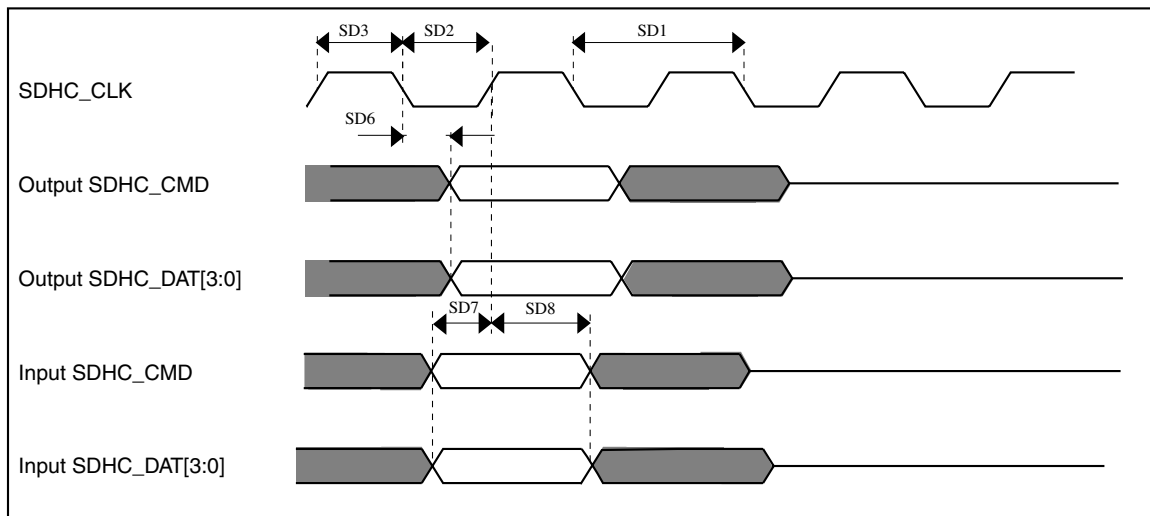


Figure 29. SDHC timing

3.8.11 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 51. I²S master mode timing

| Num | Description | Min. | Max. | Unit |
|-----|--|------|------|-------------|
| | Operating voltage | 2.7 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_BCLK cycle time | 80 | — | ns |
| S4 | I2S_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_BCLK to I2S_FS output valid | — | 15 | ns |
| S6 | I2S_BCLK to I2S_FS output invalid | 0 | — | ns |
| S7 | I2S_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_FS input setup before I2S_BCLK | 17 | — | ns |
| S10 | I2S_RXD/I2S_FS input hold after I2S_BCLK | 0 | — | ns |

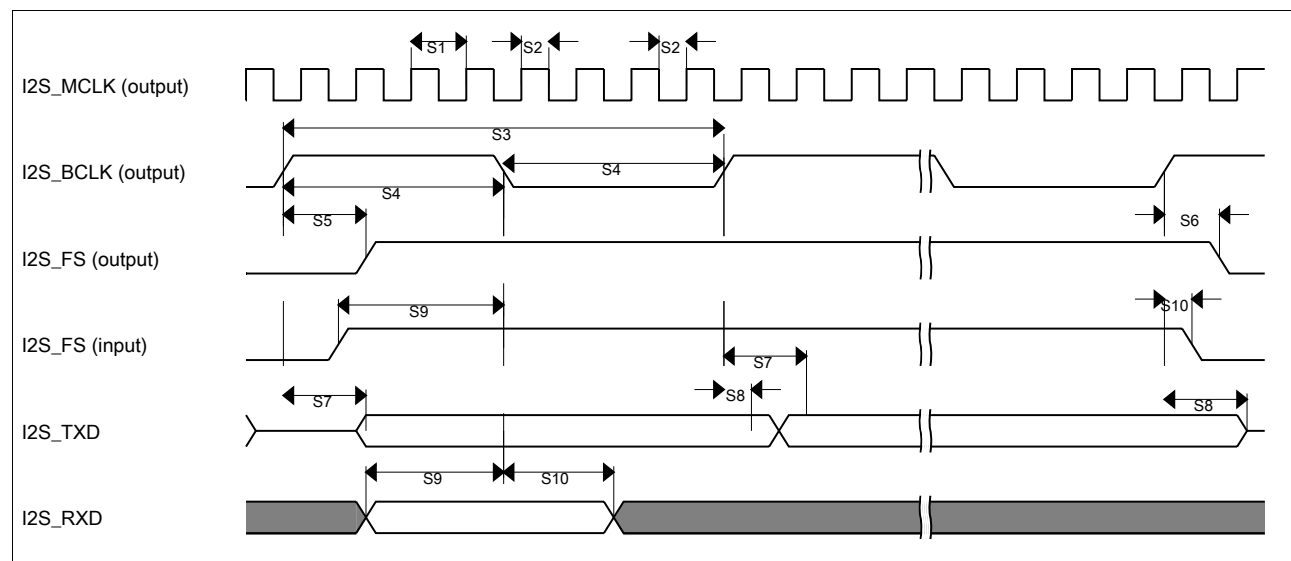


Figure 30. I²S timing — master mode

Table 52. I²S slave mode timing

| Num | Description | Min. | Max. | Unit |
|-----|--|------|------|-------------|
| | Operating voltage | 2.7 | 3.6 | V |
| S11 | I2S_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_FS input setup before I2S_BCLK | 5 | — | ns |
| S14 | I2S_FS input hold after I2S_BCLK | 2 | — | ns |
| S15 | I2S_BCLK to I2S_TXD/I2S_FS output valid | — | 19.5 | ns |
| S16 | I2S_BCLK to I2S_TXD/I2S_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_BCLK | 5 | — | ns |
| S18 | I2S_RXD hold after I2S_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | | 21 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

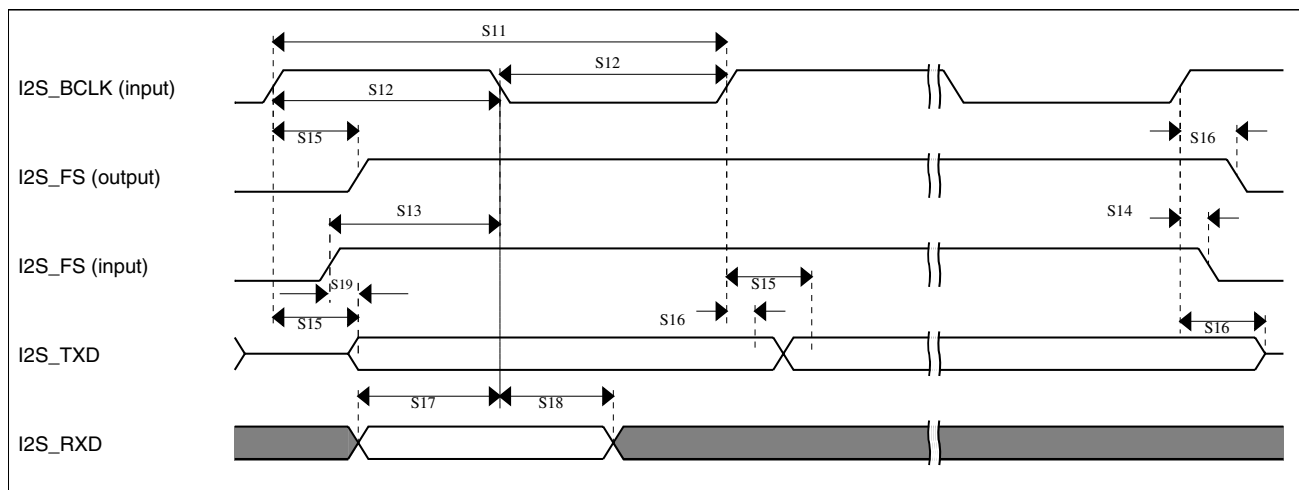


Figure 31. I²S timing — slave modes

3.8.11.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

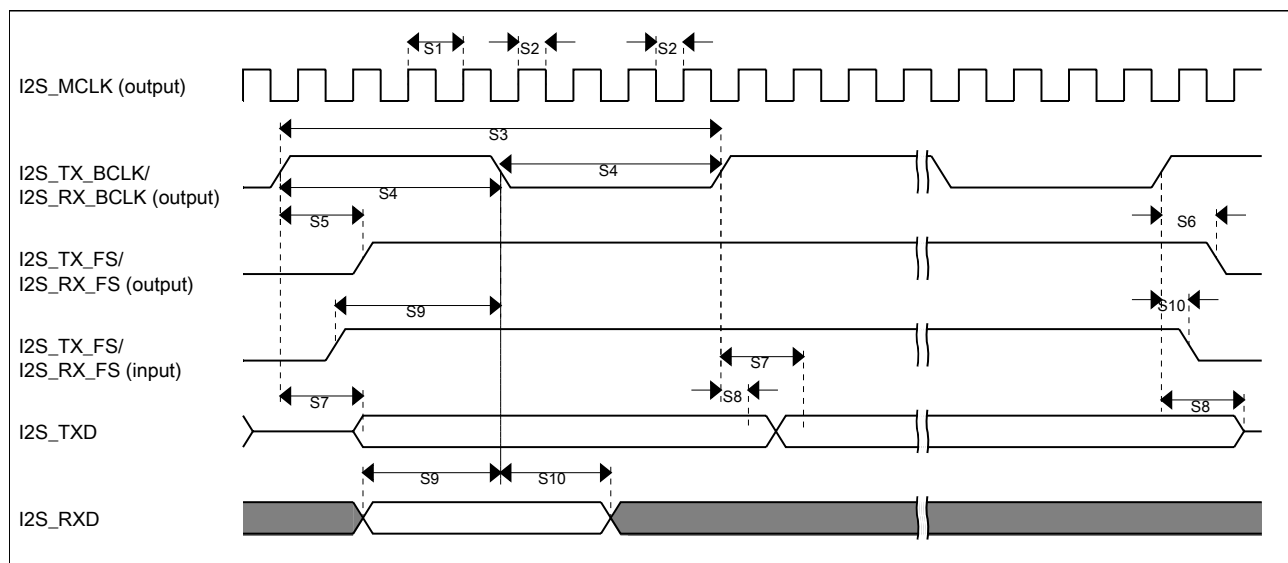
Table 53. I2S/SAI master mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK (as an input) pulse width high/low | 45% | 55% | MCLK period |

Table continues on the next page...

Table 53. I2S/SAI master mode timing (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | -1 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 22.5 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

**Figure 32. I2S/SAI timing — master modes****Table 54. I2S/SAI slave mode timing**

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 7 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |

Table continues on the next page...

Table 54. I2S/SAI slave mode timing (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|------|
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 25.5 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 3 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 5.8 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 25 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

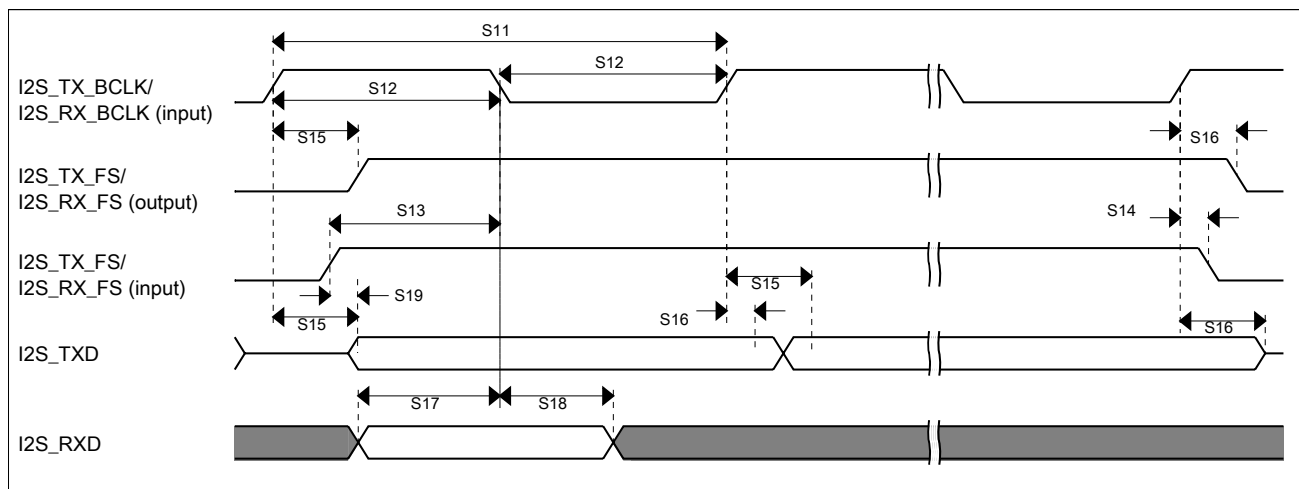


Figure 33. I2S/SAI timing — slave modes

3.8.11.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

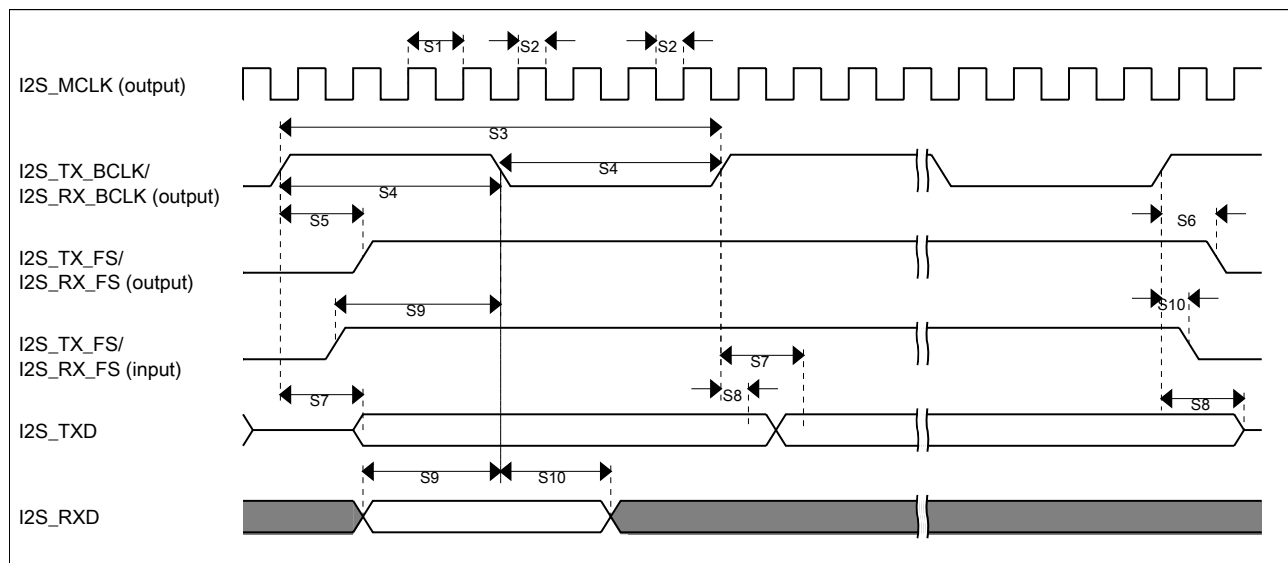
Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |

Table continues on the next page...

Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|------|
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | — | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 45 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

**Figure 34. I2S/SAI timing — master modes****Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 11 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | — | ns |

Table continues on the next page...

Dimensions

Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|------|
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 11 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 72 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

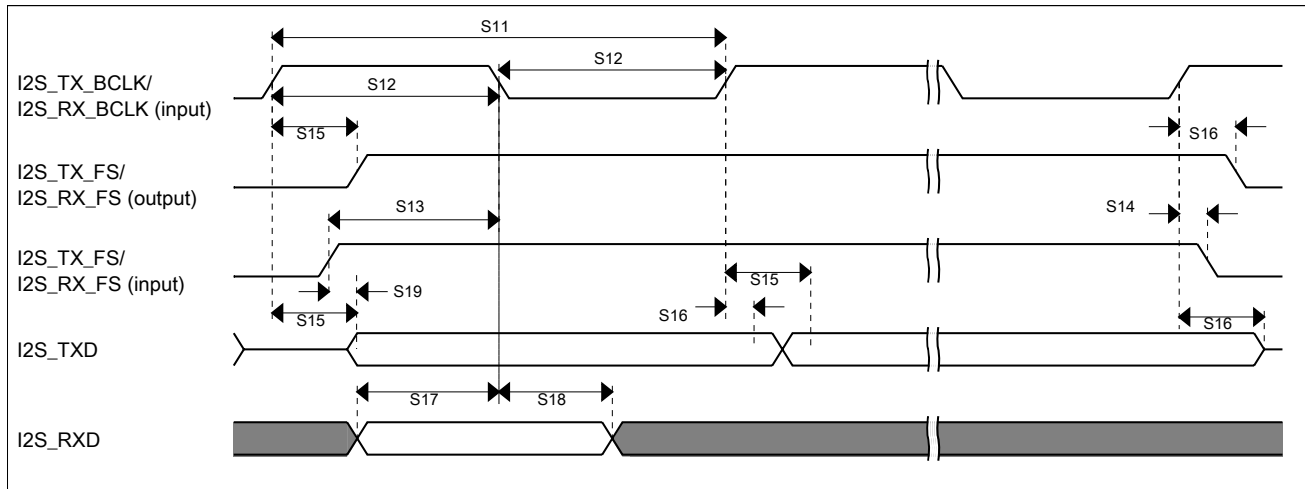


Figure 35. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 144-pin LQFP | 98ASS23177W |
| 144-pin MAPBGA | 98ASA00222D |

5 Pinout

5.1 K63 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|----------|-------------|--|--|--|------------------|-----------|-------------|------------|--------------|----------|-------------|--------|
| — | M3 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | | | | | | | | |
| — | L3 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | | | | | | | | |
| — | L4 | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | | | | | | | | |
| — | J4 | TAMPER3 | TAMPER3 | TAMPER3 | | | | | | | | |
| — | H4 | TAMPER4 | TAMPER4 | TAMPER4 | | | | | | | | |
| — | M4 | TAMPER5 | TAMPER5 | TAMPER5 | | | | | | | | |
| — | M5 | NC | NC | NC | | | | | | | | |
| — | A10 | NC | NC | NC | | | | | | | | |
| — | B10 | NC | NC | NC | | | | | | | | |
| — | C10 | NC | NC | NC | | | | | | | | |
| 1 | D3 | PTE0 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | SDHC0_D1 | TRACE_CLKOUT | I2C1_SDA | RTC_CLKOUT | |
| 2 | D2 | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | SDHC0_D0 | TRACE_D3 | I2C1_SCL | SPI1_SIN | |
| 3 | D1 | PTE2/ LLWU_P1 | ADC0_DP2/ ADC1_SE6a | ADC0_DP2/ ADC1_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_CTS_b | SDHC0_DCLK | TRACE_D2 | | | |
| 4 | E4 | PTE3 | ADC0_DM2/ ADC1_SE7a | ADC0_DM2/ ADC1_SE7a | PTE3 | SPI1_SIN | UART1_RTS_b | SDHC0_CMD | TRACE_D1 | | SPI1_SOUT | |
| 5 | E5 | VDD | VDD | VDD | | | | | | | | |
| 6 | F6 | VSS | VSS | VSS | | | | | | | | |
| 7 | E3 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | SDHC0_D3 | TRACE_D0 | | | |
| 8 | E2 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | SDHC0_D2 | | FTM3_CH0 | | |
| 9 | E1 | PTE6 | DISABLED | | PTE6 | SPI1_PCS3 | UART3_CTS_b | I2S0_MCLK | | FTM3_CH1 | USB_SOF_OUT | |

Pinout

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|----------|-------------|--------------------------------------|--------------------------------------|--------------------------------------|-------|-----------|-------------|--------------|------|----------|------|--------|
| 10 | F4 | PTE7 | DISABLED | | PTE7 | | UART3_RTS_b | I2S0_RXD0 | | FTM3_CH2 | | |
| 11 | F3 | PTE8 | DISABLED | | PTE8 | I2S0_RXD1 | UART5_TX | I2S0_RX_FS | | FTM3_CH3 | | |
| 12 | F2 | PTE9 | DISABLED | | PTE9 | I2S0_TXD1 | UART5_RX | I2S0_RX_BCLK | | FTM3_CH4 | | |
| 13 | F1 | PTE10 | DISABLED | | PTE10 | | UART5_CTS_b | I2S0_TXD0 | | FTM3_CH5 | | |
| 14 | G4 | PTE11 | DISABLED | | PTE11 | | UART5_RTS_b | I2S0_TX_FS | | FTM3_CH6 | | |
| 15 | G3 | PTE12 | DISABLED | | PTE12 | | | I2S0_TX_BCLK | | FTM3_CH7 | | |
| 16 | E6 | VDD | VDD | VDD | | | | | | | | |
| 17 | F7 | VSS | VSS | VSS | | | | | | | | |
| 18 | H3 | VSS | VSS | VSS | | | | | | | | |
| 19 | H1 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |
| 20 | H2 | USB0_DM | USB0_DM | USB0_DM | | | | | | | | |
| 21 | G1 | VOUT33 | VOUT33 | VOUT33 | | | | | | | | |
| 22 | G2 | VREGIN | VREGIN | VREGIN | | | | | | | | |
| 23 | J1 | ADC0_DP1 | ADC0_DP1 | ADC0_DP1 | | | | | | | | |
| 24 | J2 | ADC0_DM1 | ADC0_DM1 | ADC0_DM1 | | | | | | | | |
| 25 | K1 | ADC1_DP1 | ADC1_DP1 | ADC1_DP1 | | | | | | | | |
| 26 | K2 | ADC1_DM1 | ADC1_DM1 | ADC1_DM1 | | | | | | | | |
| 27 | L1 | ADC0_DP0/ ADC1_DP3 | ADC0_DP0/ ADC1_DP3 | ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| 28 | L2 | ADC0_DM0/ ADC1_DM3 | ADC0_DM0/ ADC1_DM3 | ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| 29 | M1 | ADC1_DP0/ ADC0_DP3 | ADC1_DP0/ ADC0_DP3 | ADC1_DP0/ ADC0_DP3 | | | | | | | | |
| 30 | M2 | ADC1_DM0/ ADC0_DM3 | ADC1_DM0/ ADC0_DM3 | ADC1_DM0/ ADC0_DM3 | | | | | | | | |
| 31 | H5 | VDDA | VDDA | VDDA | | | | | | | | |
| 32 | G5 | VREFH | VREFH | VREFH | | | | | | | | |
| 33 | G6 | VREFL | VREFL | VREFL | | | | | | | | |
| 34 | H6 | VSSA | VSSA | VSSA | | | | | | | | |
| 35 | K3 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | | | | | | | | |
| 36 | J3 | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | | | | | | | | |
| 37 | L5 | TAMPER0/ RTC_ WAKEUP_B | TAMPER0/ RTC_ WAKEUP_B | TAMPER0/ RTC_ WAKEUP_B | | | | | | | | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|----------|-------------|------------------|-----------------------------------|-----------|------------------|-----------------------------|-------------|-------------------------|----------|--------------|------------------------|----------|
| 38 | K5 | TAMPER1 | TAMPER1 | TAMPER1 | | | | | | | | |
| 39 | K4 | TAMPER2 | TAMPER2 | TAMPER2 | | | | | | | | |
| 40 | M7 | XTAL32 | XTAL32 | XTAL32 | | | | | | | | |
| 41 | M6 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | | |
| 42 | L6 | VBAT | VBAT | VBAT | | | | | | | | |
| 43 | — | VDD | VDD | VDD | | | | | | | | |
| 44 | — | VSS | VSS | VSS | | | | | | | | |
| 45 | — | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | | UART4_TX | | I2C0_SCL | EWM_OUT_b | | |
| 46 | — | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | | UART4_RX | | I2C0_SDA | EWM_IN | | |
| 47 | — | PTE26 | DISABLED | | PTE26 | ENET_1588_CLKIN | UART4_CTS_b | | | RTC_CLKOUT | USB_CLKIN | |
| 48 | — | PTE27 | DISABLED | | PTE27 | | UART4_RTS_b | | | | | |
| 49 | — | PTE28 | DISABLED | | PTE28 | | | | | | | |
| 50 | J5 | PTA0 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | | PTA0 | UART0_CTS_b/ UART0_COL_b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| 51 | J6 | PTA1 | JTAG_TDI/ EZP_DI | | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| 52 | K6 | PTA2 | JTAG_TDO/ TRACE_SWO/ EZP_DO | | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_SWO | EZP_DO |
| 53 | K7 | PTA3 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_RTS_b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| 54 | L7 | PTA4/ LLWU_P3 | NMI_b/ EZP_CS_b | | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| 55 | M8 | PTA5 | DISABLED | | PTA5 | USB_CLKIN | FTM0_CH2 | RMI0_RXER/ MII0_RXER | CMP2_OUT | I2S0_TX_BCLK | JTAG_TRST_b | |
| 56 | E7 | VDD | VDD | VDD | | | | | | | | |
| 57 | G7 | VSS | VSS | VSS | | | | | | | | |
| 58 | J7 | PTA6 | DISABLED | | PTA6 | | FTM0_CH3 | | | | TRACE_CLKOUT | |
| 59 | J8 | PTA7 | ADC0_SE10 | ADC0_SE10 | PTA7 | | FTM0_CH4 | | | | TRACE_D3 | |
| 60 | K8 | PTA8 | ADC0_SE11 | ADC0_SE11 | PTA8 | | FTM1_CH0 | | | FTM1_QD_PHA | TRACE_D2 | |
| 61 | L8 | PTA9 | DISABLED | | PTA9 | | FTM1_CH1 | MII0_RXD3 | | FTM1_QD_PHB | TRACE_D1 | |
| 62 | M9 | PTA10 | DISABLED | | PTA10 | | FTM2_CH0 | MII0_RXD2 | | FTM2_QD_PHA | TRACE_D0 | |

Pinout

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|----------|-------------|-------------------|-----------------------|-----------------------|-------------------|-----------|-----------------------------|----------------------------|----------|--------------|-------------|--------|
| 63 | L9 | PTA11 | DISABLED | | PTA11 | | FTM2_CH1 | MII0_RXCLK | I2C2_SDA | FTM2_QD_PHB | | |
| 64 | K9 | PTA12 | CMP2_IN0 | CMP2_IN0 | PTA12 | CAN0_TX | FTM1_CH0 | RMII0_RXD1/ MII0_RXD1 | I2C2_SCL | I2S0_TXD0 | FTM1_QD_PHA | |
| 65 | J9 | PTA13/ LLWU_P4 | CMP2_IN1 | CMP2_IN1 | PTA13/ LLWU_P4 | CAN0_RX | FTM1_CH1 | RMII0_RXD0/ MII0_RXD0 | I2C2_SDA | I2S0_TX_FS | FTM1_QD_PHB | |
| 66 | L10 | PTA14 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | RMII0_CRS_DV/ MII0_RXDV | I2C2_SCL | I2S0_RX_BCLK | I2S0_TXD1 | |
| 67 | L11 | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | RMII0_TXEN/ MII0_TXEN | | I2S0_RXD0 | | |
| 68 | K10 | PTA16 | DISABLED | | PTA16 | SPI0_SOUT | UART0_CTS_b/ UART0_COL_b | RMII0_TXD0/ MII0_TXD0 | | I2S0_RX_FS | I2S0_RXD1 | |
| 69 | K11 | PTA17 | ADC1_SE17 | ADC1_SE17 | PTA17 | SPI0_SIN | UART0_RTS_b | RMII0_TXD1/ MII0_TXD1 | | I2S0_MCLK | | |
| 70 | E8 | VDD | VDD | VDD | | | | | | | | |
| 71 | G8 | VSS | VSS | VSS | | | | | | | | |
| 72 | M12 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| 73 | M11 | PTA19 | XTAL0 | XTAL0 | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ALT1 | | |
| 74 | L12 | RESET_b | RESET_b | RESET_b | | | | | | | | |
| 75 | K12 | PTA24 | DISABLED | | PTA24 | | | MII0_TXD2 | | FB_A29 | | |
| 76 | J12 | PTA25 | DISABLED | | PTA25 | | | MII0_TXCLK | | FB_A28 | | |
| 77 | J11 | PTA26 | DISABLED | | PTA26 | | | MII0_TXD3 | | FB_A27 | | |
| 78 | J10 | PTA27 | DISABLED | | PTA27 | | | MII0_CRS | | FB_A26 | | |
| 79 | H12 | PTA28 | DISABLED | | PTA28 | | | MII0_TXER | | FB_A25 | | |
| 80 | H11 | PTA29 | DISABLED | | PTA29 | | | MII0_COL | | FB_A24 | | |
| 81 | H10 | PTB0/ LLWU_P5 | ADC0_SE8/ ADC1_SE8 | ADC0_SE8/ ADC1_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | RMII0_MDIO/ MII0_MDIO | | | FTM1_QD_PHA | |
| 82 | H9 | PTB1 | ADC0_SE9/ ADC1_SE9 | ADC0_SE9/ ADC1_SE9 | PTB1 | I2C0_SDA | FTM1_CH1 | RMII0_MDC/ MII0_MDC | | | FTM1_QD_PHB | |
| 83 | G12 | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | UART0_RTS_b | ENET0_1588_TMR0 | | | FTM0_FLT3 | |
| 84 | G11 | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | UART0_CTS_b/ UART0_COL_b | ENET0_1588_TMR1 | | | FTM0_FLT0 | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|-------------|-------------------|---------------|--------------------|--------------------|---------------|-----------|-------------|-----------------|---------|-----------|--------------|----------|
| 85 | G10 | PTB4 | ADC1_SE10 | ADC1_SE10 | PTB4 | | | ENET0_1588_TMR2 | | FTM1_FLT0 | | |
| 86 | G9 | PTB5 | ADC1_SE11 | ADC1_SE11 | PTB5 | | | ENET0_1588_TMR3 | | FTM2_FLT0 | | |
| 87 | F12 | PTB6 | ADC1_SE12 | ADC1_SE12 | PTB6 | | | | FB_AD23 | | | |
| 88 | F11 | PTB7 | ADC1_SE13 | ADC1_SE13 | PTB7 | | | | FB_AD22 | | | |
| 89 | F10 | PTB8 | DISABLED | | PTB8 | | UART3_RTS_b | | | FB_AD21 | | |
| 90 | F9 | PTB9 | DISABLED | | PTB9 | SPI1_PCS1 | UART3_CTS_b | | | FB_AD20 | | |
| 91 | E12 | PTB10 | ADC1_SE14 | ADC1_SE14 | PTB10 | SPI1_PCS0 | UART3_RX | | | FB_AD19 | FTM0_FLT1 | |
| 92 | E11 | PTB11 | ADC1_SE15 | ADC1_SE15 | PTB11 | SPI1_SCK | UART3_TX | | | FB_AD18 | FTM0_FLT2 | |
| 93 | H7 | VSS | VSS | VSS | | | | | | | | |
| 94 | F5 | VDD | VDD | VDD | | | | | | | | |
| 95 | E10 | PTB16 | DISABLED | | PTB16 | SPI1_SOUT | UART0_RX | FTM_CLKIN0 | | FB_AD17 | EWM_IN | |
| 96 | E9 | PTB17 | DISABLED | | PTB17 | SPI1_SIN | UART0_TX | FTM_CLKIN1 | | FB_AD16 | EWM_OUT_b | |
| 97 | D12 | PTB18 | DISABLED | | PTB18 | CAN0_TX | FTM2_CH0 | I2S0_TX_BCLK | | FB_AD15 | FTM2_QD_PHA | |
| 98 | D11 | PTB19 | DISABLED | | PTB19 | CAN0_RX | FTM2_CH1 | I2S0_TX_FS | | FB_OE_b | FTM2_QD_PHB | |
| 99 | D10 | PTB20 | DISABLED | | PTB20 | SPI2_PCS0 | | | | FB_AD31 | CMP0_OUT | |
| 100 | D9 | PTB21 | DISABLED | | PTB21 | SPI2_SCK | | | | FB_AD30 | CMP1_OUT | |
| 101 | C12 | PTB22 | DISABLED | | PTB22 | SPI2_SOUT | | | | FB_AD29 | CMP2_OUT | |
| 102 | C11 | PTB23 | DISABLED | | PTB23 | SPI2_SIN | SPI0_PCS5 | | | FB_AD28 | | |
| 103 | B12 | PTC0 | ADC0_SE14 | ADC0_SE14 | PTC0 | SPI0_PCS4 | PDB0_EXTRG | USB_SOF_OUT | | FB_AD14 | I2S0_TXD1 | |
| 104 | B11 | PTC1/LLWU_P6 | ADC0_SE15 | ADC0_SE15 | PTC1/LLWU_P6 | SPI0_PCS3 | UART1_RTS_b | FTM0_CH0 | | FB_AD13 | I2S0_TXD0 | |
| 105 | A12 | PTC2 | ADC0_SE4b/CMP1_IN0 | ADC0_SE4b/CMP1_IN0 | PTC2 | SPI0_PCS2 | UART1_CTS_b | FTM0_CH1 | | FB_AD12 | I2S0_TX_FS | |
| 106 | A11 | PTC3/LLWU_P7 | CMP1_IN1 | CMP1_IN1 | PTC3/LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | | CLKOUT | I2S0_TX_BCLK | |
| 107 | H8 | VSS | VSS | VSS | | | | | | | | |
| 108 | — | VDD | VDD | VDD | | | | | | | | |
| 109 | A9 | PTC4/LLWU_P8 | DISABLED | | PTC4/LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | | FB_AD11 | CMP1_OUT | |
| 110 | D8 | PTC5/LLWU_P9 | DISABLED | | PTC5/LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | I2S0_RXD0 | | FB_AD10 | CMP0_OUT | FTM0_CH2 |
| 111 | C8 | PTC6/LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/LLWU_P10 | SPI0_SOUT | PDB0_EXTRG | I2S0_RX_BCLK | | FB_AD9 | I2S0_MCLK | |
| 112 | B8 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | USB_SOF_OUT | I2S0_RX_FS | | FB_AD8 | | |

Pinout

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|----------|-------------|--------------------|------------------------|------------------------|--------------------|-----------|-------------------------------------|---------------------|--|---------------|-----------|--------|
| 113 | A8 | PTC8 | ADC1_SE4b/ CMP0_IN2 | ADC1_SE4b/ CMP0_IN2 | PTC8 | | FTM3_CH4 | I2S0_MCLK | FB_AD7 | | | |
| 114 | D7 | PTC9 | ADC1_SE5b/ CMP0_IN3 | ADC1_SE5b/ CMP0_IN3 | PTC9 | | FTM3_CH5 | I2S0_RX_ BCLK | FB_AD6 | FTM2_FLT0 | | |
| 115 | C7 | PTC10 | ADC1_SE6b | ADC1_SE6b | PTC10 | I2C1_SCL | FTM3_CH6 | I2S0_RX_FS | FB_AD5 | | | |
| 116 | B7 | PTC11/ LLWU_P11 | ADC1_SE7b | ADC1_SE7b | PTC11/ LLWU_P11 | I2C1_SDA | FTM3_CH7 | I2S0_RXD1 | FB_RW_b | | | |
| 117 | A7 | PTC12 | DISABLED | | PTC12 | | UART4_ RTS_b | | FB_AD27 | FTM3_FLT0 | | |
| 118 | D6 | PTC13 | DISABLED | | PTC13 | | UART4_ CTS_b | | FB_AD26 | | | |
| 119 | C6 | PTC14 | DISABLED | | PTC14 | | UART4_RX | | FB_AD25 | | | |
| 120 | B6 | PTC15 | DISABLED | | PTC15 | | UART4_TX | | FB_AD24 | | | |
| 121 | — | VSS | VSS | VSS | | | | | | | | |
| 122 | — | VDD | VDD | VDD | | | | | | | | |
| 123 | A6 | PTC16 | DISABLED | | PTC16 | | UART3_RX | ENET0_ 1588_TMR0 | FB_CS5_b/ FB_TSI21/ FB_BE23_ 16_BLS15_ 8_b | | | |
| 124 | D5 | PTC17 | DISABLED | | PTC17 | | UART3_TX | ENET0_ 1588_TMR1 | FB_CS4_b/ FB_TSI20/ FB_BE31_ 24_BLS7_0_ b | | | |
| 125 | C5 | PTC18 | DISABLED | | PTC18 | | UART3_ RTS_b | ENET0_ 1588_TMR2 | FB_TBST_b/ FB_CS2_b/ FB_BE15_8_ BLS23_16_b | | | |
| 126 | B5 | PTC19 | DISABLED | | PTC19 | | UART3_ CTS_b | ENET0_ 1588_TMR3 | FB_CS3_b/ FB_BE7_0_ BLS31_24_b | FB_TA_b | | |
| 127 | A5 | PTD0/ LLWU_P12 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_ RTS_b | FTM3_CH0 | FB_ALE/ FB_CS1_b/ FB_TS_b | | | |
| 128 | D4 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_ CTS_b | FTM3_CH1 | FB_CS0_b | | | |
| 129 | C4 | PTD2/ LLWU_P13 | DISABLED | | PTD2/ LLWU_P13 | SPI0_SOUT | UART2_RX | FTM3_CH2 | FB_AD4 | | I2C0_SCL | |
| 130 | B4 | PTD3 | DISABLED | | PTD3 | SPI0_SIN | UART2_TX | FTM3_CH3 | FB_AD3 | | I2C0_SDA | |
| 131 | A4 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_ RTS_b | FTM0_CH4 | FB_AD2 | EWM_IN | SPI1_PCS0 | |
| 132 | A3 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_ CTS_b/ UART0_ COL_b | FTM0_CH5 | FB_AD1 | EWM_OUT_ b | SPI1_SCK | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|-------------|-------------------|-------------------|-----------|-----------|-------------------|-----------|-----------------|-----------------|--------|-----------|-----------|--------|
| 133 | A2 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI0_PCS3 | UART0_RX | FTM0_CH6 | FB_AD0 | FTM0_FLT0 | SPI1_SOUT | |
| 134 | M10 | VSS | VSS | VSS | | | | | | | | |
| 135 | F8 | VDD | VDD | VDD | | | | | | | | |
| 136 | A1 | PTD7 | DISABLED | | PTD7 | CMT_IRO | UART0_TX | FTM0_CH7 | | FTM0_FLT1 | SPI1_SIN | |
| 137 | C9 | PTD8 | DISABLED | | PTD8 | I2C0_SCL | UART5_RX | | | FB_A16 | | |
| 138 | B9 | PTD9 | DISABLED | | PTD9 | I2C0_SDA | UART5_TX | | | FB_A17 | | |
| 139 | B3 | PTD10 | DISABLED | | PTD10 | | UART5_ RTS_b | | | FB_A18 | | |
| 140 | B2 | PTD11 | DISABLED | | PTD11 | SPI2_PCS0 | UART5_ CTS_b | SDHC0_ CLKIN | | FB_A19 | | |
| 141 | B1 | PTD12 | DISABLED | | PTD12 | SPI2_SCK | FTM3_FLT0 | SDHC0_D4 | | FB_A20 | | |
| 142 | C3 | PTD13 | DISABLED | | PTD13 | SPI2_SOUT | | SDHC0_D5 | | FB_A21 | | |
| 143 | C2 | PTD14 | DISABLED | | PTD14 | SPI2_SIN | | SDHC0_D6 | | FB_A22 | | |
| 144 | C1 | PTD15 | DISABLED | | PTD15 | SPI2_PCS1 | | SDHC0_D7 | | FB_A23 | | |

5.2 Unused analog interfaces

Table 57. Unused analog interfaces

| Module name | Pins | Recommendation if unused |
|------------------|---|---|
| ADC | ADC0_DP1, ADC0_DM1, ADC1_DP1, ADC1_DM1, ADC0_DP0/ADC1_DP3, ADC0_DM0/ADC1_DM3, ADC1_DP0/ADC0_DP3, ADC1_DM0/ADC0_DM3, ADC1_SE16/ADC0_SE22, ADC0_SE16/ADC0_SE21, ADC1_SE18 | Ground |
| DAC ¹ | DAC0_OUT, DAC1_OUT | Float |
| USB | VREGIN, USB0_GND, VOUT33 ² | Connect VREGIN and VOUT33 together and tie to ground through a 10 kΩ resistor. Do not tie directly to ground, as this causes a latch-up risk. |
| | USB0_DM, USB0_DP | Float |

1. Unused DAC signals do not apply to all parts. See the [Pinout](#) section for details.
2. USB0_VBUS and USB0_GND are board level signals

5.3 K63 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

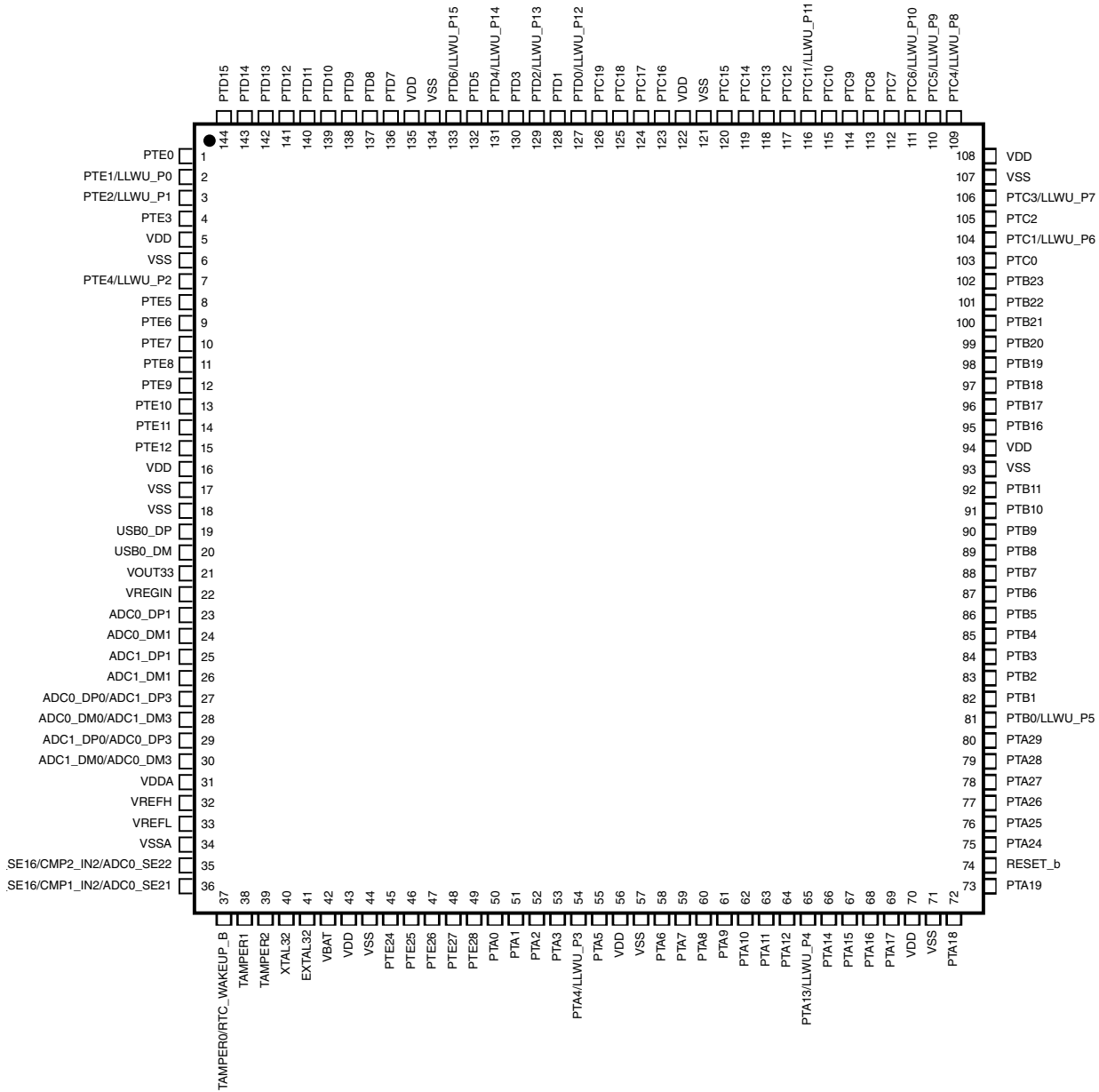


Figure 36. K63 144 LQFP Pinout Diagram

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|-----------------------|-----------------------|--|--|------------------------------|---------|--------------------|-------------------|-------------------|------------------|------------------|---------|---|
| A | PTD7 | PTD6/ LLWU_P15 | PTD5 | PTD4/ LLWU_P14 | PTD0/ LLWU_P12 | PTC16 | PTC12 | PTC8 | PTC4/ LLWU_P8 | NC | PTC3/ LLWU_P7 | PTC2 | A |
| B | PTD12 | PTD11 | PTD10 | PTD3 | PTC19 | PTC15 | PTC11/ LLWU_P11 | PTC7 | PTD9 | NC | PTC1/ LLWU_P6 | PTC0 | B |
| C | PTD15 | PTD14 | PTD13 | PTD2/ LLWU_P13 | PTC18 | PTC14 | PTC10 | PTC6/ LLWU_P10 | PTD8 | NC | PTB23 | PTB22 | C |
| D | PTE2/ LLWU_P1 | PTE1/ LLWU_P0 | PTE0 | PTD1 | PTC17 | PTC13 | PTC9 | PTC5/ LLWU_P9 | PTB21 | PTB20 | PTB19 | PTB18 | D |
| E | PTE6 | PTE5 | PTE4/ LLWU_P2 | PTE3 | VDD | VDD | VDD | VDD | PTB17 | PTB16 | PTB11 | PTB10 | E |
| F | PTE10 | PTE9 | PTE8 | PTE7 | VDD | VSS | VSS | VDD | PTB9 | PTB8 | PTB7 | PTB6 | F |
| G | VOUT33 | VREGIN | PTE12 | PTE11 | VREFH | VREFL | VSS | VSS | PTB5 | PTB4 | PTB3 | PTB2 | G |
| H | USB0_DP | USB0_DM | VSS | TAMPER4 | VDDA | VSSA | VSS | VSS | PTB1 | PTB0/ LLWU_P5 | PTA29 | PTA28 | H |
| J | ADC0_DP1 | ADC0_DM1 | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | TAMPER3 | PTA0 | PTA1 | PTA6 | PTA7 | PTA13/ LLWU_P4 | PTA27 | PTA26 | PTA25 | J |
| K | ADC1_DP1 | ADC1_DM1 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | TAMPER2 | TAMPER1 | PTA2 | PTA3 | PTA8 | PTA12 | PTA16 | PTA17 | PTA24 | K |
| L | ADC0_DP0/ ADC1_DP3 | ADC0_DM0/ ADC1_DM3 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | TAMPER0/ RTC_ WAKEUP_B | VBAT | PTA4/ LLWU_P3 | PTA9 | PTA11 | PTA14 | PTA15 | RESET_b | L |
| M | ADC1_DP0/ ADC0_DP3 | ADC1_DM0/ ADC0_DM3 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | TAMPER5 | NC | EXTAL32 | XTAL32 | PTA5 | PTA10 | VSS | PTA19 | PTA18 | M |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |

Figure 37. K63 144 MAPBGA Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK63 and MK63

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|---------------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| K## | Kinetis family | <ul style="list-style-type: none"> K63 = Ethernet, Tamper, and high RAM density |
| A | Key attribute | <ul style="list-style-type: none"> D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | <ul style="list-style-type: none"> N = Program flash only X = Program flash and FlexMemory |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB |

Table continues on the next page...

| Field | Description | Values |
|-------|-----------------------------|---|
| | | <ul style="list-style-type: none"> • 1M0 = 1 MB • 2M0 = 2 MB |
| R | Silicon revision | <ul style="list-style-type: none"> • Z = Initial • (Blank) = Main • A = Revision after main |
| T | Temperature range (°C) | <ul style="list-style-type: none"> • V = -40 to 105 • C = -40 to 85 |
| PP | Package identifier | <ul style="list-style-type: none"> • FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> • 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz • 16 = 168 MHz • 18 = 180 MHz |
| N | Packaging type | <ul style="list-style-type: none"> • R = Tape and reel • (Blank) = Trays |

7.4 Example

This is an example part number:

MK63FN1M0VMD12

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Terminology and guidelines

| Term | Definition |
|-----------------------|--|
| Rating | <p>A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:</p> <ul style="list-style-type: none"> • <i>Operating ratings</i> apply during operation of the chip. • <i>Handling ratings</i> apply when the chip is not powered. <p>NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.</p> |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | <p>A specified value for a technical characteristic that:</p> <ul style="list-style-type: none"> • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions <p>NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.</p> |

8.2 Examples

Operating rating:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | -0.3 | 1.2 | V |

Operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

Operating behavior that includes a typical value:

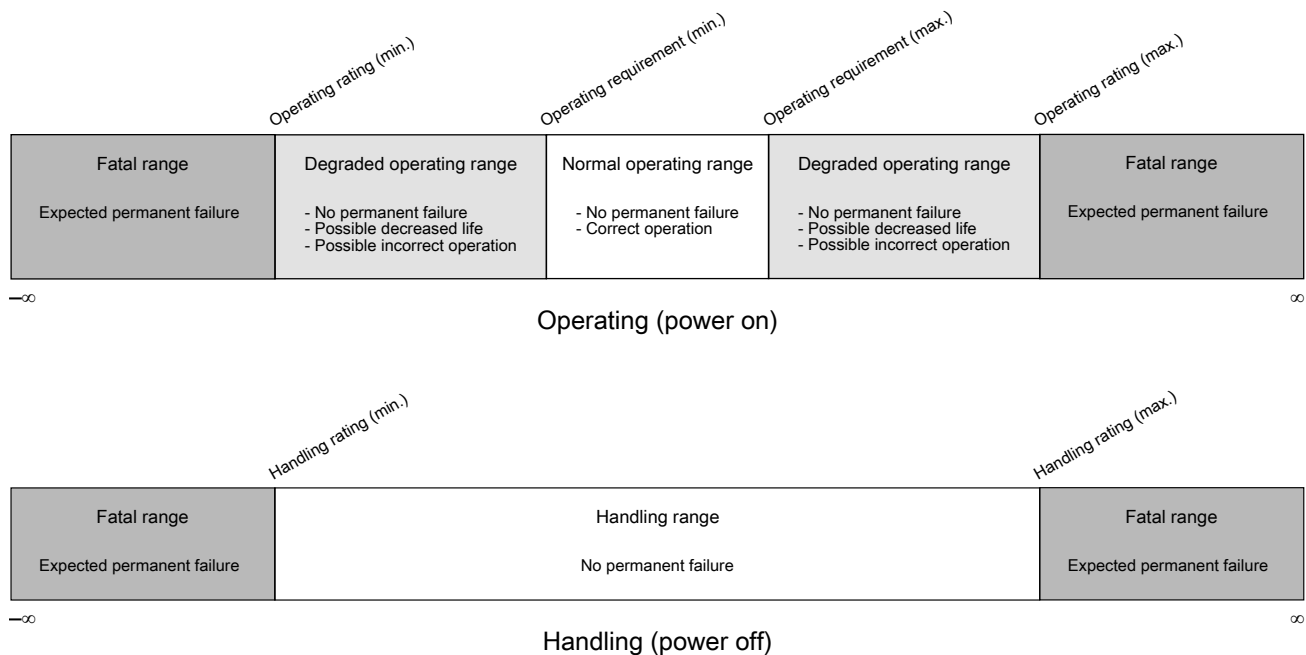
| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|--|------|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|----------|----------------------|-------|------|
| T_A | Ambient temperature | 25 | °C |
| V_{DD} | 3.3 V supply voltage | 3.3 | V |

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.

Table 58. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|---------|--|
| 2 | 01/2014 | Initial public release. |
| 3 | 04/2014 | <ul style="list-style-type: none"> Format changes |
| 4 | 09/2014 | <ul style="list-style-type: none"> Updated Table 6 "Power consumption operating behavior." Updated Table 17 "IRC48M specifications" Updated Table 35 "VREF full-range operating behavior" |
| 5 | 12/2014 | <ul style="list-style-type: none"> Updated Table 6 "Power consumption operating behavior." Added a note to the section "Power consumption operating behaviors." |
| 6 | 08/2015 | <ul style="list-style-type: none"> Added a footnote to the maximum SCL clock frequency value in the table "I²C timing" Changed the title of the table "I²C 1 MHZ timing" to "I²C 1 Mbps timing" Added a footnote and updated the table "IRC48M specifications" for open loop total deviation of IRC48M frequency at high voltage and low voltage. Added a footnote on the ambient temperature entry to the section "Thermal operating requirements." Added a note to the section "Power consumption operating behaviors" and updated values in the table "Power consumption operating behaviors." Added a note to the maximum frequency value in the table "Slave mode DSPI timing (limited voltage range)." Redeveloped the section "Terminology and guidelines." |

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