UDP C8051F960/Si1020 MCU CARD WITH MULTIPLEXED LCD USER'S GUIDE

1. Introduction

The Unified Development Platform (UDP) provides a development and demonstration platform for Silicon Laboratories microcontrollers and the Silicon Laboratories software tools, including the Silicon Laboratories Integrated Development Environment (IDE).

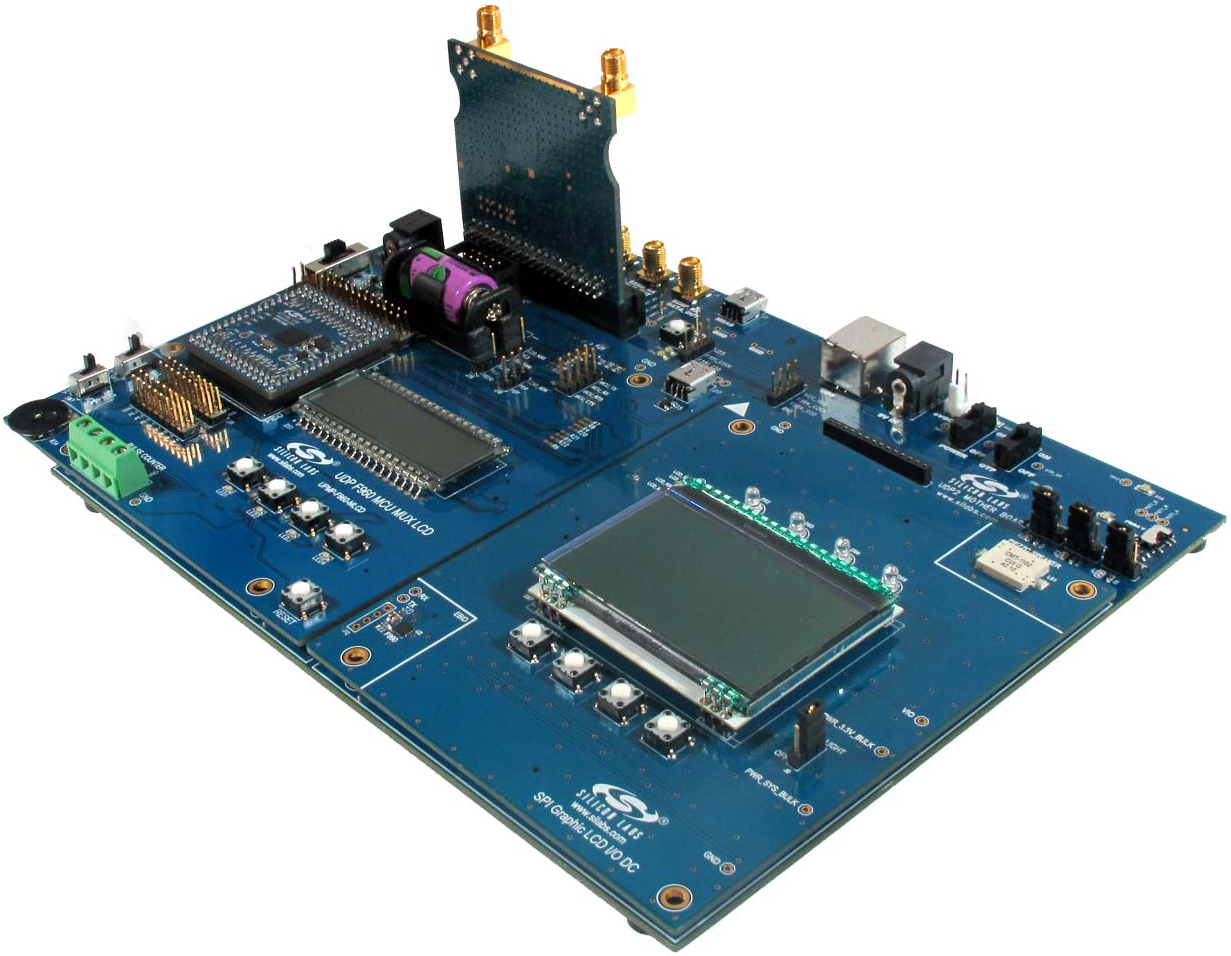

Figure 1. Unified Development Platform

2. Relevant Documents

This document provides a hardware overview for the Unified Development Platform (UDP) system UDP C8051F960/Si1020 MCU Card with Multiplexed LCD MCU card. Additional information on the UDP system can be found in the documents listed in this section.

2.1. Motherboard User's Guide

The UDP Motherboard User's Guide contains information on the motherboard features and can be found at www.silabs.com.

2.2. Card User's Guides

The UDP MCU Card and Radio Card User's Guides can be found at www.silabs.com.

3. Hardware Setup

3.1. Using the MCU Card Alone

Refer to Figure 2 for a diagram of the hardware configuration when using the MCU card without a UDP motherboard.

1. Connect the USB Debug Adapter to the 2x5 debug connector on the MCU card with the 10-pin ribbon cable.
2. Connect one end of the USB cable to the USB connector on the USB Debug Adapter.
3. Connect the other end of the USB cable to a USB Port on the PC.
4. Move the SW5 VBAT switch to the middle VREG position.
5. Move the SW7 VIO switch to the upper VBAT position.
6. Move the SW12 VIORF switch to the upper VBAT position.
7. Connect the 9 V dc adapter to P1.

Notes:

- Use the Reset button in the IDE to reset the target when connected using a USB Debug Adapter.
- Remove power from the MCU card and the USB Debug Adapter before connecting or disconnecting the ribbon cable from the MCU card. Connecting or disconnecting the cable when the devices have power can damage the device and/or the USB Debug Adapter.
- Section 5. "UDP C8051F960/Si1020 MCU Card with Multiplexed LCD MCU Card Overview," on page 12 describes additional power options.

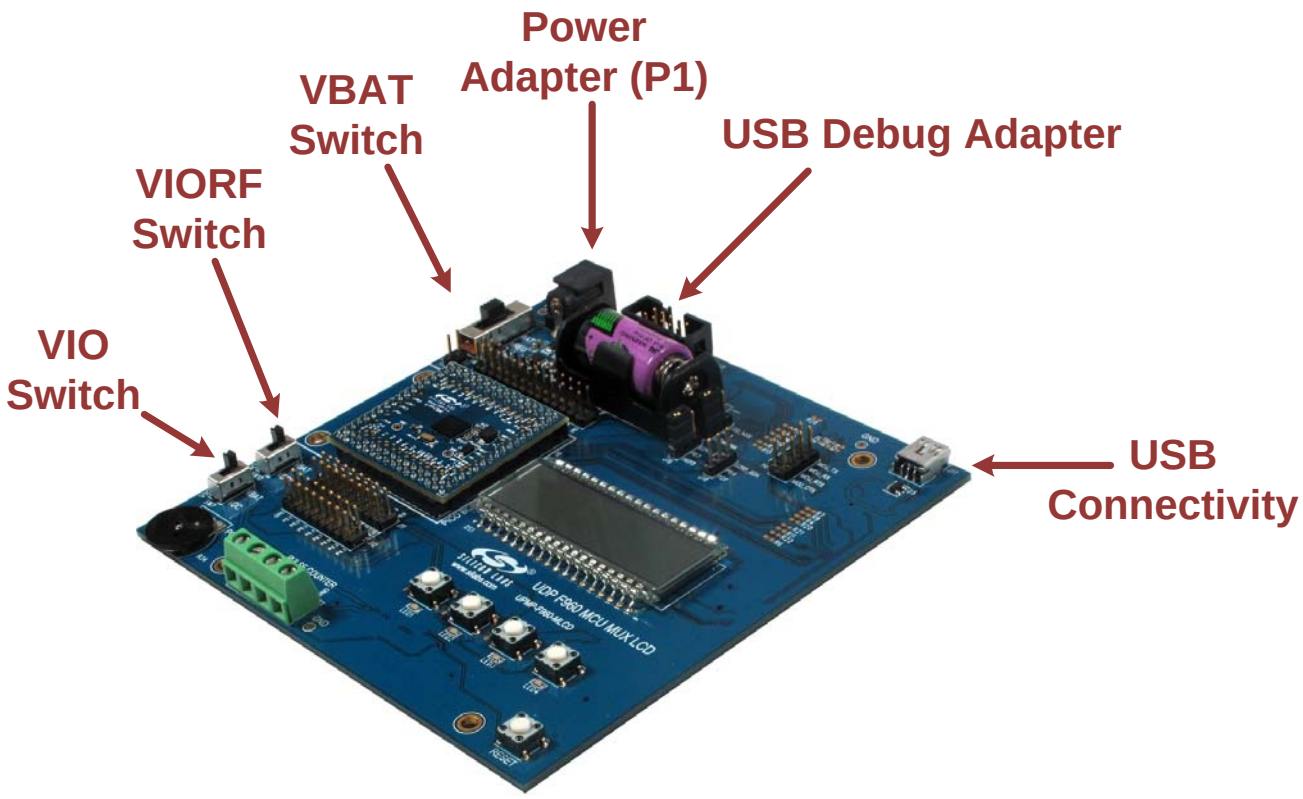

Figure 2. Hardware Setup Using the MCU Card Alone

3.2. Using the MCU Card with the UDP Motherboard

Refer to Figure 3 for a diagram of the hardware configuration when using the MCU card with a UDP motherboard.

1. Connect the MCU card to the UDP motherboard slot.
2. (Optional) Connect the I/O card to the UDP motherboard slot.
3. (Optional) Connect a radio card to the radio card slot in the UDP motherboard.
4. (Optional) Connect an EZLink card to the EZLink card slot in the UDP motherboard.
5. Connect the USB Debug Adapter to the 2x5 debug connector on the MCU card with the 10-pin ribbon cable.
6. Connect one end of the USB cable to the USB connector on the USB Debug Adapter.
7. Connect the other end of the USB cable to a USB Port on the PC.
8. Connect the ac/dc power adapter to power jack J20 on the UDP motherboard. The board can also be powered from the J16 USB or J1 mini USB connectors.
9. Move the SW5 VBAT switch on the MCU card to the VREG position.
10. Move the SW7 VIO switch on the MCU card to the upper VBAT position.
11. Move the SW12 VIORF switch on the MCU card to the upper VBAT position.
12. Move the S3 power switch on the UDP motherboard to the ON position.

Notes:

- Use the Reset button in the IDE to reset the target when connected using a USB Debug Adapter.
- Remove power from the target board and the USB Debug Adapter before connecting or disconnecting the ribbon cable from the target board. Connecting or disconnecting the cable when the devices have power can damage the device and/or the USB Debug Adapter.
- The MCU card can be used alone without the motherboard. However, the motherboard must be powered if an MCU card is connected.

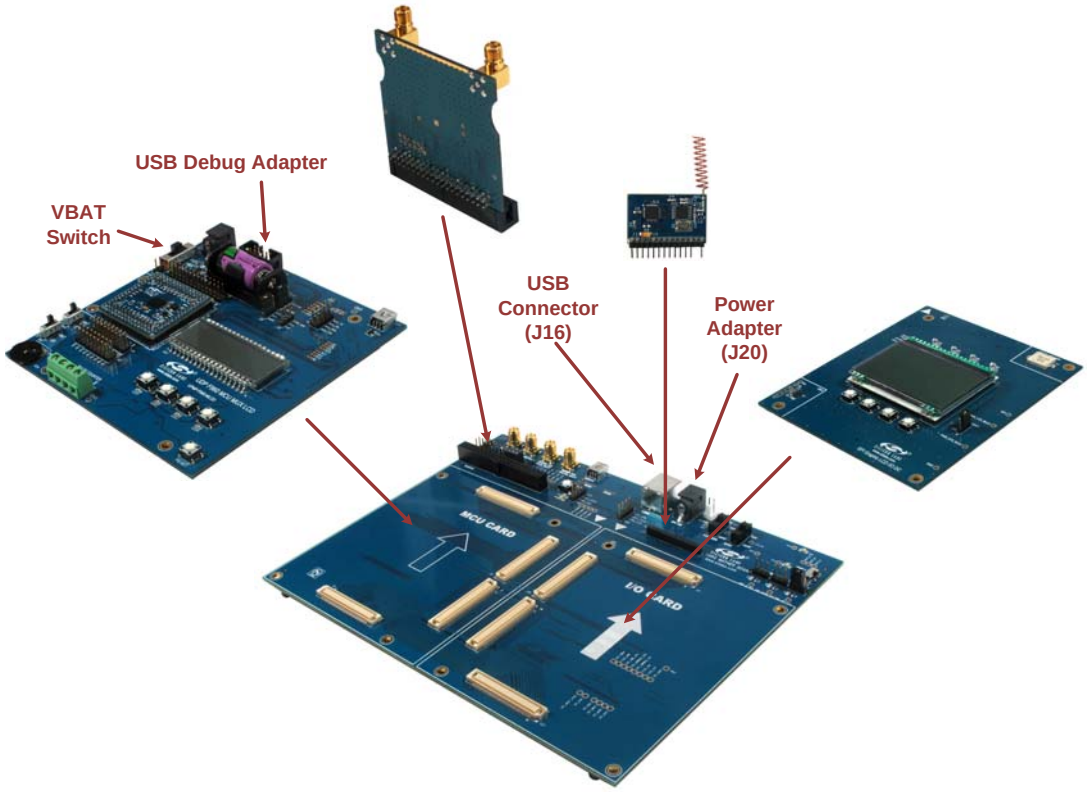

Figure 3. Hardware Setup Using the Unified Development Platform

4. Software Setup

Simplicity Studio greatly reduces development time and complexity with Silicon Labs EFM32 and 8051 MCU products by providing a high-powered IDE, tools for hardware configuration, and links to helpful resources, all in one place.

Once Simplicity Studio is installed, the application itself can be used to install additional software and documentation components to aid in the development and evaluation process.

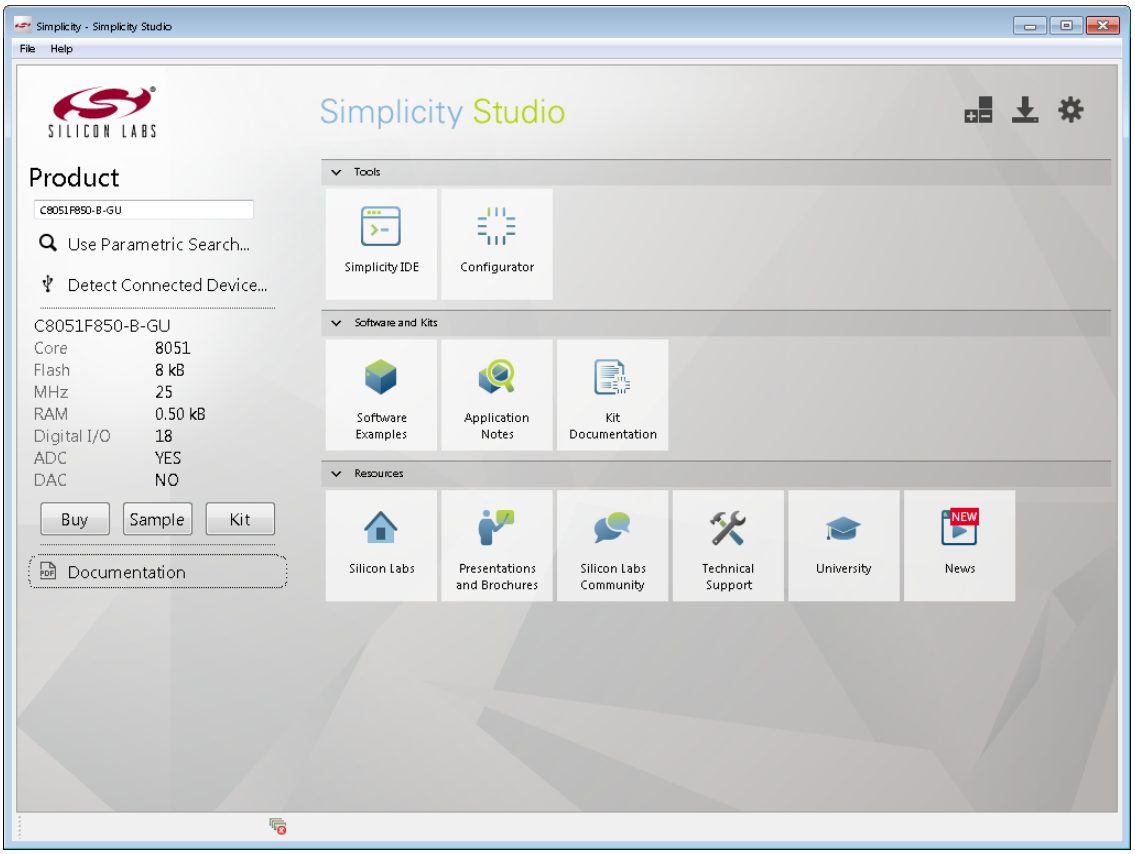

Figure 4. Simplicity Studio

The following Simplicity Studio components are required for the C8051F960 Development Kit:

- 8051 Products Part Support
- Simplicity Developer Platform

Download and install Simplicity Studio from www.silabs.com/8bit-software or www.silabs.com/simplicity-studio. Once installed, run Simplicity Studio by selecting **Start→Silicon Labs→Simplicity Studio→Simplicity Studio** from the start menu or clicking the **Simplicity Studio** shortcut on the desktop. Follow the instructions to install the software and click **Simplicity IDE** to launch the IDE.

The first time the project creation wizard runs, the **Setup Environment** wizard will guide the user through the process of configuring the build tools and SDK selection.

In the **Part Selection** step of the wizard, select from the list of installed parts only the parts to use during development. Choosing parts and families in this step affects the displayed or filtered parts in the later device selection menus. Choose the C8051F96x family by checking the **C8051F96x** check box. Modify the part selection at any time by accessing the **Part Management** dialog from the **Window→Preferences→Simplicity Studio→Part Management** menu item.

Simplicity Studio can detect if certain toolchains are not activated. If the **Licensing Helper** is displayed after completing the **Setup Environment** wizard, follow the instructions to activate the toolchain.

4.1. Running Blinky

Each project has its own source files, target configuration, SDK configuration, and build configurations such as the **Debug** and **Release** build configurations. The IDE can be used to manage multiple projects in a collection called a workspace. Workspace settings are applied globally to all projects within the workspace. This can include settings such as key bindings, window preferences, and code style and formatting options. Project actions, such as build and debug are context sensitive. For example, the user must select a project in the **Project Explorer** view in order to build that project.

To create a project based on the Blinky example:

1. Click the **Simplicity IDE** tile from the Simplicity Studio home screen.
2. Click the **Create new project** link from the welcome screen or go to **File→New→Silicon Labs MCU Project**.
3. In the **Kit** drop-down, select **C8051F960 Development Kit**, in the **Part** drop-down, select **C8051F960**, and in the **SDK** drop-down, select the desired SDK. Click **Next**.
4. Select **Example** and click **Next**.
5. Under **C8051F960 Development Kit** in the **Blinky** folder, select **F96x Blinky** and click **Finish**.
6. Click on the project in the **Project Explorer** and click **Build**, the hammer icon in the top bar. Alternatively, go to **Project→Build Project**.
7. Click **Debug** to download the project to the hardware and start a debug session.
8. Press the **Resume** button to start the code running. The LED should blink.

9. Press the **Suspend** button to stop the code.

10. Press the **Reset the device** button to reset the target MCU.

11. Press the **Disconnect** button to return to the development perspective.

4.2. Simplicity Studio Help

Simplicity Studio includes detailed help information and device documentation within the tool. The help contains descriptions for each dialog window. To view the documentation for a dialog, click the question mark icon in the window:

This will open a pane specific to the dialog with additional details.

The documentation within the tool can also be viewed by going to **Help→Help Contents** or **Help→Search**.

4.3. Legacy 8-bit IDE

Note: Using the Simplicity Studio tools with the C8051F960 Development Kit is recommended. See section 4. "Software Setup," on page 5 for more information.

Download the 8-bit software from the website (www.silabs.com/8bit-software) or use the provided installer on the CD-ROM to install the software tools for the C8051F96x devices. After installation, examples can be found in **...\Examples\C8051F96x** or **...\Examples\Si102x_3x** in the installation directory. At a minimum, the C8051F960 DK requires:

- **Silicon Labs IDE**—Software enabling initial evaluation, development, and debugging.
- **Configuration Wizard 2**—Initialization code generation software for the C8051F96x devices.
- **Keil C51 Tools**—Keil 8051 Compiler/Assembler/Linker toolchain.
- **CP210x Drivers**—Virtual COM Port (VCP) drivers for the CP210x COM interface. More information on this installation process can be found in Section 4.4.

Other software available includes:

- **Keil µVision Driver**—Driver for the Keil µVision IDE that enables development and debugging on C8051Fxxx MCUs.
- **Flash Programming Utilities** and **MCU Production Programmer**—Programming utilities for the production line. More information on the available programming options can be found on the website: http://www.silabs.com/products/mcu/Pages/ProgrammingOptions.aspx.
- **ToolStick Development Tools**—Software and examples for the ToolStick development platform. More information on this platform can be found at www.silabs.com/toolstick.

Also available on the 8-bit software webpage is the Battery Life Estimator, which gives designers a quick and easy way to understand the discharge characteristics of different system configurations to help optimize low-power applications.

The development kit includes the latest version of the C51 Keil 8051 toolset. This toolset is initially limited to a code size of 2 kB and programs start at code address 0x0800. After registration, the code size limit is removed entirely and programs will start at code address 0x0000.

To register the Keil toolset:

1. Find the **Product Serial Number** printed on the CD-ROM. If you no longer have this serial number, register on the Silicon Labs website (www.silabs.com/8bit-software) to obtain the serial number.
2. Open the Keil µVision4 IDE from the installation directory with administrative privileges.
3. Select **File→License Management** to open the License Management window.

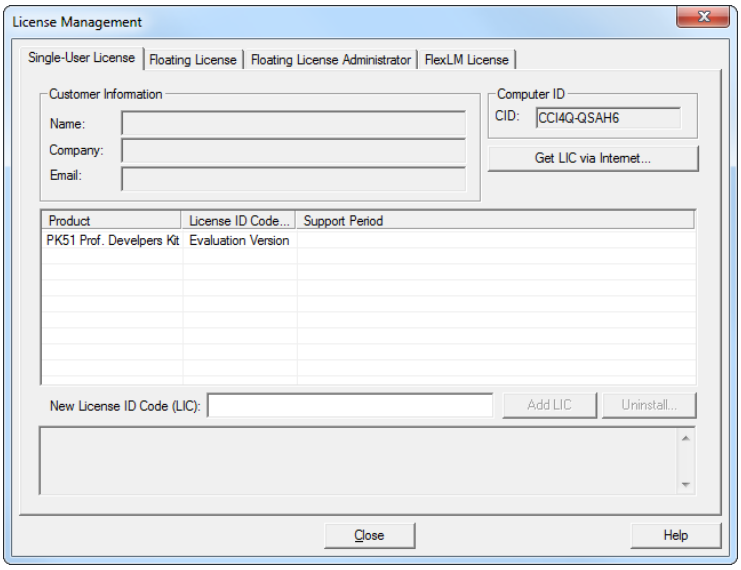

Figure 5. Keil µVision4 IDE License Management Window

4. Click on the **Get LIC via Internet...** button to open the Obtaining a License IDE Code (LIC) window.
5. Press **OK** to open a browser window to the Keil website. If the window doesn't open, navigate to www.keil.com/license/install.htm.
6. Enter the Silicon Labs **Product Serial Number** printed on the CD-ROM, along with any additional required information.
7. Once the form is complete, click the **Submit** button. An email will be sent to the provided email address with the license activation code.
8. Copy the License ID Code (LIC) from the email.
9. Paste the LIC into the **New License ID Code (LIC)** text box at the bottom of the License Management window in µVision4.
10. Press the **Add LIC** button. The window should now list the **PK51 Prof. Developers Kit for Silabs** as a licensed product.
11. Click the **Close** button.

4.4. CP210x USB to UART VCP Driver Installation

The MCU Card includes a Silicon Labs CP210x USB-to-UART Bridge Controller. Device drivers for the CP210x need to be installed before the PC software can communicate with the MCU through the UART interface. Use the drivers included CD-ROM or download the latest drivers from the website (www.silabs.com/interface-software).

1. If using the CD-ROM, the **CP210x Drivers** option will launch the appropriate driver installer. If downloading the driver package from the website, unzip the files to a location and run the appropriate installer for the system (x86 or x64).
2. Accept the license agreement and follow the steps to install the driver on the system. The installer will let you know when your system is up to date. The driver files included in this installation have been certified by Microsoft.
3. To complete the installation process, connect the included USB cable between the host computer and the **COM PORT** USB connector (J5) on the MCU Card. Windows will automatically finish the driver installation. Information windows will pop up from the taskbar to show the installation progress.
4. If needed, the driver files can be uninstalled by selecting **Windows Driver Package—Silicon Laboratories...** option in the **Programs and Features** window.

4.5. Silicon Labs Battery Life Estimator

The Battery Life Estimator is a system design tool for battery-operated devices. It allows the user to select the type of battery they are using in the system and enter the supply current profile of their application. Using this information, it performs a simulation and provides an estimated system operating time. The Battery Life Estimator is shown in Figure 6.

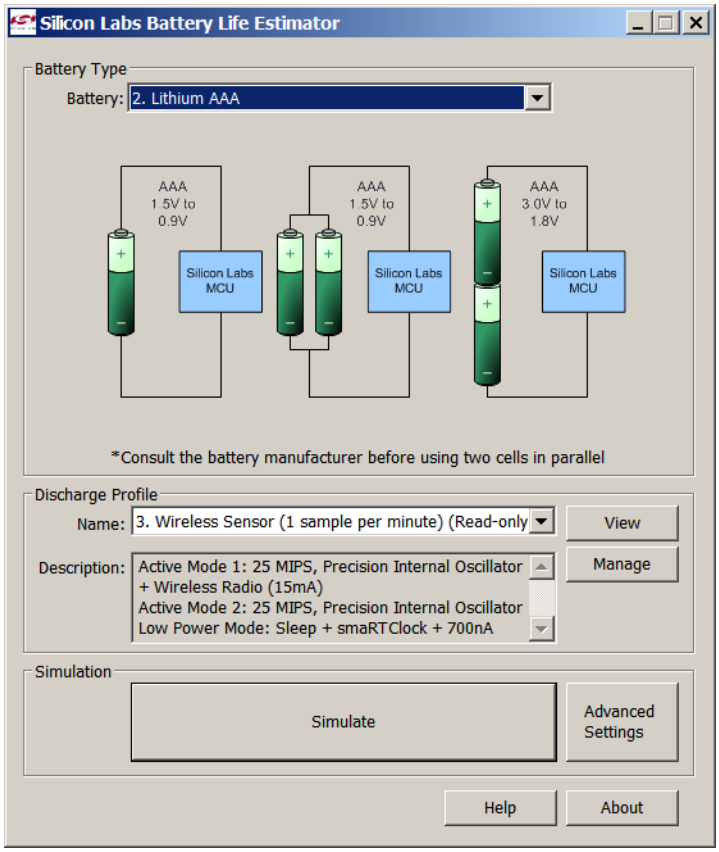

Figure 6. Battery Life Estimator Utility

From Figure 6, the two inputs to the Battery Life Estimator are battery type and discharge profile. The utility includes battery profiles for common battery types such as AAA, AA, A76 Button Cell, and CR2032 coin cell. The discharge profile is application-specific and describes the supply current requirements of the system under various supply voltages and battery configurations. The discharge profile is independent of the selected power source. Several read-only discharge profiles for common applications are included in the pulldown menu. The user may also create a new profile for their own applications.

To create a new profile:

1. Select the profile that most closely matches the target application or choose the "Custom Profile".
2. Click Manage.
3. Click Duplicate.
4. Click Edit.

Profiles may be edited with the easy-to-use GUI (shown in Figure 7).

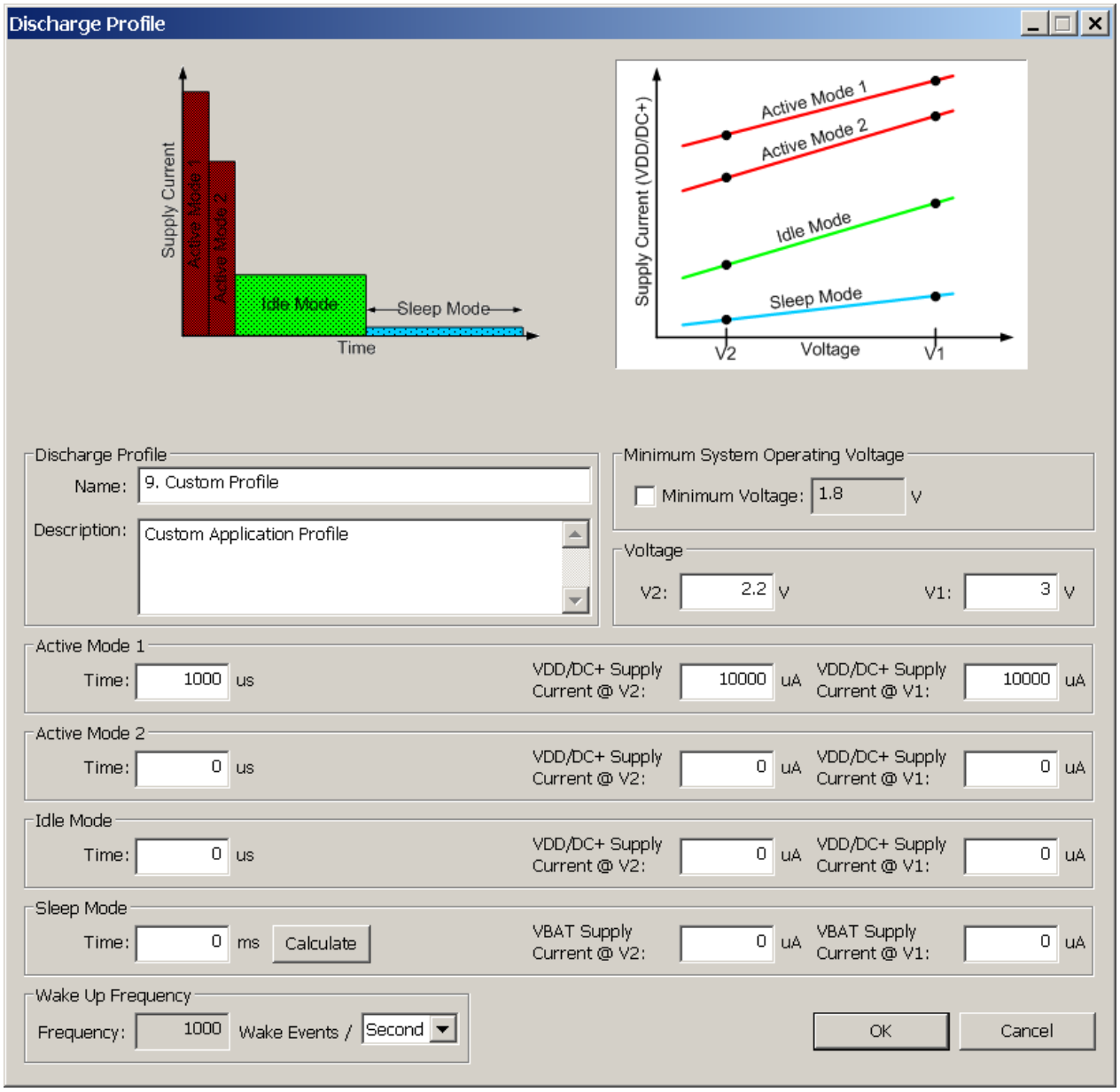

Figure 7. Battery Life Estimator Discharge Profile Editor

The Discharge Profile Editor allows the user to modify the profile name and description. The four text entry boxes on the left hand side of the form allow the user to specify the amount of time the system spends in each power mode. On the right hand side, the user may specify the supply current of the system in each power mode.

Since supply current is typically dependent on supply voltage, the discharge profile editor provides two columns for supply current. The V2 and V1 voltages at the top of the two columns specify the voltages at which the current measurements were taken. The Battery Life Estimator creates a linear approximation based on the input data and is able to feed the simulation engine with an approximate supply current demand for every input voltage.

The minimum system operating voltage input field allows the system operating time to stop increasing when the simulated battery voltage drops below a certain threshold. This is primarily to allow operating time estimates for systems that cannot operate down to 1.8 V, which is the voltage of two fully drained single-cell batteries placed in series.

The wakeup frequency box calculates the period of a single iteration through the four power modes and displays the system wake up frequency. This is typically the "sample rate" in low power analog sensors.

Once the battery type and discharge profile is specified, the user can click the "Simulate" button to start a new simulation. The simulation engine calculates the estimated battery life when using one single-cell battery, two single-cell batteries in series, and two single-cell batteries in parallel. Figure 8 shows the simulation output window.

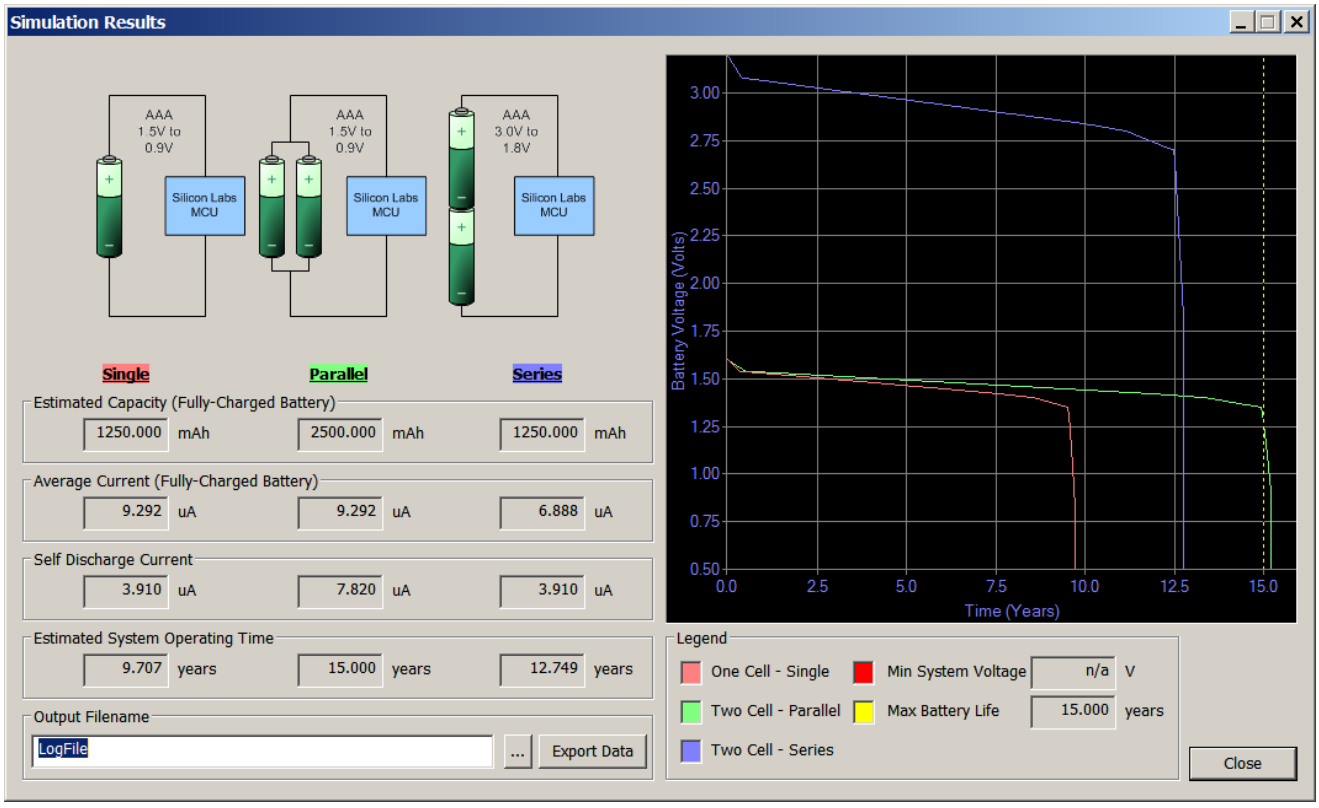

Figure 8. Battery Life Estimator Utility Simulation Results Form

The primary outputs of the Battery Life Estimator are an estimated system operating time and a simulated graph of battery voltage vs. time. Additional outputs include estimated battery capacity, average current, self-discharge current, and the ability to export graph data to a comma delimited text file for plotting in an external graphing application.

5. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD MCU Card Overview

The C8051F96x MCU card enables application development on the C8051F960 MCU. The card connects to the MCU Card expansion slot on the UDP motherboard and provides complete access to the MCU resources. Each expansion board has a unique ID that can be read out of an EEPROM or MCU on the board, which enables software tools to recognize the connected hardware and automatically select the appropriate firmware image. The target MCU card can also be detached from the UDP and used alone as a development or demonstration tool.

Figure 9 shows the C8051F96x MCU card.

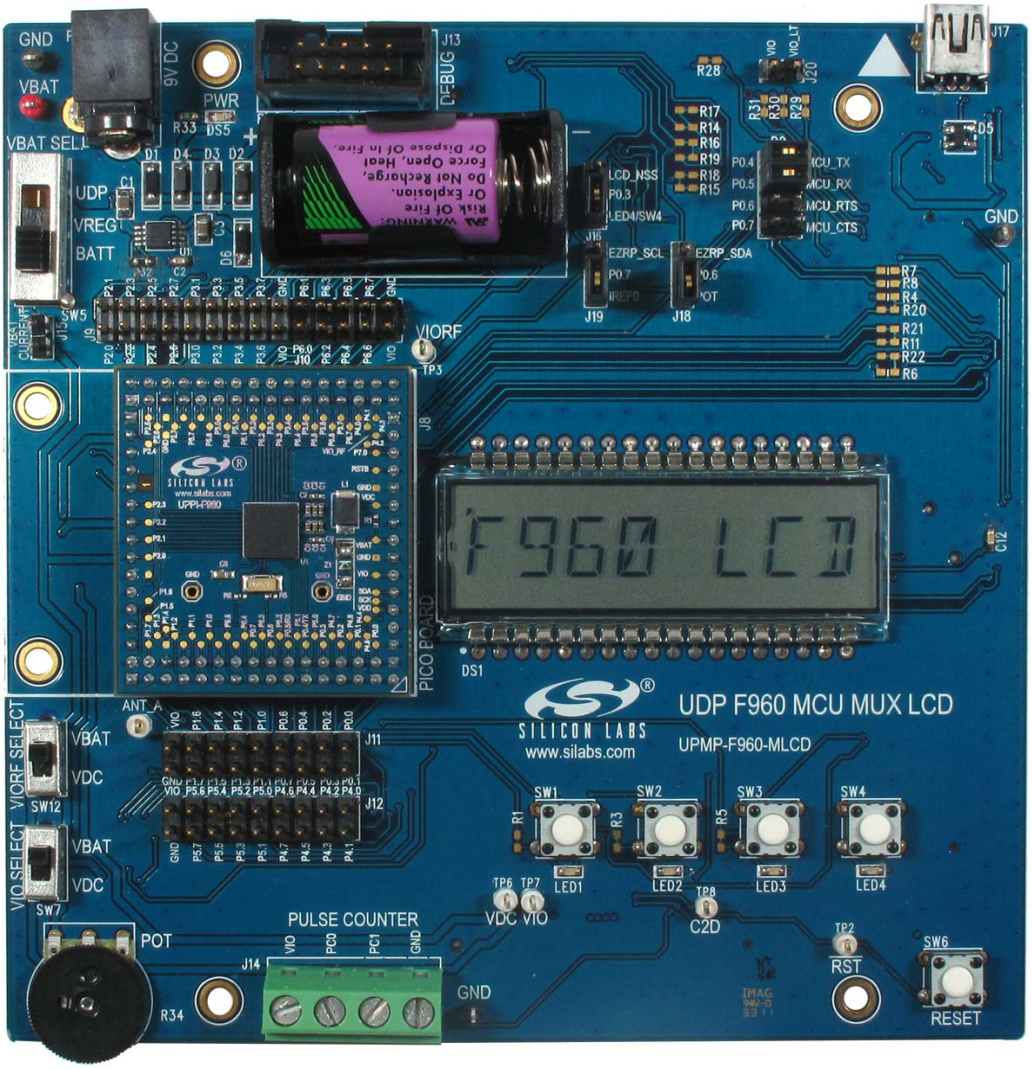

Figure 9. C8051F96x UDP MCU Card

Figure 10 highlights some of the features of the UDP C8051F960/Si1020 MCU Card with Multiplexed LCD.

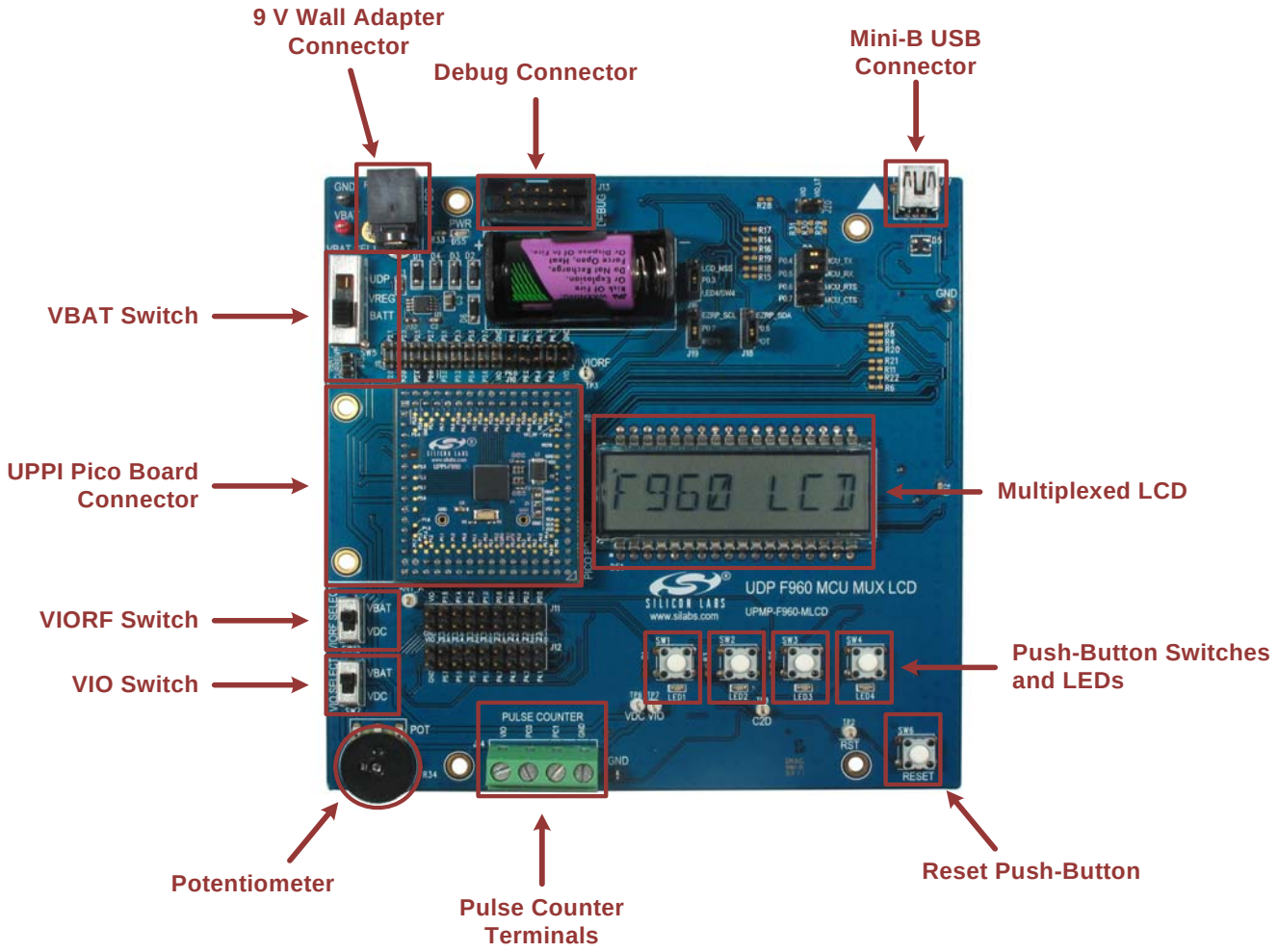

Figure 10. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD MCU Card

5.1. UPPI Pico Board Connector (J5, J6, J7, J8)

The UPPI Pico Board connector accommodates a variety of C8051F96x and Si102x/3x UPPI Pico Boards. The C8051F960 MCU and Si1020 Wireless MCU UPPI Pico Boards share a common form factor. This enables the MCU card to support a wide variety of wired and wireless applications.

The supported UPPI Pico Boards include:

- UPPI-F960
- UPPI-Si1020GMxxxTR

The Si1020/30 UPPI Pico Boards include an EZRadioPRO® transceiver. The C8051F960 UPPI Pico Boards do not include an RF transceiver; instead, these boards support most Silicon Labs 40-pin radio test cards when used with the Unified Development Platform Motherboard.

5.2. Multiplexed LCD Display (DS1)

The C8051F960 MCU Card with Multiplexed LCD includes a 4-mux, 128-segment alphanumeric LCD. The LCD has eight 14-segment characters and includes decimal points and apostrophes. The large display is easy to read from a distance.

The LCD display uses all of the C8051F960/Si1020 common and segment LCD pins, leaving 21 pins available on the C8051F960 for other purposes. For applications that do not require an LCD and need additional I/O, the UDP C8051F960 MCU card with EMIF (UPMP-F960-EMIF) has 57 available I/O pins when used with the C8051F960 UPPI Pico Board.

The provided example code makes using the alphanumeric display by calling a custom ANSI C printf function.

5.3. Push-Button Switches and LEDs (SW1-SW4, LED1-LED4)

The UDP C8051F960/Si1020 MCU Card with Multiplexed LCD has four push-button switches. The four switches connect to P0.0 through P0.3. The switches are normally open and pull the pin voltage to ground when pressed. When using P0.3 for SW4, install a shorting block on J16 connecting P0.3 to SW4/LED4.

Port pins P0.0 through P0.3 also connect to four LEDs: LED1 through LED4. The LEDs connect to VIO through a current limiting resistor.

This multiplexing arrangement reduces the number of port pins used from eight to four. Firmware may easily use either the LED or the switch for each port pin. When using both the LED and the switch on the same port pin, firmware must momentarily toggle off the LED by writing a 1 to the pin's port latch to read the push-button switch status.

5.4. VBAT Selection Switch (SW5)

The UDP C8051F960/Si1020 MCU Card with Multiplexed LCD has many power options. The VBAT selector switch (SW5) selects the power source for the main C8051F960/Si1020 VBAT supply pin.

The center VREG position selects the output of the on-board 3.3 V regulator (U1). This is the primary supply option for development. The on-board regulator has multiple 5 V and 9 V power sources connected via Schottky diodes to the regulator input. The highest voltage power source will supply power to the regulator.

The power sources for the on-board regulator (U1) are as follows:

- 9 V DC Wall Adapter power receptacle (P1).
- Mini-B USB receptacle (J17).
- 10-pin Debug connector (J13).
- UDP motherboard +5 V (when connected).

The BATT position selects the ultra long life 3.6 V lithium thionyl chloride battery (BT1). This battery is a typical power source for metering applications. The on-board regulator should be used primarily for development because the battery has a limited peak current capacity.

The UDP position on the VBAT selector selects the UDP motherboard programmable supply (PWR_VDD_OUT) as the power source for the UPPI Pico Board. Use this position when using the programmable power supply under software control.

The UDP motherboard can also provide power to the on-board regulator. The VREG position will always work with the motherboard, while the UDP switch position requires some motherboard configuration. The UDP motherboard User's Guide contains additional information.

The VBAT voltage and ground are available on test points in the top-left corner of the MCU card. Use these test points to power the board from an external lab power supply. When using a lab supply, the VBAT selector switch should be in the BATT position with the battery removed.

5.5. Debug Header (J13)

The standard 10-pin debug header supports the Silicon Labs USB Debug Adapter. This connector provides a C2 debug connection to C8051F960/Si1020 on the UPPI Pico Board. The USB Debug Adapter supports two types of debug connections: C2 and JTAG. When using this MCU card with the Silicon Labs IDE, select C2 in the connection options dialog before connecting.

The USB Debug Adapter also provides a 5 V power source that can power the regulator. When powering the MCU from the debug connector, the VBAT switch must be in the VREG position. Additionally, select the Power Target after the Disconnect check box in the Silicon Labs IDE connections options dialog to ensure the MCU always has power.

5.6. Reset Button (SW6)

The reset push-button switch is in the lower-right corner. Pushing this button will always reset the MCU. Note that pushing this button while the IDE is connected to the MCU will result in IDE disconnecting from the target.

5.7. Pin Power Supply Select Switches

The C8051F960/Si1020 MCU has two VIO pins: VIO and VIORF. These VIO pins set the logic level and drive voltage for the MCU port pins. The VIORF pin sets the level for the port pins normally supporting radio functionality: P1.5 through P2.3. The Si1020 P2.0-2.3 pins are connected internally to the EZRadioPRO. The VIO pin sets the level for all other port pins.

5.7.1. VIORF Select Switch (SW12)

When using the dc-dc buck converter to power the radio, set the VIORF selector switch to the VDC position. This connects the output of the buck converter to the VIORF pin. When using the Si1020, this switch also selects the power source for the radio. In this position, firmware controls the voltage on the VDC pin. The C8051F960/Si1020 buck converter also has a bypass switch that can power the radio from the full supply voltage. The dc-dc buck converter and bypass switch are off by default after an MCU reset, so the VDC pin voltage is floating until firmware turns on the bypass switch or configures the dc-dc converter.

When the VIORF selector switch is set to the VBAT position, the VIORF pin connects via hardware to the VBAT pin. In this position, the dc-dc buck converter cannot power the radio.

The VBAT position powers the VIORF pin without any firmware. This position is more convenient for simple code examples. Use this position for the code examples provided unless otherwise indicated.

5.7.2. VIO Select Switch (SW7)

The VIO selector switch provides the same functionality as the VIORF switch for the main VIO pin. Normally this switch should be in the VBAT position, which will set the drive and input levels of the pins to VBAT.

Setting the switch to the VDC position connects the VIO pin to the output of the buck converter. In this position, the battery powers the MCU, and all of the I/O ports operate at a lower voltage set by the buck converter. This option is best if most of the I/O pins connect to a low voltage radio or other low-voltage peripherals. Most applications should use the VBAT position.

The C2 connection requires a VIO power source and VDC is not powered by default, so the VBAT position must be used for initial development.

5.8. UART VCP Connection Options

The MCU card features a USB virtual COM port (VCP) UART connection via the mini-B USB connector (J17). The VCP connection uses the CP2102 USB-to-UART bridge chip.

The UART pins on the target MCU either connect to the CP2102 USB-to-UART bridge chip or to the UDP motherboard. The MCU card has level translators with enables that normally route the UART connections to the on-board USB-to-UART bridge chip. However, the UDP motherboard can drive the enable pins to route the UART connections to the UDP motherboard instead of the on-board USB-to-UART bridge chip. There are two enable signals: one with a default pull-down (UART_VCP_EN) and one with a default pull-up (UART_SYS_EN).

When using the UART with either the on-board USB-to-UART bridge or the UDP motherboard, install shorting blocks on header P12 to connect P0.4 to MCU_TX and P0.5 to MCU_RX.

If desired, install shorting blocks for hardware handshaking on P0.6 and P0.7 on the P12 header. Hardware handshaking is not required for most applications. Firmware must implement hardware handshaking on the target MCU using P0.6 and P0.7. The potentiometer and IREF current reference cannot be used on P0.6 and P0.7 if firmware assigns these pins to hardware handshaking, and the shorting blocks on J18 and J19 should be removed.

The MCU card includes provisions to facilitate ultra-low power measurements. The UART pins of the target MCU are completely disconnected from the USB-to-UART bridge by removing all the shorting blocks on P2. The VIO supply powers the level translator. To remove the level-shifter current from the ultra-low power measurement, cut the trace on the bottom of the board between the two pins of header J20. This will completely disconnect the level translators from VIO. After cutting this trace, a shorting block is required on J20 to use the USB-to-UART bridge or UDP UART connection.

5.9. Potentiometer (R34)

The potentiometer is available on P0.6. To use the potentiometer, install a shorting block on J18 to connect P0.6 to POT. To facilitate a low-power potentiometer, P1.4 connects to bottom of the potentiometer as a potentiometer enable (POT_EN). Drive P1.4 low to enable the potentiometer. Alternatively, install a 0 Ω resistor for R35 to continuously enable the potentiometer.

5.10. Pulse Counter Terminals (J14)

The MCU card includes a 4-position screw terminal connection. These field-wiring terminals will accept large wire for a commercial water or gas meter. The PC0 and PC1 signals connect to P1.0 and P1.1 on the target MCU. These are dedicated pins for the C8051F960/Si1020 low-power pulse counter. The VIO and ground connections are also available for Form C meters. Refer to the C8051F960 data sheet for additional information about the pulse counter.

5.11. Port Pin Headers (J9–J12)

All of the MCU port pins are available on the 0.100 inch headers on either side of the UPPI Pico Board.

Pins P1.2 and P1.3 are normally used for the RTC and are not connected by default to the P1.2 and P1.3 headers. To use P1.2 and P1.3 for other purposes, remove the RTC crystal on the UPPI Pico Board and populate the two small adjacent resistors with 0 Ω resistors.

When using the Si1020 UPPI Pico Board, the SPI1 pins are connected internally and do not connect to the header pins.

5.12. MCU with Muxed LCD Board Default and Optional Connections

The MCU card has many default and optional connections for use with different radios and the UDP motherboard. The default connections are via shorting jumpers. The shorting jumpers are a 603 resistor footprint with a cut trace between pads. To disconnect, cut the trace with a sharp utility knife. To reconnect, install a 0 Ω 603 resistor or connect the two pads with solder. The optional connections are non-populated (no-pop) resistor footprints. To connect, install a 0 Ω 603 resistor or connect the two pads with solder.

When using the Si1020 UPPI Pico Board, some of the MCU port pins connect by default to EZRadioPRO port pins. Note that plugging the UPPI Pico Board into the MCU card will connect some pins together.

Table 1 shows a summary of the default and optional connections for each pin.

Table 1. MCU Pin Functions

MCU Pin	MCU Card Function			UDP Motherboard Signal		
	Default	Optional	Optional	Default	Optional	Optional
P0.0	SW1/LED1	VREF				
P0.1	SW2/LED2	GPIO_0			EZRP_TX_DATA_IN	
P0.2	SW3/LED3	GPIO_2			EZRP_RX_CLKOUT	
P0.3	SW4/LED4				SPI_LCD_NSS	
P0.4/TX	TX					
P0.5/RX	RX					
P0.6		POT	CTS		EZR_I2C_SDA	EZR_ARSSI
P0.7		IREF	RTS		EZR_I2C_SCL	EZR_CLKIN
P1.0	PC0					
P1.1	PC1					
P1.2	XTAL3					
P1.3	XTAL4					
P1.4	POT_EN				RF_EBID_NSS	
P1.5	GPIO_1			EZRP_RX_DOUT		
P1.6	nIRQ			EZRP_NIRQ		
P1.7	SDN			EZRP_SDN		
P2.0/SCK1				EZRP_SCK	SPI_LCD_SCK	EBID_SCK
P2.1/MISO1				EZRP_MISO	SPI_LCD_MISO	EBID_MISO
P2.2/MOSI1				EZRP_MOSI	SPI_LCD_MOSI	EBID_MOSI
P2.3/NSS1				EZRP_NSS		
P2.4/COM0	COM0			PIEZO		
P2.5/COM1	COM1					
P2.6/COM2	COM2					
P2.7/COM3	COM3					
P3.0/LCD0	LCD0					
P3.1/LCD1	LCD1					
P3.2/LCD2	LCD2					
P3.3/LCD3	LCD3					
P3.4/LCD4	LCD4					

Table 1. MCU Pin Functions (Continued)

MCU Pin	MCU Card Function			UDP Motherboard Signal		
	Default	Optional	Optional	Default	Optional	Optional
P3.5/LCD5	LCD5					
P3.6/LCD6	LCD6					
P3.7/LCD7	LCD7					
P4.0/LCD8	LCD8					
P4.1/LCD9	LCD9					
P4.2/LCD10	LCD10					
P4.3/LCD11	LCD11					
P4.4/LCD12	LCD12					
P4.5/LCD13	LCD13					
P4.6/LCD14	LCD14					
P4.7/LCD15	LCD15					
P5.0/LCD16	LCD16					
P5.1/LCD17	LCD17					
P5.2/LCD18	LCD18					
P5.3/LCD19	LCD19					
P5.4/LCD20	LCD20					
P5.5/LCD21	LCD21					
P5.6/LCD22	LCD22					
P5.7/LCD23	LCD23					
P6.0/LCD24	LCD24					
P6.1/LCD25	LCD25					
P6.2/LCD26	LCD26					
P6.3/LCD27	LCD27					
P6.4/LCD28	LCD28					
P6.5/LCD29	LCD29					
P6.6/LCD30	LCD30					
P6.7/LCD31	LCD31					

5.12.1. P0.0

Pin P0.0 connects to LED1/SW1 by default. Optionally, P0.1 can connect to the VREF capacitor. To use the VREF instead of LED1/SW1, cut the trace on R1 and install a 0 Ω resistor on R2.

5.12.2. P0.1

P0.1 normally connects to LED2/SW2. P0.1 can optionally connect to EZRP_TX_DATA_IN. To use EZRP_TX_DATA_IN instead of LED2/SW2, cut the trace on R3 and install a 0 Ω resistor on R4.

5.12.3. P0.2

Pin P0.2 normally connects to LED3/SW3. Optionally, P0.2 connects to EZRP_RX_CLK_IN. To use EZRP_RX_CLK_IN instead of LED2/SW2, cut the trace on R5 and install a 0 Ω resistor on R6.

5.12.4. P0.3

Pin P0.3 connects to either LED4/SW4 or SPI_LCD_NSS, selected by J16. SPI_LCD_NSS is the SPI slave select when using the Graphic LCD I/O card with the UDP Motherboard and this C8051F96x MCU card.

5.12.5. P0.6

P0.6 connects to either the potentiometer (POT) or EZRP_I2C_SDA, selected by J18. This signal supports I2C radios using the 40-pin radio connector on the UDP motherboard. Removing the shorting jumpers from J18 and populating R7 connects P0.6 to the EZR_ARSSI signal. This signal supports EZRadio transceivers using the 40-pin radio connector on the UDP motherboard.

5.12.6. P0.7

Pin P0.7 connects to either the IREF0 current reference or EZRP_I2C_SCL, selected by J19. This signal supports I2C radios using the 40-pin radio connector on the UDP motherboard. Removing the shorting jumpers from J19 and populating R8 connects P0.7 to the EZR_CLK_IN signal. This signal supports EZRadio transceivers using the 40-pin radio connector on the UDP motherboard.

5.12.7. P1.4

P1.4 normally connects to the potentiometer enable (POT_EN) signal. P1.4 can optionally connect to RF_EBID_NSS, which allows the C8051F960 UPPI Pico Board to access the EBID on the 40-pin radio card. To use RF_EBID_NSS instead of LED2/SW2, cut the trace on R9 and install a 0 Ω resistor on R10.

5.12.8. P1.5

Pin P1.5 connects to GPIO_1 via R11 and R21 by default. To disconnect these signals, cut the trace on R11. This signal supports the clear-to-send (CTS) signal for EZRadioPRO.

5.12.9. P1.6

P1.6 normally connects to nIRQ through R12. Cut the trace on R12 to disconnect these signals. P1.6 also connects to nIRQ on the UPPI Pico Board, so a trace must also be cut on the UPPI Pico Board.

5.12.10. P1.7

Pin P1.7 normally connects to SDN via R13. To disconnect these signals, cut the trace on R13. Note that P1.7 also connects to SDN on the UPPI Pico Board. Therefore, it is necessary to also cut a trace on the UPPI Pico Board.

5.12.11. P2.0 through P2.2

P2.0 through P2.3 connect internally on the Si1020.

For the C8051F960 UPPI Pico Board, pin P2.0 connects to SPI_LCD_SCK via R14, P2.1 connects to SPI_LCD_MISO via R15, and P2.2 connects to SPI_LCD_MOSI through R16 by default. When the MCU card is connected to a UDP motherboard, these signals support the Graphic LCD I/O card.

In addition to the Graphic I/O LCD signals, these pins also support the EZRadioPRO SPI interface on the UDP motherboard.

These pins can also optionally be used as SPI connections for reading the 40-pin radio test card EBID by populating the R17, R18, and R19 pads with 0 Ω resistors.

5.12.12. EZRadio GPIO Signals

When using a Si1020 UPPI Pico Board, the four EZRadioPRO GPIO signals connect to the SMA connectors on the motherboard.

GPIO_0 connects to EZRP_TX_DATA_IN via R20. This signal supports direct mode TX input data from an external source using the SMA connector.

GPIO_1 connects to EZRP_RX_DOUT via R21. This signal supports direct mode RX data out of the SMA connector. Normally, the RX data out is used with the RX clock out.

GPIO_2 connects to EZRP_RX_CLK_OUT via R22. This signal supports direct mode RX data out of the SMA connector.

ANT_A connects to EZR_CLK_IN using R23. This provides a connection to the forth SMA connector. Cut the trace on R23 when using an external 10 MHz clock with EZRadio.

6. Using the C8051F96x with the UDP Motherboard

6.1. VBAT Selector Switch

When used with the UDP Motherboard, the motherboard can power the C8051F96x MCU card. With the VBAT selector switch in the VREG position, the motherboard powers the regulator on the card. With the VBAT selector switch in the UDP position, the UDP motherboard powers VBAT directly. This position supports software control of the variable voltage power supply and current measurements.

The S1 switch on the UDP motherboard selects between the fixed or programmable voltage. The variable supply is controlled by the C8051F384 board control MCU through the U1 digital potentiometer. Use the fixed supply when the variable supply is not under software control.

6.2. MCU Card Header Connections

The MCU card has four connectors with 100 pins each. These 400 pins are directly tied to the UDP motherboard and I/O cards. These signals are named and designed to support a wide variety of features and applications, and the UDP C8051F960/Si1020 MCU Card with Multiplexed LCD card implements a subset of these connections.

The MCU cards and I/O cards are designed so that a maximum number of functions are shared between each card. This allows a particular type of I/O card to be shared amongst all MCU cards that connect to the same signals.

The MCU card slot includes the following components:

J1 MCU card connector H1
J2 MCU card connector H2
J3 MCU card connector H3
J4 MCU card connector H4

The UDP C8051F960/Si1020 MCU Card with Multiplexed LCD card implements the signals described in Table 3, Table 4, Table 5, and Table 6 in the Appendix.

6.3. Shorting Blocks: Factory Defaults

The UDP C8051F960/Si1020 MCU Card with Multiplexed LCD MCU Card comes from the factory with pre-installed shorting blocks on several headers. Figure 11 shows the positions of the factory default shorting blocks.

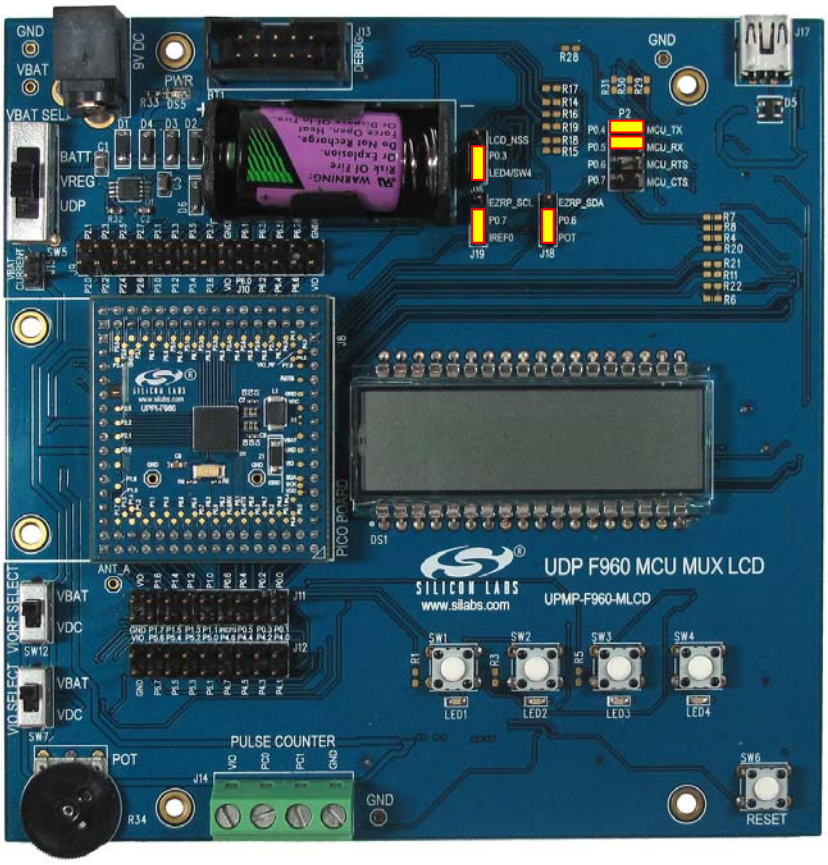

Figure 11. Shorting Blocks: Factory Defaults

Shorting blocks are installed on P2 to connect P0.4 to MCU_TX and P0.5 to MCU_RX. A shorting block is installed on J16 to connect P0.3 to LED4/SW4/LED4. Shorting blocks are installed on J19 to connect P0.7 to IREF and on J18 to connect P0.6 to POT.

7. Schematics

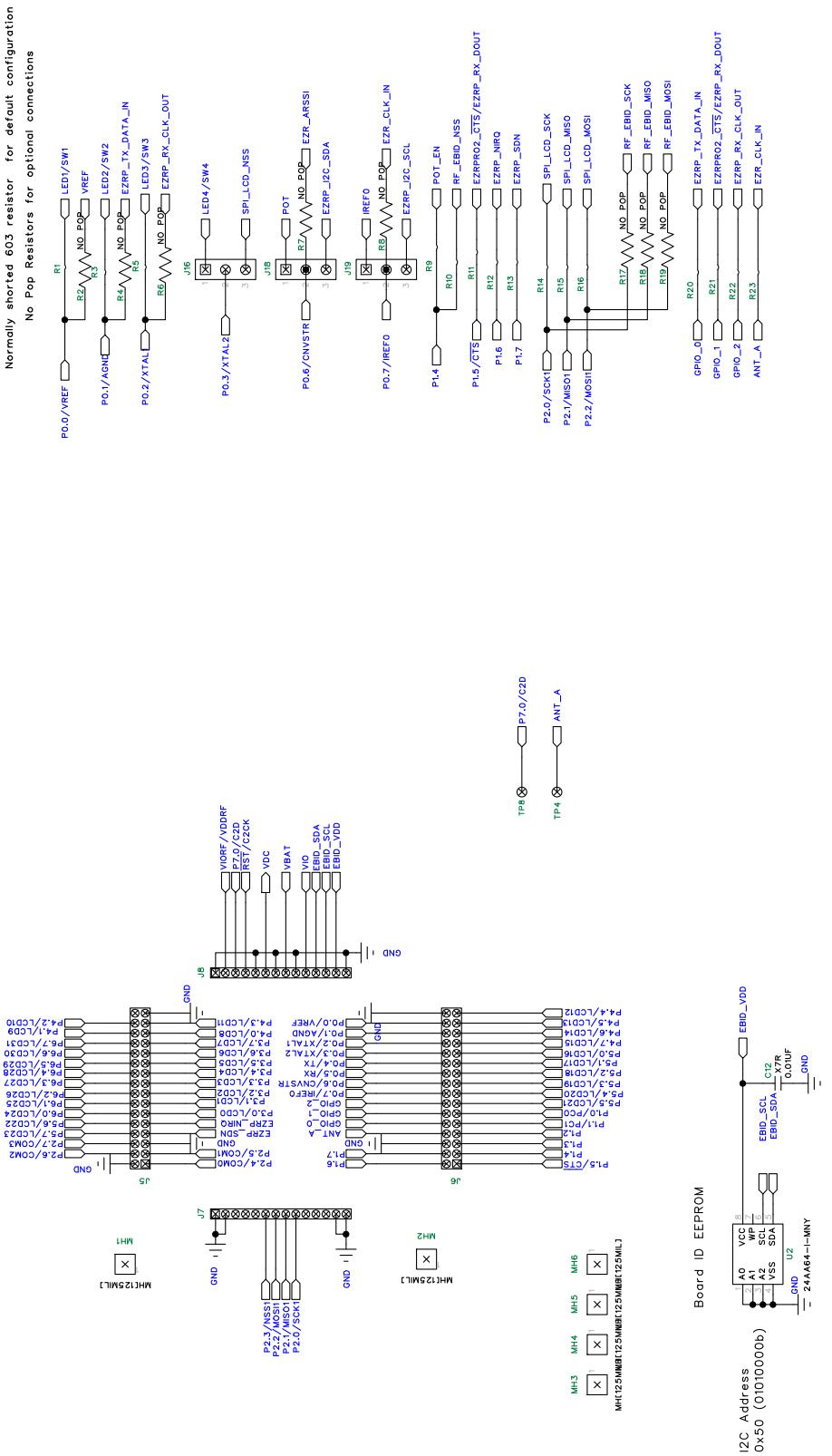

Figure 12. C8051F96x UDP MCU Card Schematic (1 of 6)

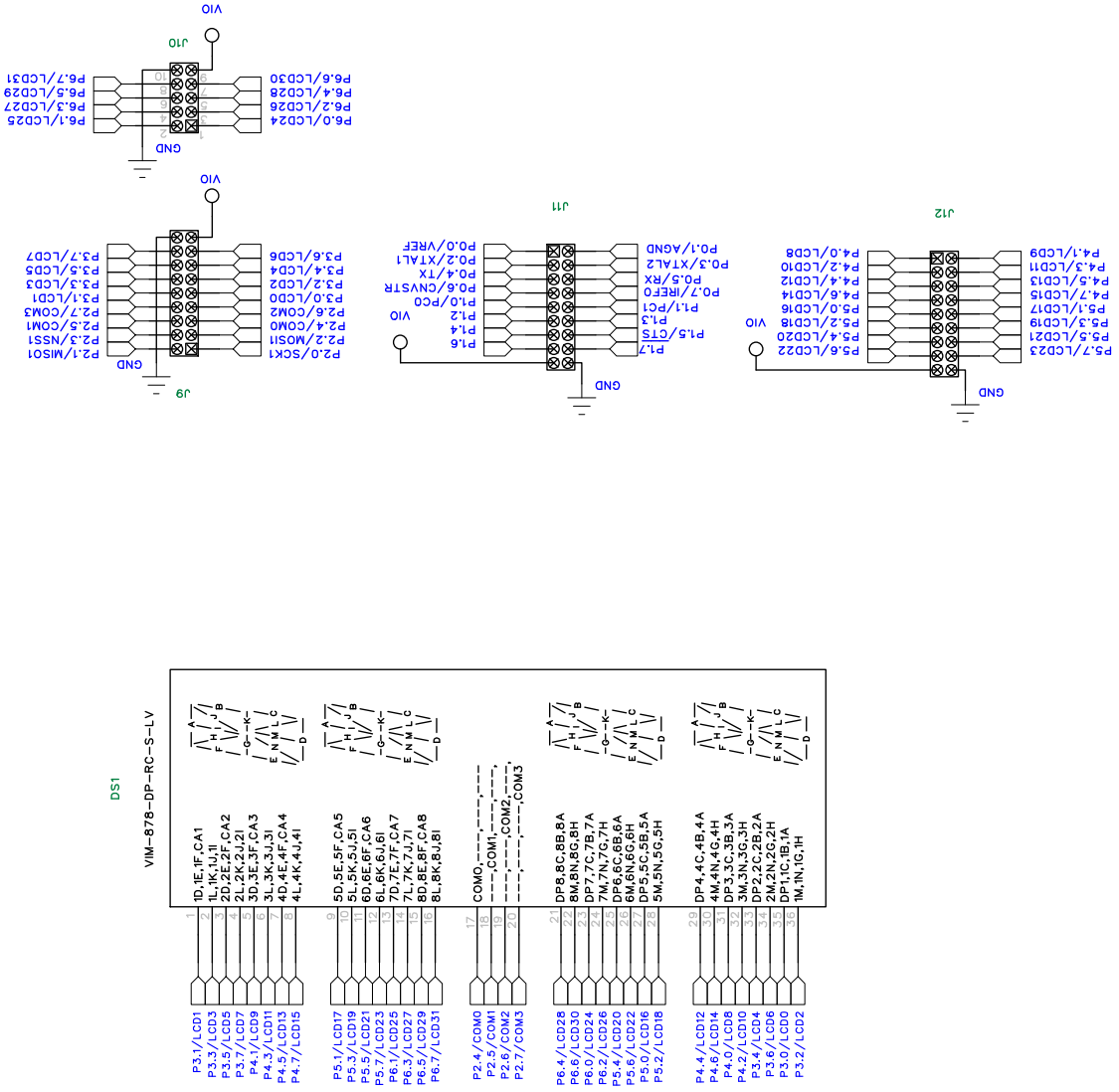

Figure 13. C8051F96x UDP MCU Card Schematic (2 of 6)

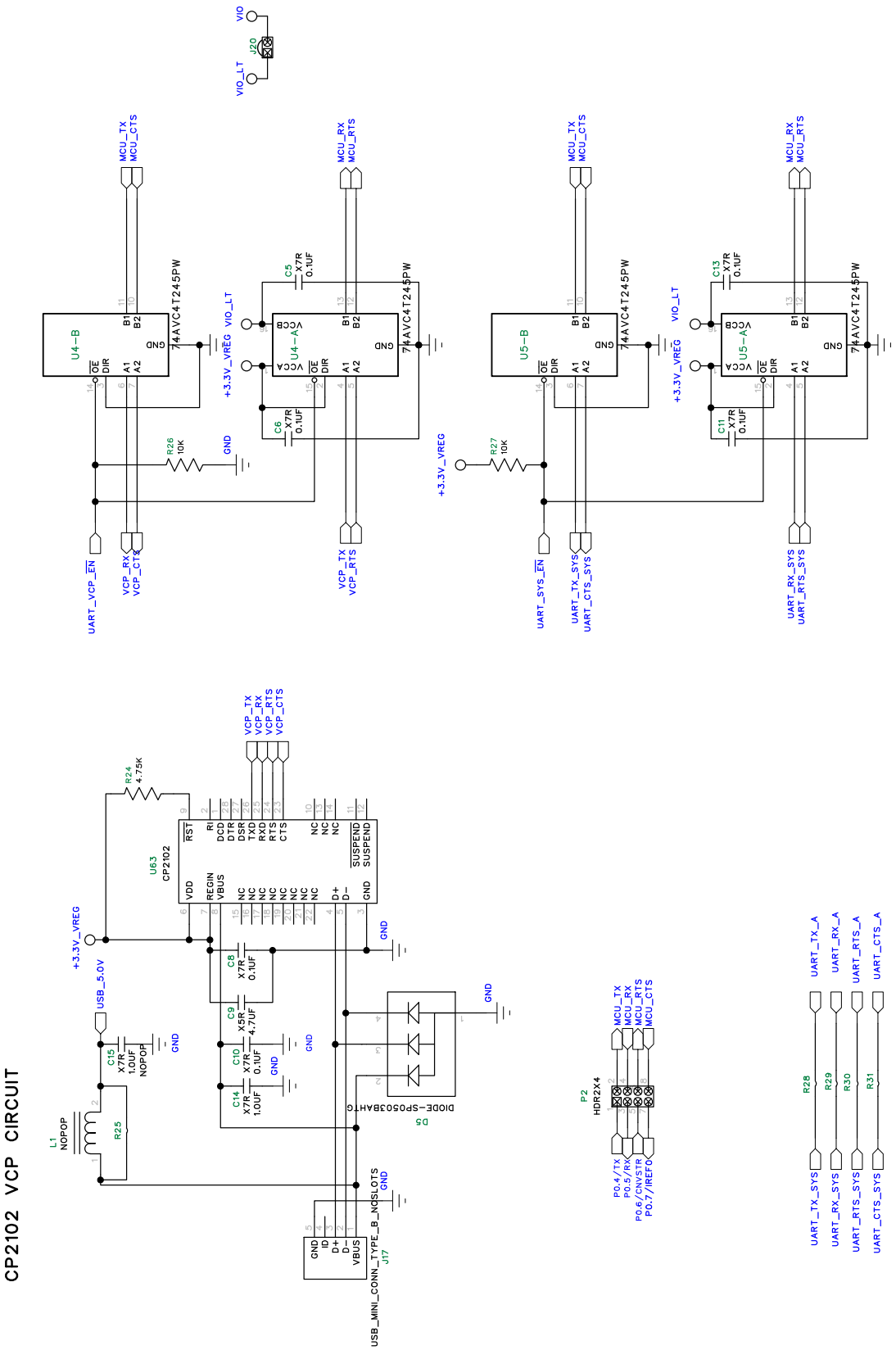

Figure 14. C8051F96x UDP MCU Card Schematic (3 of 6)

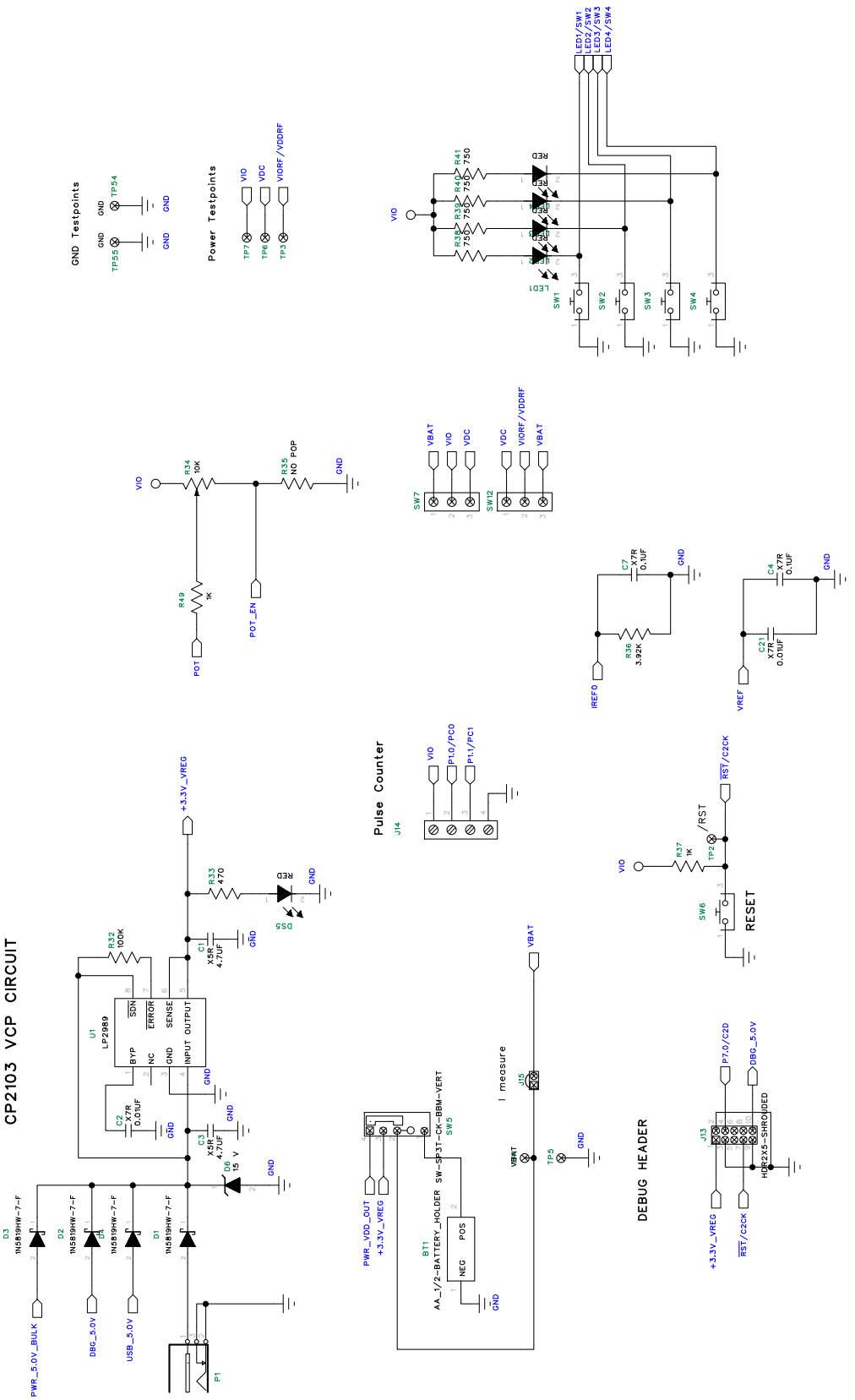

Figure 15. C8051F96x UDP MCU Card Schematic (4 of 6)

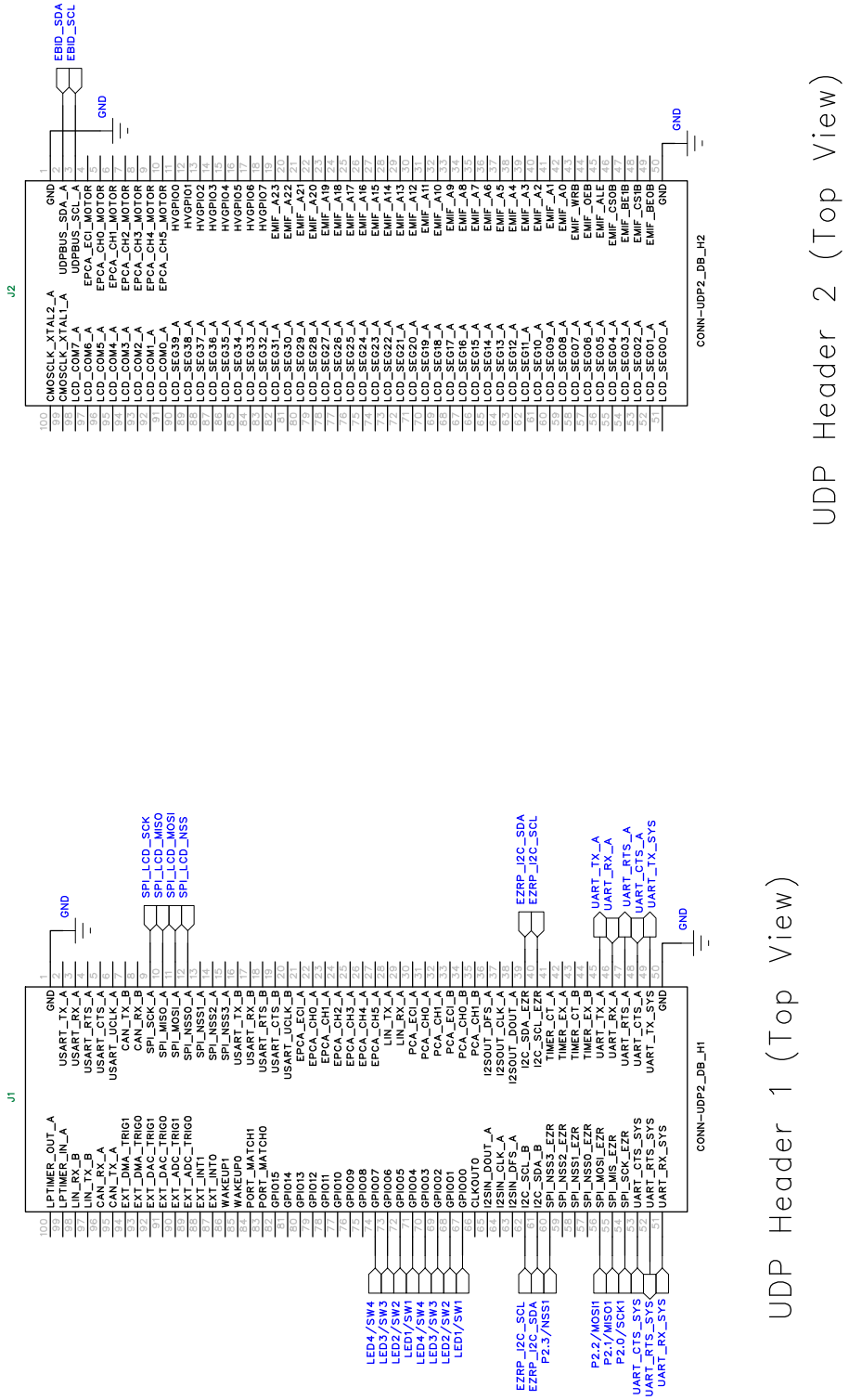

Figure 16. C8051F96x UDP MCU Card Schematic (5 of 6)

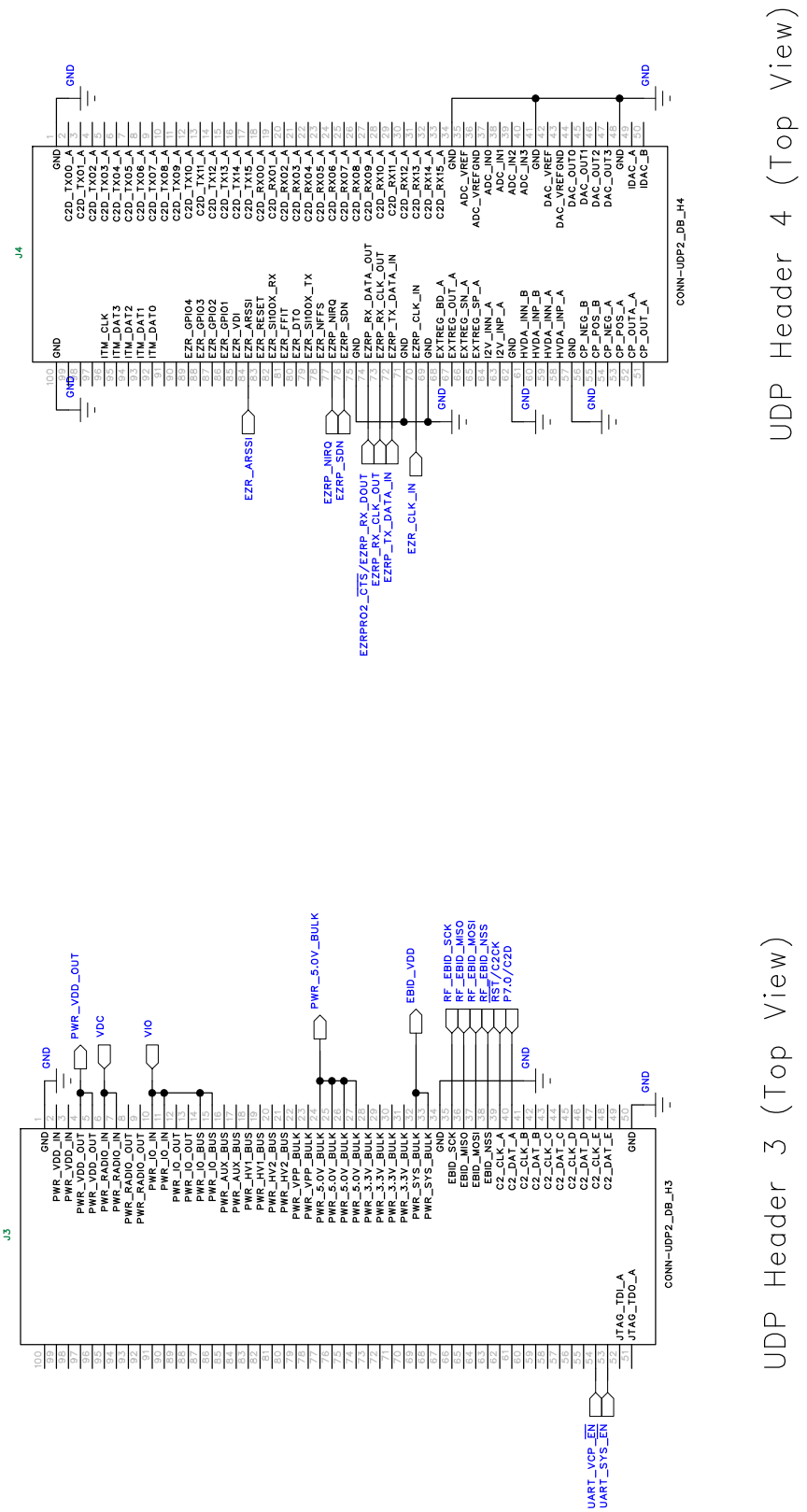

Figure 17. C8051F96x UDP MCU Card Schematic (6 of 6)

8. Bill of Materials

Table 2. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD Bill of Materials

Reference	Part Number	Source	Description
U2	24AA64T-I/MNY	Microchip Technology	64KBIT I2C SERIAL FLASH, 400kHZ, 8-TDFN
U4-5	SN74AVC4T245PWR	Texas Instruments	Quad Dual-Supply Level Shifter, TSSOP
BT1	12BH1/2AA-2P-GR	Eagle Plastic Devices	HOLDER BATTERY, 1/2 CELL AA, PCB MNT OR EQ, RoHS
C2, C12, C21	06035C103KAT2A	AVX Corporation	CAP, 0.01UF (10000PF), X7R, CERAMIC, 0603, 50V, ±10%, OR EQ, RoHS
C4-8, C10-11, C13	C0603C104J3RACTU	Kemet	CAP, 0.1UF, X7R, CERAMIC, 0603, 25V, ±5%, OR EQ, RoHS
C14	GRM188R71A105KA61D	Murata Electronics North America	CAP CERAMIC, 1.0UF, X5R, 0603, 10V, ±10%, RoHS
C15	GRM188R71A105KA61D	Murata Electronics North America	CAP CERAMIC, 1.0UF, X5R, 0603, 10V, ±10%, RoHS, NOPOP
C1, C3, C9	EMK212BJ475KG-T	Taiyo Yuden	CAP, 4.7UF, X5R, CERAMIC, 0805, 16V, ±10%, OR EQ, RoHS
P1	RAPC722X	Switchcraft Inc.	CONN, POWERJACK MINI.08" RA PC MNT, RoHS
J1-4	FX8-100P-SV1(91)	Hirose Electric Co Ltd	CONN, HDR, 100POS, .6MM, GOLD, SMD, RoHS
U63	CP2102	Silicon Labs	SINGLE-CHIP USB TO UART BRIDGE, QFN28, RoHS
D1-4	1N5819HW-7-F	Diodes Inc	DIODE SCHOTTKY, 40V, 1A, SOD123, RoHS
D6	MMSZ5245B-7-F	Diodes Inc	DIODE, ZENER, 15V, 500MW, SMT, SOD123, RoHS
D5	SP0503BAHTG	Littelfuse	TVS AVAL DIODE ARRAY, 3 CH, SOT143, RoHS
J16, J18-19	PBC03SAAN	Sullins Connector Solutions	STAKE HEADER, 1X3, 0.1" CTRS, OR EQ, RoHS
J7-8	25631401RP2	Norcomp Inc.	14POS, 2MM VERT SGL ROW RECEPTACLE
J15, J20	PBC02SAAN	Sullins Connector Solutions	STAKE HEADER, 1X2, 0.1"CTR, GOLD, OR EQ, RoHS, NOPOP
P2	PBC04DAAN	Sullins Connector Solutions	STAKE HEADER, 2X4, 0.1"CTR, OR EQ, RoHS
J10	PBC05DAAN	Sullins Connector Solutions	STAKE HEADER, 2X5, 0.1"CTR, GOLD, OR EQ, RoHS
J9, J11-12	PBC09DAAN	Sullins Connector Solutions	STAKE HEADER, 2X9, 0.1' CTR GOLD, OR EQ, RoHS
J5-6	A3C-32DA-2DSC(71)	Hirose Electric Co Ltd	HEADER RECEPTACLE, 32 POS, 2MM, DUAL ROW
J13	N2510-6002-RB	3M	HEADER, SHROUDED, 2X5, OR EQ, RoHS

Table 2. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD Bill of Materials (Continued)

Reference	Part Number	Source	Description
L1	NLV25T-R68J-PF	TDK	INDUCTOR, POWER, 0.68UH, 1008 SMD, RoHS, NOPOP
DS1	VIM-878-DP-RC-S-LV	Varitronix	LCD 8-CHAR, 14-SEG 0.275" REFL, (153-1115-ND), RoHS
DS5, LED1-4	SML-LX0603IW-TR	Lumex Opto/Components Inc	LED, RED DIFF, 635NM, SMT0603, OR EQ, RoHS
U1	LP2989AIMM-3.3/NOPB	National Semiconductor	LDO REG, 500MA, ADJ, MSOP, RoHS
R34	RV100F-30-4K1B-B10K-B301	Alpha (Taiwan)	POT, 10K, THUMBWHEEL LINEAR, 0.03W, ±20%, OR EQ, RoHS
R32	ERJ-3GEYJ104V	Panasonic - ECG	RES, 100K, SMT, 0603, 1/10W, ±5%, OR EQ, RoHS
R26-27	ERJ-3EKF1002V	Panasonic - ECG	RES, EQ. 10.0K OHM, SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
R37, R49	ERJ-3EKF1001V	Panasonic - ECG	RES, 1K OHM, SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
R36	ERJ-3EKF3921V	Panasonic - ECG	RES, 3.92K OHM, SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
R24	ERJ-3EKF4751V	Panasonic - ECG	RES, 4.75K OHM , SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
R33	MCR03EZPJ471	Rohm Semiconductor	RES, 470 OHM, SMT, 0603, 1/10W, ±5%, OR EQ, RoHS
R38-41	ERJ-3EKF7500V	Panasonic - ECG	RES, 750 OHM, SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
R2, R4, R6-8, R17-19, R35			RES, SMT, 0603, OR EQ, RoHS, NOPOP
R1, R3, R5, R9-16, R20-23, R25, R28-31			0603 SHORT, NOPOP
SW7, SW12	OS102011MS2QN1	C&K Components	SWITCH, SPDT, 12VDC, OR EQ, RoHS
SW1-4, SW6	EVQ-PAD04M	Panasonic - ECG	SWITCH, LIGHT TOUCH, 130GF, 6MM SQ, RoHS
SW5	OS103012MU1QP1	C&K Components	SWITCH SLIDE SP3T COMPACT PIN, PCB MNT, OR EQ, RoHS
J14	1729144	Phoenix Contact	CONN TERM BLOCK, 5.08MM CTRS PCB, 4 POS, RoHS
J17	54819-0519	Molex Inc	CONN, USB MINI RECEPT, 5POS RT ANG, TYPE B OR EQ, RoHS

APPENDIX—MCU CARD HEADER PIN DESCRIPTIONS

Table 3. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H1 Pin Descriptions (J1)

MCU Card Pin	Signal Name	Usage
1	GND	
2	USART_TX_A	
3	USART_RX_A	
4	USART_RTS_A	
5	USART_CTS_A	
6	USART_UCLK_A	
7	CAN_TX_B	
8	CAN_RX_B	
9	SPI_SCK_A	Graphical LCD I/O Card SPI clock
10	SPI_MISO_A	Graphical LCD I/O Card SPI master-in, slave-out
11	SPI_MOSI_A	Graphical LCD I/O Card SPI master-out, slave-in
12	SPI_NSS0_A	Graphical LCD I/O Card SPI slave select
13	SPI_NSS1_A	
14	SPI_NSS2_A	
15	SPI_NSS3_A	
16	USART_TX_B	
17	USART_RX_B	
18	USART_RTS_B	
19	USART_CTS_B	
20	USART_UCLK_B	
21	EPCA_ECI_A	
22	EPCA_CH0_A	
23	EPCA_CH1_A	
24	EPCA_CH2_A	
25	EPCA_CH3_A	
26	EPCA_CH4_A	
27	EPCA_CH5_A	
28	LIN_TX_A	
29	LIN_RX_A	
30	PCA_ECI_A	
31	PCA_CH0_A	
32	PCA_CH1_A	
33	PCA_ECI_B	
34	PCA_CH0_B	
35	PCA_CH1_B	
36	I2SOUT_DFS_A	

Table 3. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H1 Pin Descriptions (J1)

MCU Card Pin	Signal Name	Usage
37	I2SOUT_CLK_A	
38	I2SOUT_DOUT_A	
39	I2C_SDA_EZR	EZRadio I2C data
40	I2C_SCL_EZR	EZRadio I2C clock
41	TIMER_CT_A	
42	TIMER_EX_A	
43	TIMER_CT_B	
44	TIMER_EX_B	
45	UART_TX_A	UART A transmit
46	UART_RX_A	UART A receive
47	UART_RTS_A	UART A hardware handshaking
48	UART_CTS_A	UART A hardware handshaking
49	UART_TX_SYS	System UART transmit
50	GND	
51	UART_RX_SYS	System UART receive
52	UART_RTS_SYS	System UART hardware handshaking
53	UART_CTS_SYS	System UART hardware handshaking
54	SPI_SCK_EZR	EZRadioPRO SPI clock (P2.0)
55	SPI_MISO_EZR	EZRadioPRO SPI master-in, slave-out (P2.1)
56	SPI_MOSI_EZR	EZRadioPRO SPI master-out, slave-in (P2.2)
57	SPI_NSS0_EZR	
58	SPI_NSS1_EZR	
59	SPI_NSS2_EZR	
60	SPI_NSS3_EZR	EZRadioPRO SPI slave select (P2.3)
61	I2C_SDA_B	EZRadioPRO I2C data
62	I2C_SCL_B	EZRadioPRO I2C clock
63	I2SIN_DFS_A	
64	I2SIN_CLK_A	
65	I2SIN_DOUT_A	
66	CLKOUT0	
67	GPIO00	LED1/SW1
68	GPIO01	LED2/SW2
69	GPIO02	LED3/SW3
70	GPIO03	LED4/SW4
71	GPIO04	LED1/SW1
72	GPIO05	LED2/SW2
73	GPIO06	LED3/SW3

Table 3. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H1 Pin Descriptions (J1)

MCU Card Pin	Signal Name	Usage
74	GPIO07	LED4/SW4
75	GPIO08	
76	GPIO09	
77	GPIO10	
78	GPIO11	
79	GPIO12	
80	GPIO13	
81	GPIO14	
82	GPIO15	
83	PORT_MATCH0	
84	PORT_MATCH1	
85	WAKEUP0	
86	WAKEUP1	
87	EXT_INT0	
88	EXT_INT1	
89	EXT_ADC_TRIG0	
90	EXT_ADC_TRIG1	
91	EXT_DAC_TRIG0	
92	EXT_DAC_TRIG1	
93	EXT_DMA_TRIG0	
94	EXT_DMA_TRIG1	
95	CAN_TX_A	
96	CAN_RX_A	
97	LIN_TX_B	
98	LIN_RX_B	
99	LPTIMER_IN_A	
100	LPTIMER_OUT_A	

Table 4. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H2 Pin Descriptions (J2)

MCU Card Pin	Signal Name	Usage
1	GND	
2	UDPBUS_SDA_A	Electronic Board ID I2C data
3	UDPBUS_SCL_A	Electronic Board ID I2C clock
4	EPCA_ECI_MOTOR	
5	EPCA_CH0_MOTOR	
6	EPCA_CH1_MOTOR	
7	EPCA_CH2_MOTOR	
8	EPCA_CH3_MOTOR	
9	EPCA_CH4_MOTOR	
10	EPCA_CH5_MOTOR	
11	HVGPIO0	
12	HVGPIO1	
13	HVGPIO2	
14	HVGPIO3	
15	HVGPIO4	
16	HVGPIO5	
17	HVGPIO6	
18	HVGPIO7	
19	EMIF_A23	
20	EMIF_A22	
21	EMIF_A21	
22	EMIF_A20	
23	EMIF_A19	
24	EMIF_A18	
25	EMIF_A17	
26	EMIF_A16	
27	EMIF_A15	
28	EMIF_A14	
29	EMIF_A13	
30	EMIF_A12	
31	EMIF_A11	
32	EMIF_A10	
33	EMIF_A9	
34	EMIF_A8	
35	EMIF_A7	
36	EMIF_A6	
37	EMIF_A5	

Table 4. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H2 Pin Descriptions (J2)

MCU Card Pin	Signal Name	Usage
38	EMIF_A4	
39	EMIF_A3	
40	EMIF_A2	
41	EMIF_A1	
42	EMIF_A0	
43	EMIF_WRB	
44	EMIF_OEB	
45	EMIF_ALE	
46	EMIF_CS0B	
47	EMIF_BE1B	
48	EMIF_CS1B	
49	EMIF_BE0B	
50	GND	
51	LCD_SEG00_A	
52	LCD_SEG01_A	
53	LCD_SEG02_A	
54	LCD_SEG03_A	
55	LCD_SEG04_A	
56	LCD_SEG05_A	
57	LCD_SEG06_A	
58	LCD_SEG07_A	
59	LCD_SEG08_A	
60	LCD_SEG09_A	
61	LCD_SEG10_A	
62	LCD_SEG11_A	
63	LCD_SEG12_A	
64	LCD_SEG13_A	
65	LCD_SEG14_A	
66	LCD_SEG15_A	
67	LCD_SEG16_A	
68	LCD_SEG17_A	
69	LCD_SEG18_A	
70	LCD_SEG19_A	
71	LCD_SEG20_A	
72	LCD_SEG21_A	
73	LCD_SEG22_A	
74	LCD_SEG23_A	

Table 4. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H2 Pin Descriptions (J2)

MCU Card Pin	Signal Name	Usage
75	LCD_SEG24_A	
76	LCD_SEG25_A	
77	LCD_SEG26_A	
78	LCD_SEG27_A	
79	LCD_SEG28_A	
80	LCD_SEG29_A	
81	LCD_SEG30_A	
82	LCD_SEG31_A	
83	LCD_SEG32_A	
84	LCD_SEG33_A	
85	LCD_SEG34_A	
86	LCD_SEG35_A	
87	LCD_SEG36_A	
88	LCD_SEG37_A	
89	LCD_SEG38_A	
90	LCD_SEG39_A	
91	LCD_COM0_A	
92	LCD_COM1_A	
93	LCD_COM2_A	
94	LCD_COM3_A	
95	LCD_COM4_A	
96	LCD_COM5_A	
97	LCD_COM6_A	
98	LCD_COM7_A	
99	CMOSCLK_XTAL1_A	
100	CMOSCLK_XTAL2_A	

Table 5. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H3 Pin Descriptions (J3)

MCU Card Pin	Description	Usage
1	GND	
2	PWR_VDD_IN	
3	PWR_VDD_IN	
4	PWR_VDD_OUT	Programmable Supply from UDP to VBAT (VBAT Select set to UDP)
5	PWR_VDD_OUT	
6	PWR_RADIO_IN	VDC Output of DCDC to power 40-pin radio card
7	PWR_RADIO_IN	
8	PWR_RADIO_OUT	Power input for the radio card
9	PWR_RADIO_OUT	Power input for the radio card
10	PWR_IO_IN	VIO (controlled by VIO select)
11	PWR_IO_IN	
12	PWR_IO_OUT	
13	PWR_IO_OUT	
14	PWR_IO_BUS	VIO (controlled by VIO select)
15	PWR_IO_BUS	
16	PWR_AUX_BUS	
17	PWR_AUX_BUS	
18	PWR_HV1_BUS	
19	PWR_HV1_BUS	
20	PWR_HV2_BUS	
21	PWR_HV2_BUS	
22	PWR_VPP_BULK	
23	PWR_VPP_BULK	
24	PWR_5.0_BULK	5.0 V power from the UDP motherboard (Powers MCU Card regulator)
25	PWR_5.0_BULK	
26	PWR_5.0_BULK	
27	PWR_5.0_BULK	
28	VCC_3.3V	
29	VCC_3.3V	
30	VCC_3.3V	
31	VCC_3.3V	
32	PWR_SYS_BULK	3.3 V power supply for EBID EEPROM
33	PWR_SYS_BULK	
34	GND	
35	EBID_SCK	RF EBID SPI clock
36	EBID_MOSI	RF EBID SPI master-out, slave in
37	EBID_MISO	RF EBID SPI master-in, slave-out

Table 5. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H3 Pin Descriptions (J3)

MCU Card Pin	Description	Usage
38	EBID_NSS	RF EBID SPI slave select
39	C2_CLK_A	Reset/C2 interface clock
40	C2_DAT_A	P7.0/C2 interface data,
41	C2_CLK_B	
42	C2_DAT_B	
43	C2_CLK_C	
44	C2_DAT_C	
45	C2_CLK_D	
46	C2_DAT_D	
47	C2_CLK_E	
48	C2_DAT_E	
49	nc	
50	GND	
51	JTAG_TDO_A	
52	JTAG_TDI_A	
53	VCP_EN	Active-low enable for MCU Card VCP Bridge (default)
54	UART_SYS_EN	Active-low enable for MCU to UDP UART path
55	H3_55	
56	H3_56	
57	H3_57	
58	H3_58	
59	H3_59	
60	H3_60	
61	H3_61	
62	H3_62	
63	H3_63	
64	H3_64	
65	H3_65	
66	H3_66	
67	H3_67	
68	H3_68	
69	H3_69	
70	H3_70	
71	H3_71	
72	H3_72	
73	H3_73	
74	H3_74	

Table 5. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H3 Pin Descriptions (J3)

MCU Card Pin	Description	Usage
75	H3_75	
76	H3_76	
77	H3_77	
78	H3_78	
79	H3_79	
80	H3_80	
81	H3_81	
82	H3_82	
83	H3_83	
84	H3_84	
85	H3_85	
86	H3_86	
87	H3_87	
88	H3_88	
89	H3_89	
90	H3_90	
91	H3_91	
92	H3_92	
93	H3_93	
94	H3_94	
95	H3_95	
96	H3_96	
97	H3_97	
98	H3_98	
99	H3_99	
100	H3_100	

Table 6. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H4 Pin Descriptions (J4)

MCU Card Pin	Description	Usage
1	GND	
2	C2D_TX00_A	
3	C2D_TX01_A	
4	C2D_TX02_A	
5	C2D_TX03_A	
6	C2D_TX04_A	
7	C2D_TX05_A	
8	C2D_TX06_A	
9	C2D_TX07_A	
10	C2D_TX08_A	
11	C2D_TX09_A	
12	C2D_TX10_A	
13	C2D_TX11_A	
14	C2D_TX12_A	
15	C2D_TX13_A	
16	C2D_TX14_A	
17	C2D_TX15_A	
18	C2D_RX00_A	
19	C2D_RX01_A	
20	C2D_RX02_A	
21	C2D_RX03_A	
22	C2D_RX04_A	
23	C2D_RX05_A	
24	C2D_RX06_A	
25	C2D_RX07_A	
26	C2D_RX08_A	
27	C2D_RX09_A	
28	C2D_RX10_A	
29	C2D_RX11_A	
30	C2D_RX12_A	
31	C2D_RX13_A	
32	C2D_RX14_A	
33	C2D_RX15_A	
34	GND	
35	ADC_VREF	
36	ADC_VREFGND	
37	ADC_IN0	

Table 6. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H4 Pin Descriptions (J4)

MCU Card Pin	Description	Usage
38	ADC_IN1	
39	ADC_IN2	
40	ADC_IN3	
41	GND	
42	DAC_VREF	
43	DAC_VREFGND	
44	DAC_OUT0	
45	DAC_OUT1	
46	DAC_OUT2	
47	DAC_OUT3	
48	GND	
49	IDAC_A	
50	IDAC_B	
51	CP_OUT_A	
52	CP_OUTA_A	
53	CP_POS_A	
54	CP_NEG_A	
55	CP_POS_B	
56	CP_NEG_B	
57	GND	
58	HVDA_INP_A	
59	HVDA_INN_A	
60	HVDA_INP_B	
61	HVDA_INN_B	
62	GND	
63	I2V_INP_A	
64	I2V_INN_A	
65	EXTREG_SP_A	
66	EXTREG_SN_A	
67	EXTREG_OUT_A	
68	EXTREG_BD_A	
69	GND	
70	EZRP_CLK_IN	Radio card clock input (SMA connector)
71	GND	
72	EZRP_TX_DATA_IN	Radio card transmit data input (SMA connector)
73	EZRO_RX_CLK_OUT	Radio card receive clock output (SMA connector)
74	EZRP_RX_DATA_OUT	Radio card receive data output (SMA connector)

Table 6. UDP C8051F960/Si1020 MCU Card with Multiplexed LCD H4 Pin Descriptions (J4)

MCU Card Pin	Description	Usage
75	GND	
76	EZRP_SDN	Radio card shutdown
77	EZRP_NIRQ	Radio card active-low interrupt
78	EZR_NFFS	
79	EZR_SI100X_TX	
80	EZR_DTO	
81	EZR_FFIT	
82	EZR_SI100X_RX	
83	EZR_RESET	
84	EZR_ARSSI	EZRadio Analog RSSI
85	EZR_VDI	
86	EZR_GPIO0	
87	EZR_GPIO1	
88	EZR_GPIO2	
89	EZR_GPIO3	
90	EZR_GPIO4	
91	H4_91	
92	ITM_DAT0	
93	ITM_DAT1	
94	ITM_DAT2	
95	ITM_DAT3	
96	ITM_CLK	
97	H4_97	
98	H4_98	
99	H4_99	
100	GND	

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http://www.silabs.com/support
and register to submit a technical support request.

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.

UDP UPPI CARD USER'S GUIDE

1. Introduction

The UPPI-series evaluation cards are the engine of an MCU-based system, containing an MCU, optional radio, and minimal support circuitry.

These cards are designed around either a C8051F96xMCU or a Si102x/3x Wireless MCU. Only placement-critical items, such as bypass capacitors, crystals, dc-dc inductor, and RF front end circuitry are included. All other circuits reside on the hosting platform.

These cards are compatible with Silicon Labs Unified Development Platform MCU cards (UDP-F960-MCU series). They may also be used as prototyping modules, as they fit on a 2 mm-center prototyping board.

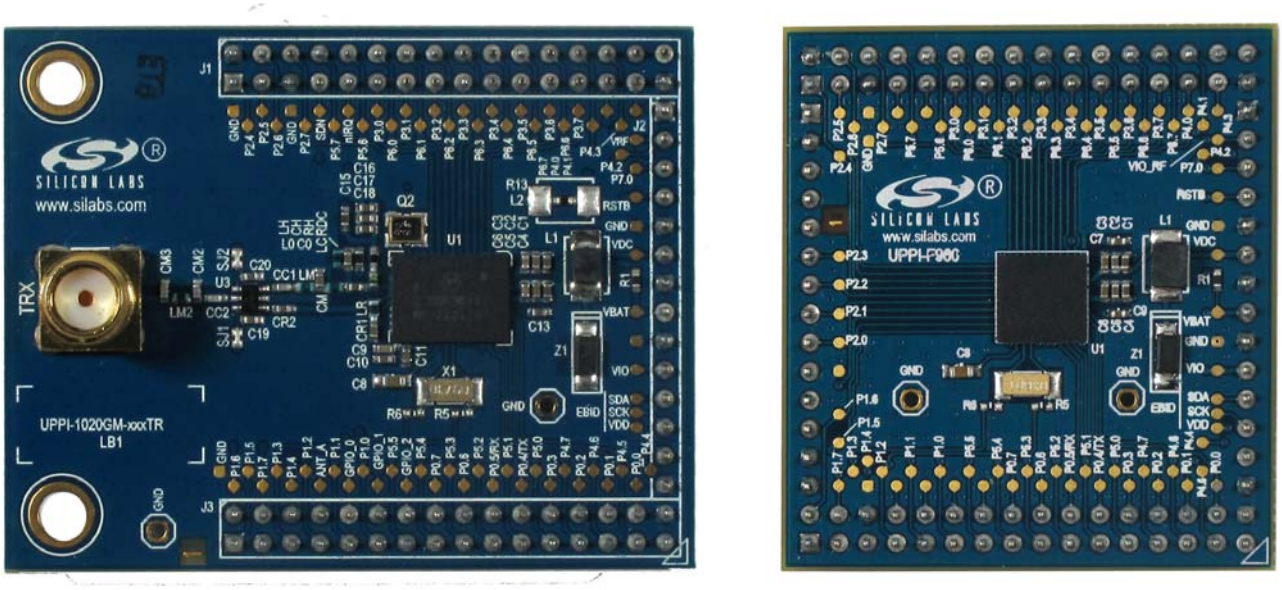


Figure 1. UPPI Cards with and without Radio

2. Description

The UPPI cards contain the MCU device and a minimal number of supporting components. Most of the core device pins are connected directly to headers, allowing signal mapping to be defined by the host board, typically a UDP MCU card. (See “2.3. Compatibility” for more information.)

Each board design varies in schematic and features. Refer to the board design files available from www.silabs.com for specifics.

2.1. Features

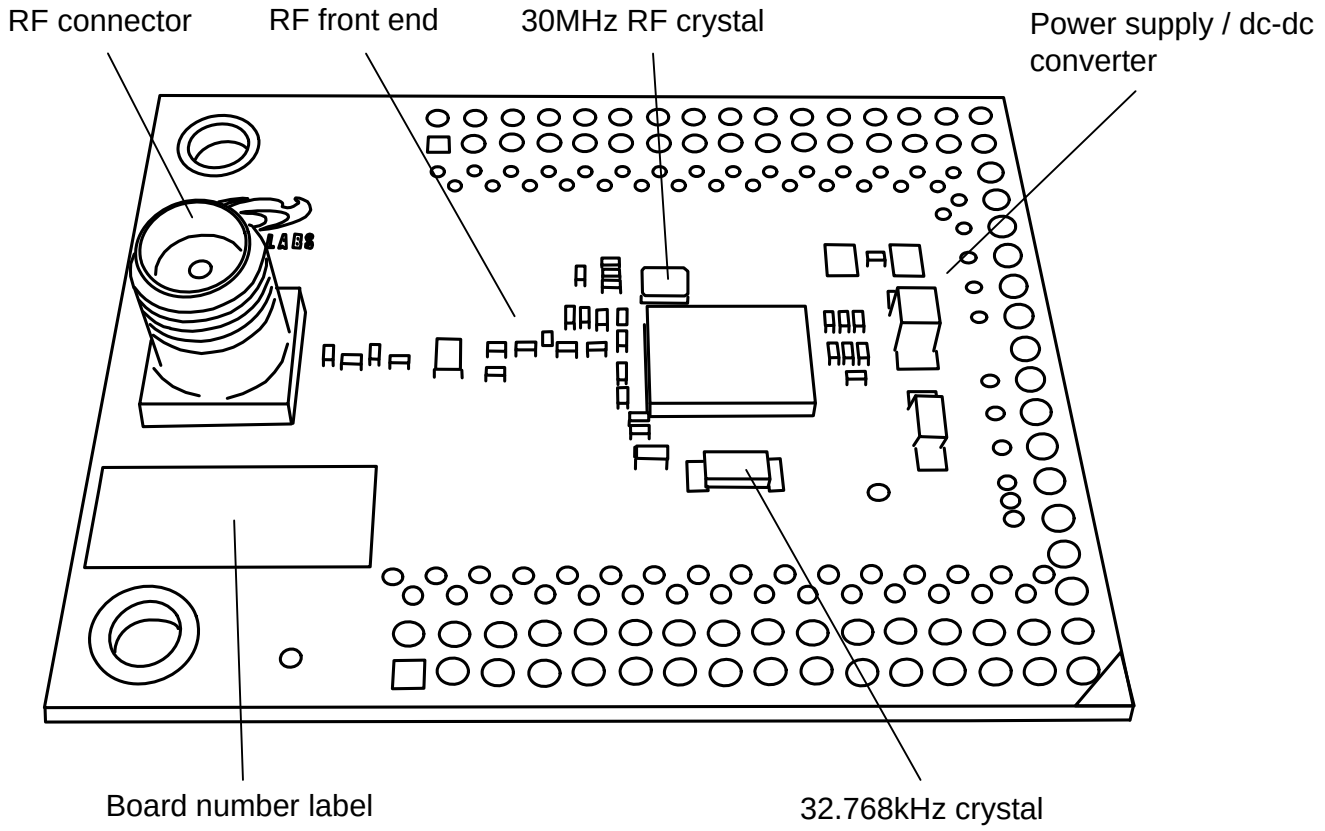


Figure 2. Top View: UPPI-10xx-fffTR and UPPI-10xx-fffDT Wireless MCU Boards

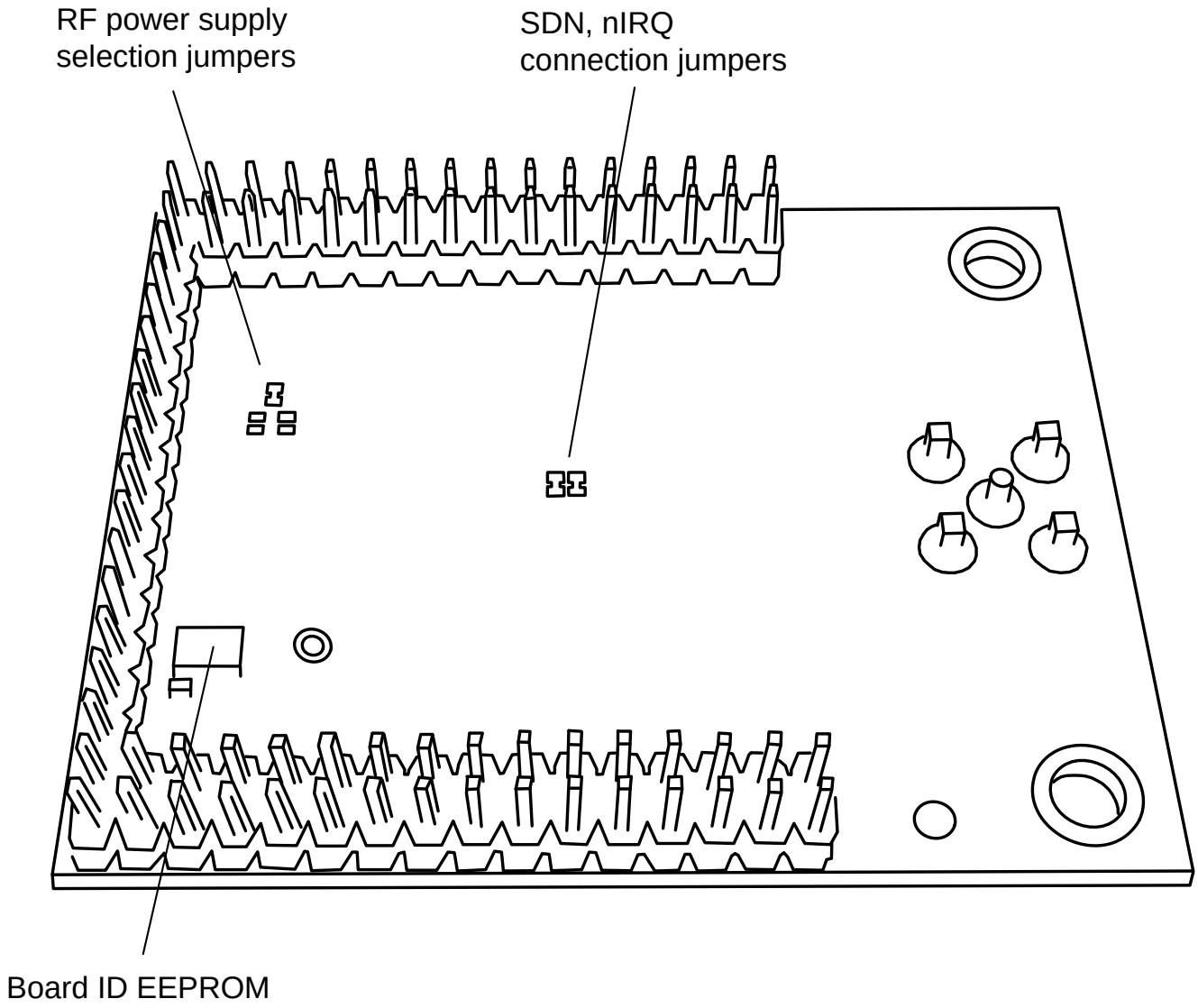


Figure 3. Bottom View: UPPI-10xx-fffTR and UPPI-10xx-fffDT Wireless MCU Boards

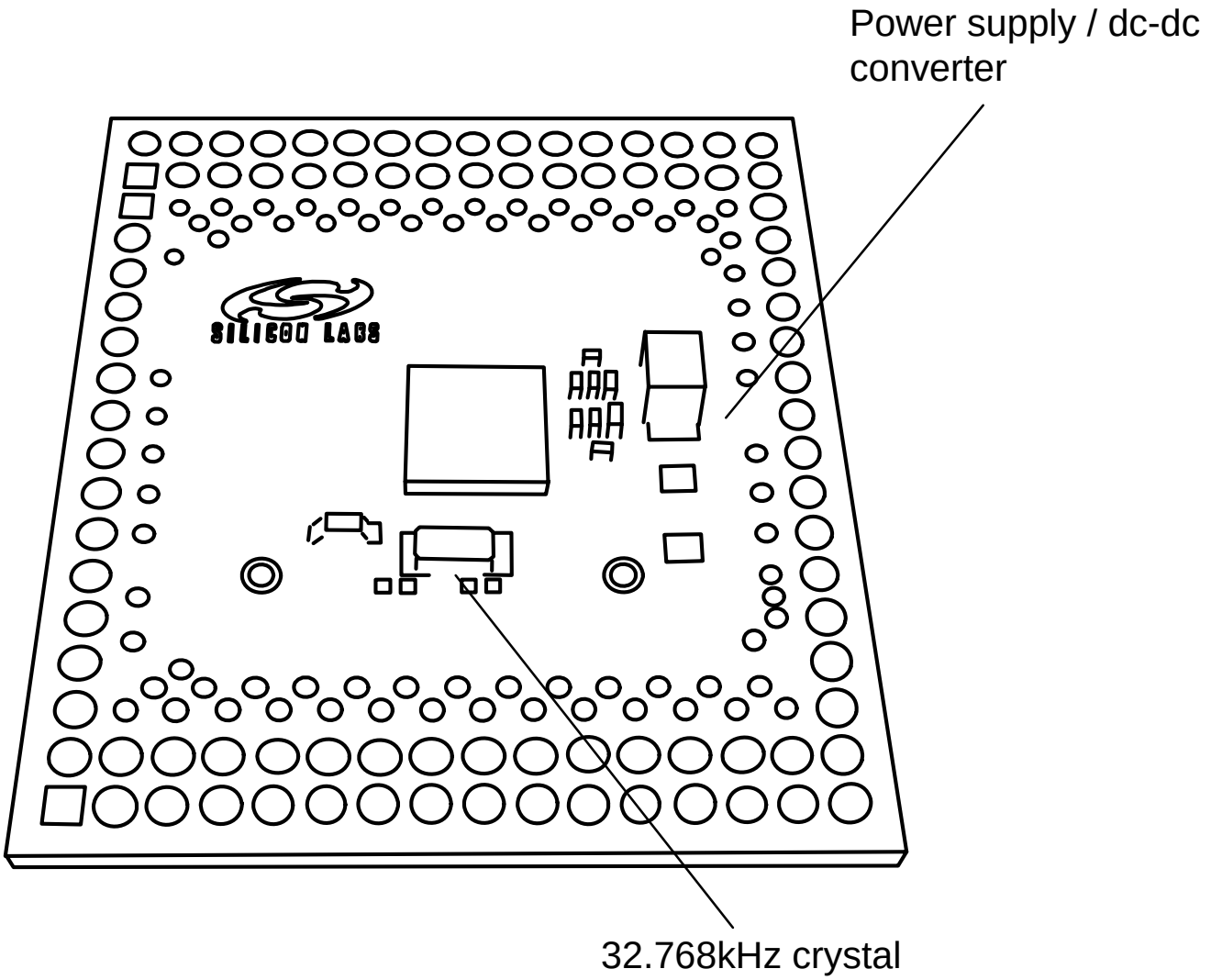


Figure 4. Top View: UPPI-F960

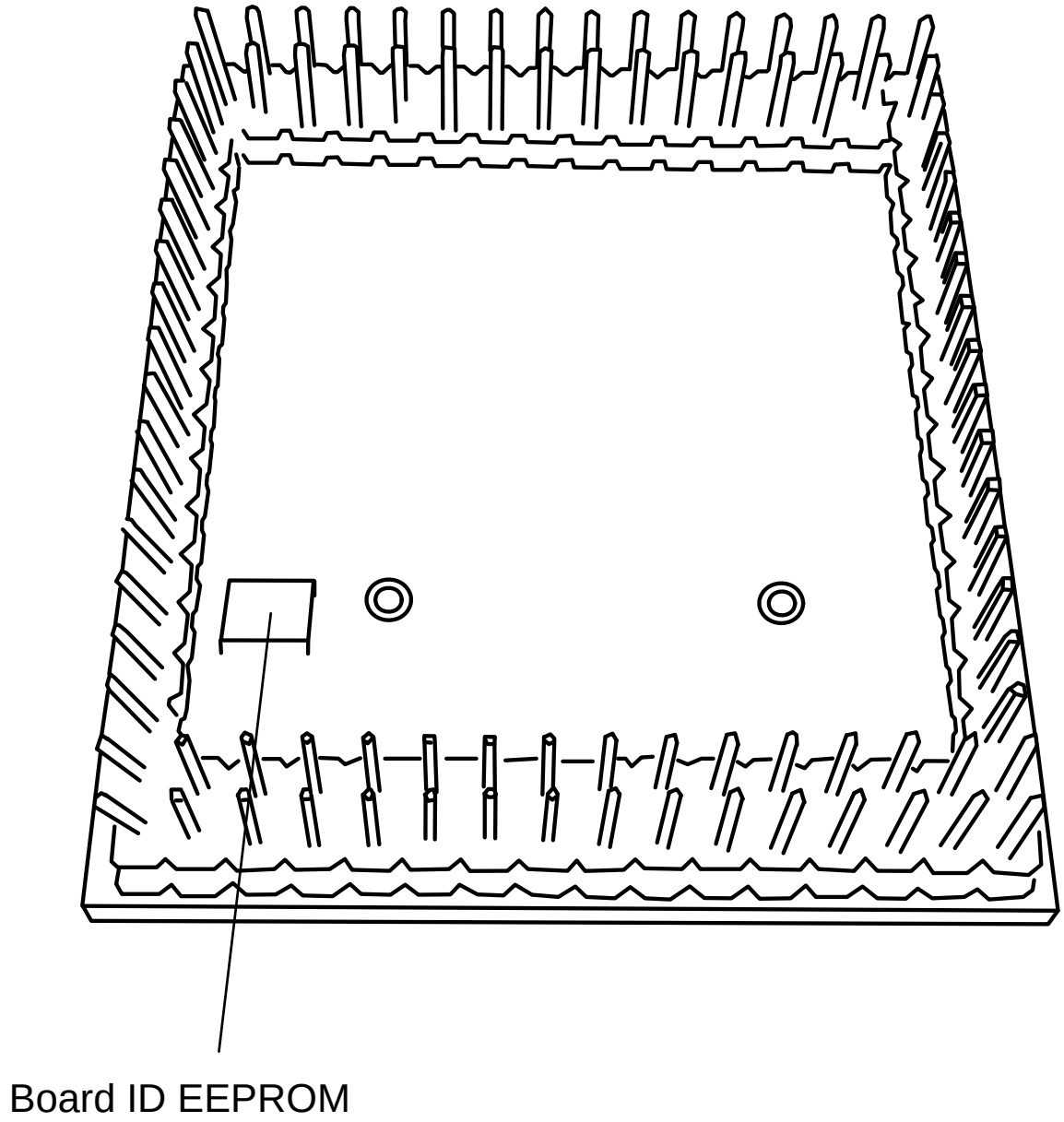


Figure 5. Bottom View: UPPI-F960

The UPPI cards contain the following functions:

- **Power Supply**
  The device's VBAT and VDC pins are connected to external pins. The dc-dc inductor, optional diode, and bypass capacitors are all included on the UPPI board as recommended in the data sheet.
  The VIO connection is routed to a pin and must be connected on the host board.
  The VIO_RF pin (if applicable) is connected to the VRF net and routed to a pin. This net supplies both the radio section power and the VIO_RF I/O voltage . The source is set on the host board, but may be optionally hard-wired via solder jumpers on the back of the board.
- **Crystal Oscillators**
  The MCU has a 32.768kHz crystal connected to the XTAL 3/4 pins. Devices with a radio have a 30 MHz crystal connected to the radio's XOUT/XIN pins. These nets are not connected to pins.
- **RF Front End**
  All RF matching circuitry is on-board. The transmitter and receiver pins are both matched to a 50 Ω SMA connector. This connector may be used with test equipment or an appropriate antenna.
  The matching is based on either a T/R switch or a Direct Tie topology. The T/R switch topology uses a TX/RX switch device to share the RF port between TX and RX paths. T/R is used with high power (+20dBm) devices. The Direct Tie topology passively sums TX and RX paths and is suitable for low-power (+13dBm) devices.
  Both matching topologies are discussed in detail in the following application notes:
  - AN427: EZRadioPRO™ Si433X & Si443X RX LNA Matching (+20dBm, T/R switch)
  - AN435: Si4032/4432 PA Matching (+20 dBm, T/R switch)
  - AN436: Si4030/4031/4430/4431 PA Matching (+13 dBm, Direct Tie)
- **RF GPIO Signals**
  The radio's GPIO_0 - GPIO_2 and ANT_A nets are connected to pins. GPIO_1 and GPIO_2 are also connected on-board to the RF transmit/receive switch on high power (“TR” version) boards.
- **RF to MCU Interface Signals**
  The radio and MCU are interconnected within the Si102x/3x device. Two external signals, shutdown (SDN) and the interrupt (nIRQ) are connected to MCU port pins on the board. These signals may be disconnected by cutting jumpers on the back of the board.
- **Port Pins**
  Most port pins are connected directly to the module's pins. Exceptions include
  - Pins dedicated to the on-board radio interface
  - P1.2 / P1.3, as these pins are used for the 32.768kHz crystal. These may be connected by adding 0-ohm resistors.
- **Programming/Debugging**
  C2CK/RSTB and C2D are connected to the module header. C2CK/RSTB has an on-board pullup resistor to VBAT.
- **Unified Development Platform Support**
  An EEPROM is included on the back side of the board to identify board information to the UDP system. This EEPROM is electrically isolated from the rest of the board except for a common ground.

The UPPI boards are based on 2mm-center headers. The footprint fits any C8051F96x- or Si102x/3x compatible Unified Development Platform MCU card. The UPPI boards may also be used for prototyping, using a 2mm-center perforated prototyping board.

The UPPI boards should be fastened to the base board using two 4-40 screws and 6.5mm standoffs to resist twisting moments from the antenna or RF cabling.

2.2. Ordering Information

A variety of UPPI boards are available, each tailored to a specific RF frequency band, transmitter power, and RF front end configuration. Refer to www.silabs.com for specific ordering information.

Table 1. Ordering Information

	Device	Description	Frequency	Tx Power (Max)	Rf Front End
MCU Only					
UPPI-F960	C8051F960	'F960 microcontroller only	—	—	—
Wireless MCU					
UPPI-1020-fffTR	Si1020	Si1020 Wireless MCU with T/R switch (+20 dBm)	fff MHz	+20 dBm max	T/R switch
UPPI-1024-fffDT	Si1024	Si1023 Wireless MCU with Direct Tie RF front end (+13 dBm)	fff MHz	+13 dBm max	Direct Tie
***Note:** refer to www.silabs.com for an up to date list of supported frequency variants					

2.3. Compatibility

These boards are compatible with the following UDP MCU cards:

- UDP F960 MCU card with Multiplexed LCD (UPMP-F960-MLCD)
- UDP F960 MCU card with EMIF (UPMP-F960-EMIF)

2.4. Schematics

These schematics show circuit topologies of the various cards. Refer to the latest schematics, available from www.silabs.com, for actual values.

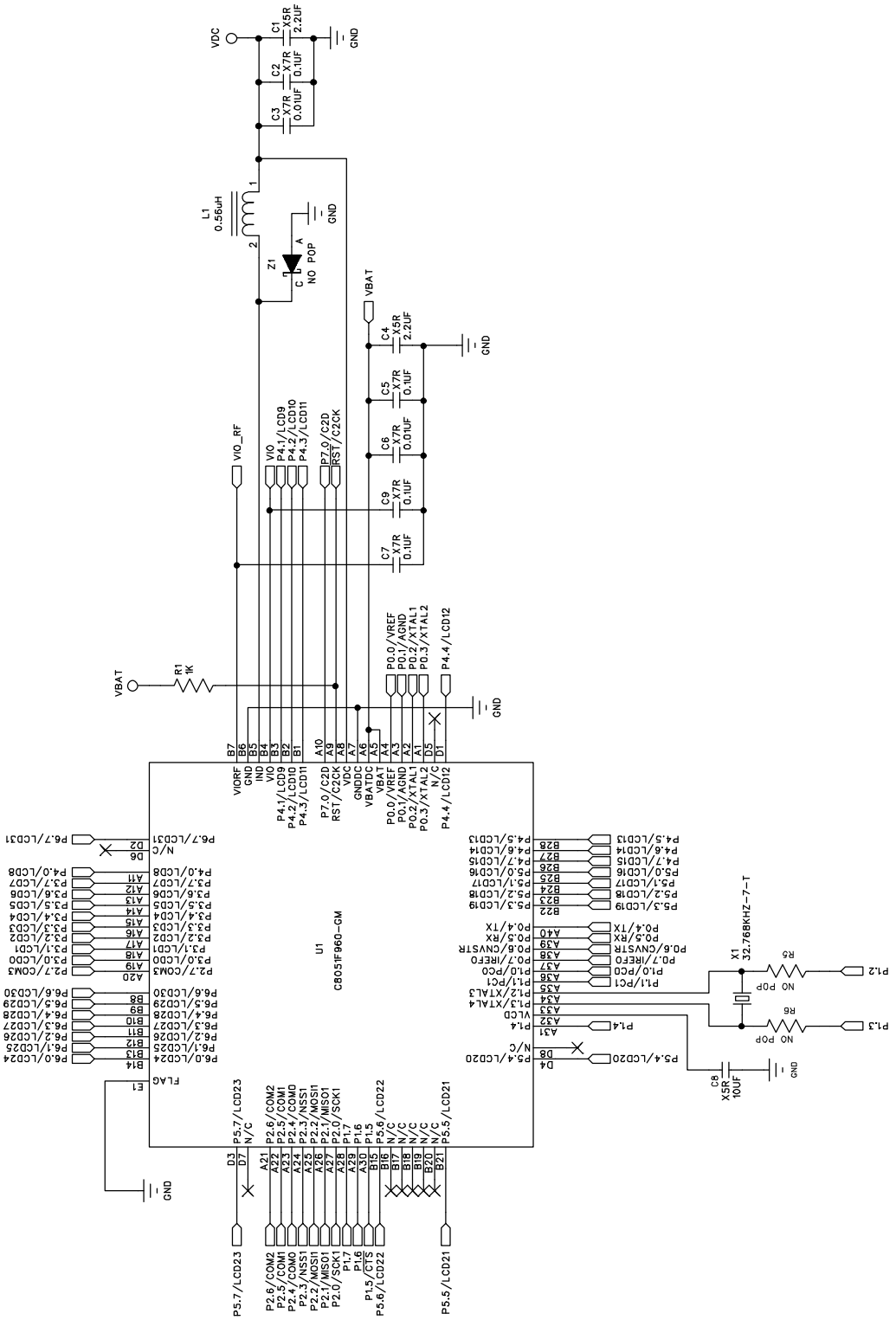


Figure 6. UPPI-F960 (1 of 2)

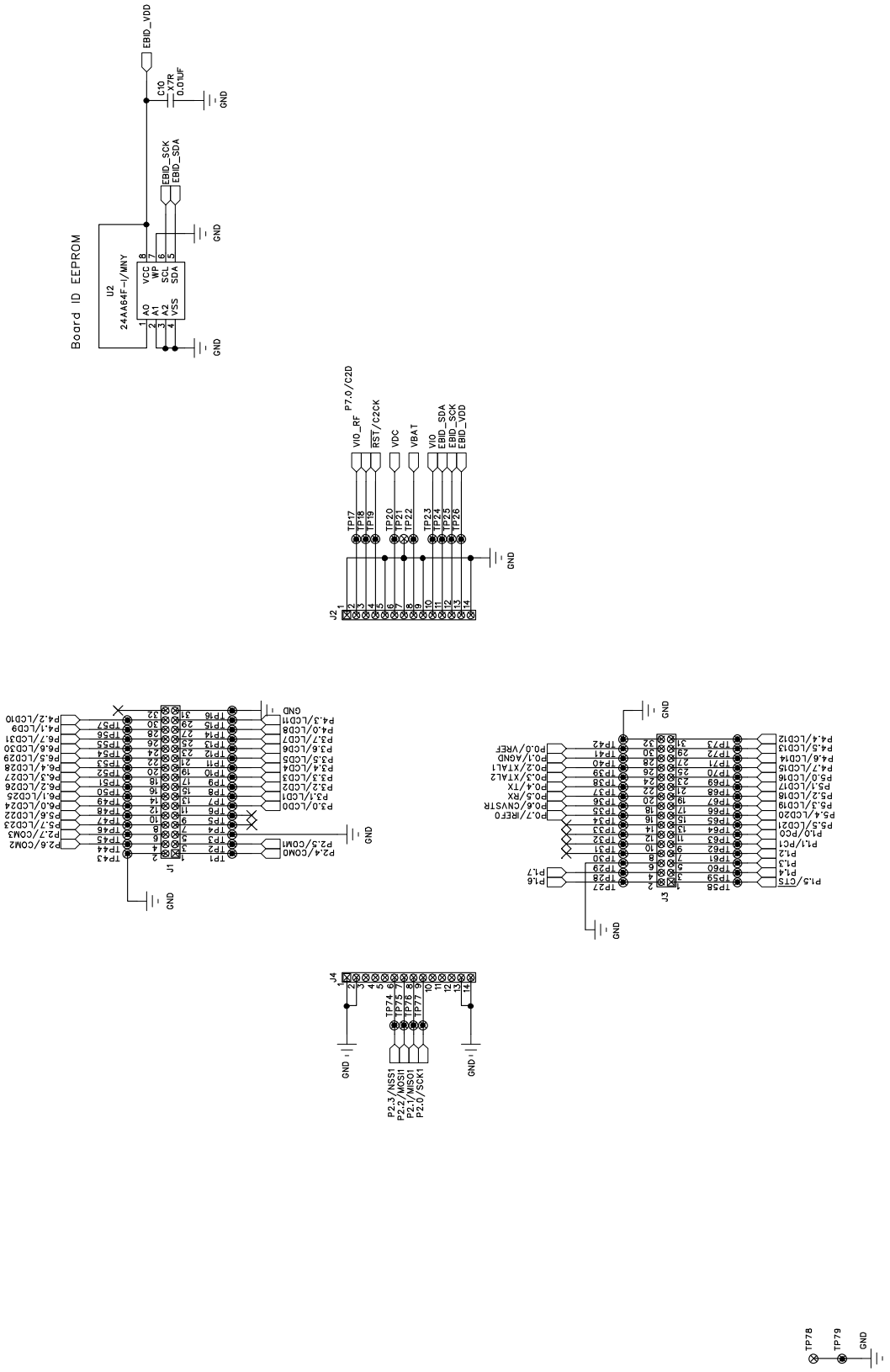


Figure 7. UPPI-F960 (2 of 2)

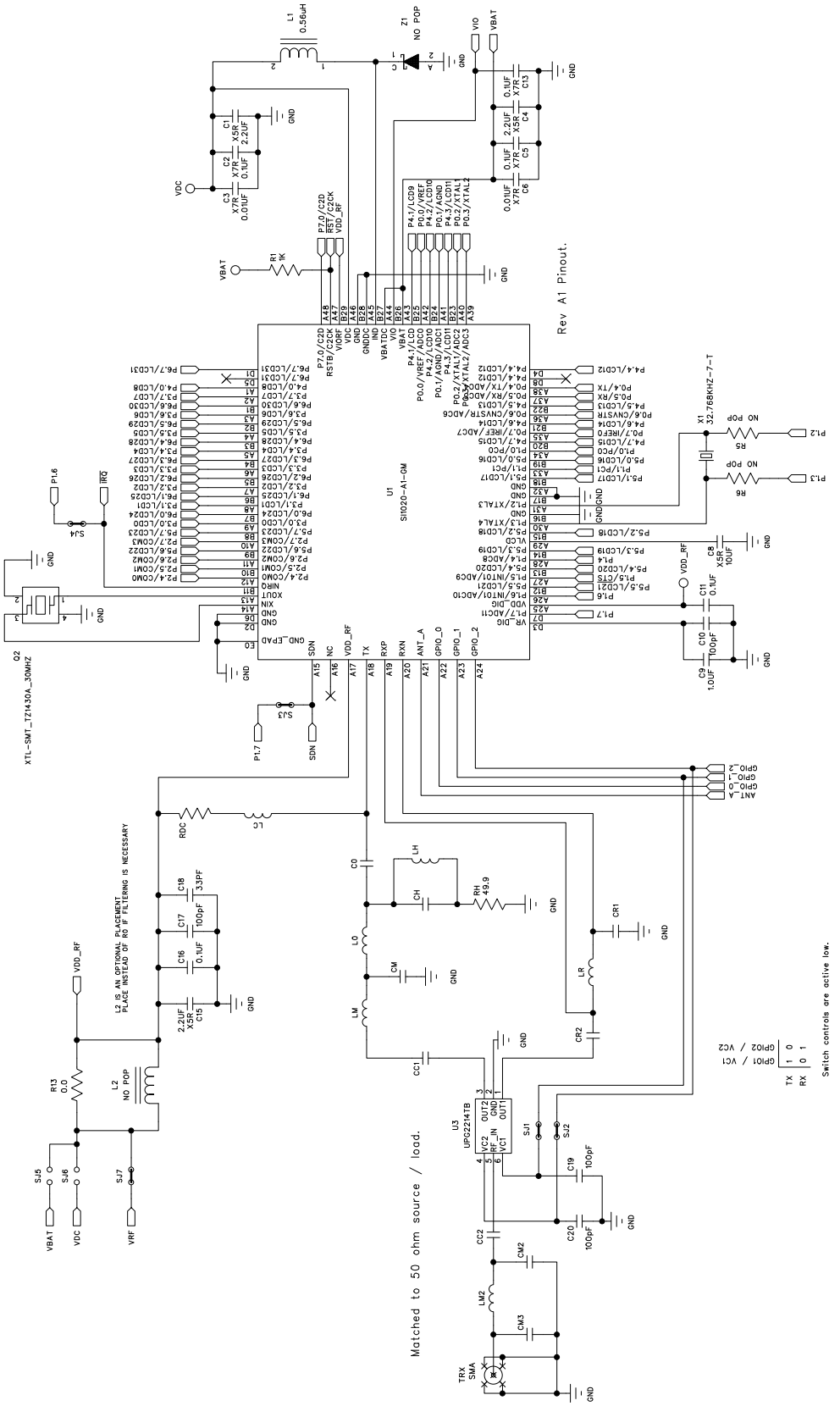


Figure 8. UPPI-1020-fffTR (1 of 2)

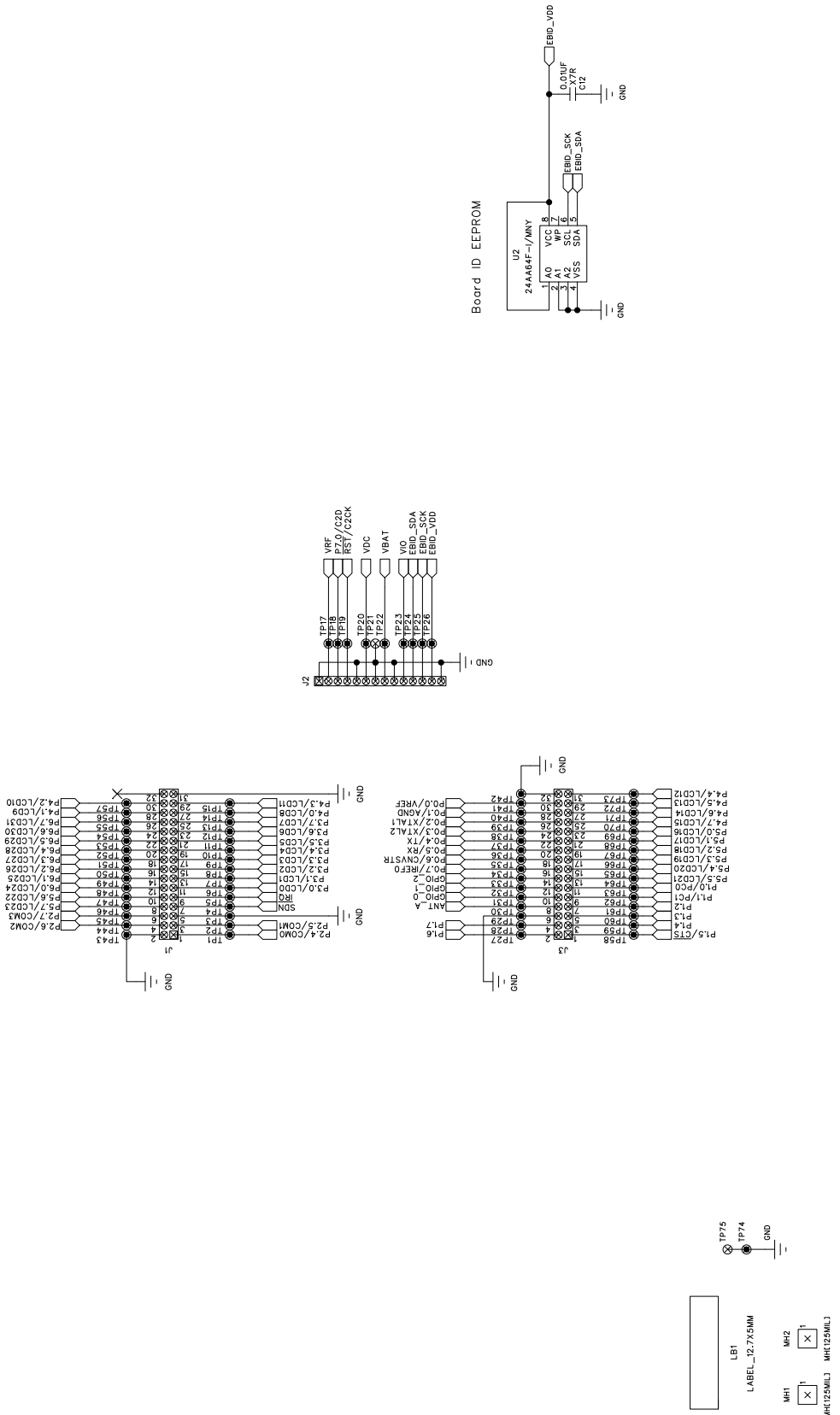


Figure 9. UPPI-1020-ffTR (2 of 2)

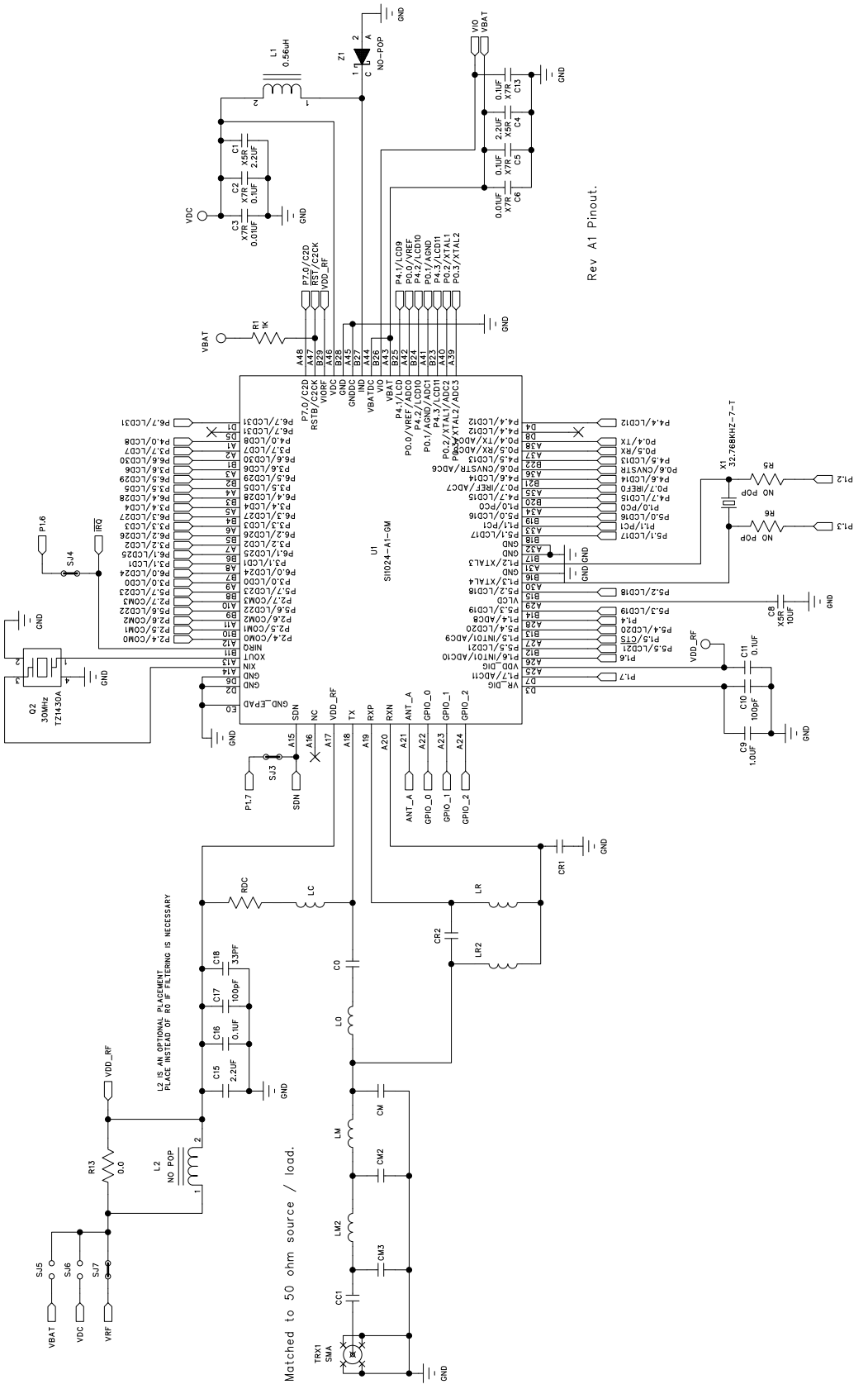


Figure 10. UPPI-1024-fffDT (1 of 2)

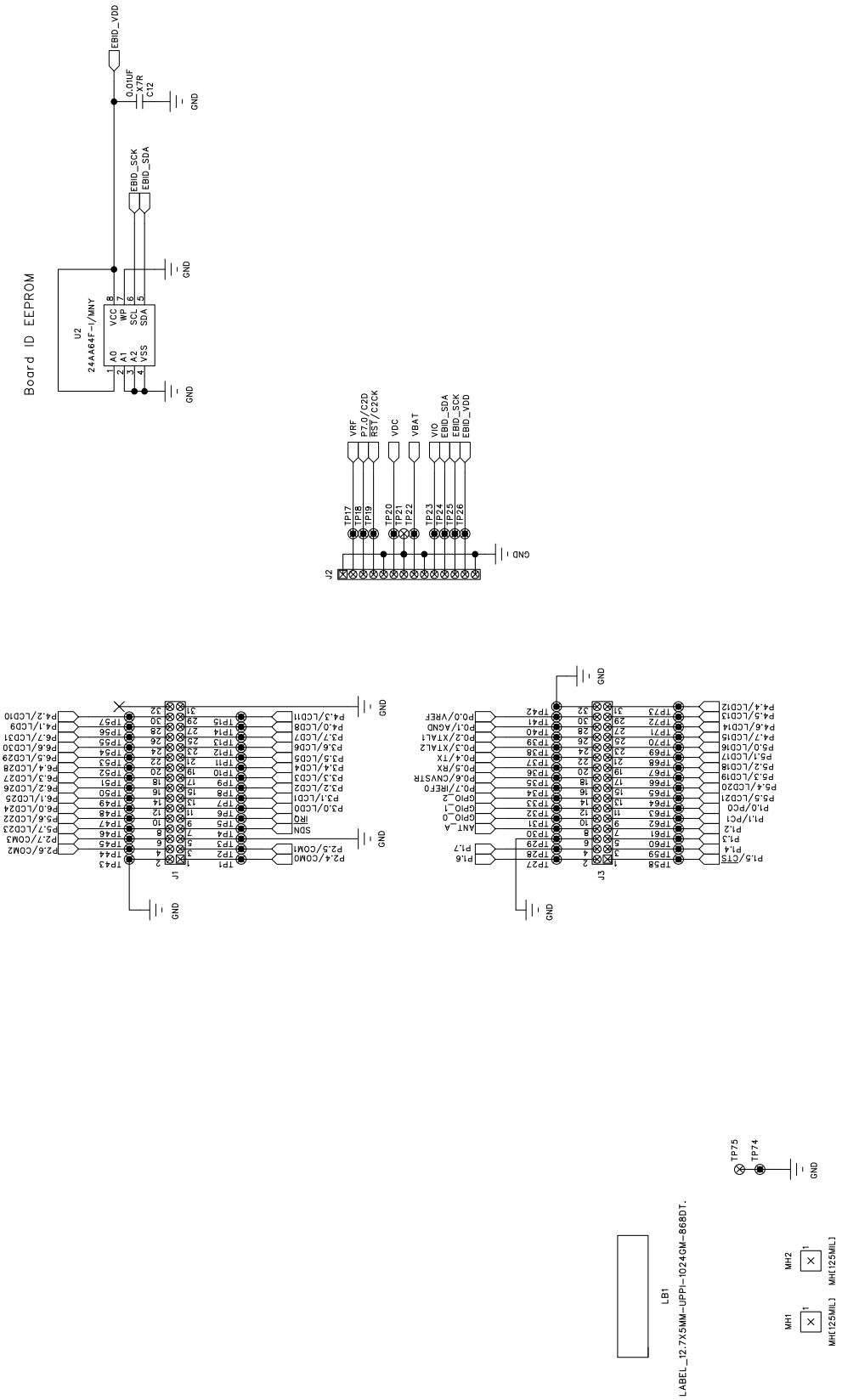


Figure 11. UPPI-1024-fffDT (2 of 2)

2.5. PCB Layouts

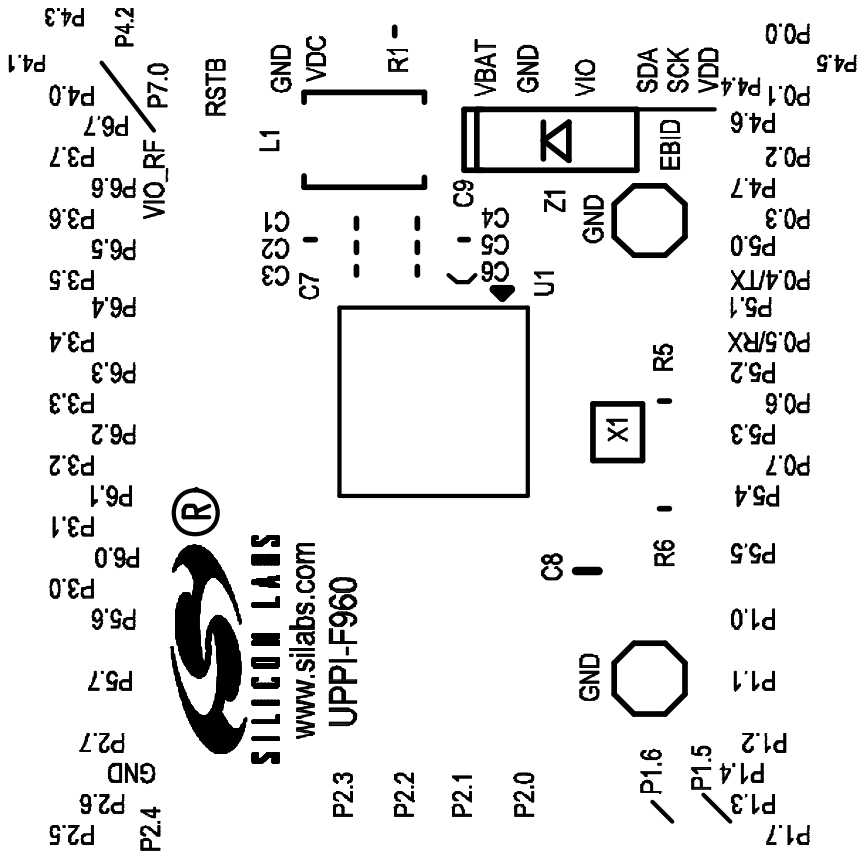


Figure 12. UPPI-F960 Silkscreen Top

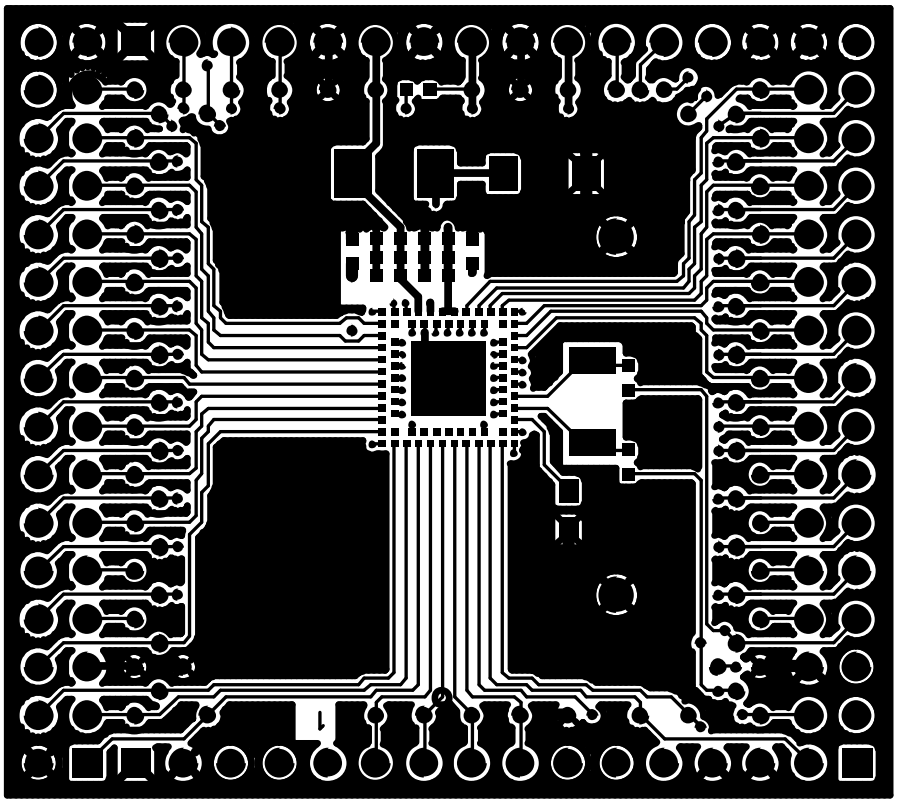


Figure 13. UPPI-F960 Top Side

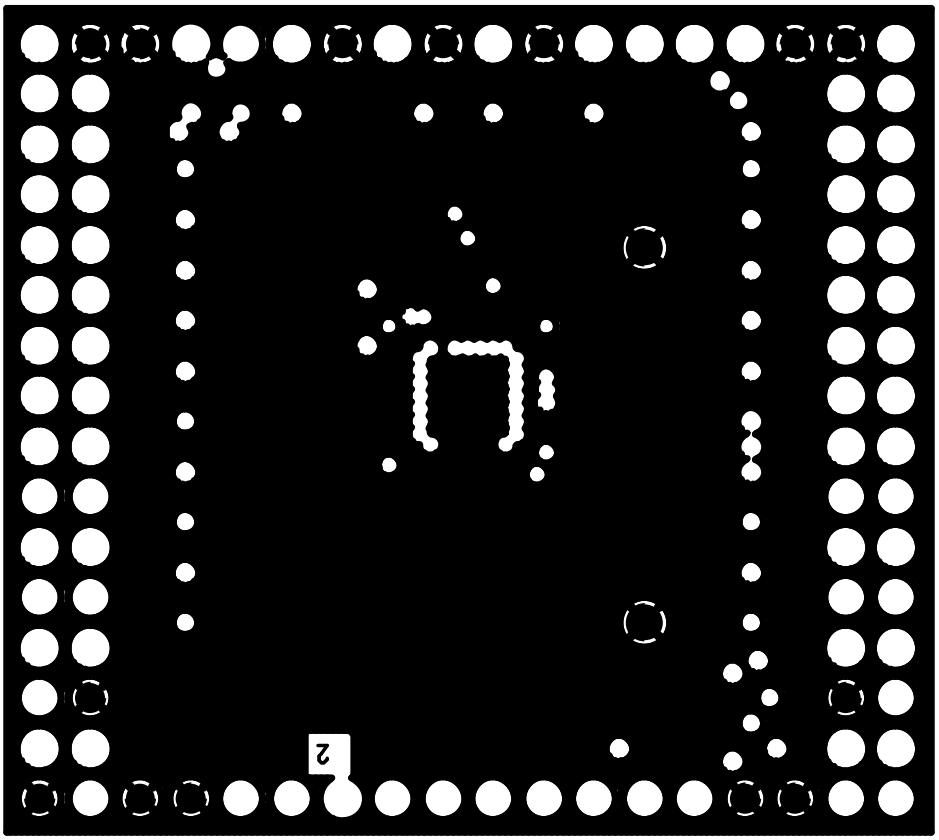


Figure 14. UPPI-F960 Layer 2

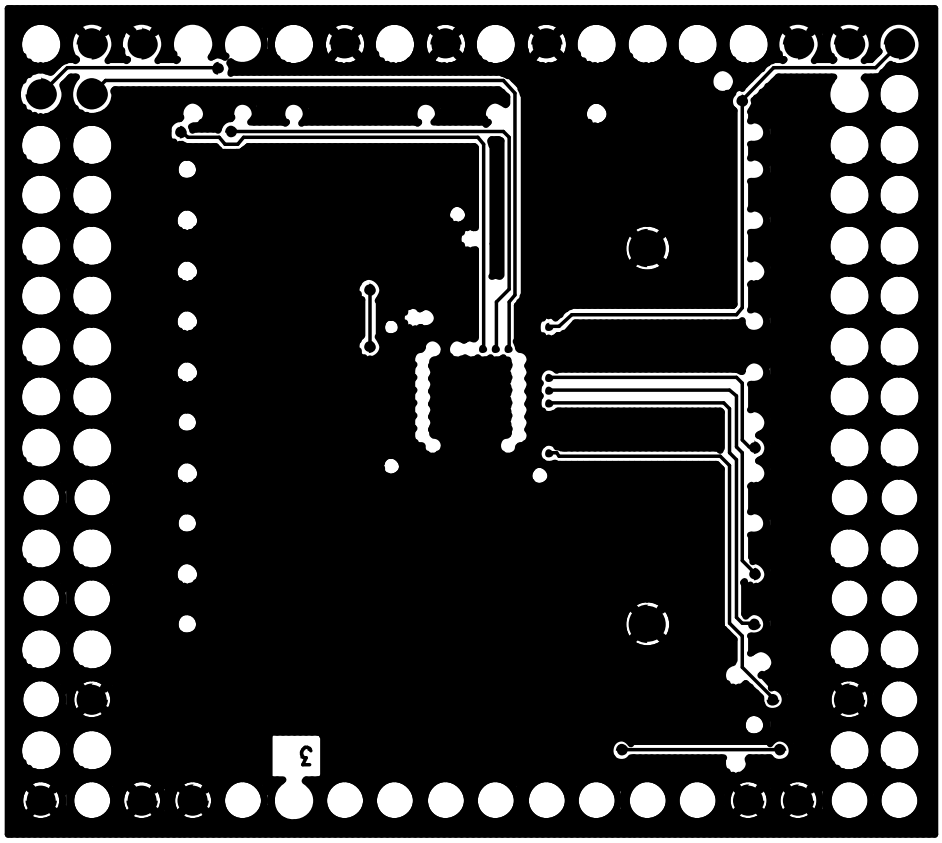


Figure 15. UPPI-F960 Layer 3

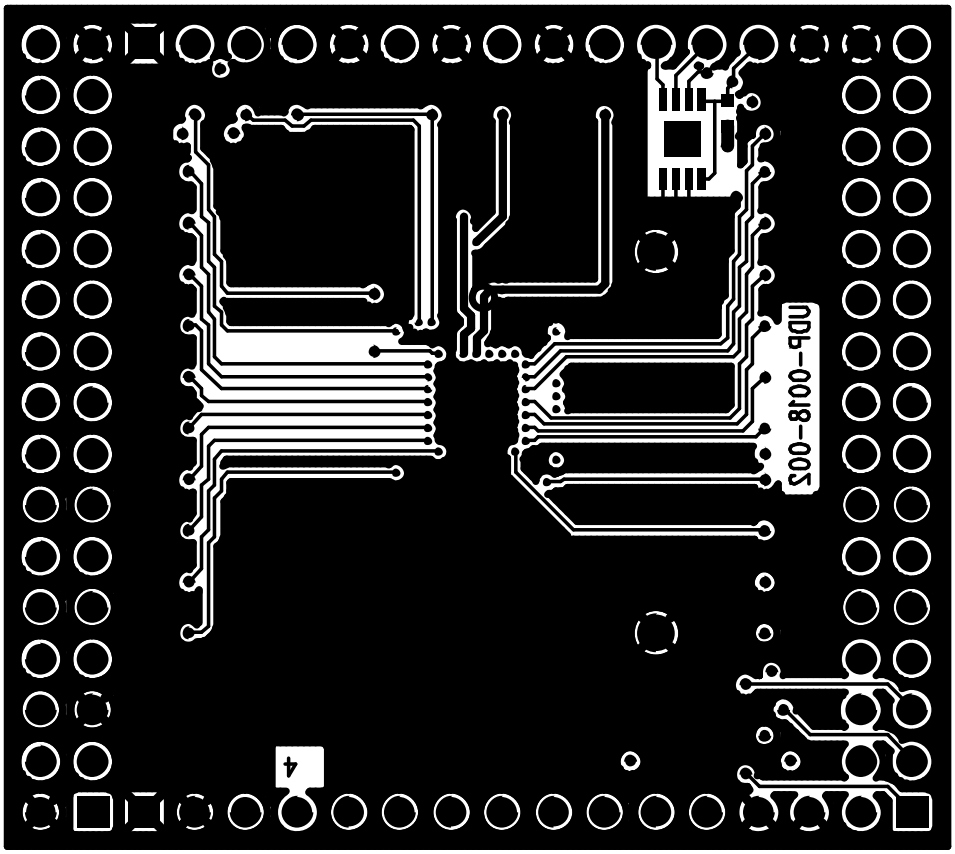
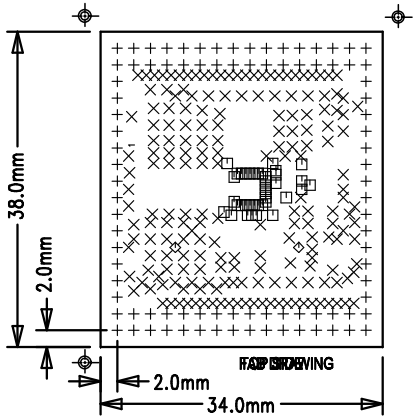


Figure 16. UPPI-F960 Bottom Side

NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345€C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING, UNLESS OTHERWISE SPECIFIED.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE +/- 0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" +/-10% ACROSS PADS.
10. WARP/TWIST SHALL NOT EXCEED 0.010 INCH PER INCH.
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. NO VENDOR MARKINGS OR ALTERATIONS SHALL BE PERMITTED ON ANY METAL OR SILKSCREEN LAYERS.
14. BOARD STACKUP:
    TOP LAYER PLATED TO 1 OZ
    PREPREG FR4: 12 MILS +/- 1 MIL
    L2-GND 1 OZ Cu
    PREPREG FR4: 28 MILS
    L3-POWER 1 OZ Cu
    PREPREG FR4: 12 MILS +/- 1 MIL
    BOTTOM LAYER PLATED TO 1 OZ
15. PLATE IN ACCORDANCE WITH IPC-4552, 118-236uIN of NICKEL, WITH AN ADDITIONAL 2-6 uIN OF GOLD ON TOP.

SIZE	QTY	SYM	PLATED	TOL
30	92	+	YES	+/-0.003"
8	194	X	YES	+/-0.003"
6	39	⊡	YES	+/-0.003"
40	2	◇	YES	+/-0.003"



SILICON LABS - UDP-0018-002 (UPPI-F960)

LAYER STACKUP	FILE NAMES
TOP SILKSCREEN	TOPSILK.TSP
TOP SOLDER MASK	SMASKTOP.SMT
TOP SIDE	TOP.TOP
L2	LAYER2.L2
L3	LAYER3.L3
BOTTOM SIDE	BOTTOM.BOT
BOTTOM SOLDER MASK	SMASKBOT.SMB
BOTTOM SILKSCREEN	BOTSILK.BSK

SCALE: NONE

Figure 17. UPPI-F960 Assembly Layer

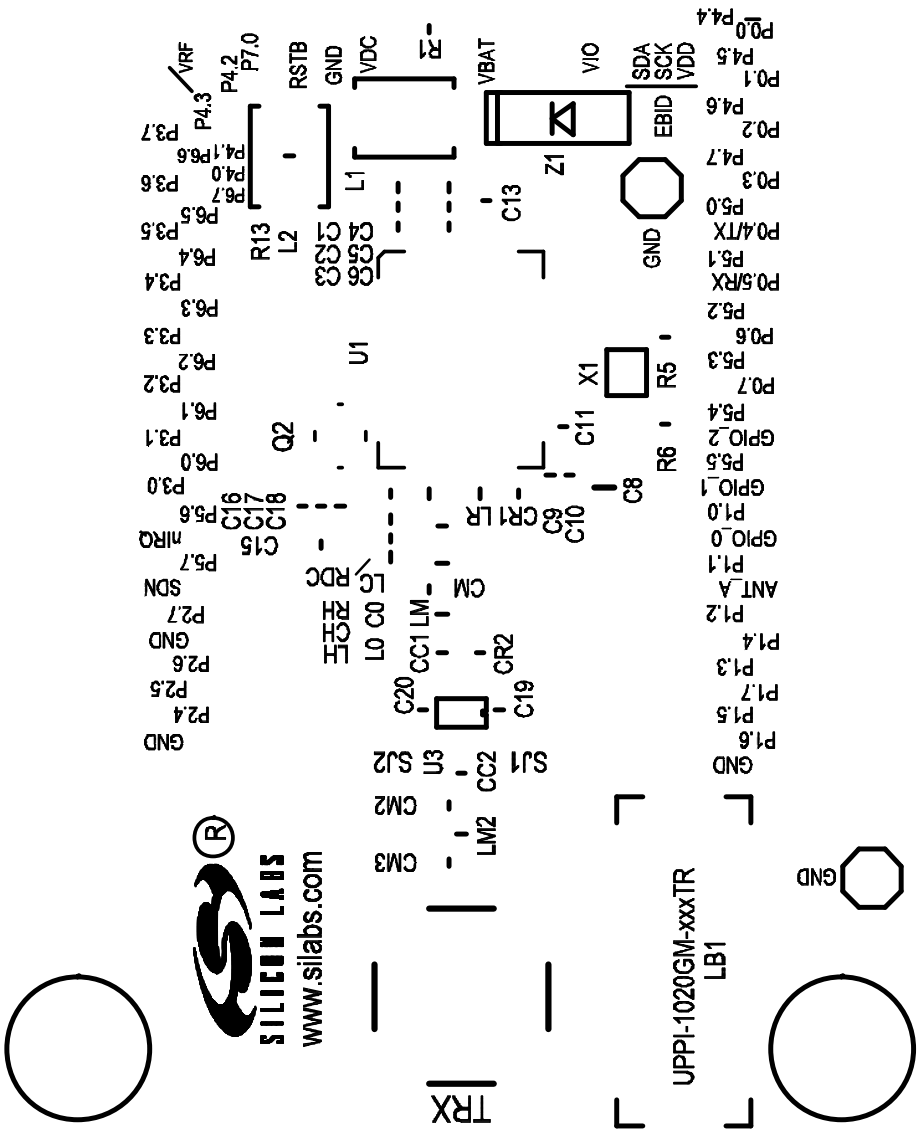


Figure 18. UPPI-1020-fffTR Silkscreen Top

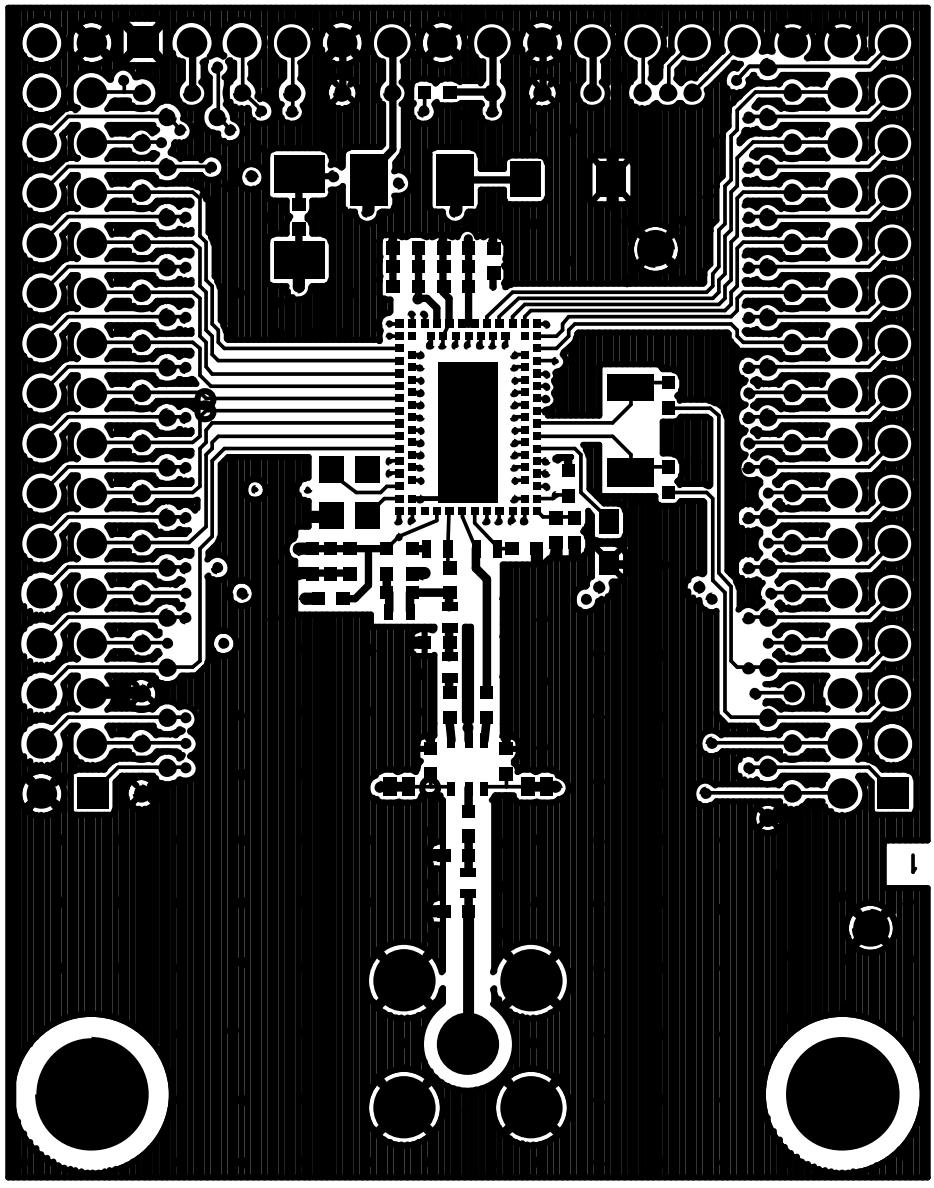


Figure 19. UPPI-1020-fffTR Top Side

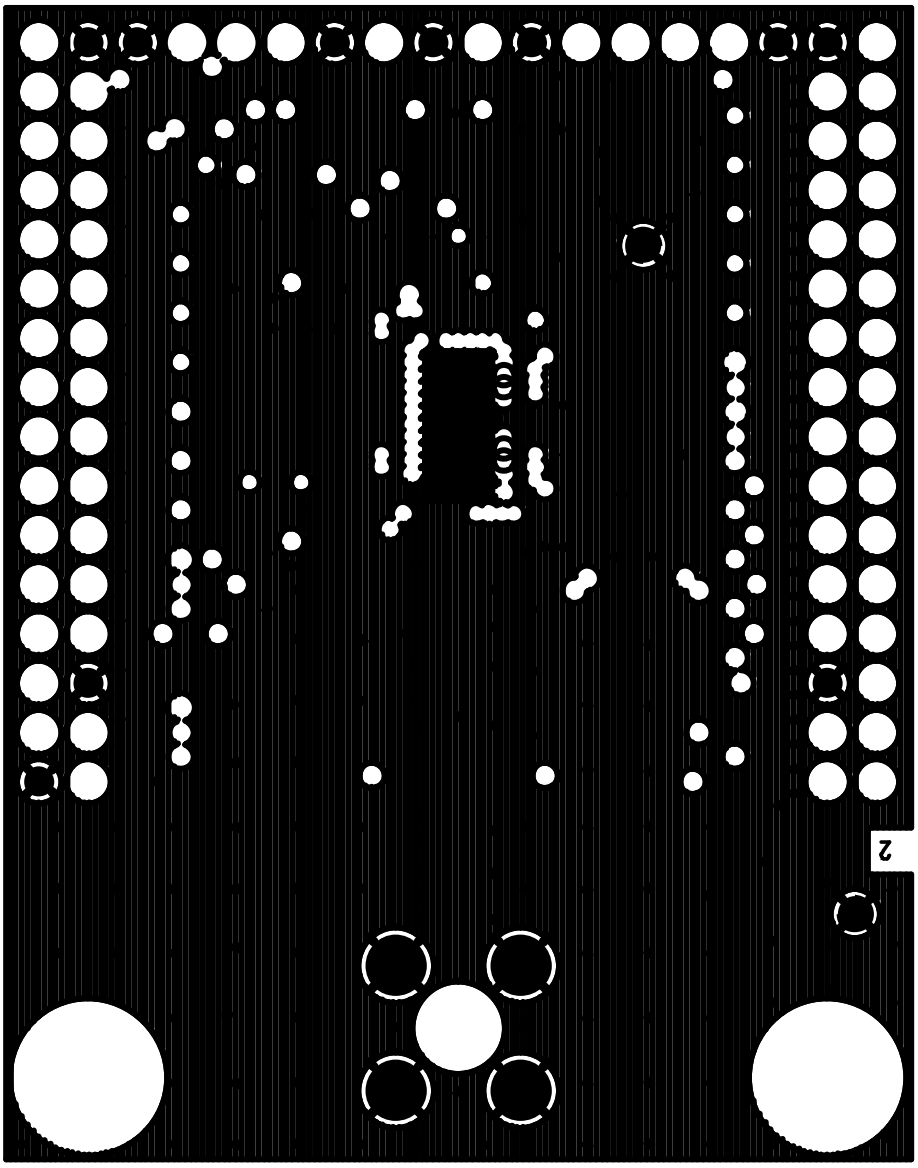


Figure 20. UPPI-1020-fffTR Layer 2

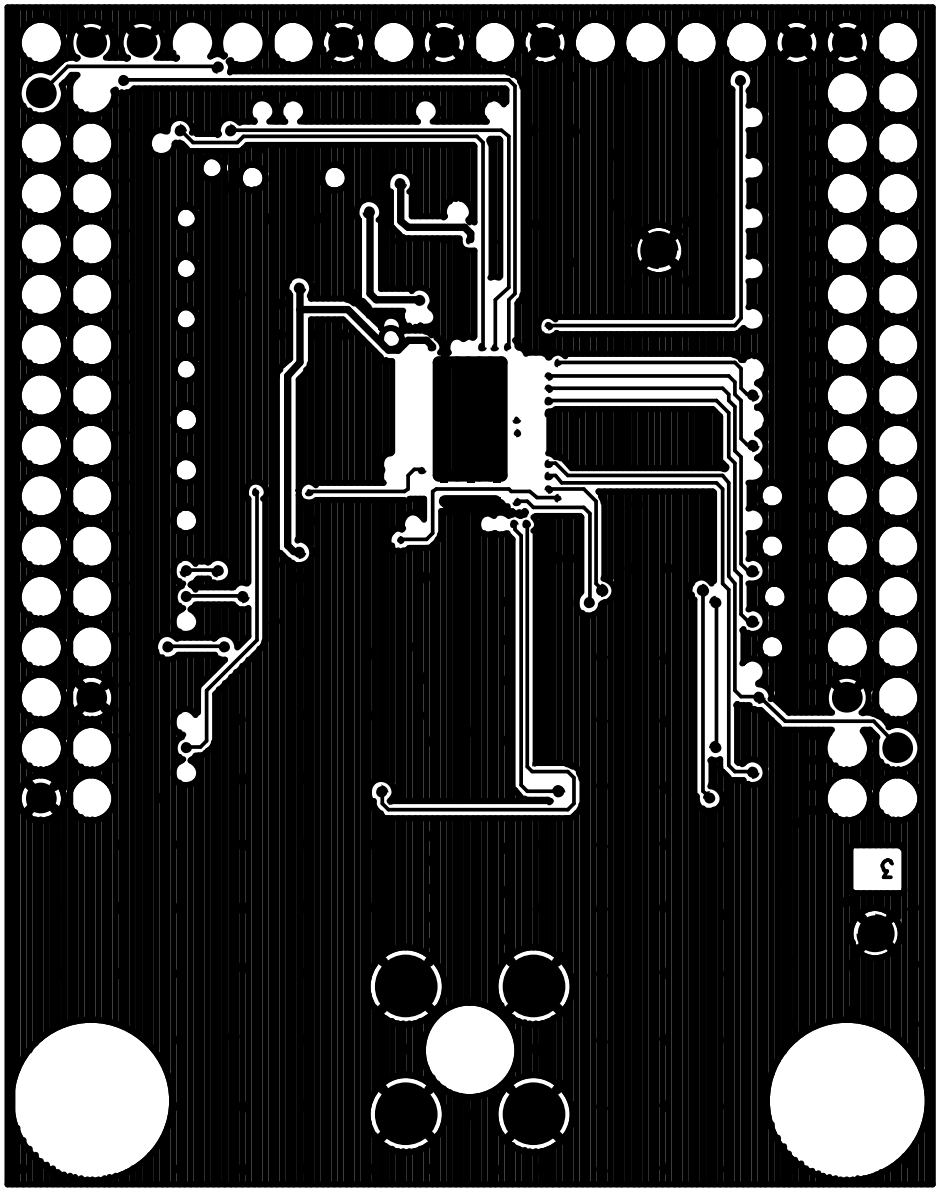


Figure 21. UPPI-1020-fffTR Layer 3

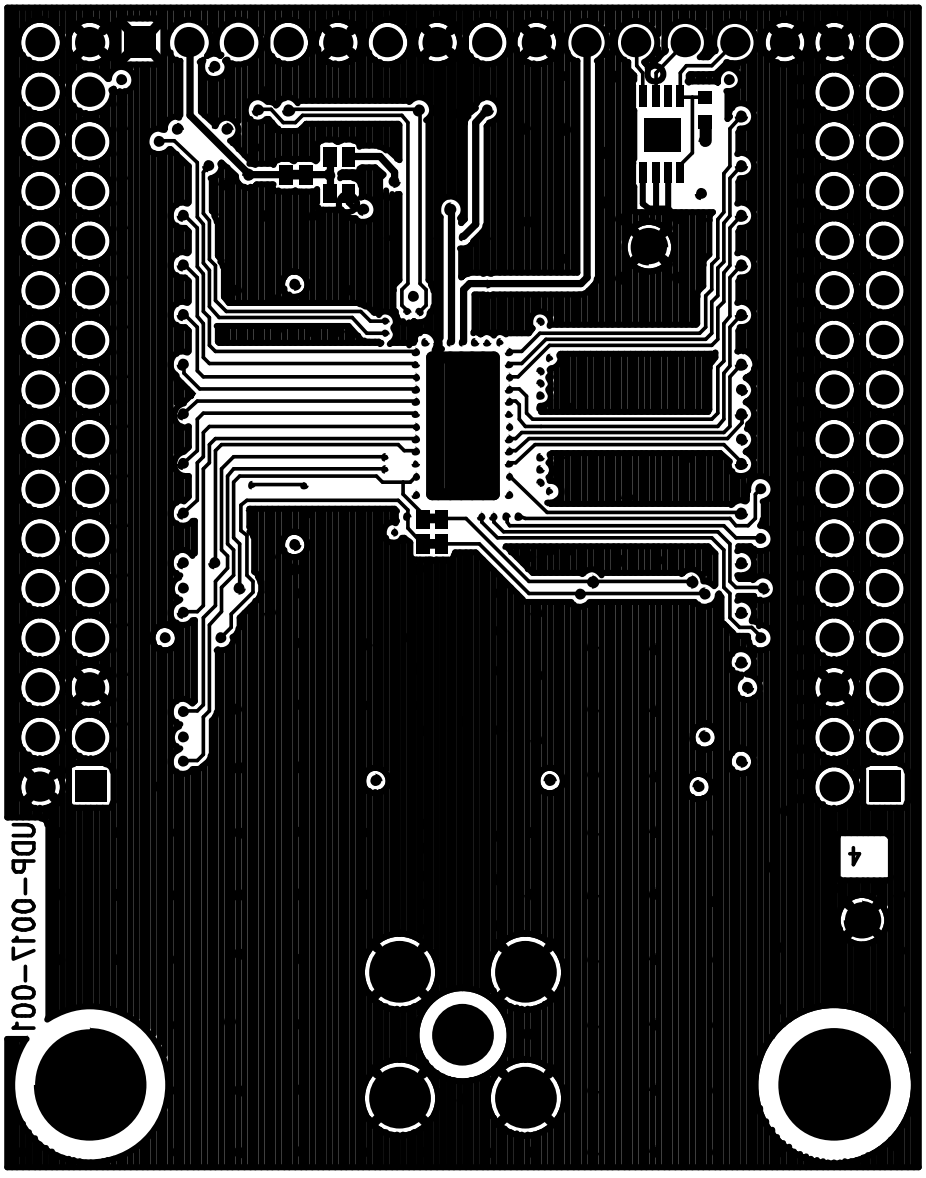
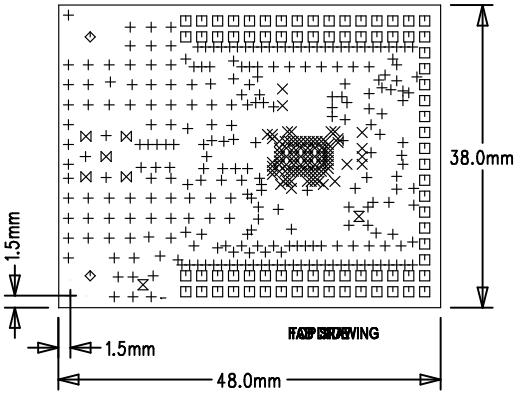


Figure 22. UPPI-1020-fffTR Bottom Side

NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345€C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING, UNLESS OTHERWISE SPECIFIED.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE +/- 0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" +/-10% ACROSS PADS.
10. WARP/TWIST SHALL NOT EXCEED 0.010 INCH PER INCH.
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. NO VENDOR MARKINGS OR ALTERATIONS SHALL BE PERMITTED ON ANY METAL OR SILKSCREEN LAYERS.
14. BOARD STACKUP:
    TOP LAYER PLATED TO 1 OZ
    PREPREG FR4: 12 MILS +/- 1 MIL
    L2-GND 1 OZ Cu
    PREPREG FR4: 28 MILS
    L3-POWER 1 OZ Cu
    PREPREG FR4: 12 MILS +/- 1 MIL
    BOTTOM LAYER PLATED TO 1 OZ
15. PLATE IN ACCORDANCE WITH IPC-4552, 118-236uIN of NICKEL, WITH AN ADDITIONAL 2-6 uIN OF GOLD ON TOP.

SIZE	QTY	SYM	PLATED	TOL
0.008	261	+	YES	+/-0.003"
0.006	91	X	YES	+/-0.003"
0.03	78	◫	YES	+/-0.003"
0.125	2	◈	YES	+/-0.003"
0.04	2	⧖	YES	+/-0.003"
0.07	5	⋈	YES	+/-0.003"



SILICON LABS - UDP-0017-001 (UPPI-1020GM-915TR)

LAYER STACKUP	FILE NAMES
TOP SILKSCREEN	TOPSILK.TSP
TOP SOLDER MASK	SMASKTOP.SMT
TOP SIDE	TOP.TOP
L2	LAYER2.L2
L3	LAYER3.L3
BOTTOM SIDE	BOTTOM.BOT
BOTTOM SOLDER MASK	SMASKBOT.SMB
BOTTOM SILKSCREEN	BOTSILK.BSK

SCALE: NONE

Figure 23. UPPI-1020-fffTR Assembly Layer

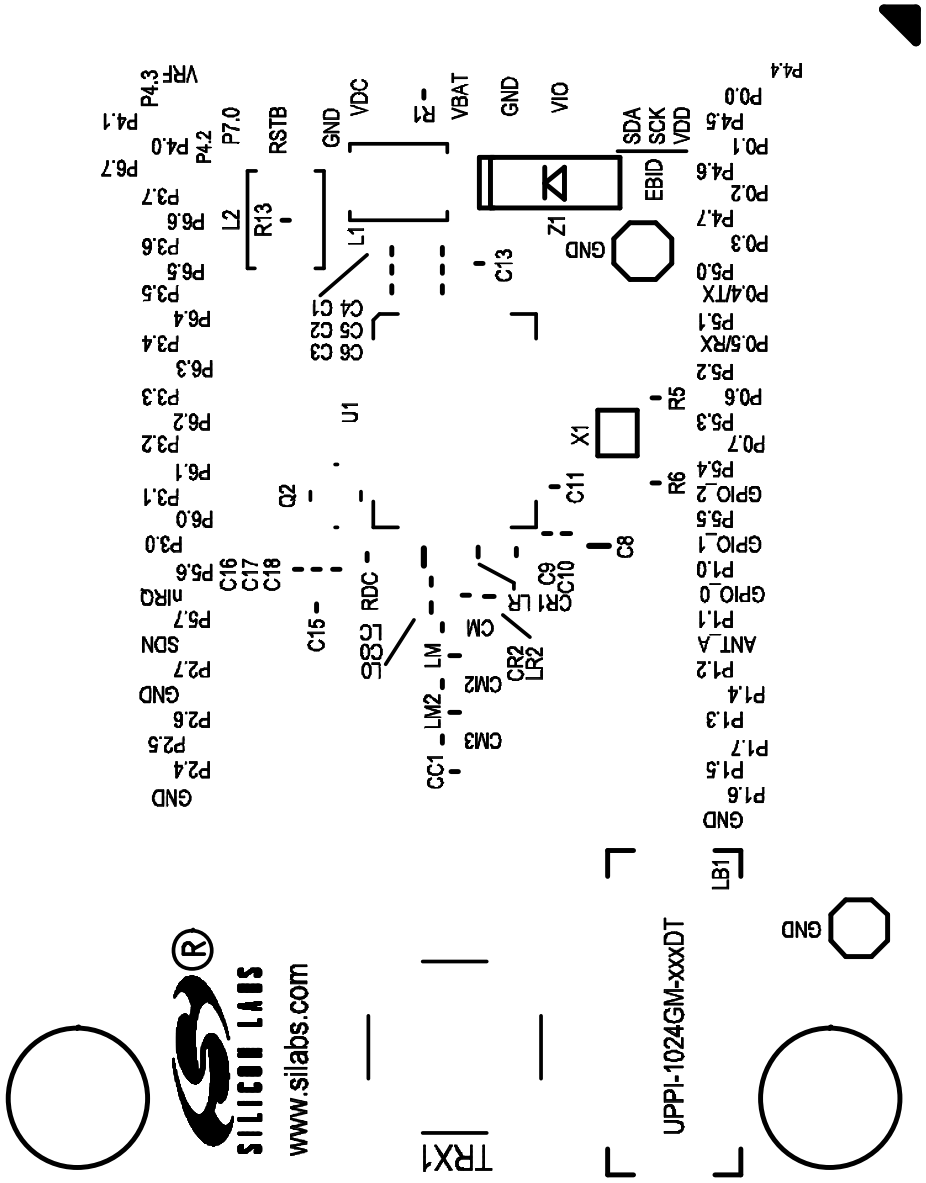


Figure 24. UPPI-1024-fffDT Silkscreen Top

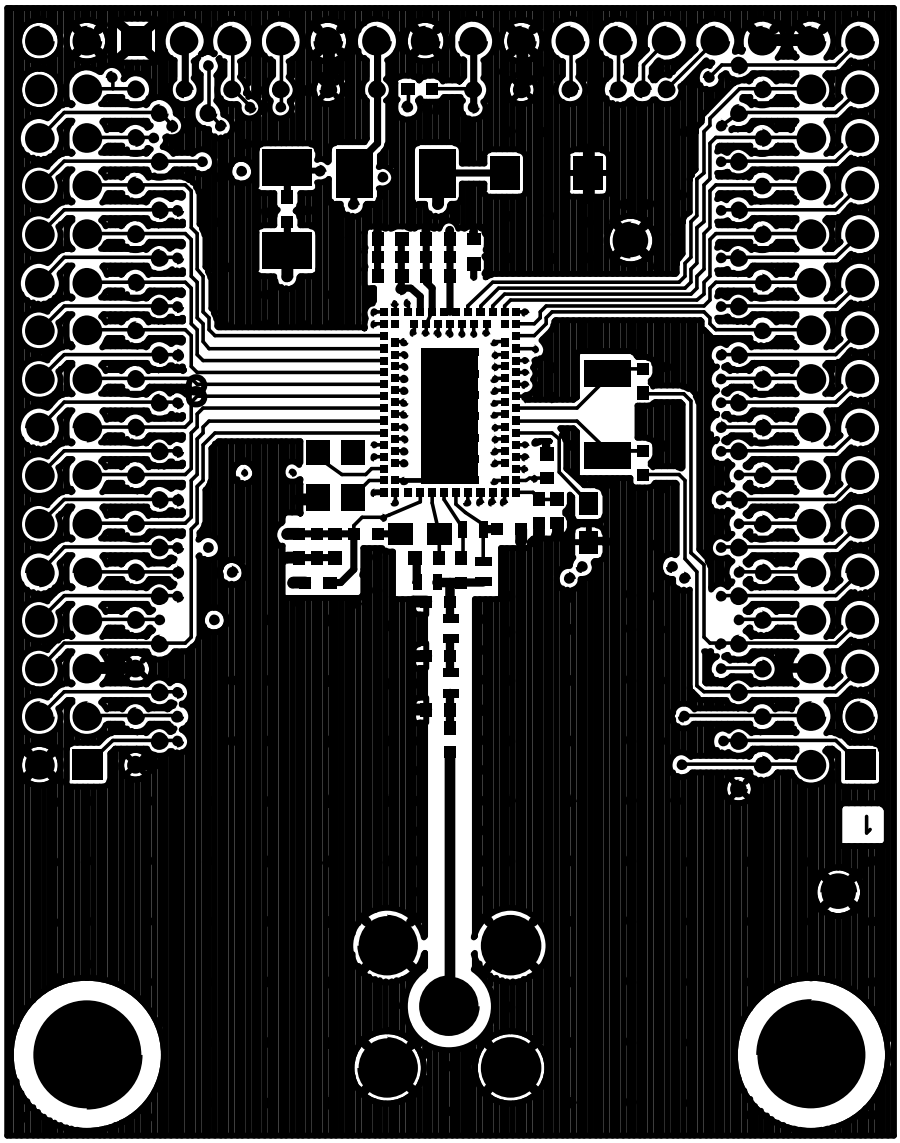


Figure 25. UPPI-1024-fffDT Top Side

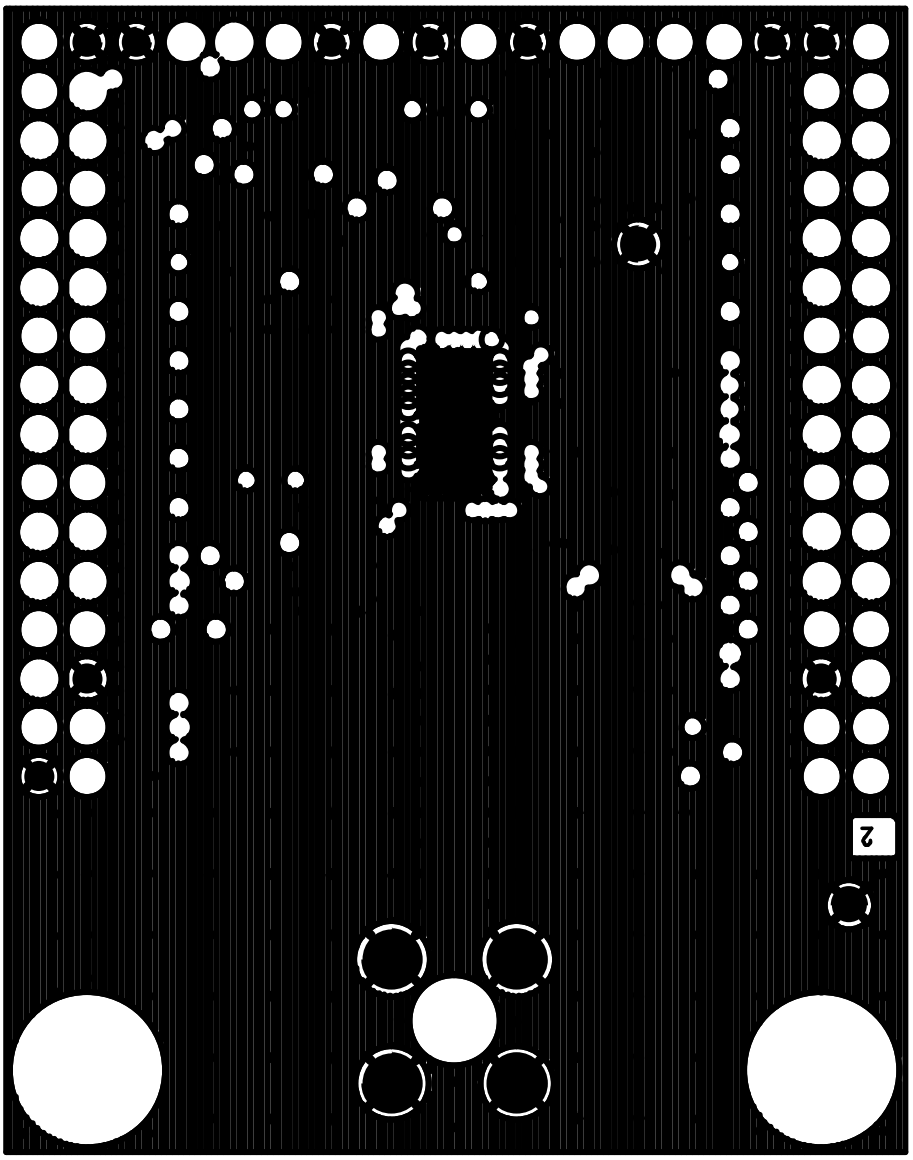


Figure 26. UPPI-1024-fffDT Layer 2

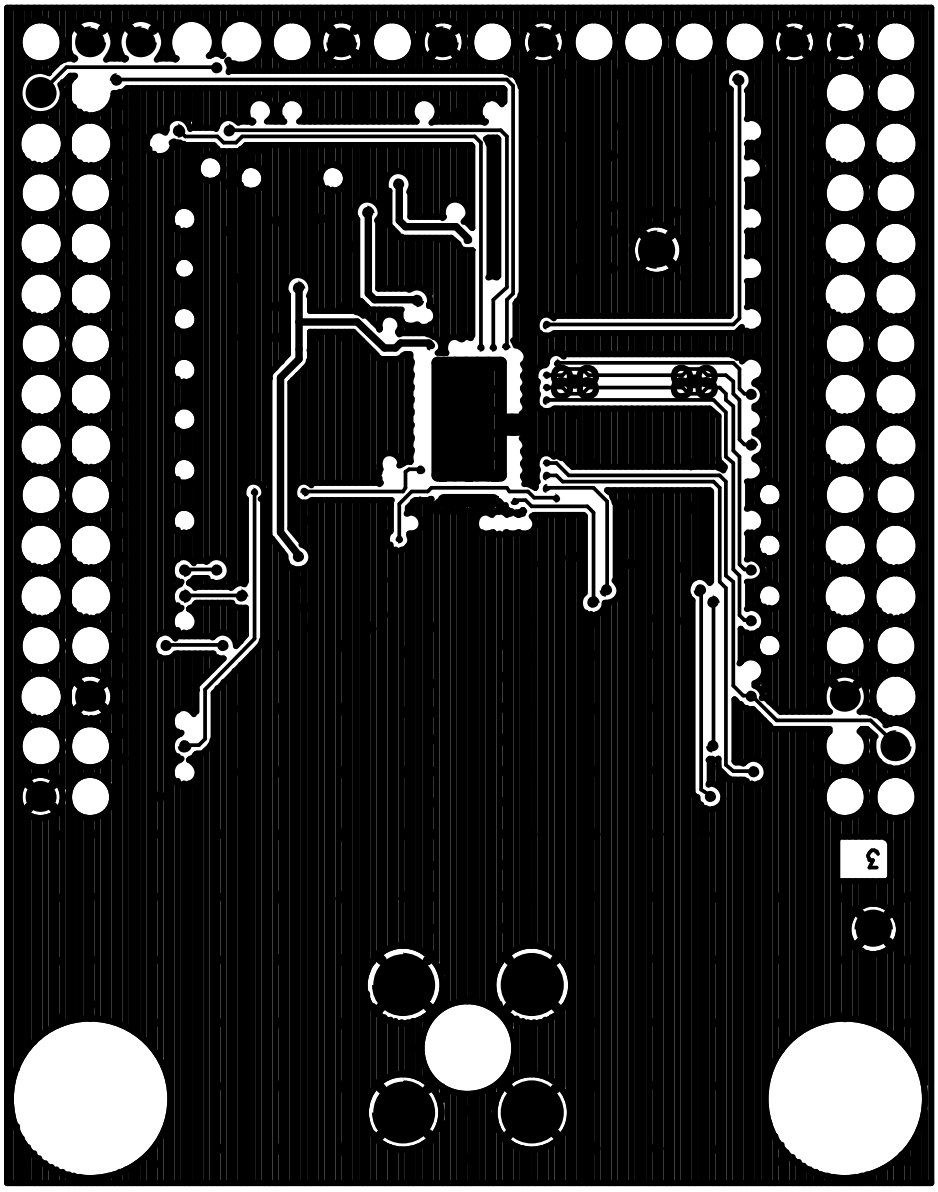


Figure 27. UPPI-1024-fffDT Layer 3

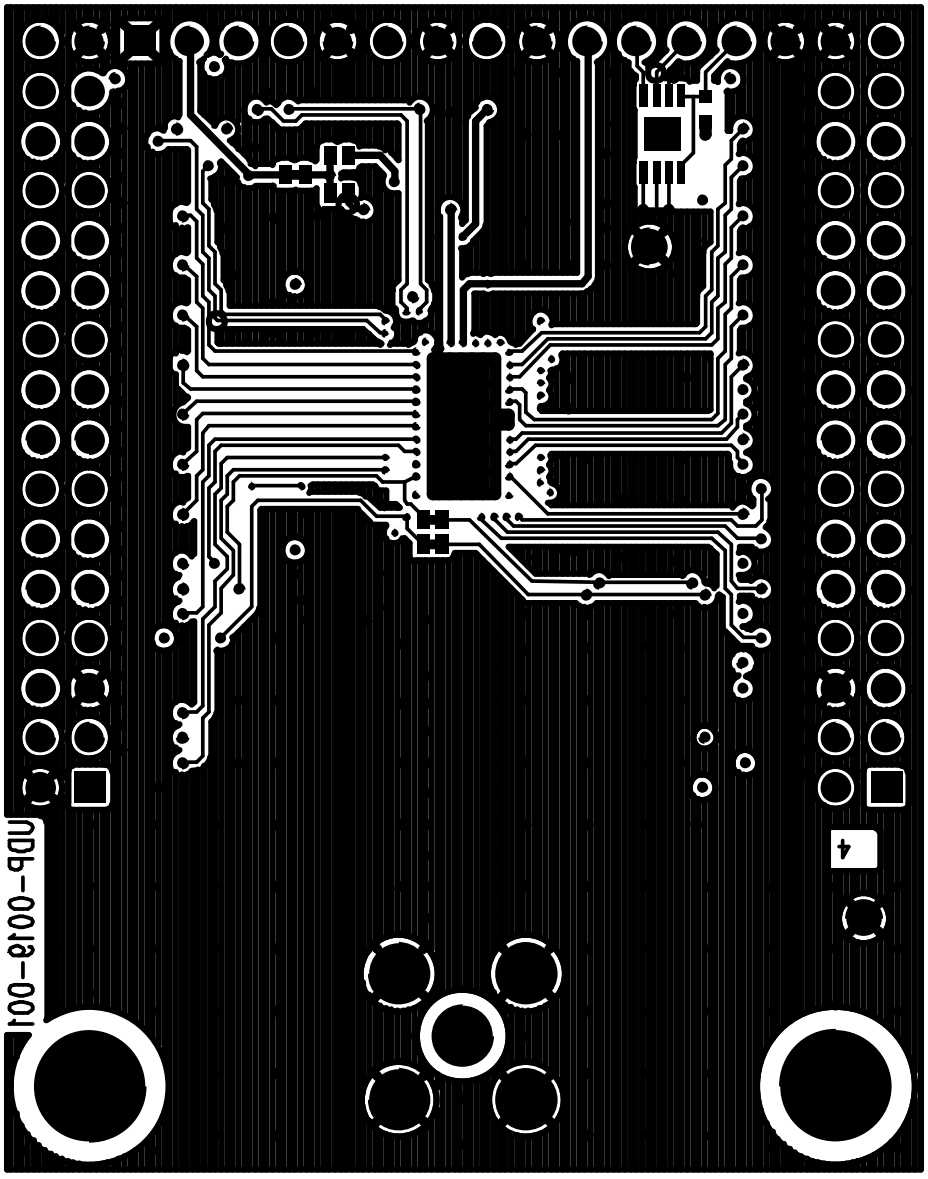


Figure 28. UPPI-1024-fffDT Bottom Side

NOTES : UNLESS OTHERWISE SPECIFIED

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    L3-POWER 1 OZ Cu
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SIZE	QTY	SYM	PLATED	TOL
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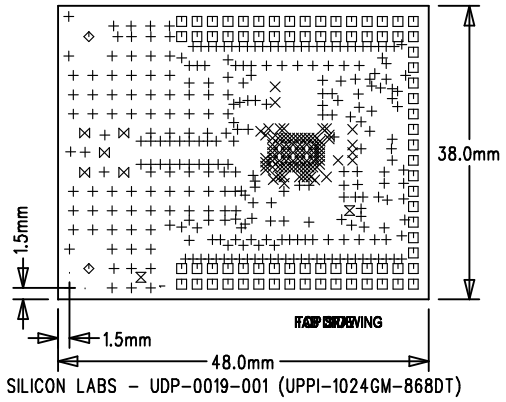
0.03	78	□	YES	+/-0.003"
0.125	2	◇	YES	+/-0.003"
0.04	2	⧖	YES	+/-0.003"
0.07	5	⋈	YES	+/-0.003"



LAYER STACKUP	FILE NAMES
TOP SILKSCREEN	TOPSILK.TSP
TOP SOLDER MASK	SMASKTOP.SMT
TOP SIDE	TOP.TOP
L2	LAYER2.L2
L3	LAYER3.L3
BOTTOM SIDE	BOTTOM.BOT
BOTTOM SOLDER MASK	SMASKBOT.SMB
BOTTOM SILKSCREEN	BOTSILK.BSK

SCALE: NONE

Figure 29. UPPI-1024-fffDT Assembly Layer

CONTACT INFORMATION

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