

ADC3xxx, ADC3xJxx EVM User's Guide

This document is intended to serve as a user's guide for the ADC3xxx EVM and ADC3xJxx EVM. The EVMs provide a platform for evaluating the ADC3xxx which is a dual- or quad-channel, 12- or 14-bit serial LVDS interface, analog-to-digital converter (ADC) with sampling speed grades of 25, 50, 80, and 125 Msps. The ADC3xJxx is a dual- or quad-channel, 12- or 14-bit JESD204B-compliant interface ADC with sampling speed grades of 50, 80, 125, and 160 Msps. This family of converters only requires a single 1.8-V supply, provides flexible input clock dividers, and provides internal features for improved 1/f (ADC32xx, ADC34xx) and SFDR performance. Throughout this document, the abbreviations EVM and ADC3xxxx, and the term *evaluation module* are synonymous with the ADC3xxx EVM and ADC3xJxx EVM, unless otherwise noted.

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1 Introduction

The family of parts and 32 associated EVMs are categorized in [Table 1](#).

Table 1. ADC3xxx Family of Parts and EVMs

ADC Device	Interface	Number of channels	Number of bits	Max Msp/s	EVM
ADC3221	sLVDS	Dual	12	25	ADC3221EVM
ADC3222			12	50	ADC3222EVM
ADC3223			12	80	ADC3223EVM
ADC3224			12	125	ADC3224EVM
ADC3241			14	25	ADC3241EVM
ADC3242			14	50	ADC3242EVM
ADC3243			14	80	ADC3243EVM
ADC3244			14	125	ADC3244EVM
ADC3421	sLVDS	Quad	12	25	ADC3421EVM
ADC3422			12	50	ADC3422EVM
ADC3423			12	80	ADC3423EVM
ADC3424			12	125	ADC3424EVM
ADC3441			14	25	ADC3441EVM
ADC3442			14	50	ADC3442EVM
ADC3443			14	80	ADC3443EVM
ADC3444			14	125	ADC3444EVM
ADC32J22	JESD204B	Dual	12	50	ADC32J22EVM
ADC32J23			12	80	ADC32J23EVM
ADC32J24			12	125	ADC32J24EVM
ADC32J25			12	160	ADC32J25EVM
ADC32J42			14	50	ADC32J42EVM
ADC32J43			14	80	ADC32J43EVM
ADC32J44			14	125	ADC32J44EVM
ADC32J45			14	160	ADC32J45EVM
ADC34J22	JESD204B	Quad	12	50	ADC34J22EVM
ADC34J23			12	80	ADC34J23EVM
ADC34J24			12	125	ADC34J24EVM
ADC34J25			12	160	ADC34J25EVM
ADC34J42			14	50	ADC34J42EVM
ADC34J43			14	80	ADC34J43EVM
ADC34J44			14	125	ADC34J44EVM
ADC34J45			14	160	ADC34J45EVM

There are 3 package sizes and pinouts for all of these parts. The sLVDS dual devices use a 7 × 7 mm, 48-pin QFN, the sLVDS quad devices use an 8 × 8 mm, 56-pin QFN, and the dual and quad JESD204B device share the same package using a 7 × 7 mm 48-pin QFN.

The Dual ADCs comprise 2 buffered inputs, 2 ADC cores, and a common input clock circuit. The quad ADCs comprise 4 buffered inputs, 4 ADC cores and a common input clock circuit. The sLVDS versions have a 2-wire interface per ADC (2 pairs of p/n signals) – for the dual this means 2 sets of 2-wire interfaces (4 p/n pairs), the quad would have 4 sets of 2-wire interfaces (8 p/n pairs). Each of these 2 wire interfaces can be operated in 1-wire mode (14x serialization) or 2-wire mode (7x serialization). For the 12 bit devices this equates to 12x and 6x serialization. The JESD204B versions have 1 lane per ADC core. For the dual this means there will be 2 lanes per device and 4 lanes per device for the quad. Please refer to the data sheet for more information on sLVDS serialization and JESD204B lane configurations.

1.1 EVM Block Diagram

Figure 1 and Figure 2 show a simplified block diagram of the default configuration of the EVM. The two or four analog inputs are supplied to the EVM through a single-ended SMA connection, then transformer coupled to turn the single ended signal into a balanced differential signal and then input to the ADC32xxx or ADC34xxx. A dual transformer input circuit is used for better phase and amplitude balance of the input signal than would typically be produced by a single transformer input circuit.

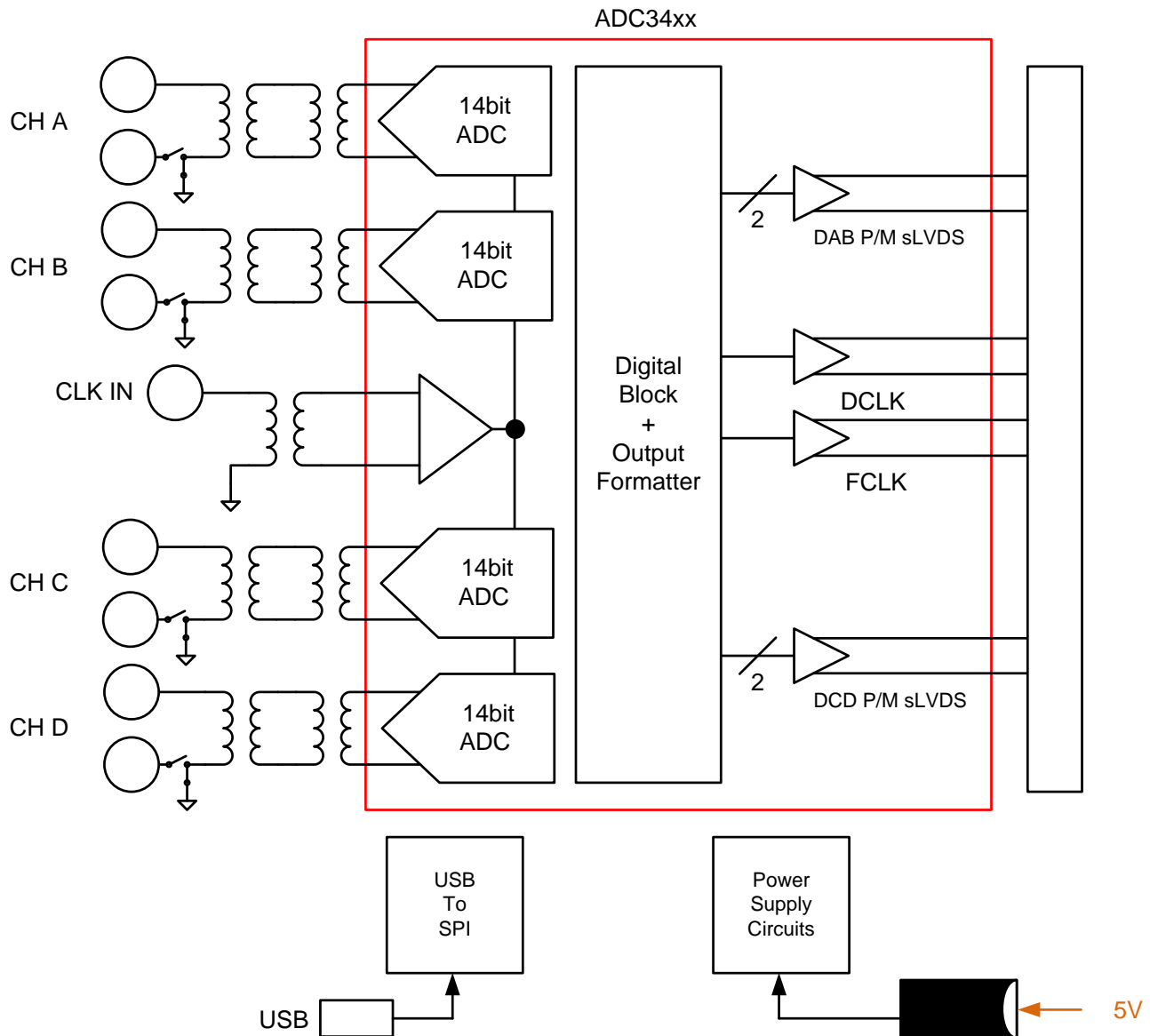


Figure 1. Simplified ADC344x EVM Block Diagram

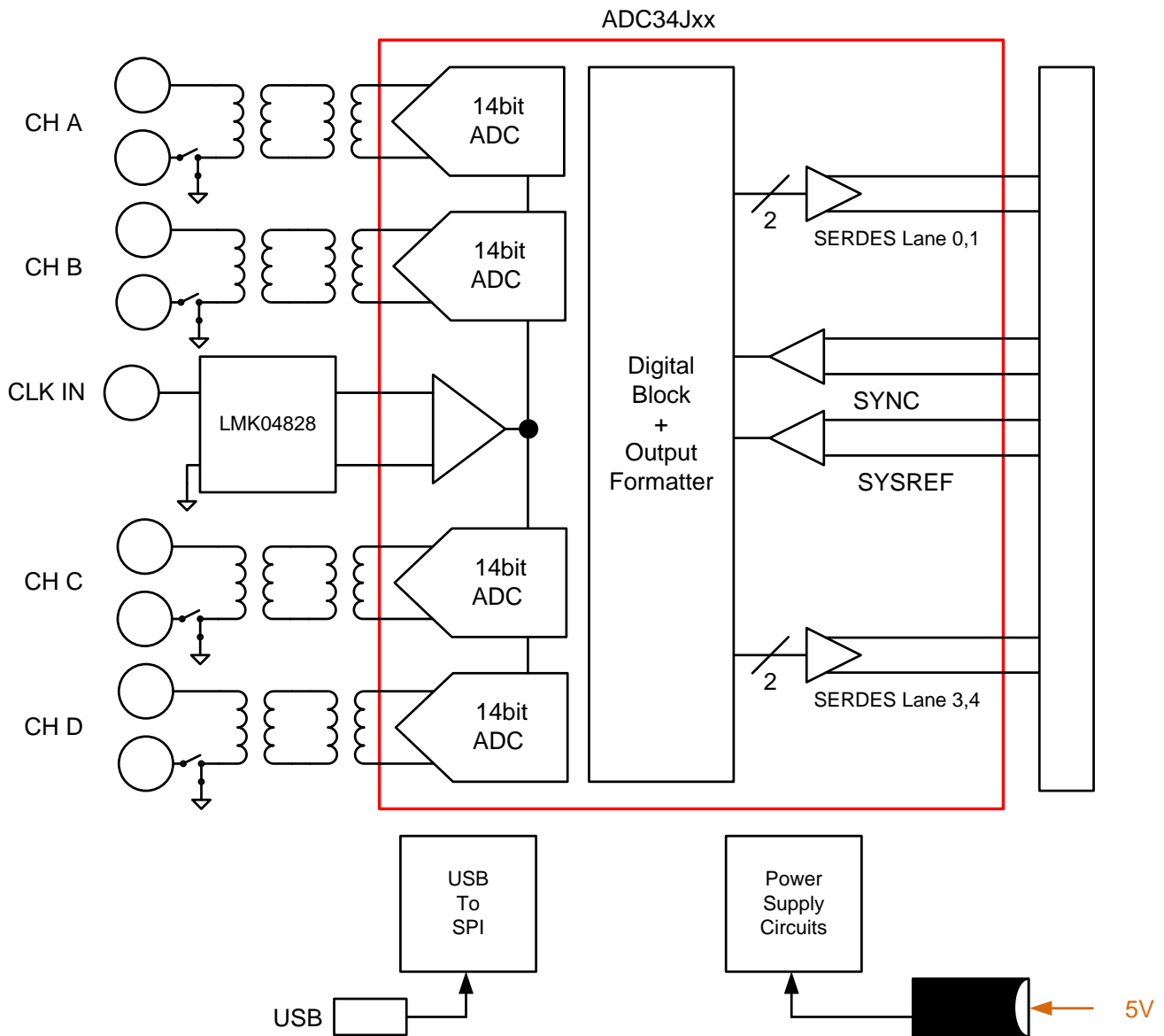


Figure 2. Simplified ADC34Jxx EVM Block Diagram

The clock input is supplied by way of a single-ended signal to an SMA connector and transformer coupled to produce a differential clock signal for the ADC32/34xx EVM. For the ADC32J/34Jxx EVM the clock input can be generated on board using the LMK04828.

Power to the ADC3xxx EVM is typically supplied from a 5V bench supply via the onboard barrel connector and the provided cable, or from an appropriate 5-V, 3A minimum power brick. All necessary voltages for the ADC EVM are derived from the 5-V input connection.

1.2 EVM Power Supply

Figure 3 illustrates the power supply options available on the ADC3xxx EVM. Jumpers are used to choose the power supply options, with the default jumper positions indicated by the darker portion of the jumper that represents the presence of the jumper. Refer to Table 2 for jumper and feedback resistor configuration.

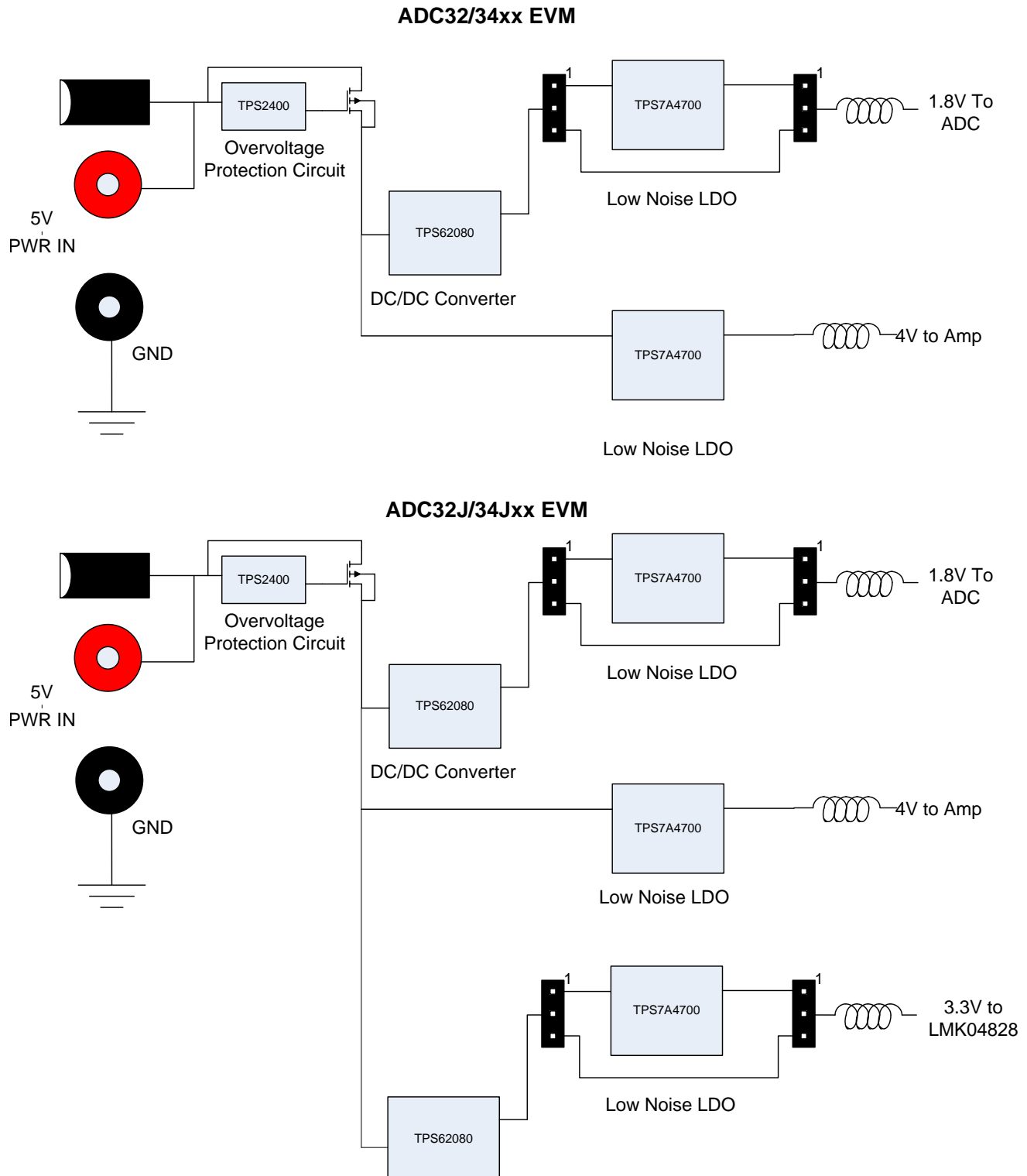


Figure 3. Simplified EVM Power Supply

Table 2. Power Supply Options

Device	Description
ADC32xx JP6: 1-2, JP7: 1-2	Default connection for LDO 1.8-V supply, switch both to 2-3 to use the switcher U4, install R79 for 1.8-V switcher output
ADC34xx JP6: 1-2, JP7: 1-2	Default connection for LDO 1.8-V supply, switch both to 2-3 to use the switcher U4, install R79 for 1.8-V switcher output
ADC342J/34Jxx JP9: 1-2, JP10: 1-2	Default connection for LDO 1.8-V supply, switch both to 2-3 to use the switcher U8, install R152 for 1.8-V switcher output
JP12: 1-2, JP13: 1-2	Default Connection for LDO 3.3 V for LMK04828 power and onboard SPI/CPLD, switch both to 2-3 to use U11 switcher output, install R163 for 3.3-V switcher output

The default power path has an efficient dual output DC-DC switching power supply to first step down the input supplies from 5 V to 4 V and 2.8 V for the subsequent low noise LDOs. The 4 V is used by an LDO to derive 3.3 V for the LMK04828 clock circuits on the ADC3xJxx EVMs. The 2.8 V is used by an LDO to derive a 1.8-V supply for the ADC and USB circuits.

The low noise LDOs can be bypassed to allow the DC/DC power supply to directly provide the ADC power. Please note that the feedback resistors of the DC/DC converter need to be adjusted accordingly. Refer to the ADC EVM schematic for details.

1.3 EVM Connectors and Jumpers

Figure 4 and Figure 5 show the locations of the connectors, jumpers, pushbutton switches, and LED.

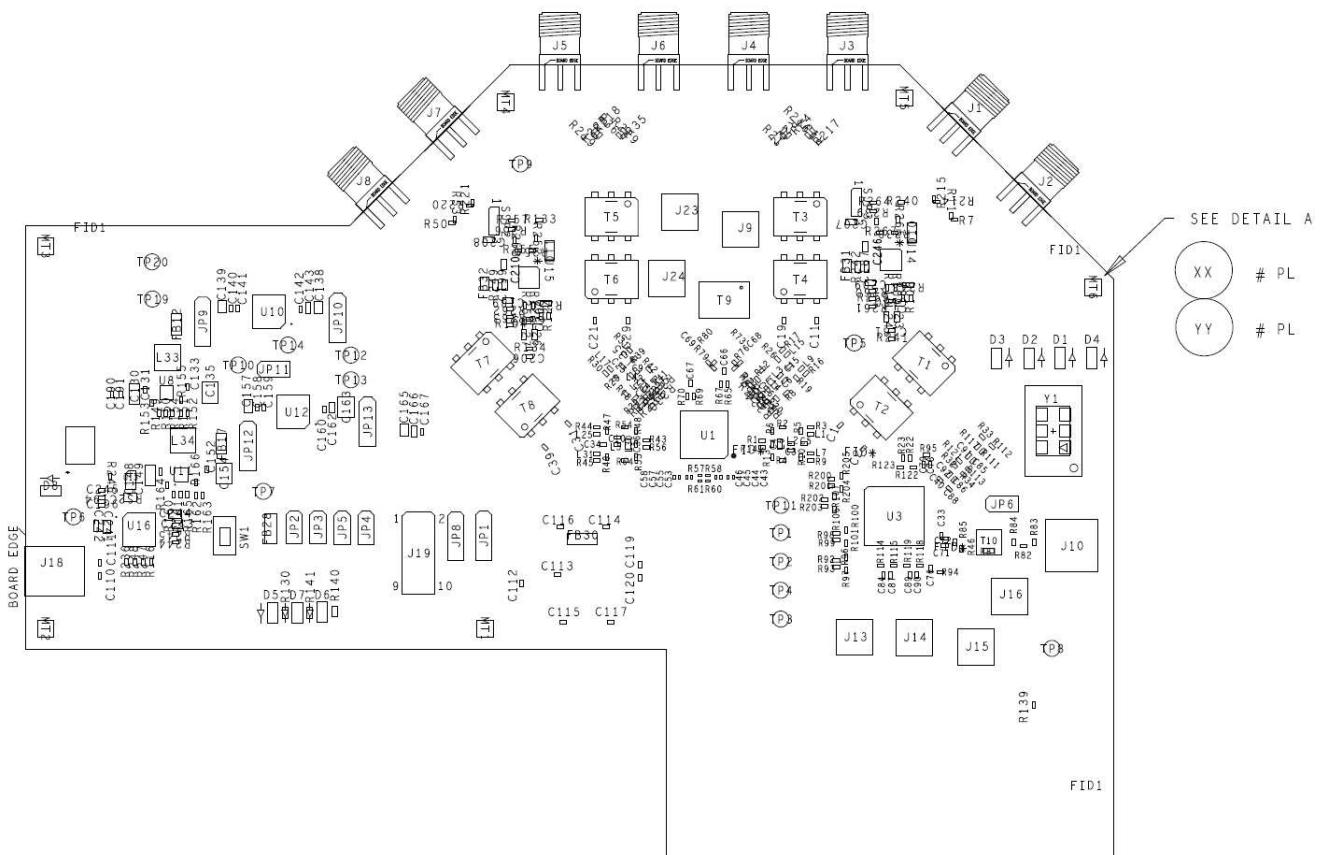


Figure 4. ADC34Jxx EVM Connector and Jumper Locations

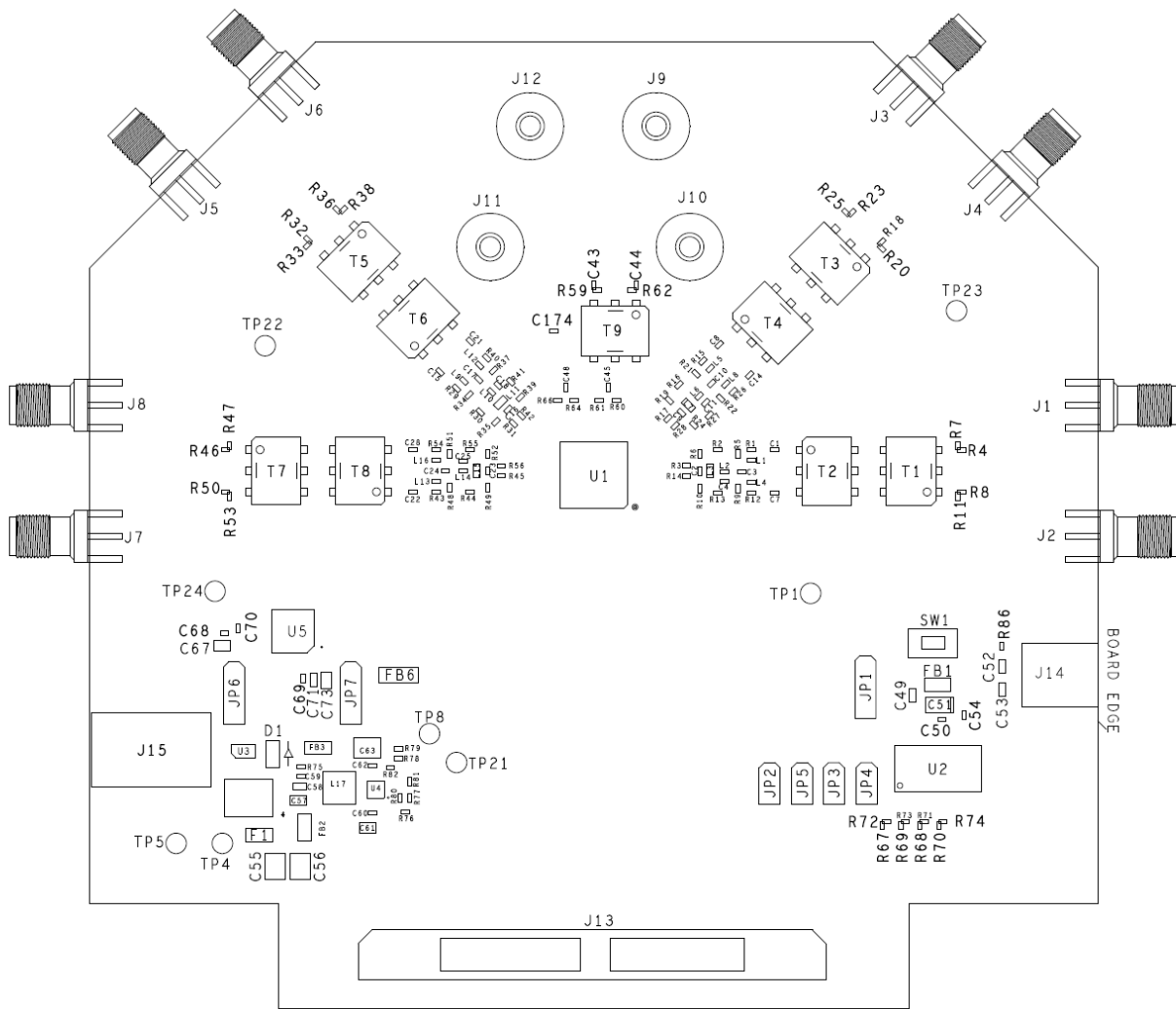


Figure 5. ADC34xx EVM Connector and Jumper Locations

The EVM has a barrel connector for 5-V power. The SMA connectors connect the ADC input and ADC clock input to the ADC. Typically, the ADC inputs are transformer-coupled to accept single-ended connections. The input circuit can be configured to connect to two SMA connectors for differential signaling, if desired. [Table 3](#) lists the connector information for the ADC3xxxx.

Table 3. ADC3xxxx EVM Connectors

Device	Connector	Description
ADC32xx	J1	AINP – positive input for A, Ch1 single ended input
	J2	AINM – negative input for A, DNI
	J3	BINM – negative input for B, DNI
	J4	BINP – positive input for B, Ch2 single ended input
	J9	CLK_INP – positive CLK input, single ended clock input
	J10	CLK_INM – negative CLK input, DNI
	J11	SYSREF_INP – positive input for SYSREF frame clock, single ended input
	J12	SYSREF_INM – negative SYSREF input, DNI
	J13A, B	HSMC data connector to TSW1400 evaluation platform
	J14	Mini USB connector for SPI control
J15	Power connector for 5-V adapter	
ADC34xx	J1	AINP – positive input for A, Ch1 single ended input
	J2	AINM – negative input for A, DNI
	J3	BINM – negative input for B, DNI
	J4	BINP – positive input for B, Ch2 single ended input
	J5	CINP – positive input for C, Ch3 single ended input
	J6	CINM – negative input for C, DNI
	J7	DINM – negative input for D, DNI
	J8	DINP – positive input for D, Ch4 single ended input
	J9	CLK_INP – positive CLK input, single ended clock input
	J10	CLK_INM – negative CLK input, DNI
	J11	SYSREF_INP – positive input for SYSREF frame clock, single ended input
	J12	SYSREF_INM – negative SYSREF input, DNI
	J13A, B	HSMC data connector to TSW1400 evaluation platform
	J14	Mini USB connector for SPI control
J15	Power connector for 5-V adapter	
ADC32J/34Jxx	J1	AIN_CH-AP – positive input for CHA, single ended input (DNI for ADC32Jxx)
	J2	AIN_CH-AM – negative input, (DNI for ADC32Jxx)
	J3	BIN_CH-BP – positive input for CHB (CHA input for ADC32Jxx), single ended input
	J4	BIN_CH-BM – negative input for CHB (CHA input for ADC32Jxx)
	J5	CIN_CH-CP – positive input for CHC (CHB input for ADC32Jxx), single ended input
	J6	CIN_CH-CM – negative input for CHC (CHB input for ADC32Jxx)
	J7	DIN_CH-DP – positive input for CHD, single ended input (DNI for ADC32Jxx)
	J8	DIN_CH-DM – negative input, (DNI for ADC32Jxx)
	J9	EXT_ADC_CLK – external ADC clock connection for ADC, if needed
	J23	EXT SYSREF+ - external SYSREF connection for ADC, if needed (positive input)
	J24	EXT SYSREF- - external SYSREF connection for ADC, if needed (negative input)
	J10	LMK_CLKIN – external input clock for LMK use, if needed (for clock distribution mode)
	J13	DCLKOUT6P – LMK output test point, positive
	J14	DCLKOUT6N – LMK output test point, negative
	J15	DCLKOUT7P – LMK output test point, positive
	J16	DCLKOUT7N – LMK output test point, positive
	J20	5-V input power jack
	J18	Mini USB connector for SPI GUI control
	J19	CPLD JTAG port

The on-board jumper options allow configuration of on-board power supplies and ADC options. Many of the jumper selections that involve DC inputs or static control signals are by way of push-on square post jumpers. The jumper options are listed in [Table 4](#). [Table 4](#) indicates the default settings of the jumpers as the EVM is normally shipped.

Table 4. ADC3xxxx EVM Jumper Options

Device	Jumper	Description
ADC32xx/ADC34xx	JP1	3 pin Jumper – 2-3 Default connection, 1-2 to enable PwDn function
	JP2, J3, JP4,JP5	2 pin Jumper - SPI access points, if needed – default should be installed
ADC32J/34Jxx	JP1	3 pin Jumper – 2-3 Default connection, 1-2 to enable PwDn function
	JP2, J3, JP4,JP5	2 pin Jumper - SPI access points, if needed – default should be installed
	JP6	2 pin, default is connected for powering onboard VCXO
	SJP1	3 pin, DNI, optional for VCXO that require enable on pin 2
	JP11	2 pin, normally connected to enable current monitor for 1.8-V supply to ADC
	JP8	3 pin, default 2-3 for USB SPI selection through CPLD, 1-2 used for FMC connector based SPI port

There is a pushbutton on the ADC3xxxx EVM – *SW1*. Upon powering up, the ADC can either accept hardware reset by pressing *SW1* or toggling the software reset switch on the ADC3xxxx EVM GUI. The default reset configuration of the ADC is given in its respective data sheet.

LED D1 on the ADC32/34xxx is lit to show the presence of the 5-V supply voltage to the EVM. On the ADC32J/34Jxx EVMs, LED D8 is used to show the presence of the 5-V supply voltage to the EVM.

[Table 5](#) lists the description of each LED indicator.

Table 5. ADC3xxxx EVM LED Indicators

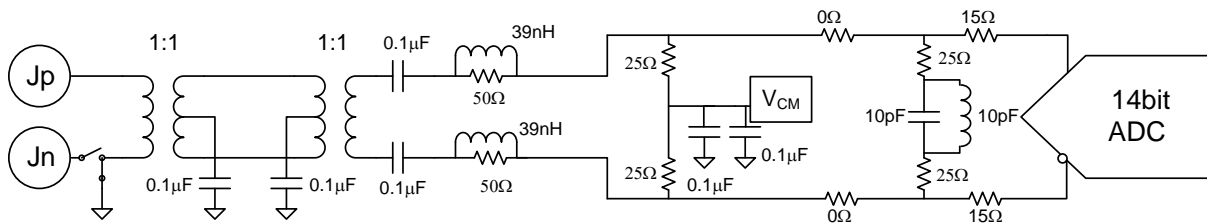
Device	LED	Description
ADC32xx/ADC34xx	D1	5-V power indicator
ADC32J/34Jxx	D1, D2	Status LED from CLKin SEL0/1 on LMK
	D3, D4	Status LED used to indicate LMK Lock or PLL Lock
	D5	Status LED for JESD SYNC
	D6, D7	Spare LED indicators for FMC connector
	D8	5-V power indicator

1.4 EVM ADC Input Circuit Configurations

[Figure 6](#) shows the ADC3xxxx ADC input circuit. The default setup has a dual 1:1 impedance ratio transformer input circuit to achieve better phase and amplitude balance of the input signal than would typically be produced by a single transformer input circuit.

The default input termination is 50 Ω , which is formed by two 25- Ω resistors connected to the ADC VCM node. By default the input circuit is set for operation within the 1st 2 Nyquist zones. For higher frequency inputs use the high frequency input circuit as shown in [Figure 6](#).

Default – Low Input Frequency



High Input Frequency

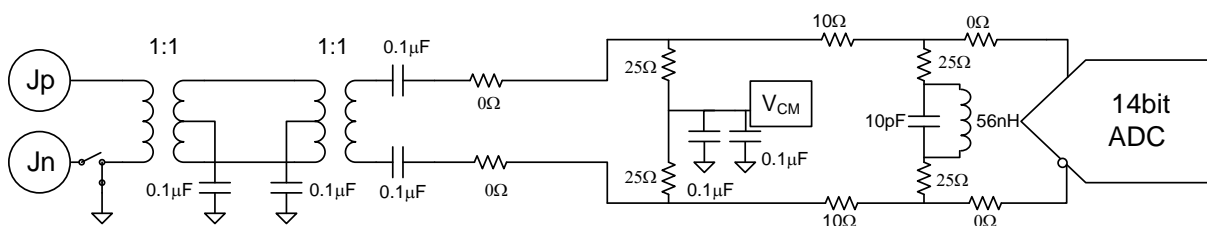


Figure 6. ADC3xxx ADC Input Circuit options

Figure 7 shows the ADC3xxx clock input circuit. The clock signal will go through 1:4 impedance ratio transformer to increase the clock amplitude by two (that is, 1:4 impedance ratio equals to 1:2 voltage ratio). The two 100-Ω resistors will impedance transform back to the primary side as 50-Ω load impedance for the signal source generator. For ADC evaluation, set the signal generator output to approximately +10 dBm.

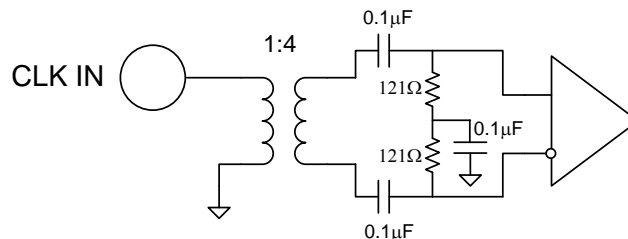


Figure 7. DC34xx Clock Input Circuit

2 Software Control

2.1 Installation Instructions

1. Open the folder named *ADC3xxxx_Installer_vxpx* (xpx represents the latest version)
2. Run *Setup.exe*
3. Follow the on-screen instructions
4. Once installed, launch by clicking on the *ADC3xxxx_GUI_vxpx* program in Start → All Programs → Texas Instruments ADCs
5. When plugging in the USB cable for the first time, you are prompted by the Found-New-Hardware-Wizard to install the USB drivers.
 - (a) When a pop-up screen opens, select *Continue Downloading*.
 - (b) Follow the on-screen instructions to install the USB drivers
 - (c) If needed, access the drivers directly in the install directory

2.2 Software Operation

The software allows programming control of the ADC3xxxx device. The front panel provides a tab for full programming of the register map of the ADC3xxxx and an advanced tab that allows for custom register accesses. The GUI tabs provide a convenient and simplified interface to the most used registers of each device.

2.2.1 ADC3xxxx Control Options

The ADC3xxxx family shares some common registers. These common registers are organized within the common tab. Other specific device registers are in specific device tabs for the ADC3xxxx family and the LMK04828 for the JESD204B devices. For a more detailed description of each register, please see the data sheet.

Common Register Tab

Figure 8 illustrates the following parts of the common tab.

- Software Reset – Resets the registers to default configuration – similar to pressing SW1, self clearing
- Global Power Down – power down the entire chip, default 0
- ADC Standby – All ADCs enter standby mode, default 0
- Configure PwDn pin function – either global power down or ADC standby mode
- Data Format – 0 – 2s Complement, 1- Offset Binary, default 0
- Disable SYSREF BUF – Disable SYSREF Buffer, default 0
- Clk Diver – Internal clock divider to allow harmonic clocking, a higher frequency clock can be provided to the ADC and then divided down to the desired sample rate.

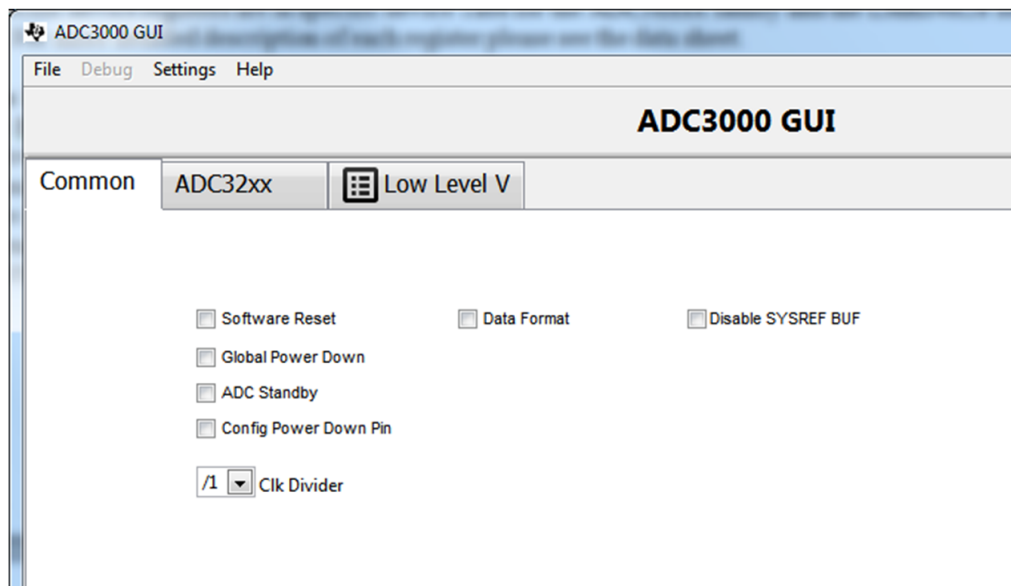


Figure 8. Common Tab

ADC32XX Tab

Figure 9 illustrates the following parts of the ADC32XX tab.

- Disable Dither CHA – disables the dither circuit, if asserted, dither is on by default
- Disable Dither CHB – disables the dither circuit, if asserted, dither is on by default
- CHA PwDn – power down CHA
- CHB PwDn – power down CHB
- CHA Gain Enable – enable the digital gain block for CHA
- CHB Gain Enable – enable the digital gain block for CHB
- Gain CHA – digital gain setting from 0 dB to 6 dB
- Gain CHB – digital gain setting from 0 dB to 6 dB
- Enable Test Pattern – enable the use of test patterns instead of sample data
- Align Test Data – align all test data on the outputs
- Test Pattern CHA – different available test patterns
- Test Pattern CHB – different available test patterns
- Custom Pattern – 14-bit custom bit pattern used when *Custom Pattern* is selected
- Disable Chopper CHA – disable the chopper function which shifts 1/f noise to $F_s/2$, by default it is on
- Disable Chopper CHB – disable the chopper function which shifts 1/f noise to $F_s/2$, by default it is on
- Low Freq Mode – enable for sampling frequencies lower than 35 MHz
- OVR on LSB – over range indication on LSB, by default it is normal LSB function
- LVDS Swing – control the LVDS swing on the LVDS signals

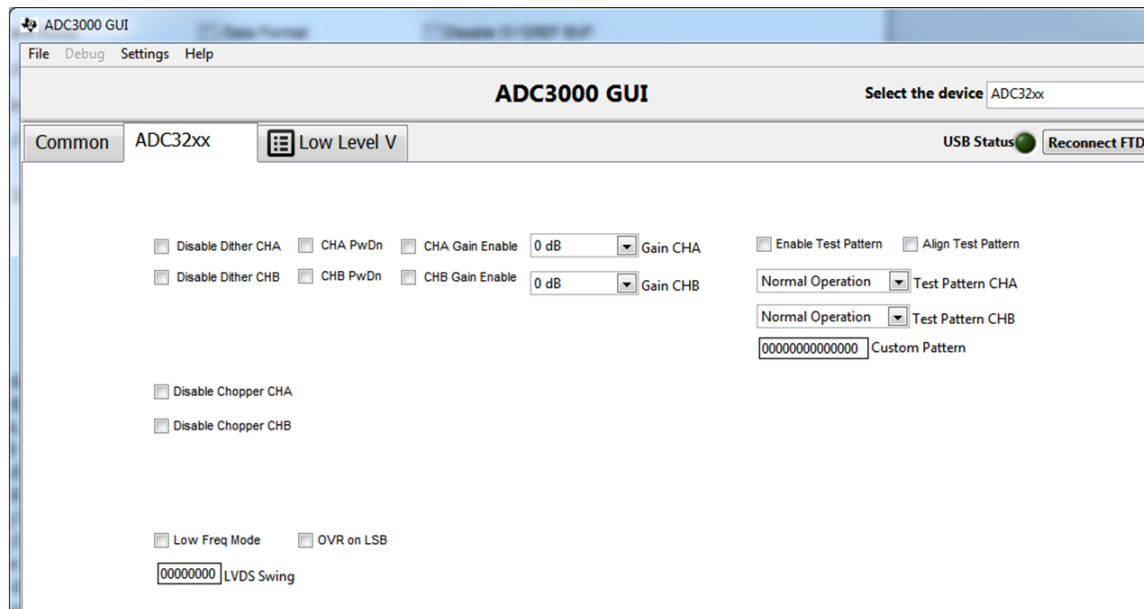


Figure 9. ADC32xx Tab

ADC34XX Tab

- Disable Dither CHA – disables the dither circuit, if asserted, dither is on by default
- Disable Dither CHB – disables the dither circuit, if asserted, dither is on by default
- Disable Dither CHC – disables the dither circuit, if asserted, dither is on by default
- Disable Dither CHD – disables the dither circuit, if asserted, dither is on by default
- CHA PwDn – power down CHA
- CHB PwDn – power down CHB
- CHC PwDn – power down CHC
- CHD PwDn – power down CHD
- CHA Gain Enable – enable the digital gain block for CHA
- CHB Gain Enable – enable the digital gain block for CHB
- CHC Gain Enable – enable the digital gain block for CHC
- CHD Gain Enable – enable the digital gain block for CHD
- Gain CHA – digital gain setting from 0 dB to 6 dB
- Gain CHB – digital gain setting from 0 dB to 6 dB
- Gain CHC – digital gain setting from 0 dB to 6 dB
- Gain CHD – digital gain setting from 0 dB to 6 dB
- Enable Test Pattern – enable the use of test patterns instead of sample data
- Align Test Data – align all test data on the outputs
- Test Pattern CHA – different available test patterns
- Test Pattern CHB – different available test patterns
- Test Pattern CHC – different available test patterns
- Test Pattern CHD – different available test patterns
- Custom Pattern – 14-bit custom bit pattern used when *Custom Pattern* is selected
- Disable Chopper CHA – disable the chopper function which shifts $1/f$ noise to $F_s/2$, default is on
- Disable Chopper CHB – disable the chopper function which shifts $1/f$ noise to $F_s/2$, default is on
- Disable Chopper CHC – disable the chopper function which shifts $1/f$ noise to $F_s/2$, default is on
- Disable Chopper CHD – disable the chopper function which shifts $1/f$ noise to $F_s/2$, default is on
- Low Freq Mode – enable for sampling frequencies lower than 35 MHz
- OVR on LSB – over range indication on LSB, by default it is normal LSB function
- LVDS Swing – control the LVDS swing on the LVDS signals

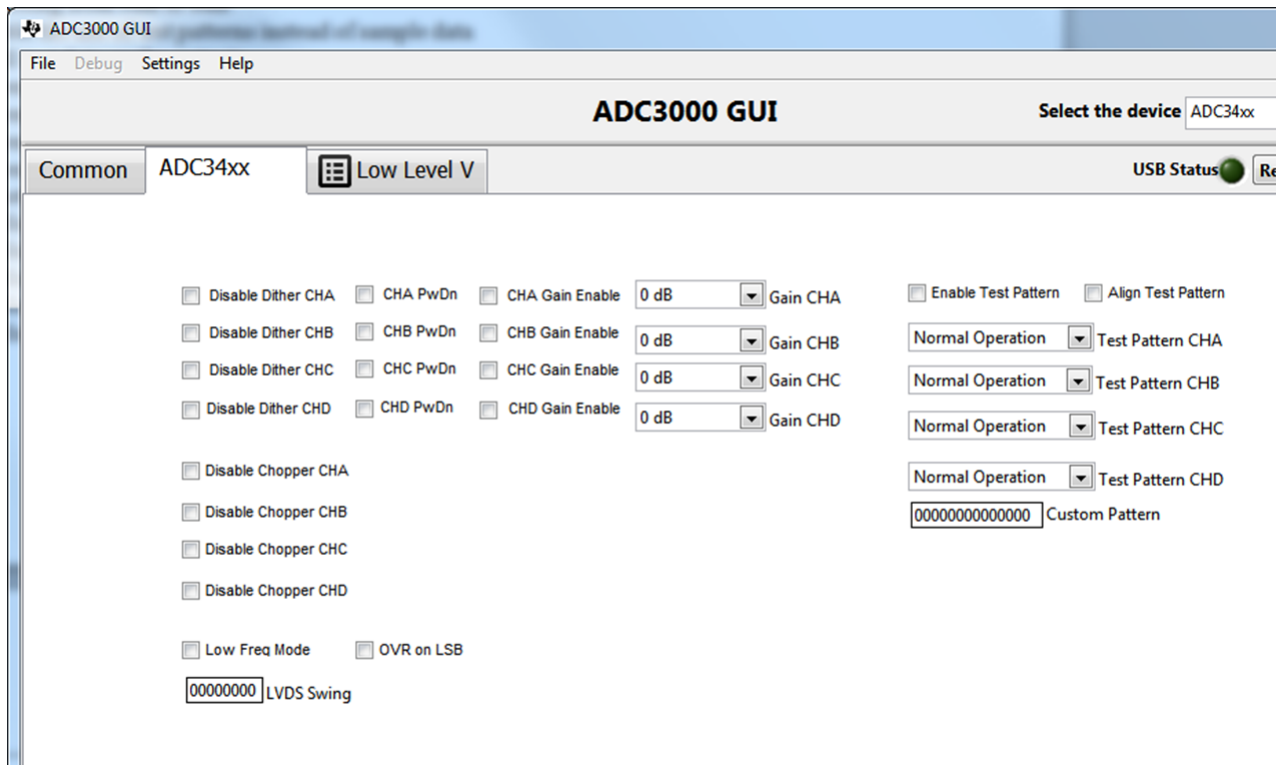


Figure 10. ADC34XX Tab

ADC32Jxx Tab

- Disable Dither CHA – disables the dither circuit if asserted, dither is on by default
- Disable Dither CHB – disables the dither circuit if asserted, dither is on by default
- CHA PwDn – power down CHA
- CHB PwDn – power down CHB
- CHA Gain Enable – enable the digital gain block for CHA
- CHB Gain Enable – enable the digital gain block for CHB
- Gain CHA – digital gain setting from 0 dB to 6 dB
- Gain CHB – digital gain setting from 0 dB to 6 dB
- Enable Test Pattern – enable the use of test patterns instead of sample data
- Align Test Data – align all test data on the outputs
- Test Pattern CHA – different available test patterns
- Test Pattern CHB – different available test patterns
- Custom Pattern – 14-bit custom bit pattern to be used when *Custom Pattern* is selected
- SerDes Test Pattern – available test patterns at the SerDes block
- Idle Sync Pattern – pattern used for SYNC request (K28.5 default)
- Test Mode Enable – option to enable long test pattern as per clause 5.1.6.3
- Flip ADC Data – normal operation is LSB first, enable for MSB first
- Insert Lane Alignment Chars – option to insert lane alignment chars as per clause 5.3.3.4
- TX Link Config – option to disable ILA when SYNC is de-asserted
- Ctrl K – default is 9 (20x mode), enable to use 0x31 for control
- Ctrl F – default is 2 (20x mode), enable to use 0x30 for control
- Scramble EN – optional scrambler
- Subclass – select subclass, default subclass 2
- Generate SYNC Request – generate Sync request
- JESD Buffer Output Current – change output buffer current, default 16 mA
- Link Layer RPAT – change running disparity in RPAT pattern test mode
- Link Layer Test Mode – generate test pattern per clause 5.3.3.8.2
- Pulse Detect Modes – select different Pulse Detection for SYSREF and SYNC
- Force LMF count – force LMF count
- LMF Count INIT – LMF count INIT
- Release ILA SEQ – delay generation of ILA sequence by 0, 1, 2, 3 MF after CGS

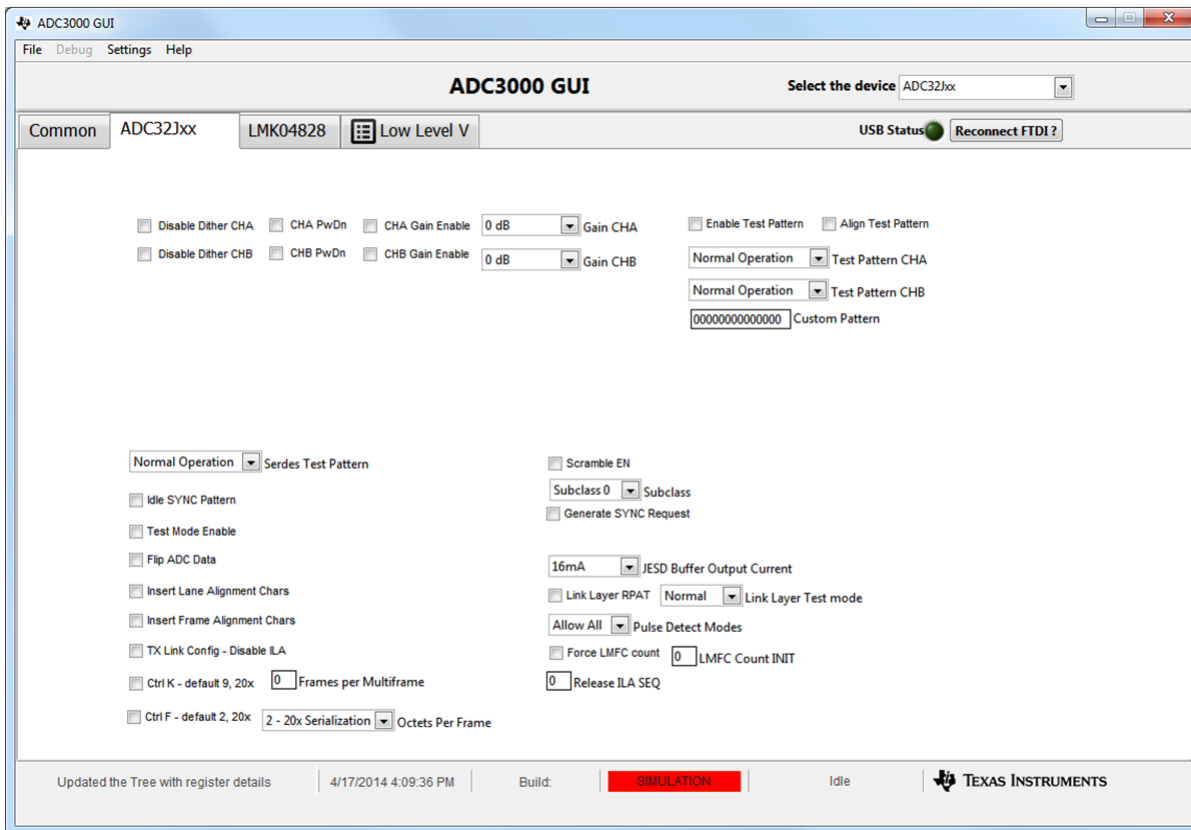


Figure 11. ADC32Jxx Tab

ADC34JXX Tab

- Disable Dither CHA – disables the dither circuit if asserted, dither is on by default
- Disable Dither CHB – disables the dither circuit if asserted, dither is on by default
- Disable Dither CHC – disables the dither circuit if asserted, dither is on by default
- Disable Dither CHD – disables the dither circuit if asserted, dither is on by default
- CHA PwDn – power down CHA
- CHB PwDn – power down CHB
- CHC PwDn – power down CHC
- CHD PwDn – power down CHD
- CHA Gain Enable – enable the digital gain block for CHA
- CHB Gain Enable – enable the digital gain block for CHB
- CHC Gain Enable – enable the digital gain block for CHC
- CHD Gain Enable – enable the digital gain block for CHD
- Gain CHA – digital gain setting from 0 dB to 6 dB
- Gain CHB – digital gain setting from 0 dB to 6 dB
- Gain CHC – digital gain setting from 0 dB to 6 dB
- Gain CHD – digital gain setting from 0 dB to 6 dB
- Enable Test Pattern – enable the use of test patterns instead of sample data
- Align Test Data – align all test data on the outputs
- Test Pattern CHA – different available test patterns
- Test Pattern CHB – different available test patterns
- Test Pattern CHC – different available test patterns
- Test Pattern CHD – different available test patterns
- Custom Pattern – 14-bit custom bit pattern to be used when *Custom Pattern* is selected
- SerDes Test Pattern – available test patterns at the SerDes block
- Idle Sync Pattern – pattern used for SYNC request (K28.5 default)
- Test Mode Enable – option to enable long test pattern as per clause 5.1.6.3
- Flip ADC Data – normal operation is LSB first, enable for MSB first
- Insert Lane Alignment Chars – option to insert lane alignment chars as per clause 5.3.3.4
- TX Link Config – option to disable ILA when SYNC is de-asserted
- Ctrl K – default is 9 (20x mode), enable to use 0x31 for control
- Ctrl F – default is 2 (20x mode), enable to use 0x30 for control
- Scramble EN – optional scrambler
- Subclass – select subclass, default subclass 2
- Generate SYNC Request – generate Sync request
- JESD Buffer Output Current – change output buffer current, default 16 mA
- Link Layer RPAT – change running disparity in RPAT pattern test mode
- Link Layer Test Mode – generate test pattern per clause 5.3.3.8.2
- Pulse Detect Modes – select different pulse detection for SYSREF and SYNC
- Force LMF count – force LMF count
- LMF Count INIT – LMF count INIT
- Release ILA SEQ – delay generation of ILA sequence by 0, 1, 2, 3 MF after CGS

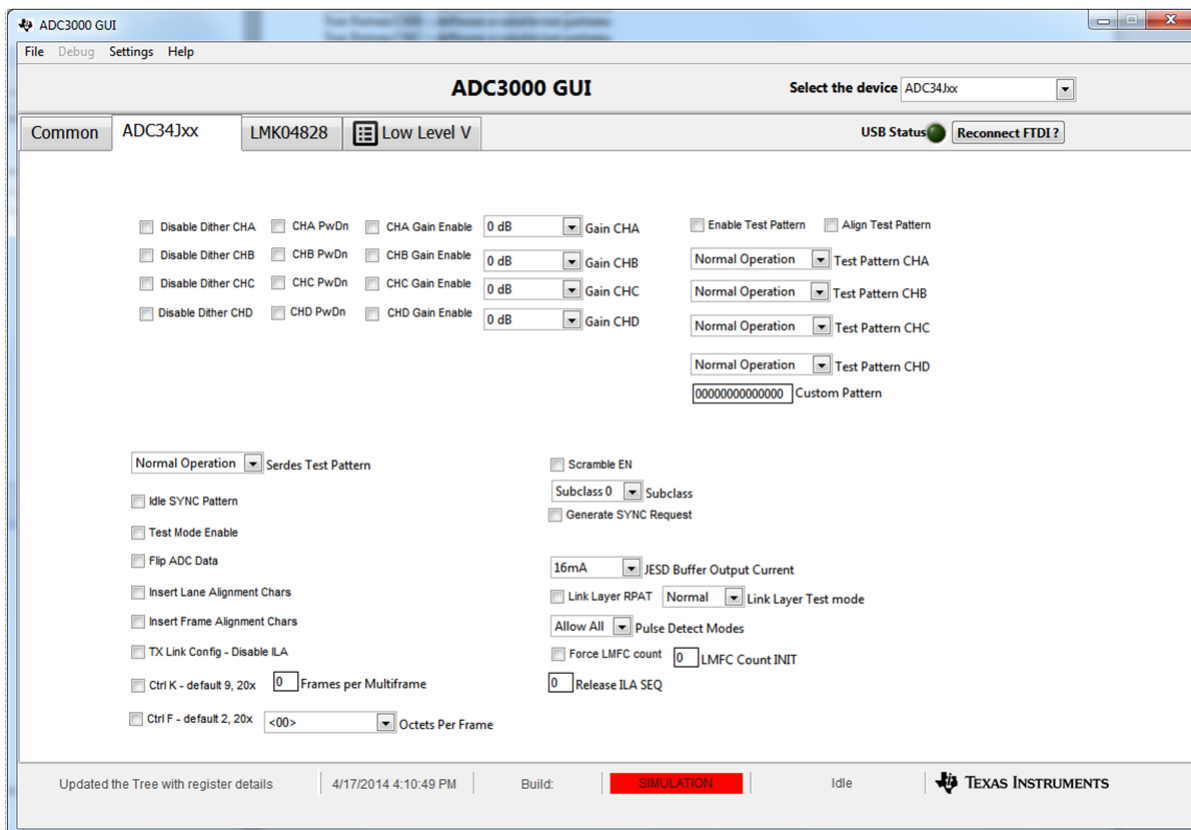


Figure 12. ADC34Jxx Tab

LMK04828

The registers for the LMK04828 are best described in the LMK04828 data sheet – they are not covered in this users guide.

2.2.2 Low Level Register Control

- **Send All:** Sends the register configuration to all devices
- **Read All:** Reads register configuration from ADS58H40 device (not implemented in revision 1.x)
- **Save Regs:** Saves the register configuration for all devices
- **Load Regs:** Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory.
 - Select the **Load Regs** button
 - Double click on the *data* folder
 - Double click on the desired register file
 - Click on **Send All** to ensure all the values are loaded properly

2.2.3 Misc Settings

- **Reconnect FTDI:** Toggle this button if the USB port is not responding. This generates a new USB handle address
NOTE: Reset the board after every power cycle and then click the **reconnect FTDI** button on the GUI.
- **File→Exit:** Stops the program

3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM. There are 2 test platforms which can be used: (1) TSW1400 with ADC32xx and ADC34xx and (2) TSW14J56 or TSW14J50 with ADC32Jxx and ADC34Jxx.

3.1 Test Block Diagram with ADC32xx and ADC34xx

Figure 13 shows the test set-up for evaluation of the ADC3xxx EVM with the TSW1400 Capture Card. As seen in this figure, the evaluation setup involves a clock from a high-quality signal generator and a sine wave for the analog input from a high-quality signal generator. High order, narrow bandpass filters are usually required on clock and input frequencies to remove phase noise and harmonic content from the input sine waves. If the two signal generators are not synchronized by an external reference signal to make the clock and input frequency coherent, then the resulting fast Fourier transform (FFT) will first need to have a windowing function such as Blackman-Harris/Hamming/Hanning applied to the data.

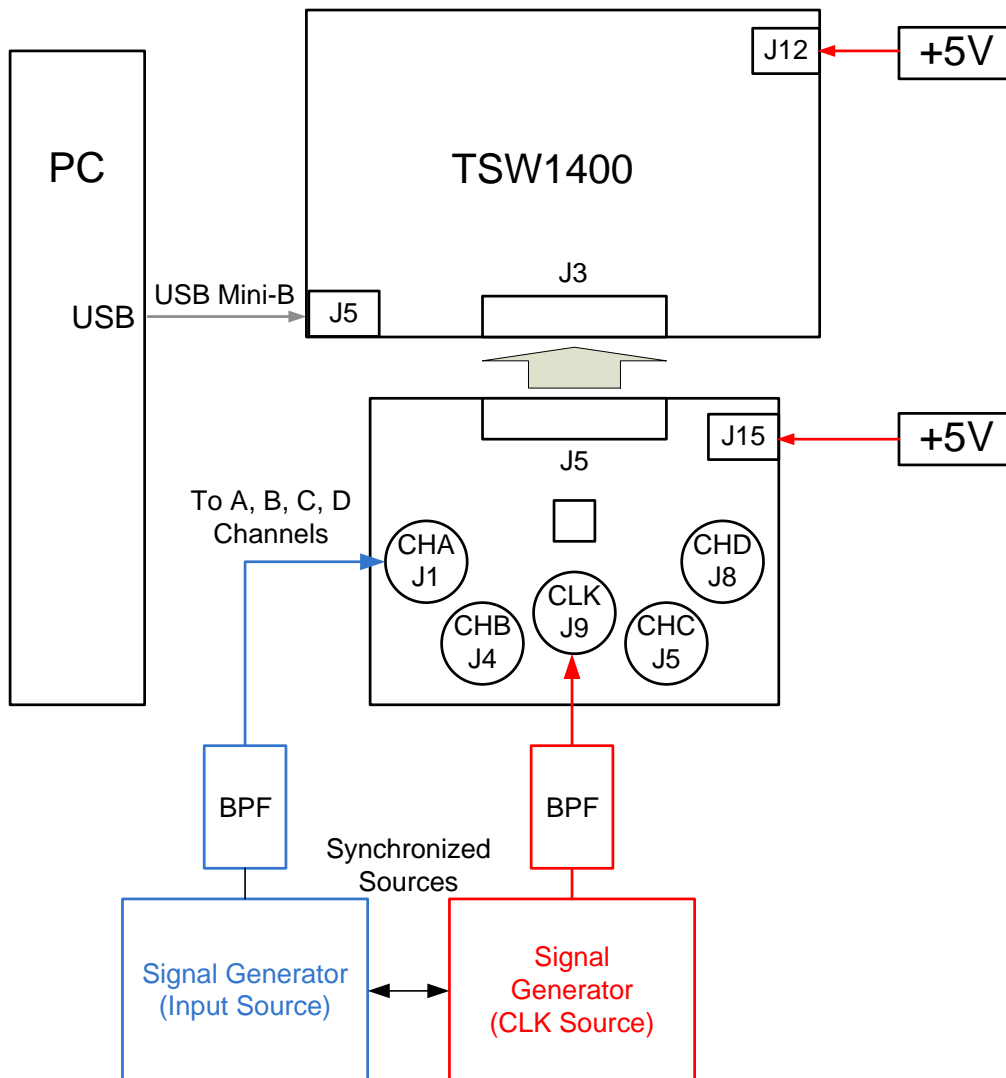


Figure 13. ADC32xx/ADC34xx and TSW1400 Test Setup Block Diagram

3.2 Test Set-up Connection

1. Connect the ADC32xx/ADC34xx EVM J13 connector to the TSW1400 EVM J3 connector
2. Connect 5 V to the TSW1400 J12 supply input connector and 5 V to the ADC32xx/34xx EVM J15 supply input connector
3. Provide a sample clock at the ADC32xx/34xx EVM J9 SMA connector
4. Provide a sine wave for the ADC32xx EVM J1 or J4 analog input and J1, J4, J5, or J8 of the ADC34xx EVM
5. Connect a USB cable from the TSW1400 to the programming computer
6. For basic testing, the USB/SPI connection is not needed on the ADC32/34xx. Press SW1 to perform a hardware reset. This will work with the default settings.
7. Verify the following jumper connections on the ADC32/34xx EVM:
 - **JP1** – 2,3 default condition PDN is low
 - **JP2, JP3, JP4, JP5** – Closed – default condition for SPI connection
 - **JP6** – 1,2 default condition to select LDO power supply
 - **JP7** – 1,2 default condition to select LDO power supply

3.3 ADC32/34xx and TSW1400 Setup Guide

Please reference the TSW1400 User's Guide for more detailed explanations of the TSW1400 set-up and operation. This document assumes the High-Speed Data Converter (HSDC) Pro software and the TSW1400 hardware are installed and functioning properly. *The ADC32/34xx EVM requires High-Speed Data Converter Pro software version 2.6 or higher with TSW1400 hardware of Rev D (or higher).*

Single tone FFT test

1. Start the HSDC Pro GUI program. When the program starts, select the ADC tab and then select ADC324x_2W_14bit.ini or ADC344x_2W_14bit.ini device in the *Select ADC* drop down menu.

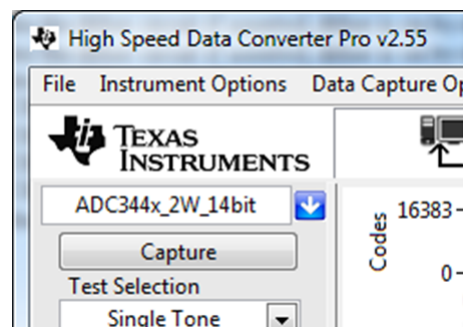


Figure 14. Select ADC32xx or 34xx in the HSDC Pro GUI Program

2. When prompted with *Load ADC Firmware?*, select YES
3. Select Single Tone FFT Test under *Test Selection*
4. Select number of sample points (and resulting number of FFT bins) to be used. The example shown in [Figure 15](#) has 65536 samples.
5. Enter the ADC32/34xx Sampling rate. The example shown in [Figure 15](#) has the sample rate set at 125 Msps (filtered clock input around 10 dBm).
6. Enter the input frequency desired. If the clock and input frequency signal generators are synchronized, then make sure the checkbox for coherent frequency is checked and set the input frequency signal generator to the input frequency displayed. The example shown in [Figure 15](#) has the input frequency set at 10MHz (9.98878479MHz if coherent). Filtered signal input around 10 dBm – adjust to achieve –1 dBFs on the HSDC Pro FFT.
7. Select channel 1, 2, 3, or 4 depending on the channel to which the signal generator is connected
8. Press the **Capture** button on the HSDC Pro GUI

9. Observe an FFT result similar to that of [Figure 15](#)

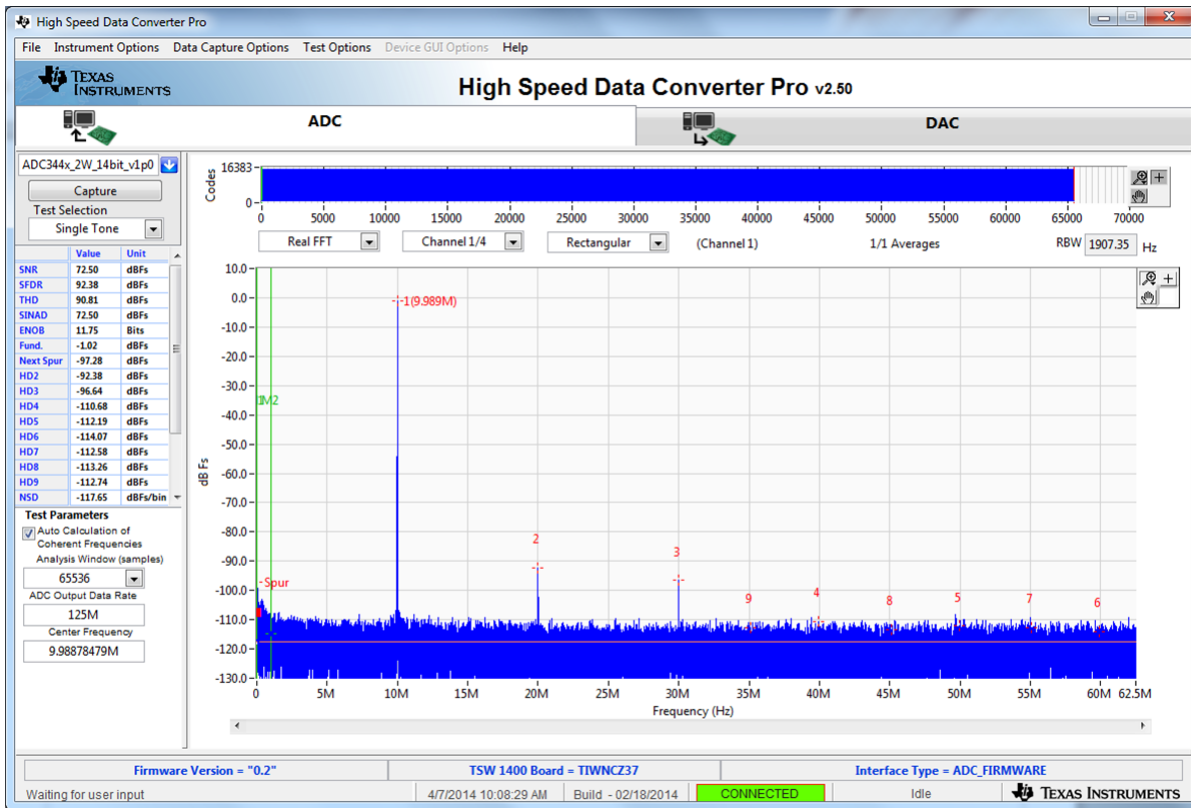


Figure 15. ADC3xxx Operating in 14-Bit Mode at 125 Msps with 10-MHz Input Signal

If the basic capture at this point is correct, then the front panel options of the SPI GUI and the front panel options of the TSW1400 GUI may be varied as desired to test out different device options.

3.4 Test Block Diagram with ADC32Jxx and ADC34Jxx

The test set-up for evaluation of the ADC32J/34Jxx EVM with the TSW14J56 or TSW14J50 Capture Card is shown in Figure 16. As seen in this figure, the evaluation setup involves a clock from a high quality on board clock chip LMK04828 and a sine wave for the analog input from a high-quality signal generator. High order, narrow bandpass filters are usually required to remove phase noise and harmonic content from the input sine waves. Since the on board clock and input sinewave are not coherent then the resulting FFT will need to have a windowing function such as Blackman-Harris/Hamming/Hanning applied to the data.

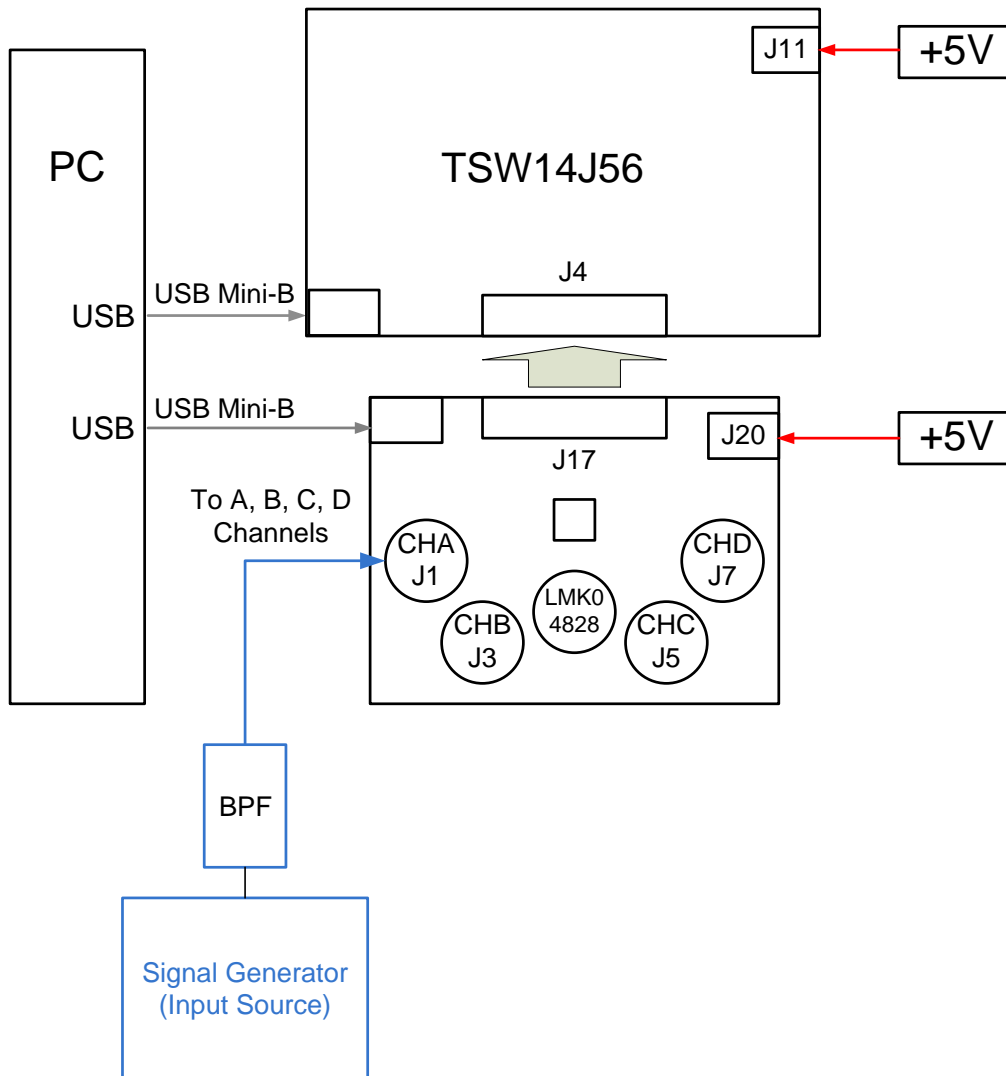


Figure 16. ADC32Jxx/ADC34Jxx and TSW14J56 Test Setup Block Diagram

3.5 Test Set-up Connection (Onboard LMK04828 Clock)

1. Connect J17 connector of ADC32Jxx/ADC34Jxx EVM to J4 connector of TSW14J56 EVM (or TSW14J50 if desired)
2. Connect 5V to the J11 supply input connector of the TSW14J56 and 5V to the J20 supply input connector of the ADC32Jxx/34Jxx EVM
3. Connect a USB cable from the ADC32J/34Jxx EVM to the PC for SPI programming. The ADC32J/34Jxx EVMs require some programming for the on board clock requirements of the JESD204B interface.
4. Provide a sine wave for the analog input at J3 or J6 of ADC32Jxx EVM and J1, J3, J5, or J7 of the ADC34Jxx EVM.
5. Connect USB cable from the TSW14J56 to the programming computer
6. Verify the following jumper connections on the ADC32J/34Jxx EVM
 - JP1 – 1,2 default condition PDN is low
 - JP2, JP3, JP4, JP5 – closed – default condition for SPI connection
 - JP6 – Closed – power for the onboard clock
 - JP8 – 2,3 – default condition to select USB port for SPI communication
 - JP9 – 1,2 – default condition select LDO power
 - JP10 – 1,2 – default condition select LDO power
 - JP12 – 1,2 – default condition select LDO power
 - JP13 – 1,2 – default condition select LDO power

3.6 ADC32J/34Jxx and TSW14J56 Setup Guide

Please reference the TSW14J56 User's Guide for more detailed explanations of the TSW14J56 set-up and operation. This document assumes the HSDC Pro software and the TSW14J56 hardware are installed and functioning properly. *The ADC32/34xx EVM requires HSDC Pro software version 2.6 or higher with TSW14J56 hardware of Rev D (or higher).*

Single Tone FFT Test

- The evaluation of the ADC32J/34Jxx EVM requires programming the LMK04828 clock source with the correct PLL settings to provide a 160 Msps clock.
 - Connect a USB cable from the ADC32J/34Jxx EVM to the PC
 - Open the ADC3000 GUI, and connect to the ADC32Jxx or ADC34Jxx EVM
 - Go to the *Low Level* tab and click **Load Config**
 - Browse and find the *ADC3xJxx_160MSPS_Operation_LMK_Setting.cfg*
 - Check that the PLL2 LED D4 is lit – this indicates that the PLL is programmed properly and the correct clocks are being generated
- Start the HSDC Pro GUI program. When the program starts, select the *ADC* tab and then select *ADC32Jxx_LMF_222* or *ADC34Jxx_LMF_442* device in the *Select ADC* drop-down menu.

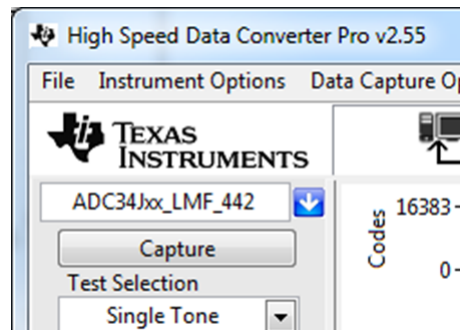


Figure 17. Select ADC32Jxx or 34Jxx in the HSDC Pro GUI Program

- When prompted by *Load ADC Firmware?*, select YES
- Select *Single Tone FFT Test* under *Test Selection*
- Select the number of sample points (and resulting number of FFT bins) to be used. The example shown in [Figure 18](#) has 65536 samples.
- Enter the ADC32J/34Jxx sampling rate. The example shown in [Figure 16](#) has the sample rate set at 160 Msps
- Enter the input frequency desired. The example shown in [Figure 16](#)[Figure 18](#) has the filtered input frequency set at 10 MHz and around 10 dBm – adjust to achieve –1 dBFs on the HSDC Pro FFT plot
- Select channel 1, 2, 3, 4 depending on the channel to which the signal generator is connected
- Press the Capture button on the HSDC Pro GUI
- Observe an FFT result similar to that of [Figure 16](#)

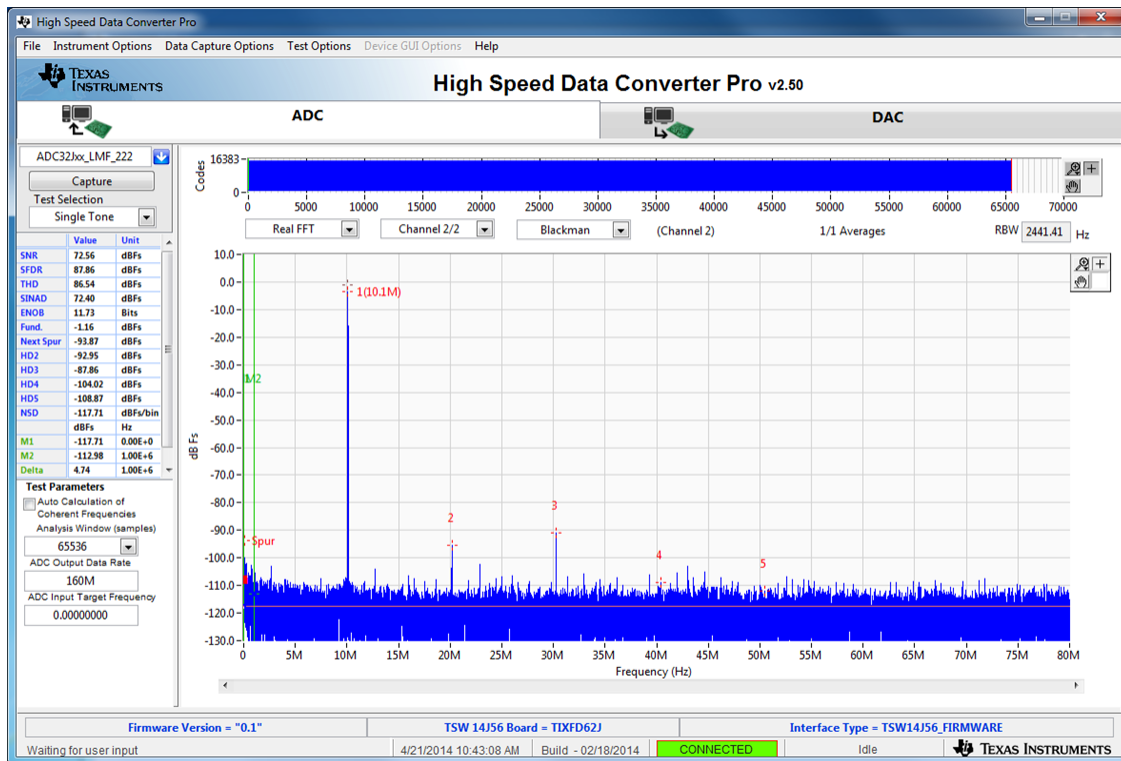


Figure 18. ADC32Jxx Operating in 14-Bit Mode at 160 Msp/s with 10-MHz Input Signal

If the basic capture at this point is correct, then the front panel options of the ADC3xxx SPI GUI and the front panel options of the High Speed Data Converter Pro GUI may be varied as desired to test out different device-specific SPI options.

Revision History

Changes from B Revision (January 2016) to C Revision	Page
• Deleted references to future EVM releases from the <i>ADC3xxx Family of Parts and EVMs</i> table.	3
• Added reference to TSW14J50 in the <i>Basic Test Procedure</i> section.	21
• Added reference to TSW14J50 in the <i>Test Block Diagram with ADC32Jxx and ADC34Jxx</i> section.	24
• Added reference to TSW14J50 in the <i>Test Set-up Connection (Onboard LMK04828 Clock)</i> section.	25

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

Changes from A Revision (September 2014) to B Revision	Page
• Changed the power supply reference to include options for using a 5-V brick or the provided power supply cable with barrel connector.	5

Revision History

Changes from Original (June 2014) to A Revision	Page
• Deleted future release note from ADC3224EVM, ADC3424EVM, ADC34J25EVM, and ADC34J44EVM in Table 1.	3
• Added ADC32J22EVM, ADC32J42EVM, ADC34J22EVM, ADC34J42EVM to <i>ADC3xxx Family of Parts and EVMs</i> table.	3
• Deleted last sentence in paragraph following <i>Power Supply Options</i> table.	7
• Deleted last sentence in the first paragraph on the page.	10
• Deleted entire paragraph preceding <i>ADC3xxxx EVM Jumper Options</i> table.	10
• Deleted several rows from <i>ADC3xxxx EVM Jumper Options</i> table.	10

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