Atmel AVR UC3 32-bit Microcontrollers

UC3L Evaluation Kit

USER GUIDE

Introduction

The Atmel® AT32UC3L-EK is an evaluation kit and development system for the Atmel AVR® UC3 AT32UC3L064 microcontroller.

As an evaluation kit, the board focus is towards Atmel QTouch® and QMatrix™ support, and Atmel picoPower® technology.

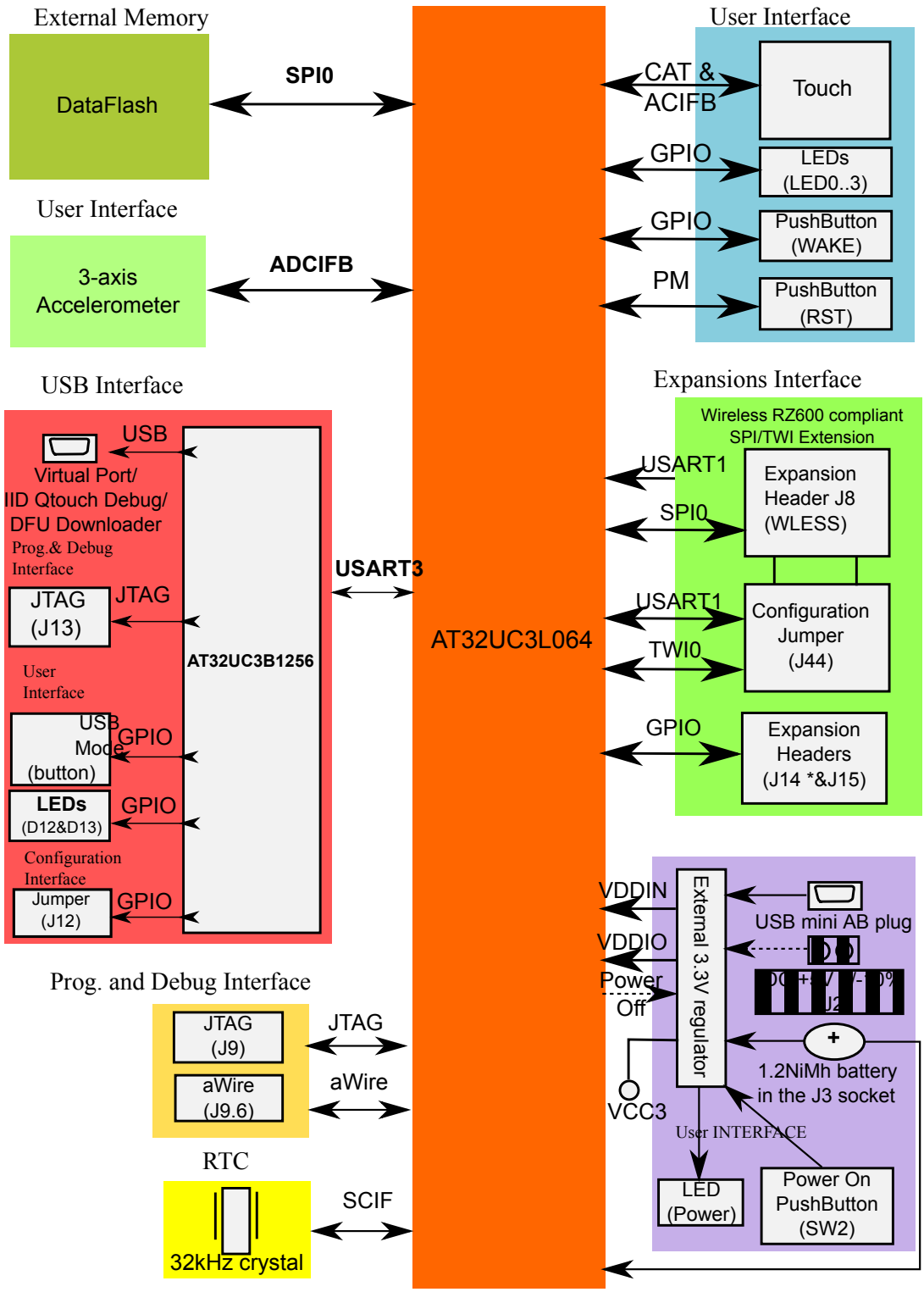
As a development system, the board notably provides on-board memory, a USB communication interface, an accelerometer, and the JTAG programming and debugging interface. The AT32UC3L-EK also features expansion headers; one of these is the wireless expansion header (named WLESS on the PCB), which is the receptacle for one of the two RZ600 radio boards provided in the kit package.

Table of Contents

1. Kit Overview

This chapter lists the features provided by the AT32UC3L-EK evaluation kit and describes the content of the box the kit is packaged in.

Figure 1-1 AT32UC3L-EK Block Diagram



1.1. Features

The following is a list of the main components and interfaces on the AT32UC3L-EK:

- Main MCU: Atmel AVR UC3 32-bit AT32UC3L064 (TQFP48)
  - 64KB internal flash, 16KB internal RAM
  - Up to 50MHz operation
  - Very low power consumption
  - Capacitive touch module for support of QTouch and QMatrix capture from capacitive touch sensors
  - Peripheral event system
  - FlashVault™ allows pre-programmed, secure library support for end user applications
- One touch rotor and five touch sensors
- One 3-axis accelerometer (connected to channels 6, 7, and 8 of the ADCIFB module)
- One serial data flash, 64Mb
- One RTC 32kHz crystal
- Four LEDs
- One pushbutton
- One reset pushbutton
- Wireless expansion connector for the RZ600 AT86RF231 radio board PCBA or for y SPI-based, TWI-based, or USART-based external communication
- 36-pin raw expansion header for GPIO access
- JTAG connector for programming and debugging on the AT32UC3L064 MCU
- Powered through the USB connector, through an external power supply (header), or through a 1.2V battery (header J3)
- USB (2.0 Mini-AB receptacle) connected to the 32-bit AVR UC3 AT32UC3B1256
  - AT32UC3L064 and AT32UC3B1256 are connected through two pins
  - One of the pre-loaded firmware on the AT32UC3B1256 acts as a UART-USB CDC virtual com port gateway
  - One of the pre-loaded firmware on the AT32UC3B1256 acts as UART-to-USB HID QTouch Debug interface to AVR QTouch Studio
  - USB mode pushbutton: with the default pre-loaded firmware on the AT32UC3B1256, the USB mode button is used to select between the UART-USB CDC virtual com port gateway firmware (press the USB mode upon power up of the board) and the UART-to-USB HID QTouch Debug interface to AVR QTouch Studio
  - The J12 jumper can be used to set the AT32UC3B1256 in boot loader mode at power up
  - JTAG connector for programming and debugging the AT32UC3B1256 (J13)

1.2. Kit Contents

The AT32UC3L-EK toolbox contains the following items:

- One AVR Technical Library DVD
- One AT32UC3L-EK customer letter
- One AT32UC3L-EK Getting Started Guide
- One AT32UC3L-EK evaluation kit

- One RZ600 USB adapter board PCBA
- Two RZ600 AT86RF231 radio board PCBA
- Two RF antennas
- One Mini-B plug to std-A plug ~1.5m USB cable
- One 1.2V NiMh rechargeable battery

Figure 1-2 Unpacked AT32UC3L-EK Toolbox

1.3. Power-up and Getting Started

Refer to the AVR32777: AT32UC3L-EK Getting Started Guide.

1.4. Reference Materials

1. The AVR UC3 L0 series datasheet
2. The AT32UC3L-EK Schematics
3. AVR32777: AT32UC3L-EK Getting Started Guide
4. The 32-bit AVR UC3 L series Schematic Checklist
5. The AVR Software Framework

   All pre-loaded firmware source code is available in the AVR Software Framework version 2.0 or higher.
6. The AVR UC3 UART Boot loader
7. The Atmel QTouch Library
8. QTouch Studio
9. Debuggers

2. Hardware Description

This chapter presents the hardware blocks of the AT32UC3L-EK hardware design. Each hardware block is described with:

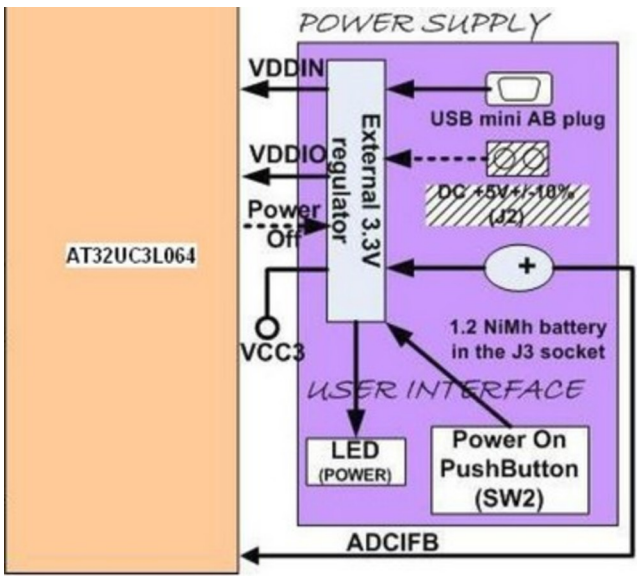
- An overview of the hardware block
- A location in the schematics document
- AT32UC3L-specific information (when relevant)
- All possible hardware configurations of the block and available test points

2.1. Power Supply

The power supply block of the AT32UC3L-EK is in charge of distributing power to all components of the board.

2.1.1. Overview

Figure 2-1 AT32UC3L-EK Power Supply Logical View



The AT32UC3L-EK can be powered from three different sources: the USB Mini-AB plug (5V input), an external power supply connected to the J2 header (DC 5V ± 10%), or a 1.2V NiMh battery (in the J3 socket on the bottom side of the board).

These inputs go through an external 3.3V switch mode regulator, which in turn supplies the rest of the board with a 3.3V voltage.

The power indicator LED, D4, labeled POWER, indicates if the 3.3V from the external regulator is present.

The pushbutton labeled SW2 is there to activate the use of the battery when one is installed in the J3 socket.

The AT32UC3L064 firmware may read the battery current voltage with an ADCIFB channel.

The "Power Off" signal from the AT32UC3L064 to the on-board power supply block can be used to lower the power consumption by software.

To customize the hardware configuration of this block, see Section Configurations and Test Points on page 9, for a description of the possible hardware configurations of the power supply block.

Figure 2-2 AT32UC3L-EK Top View Power Supply Location

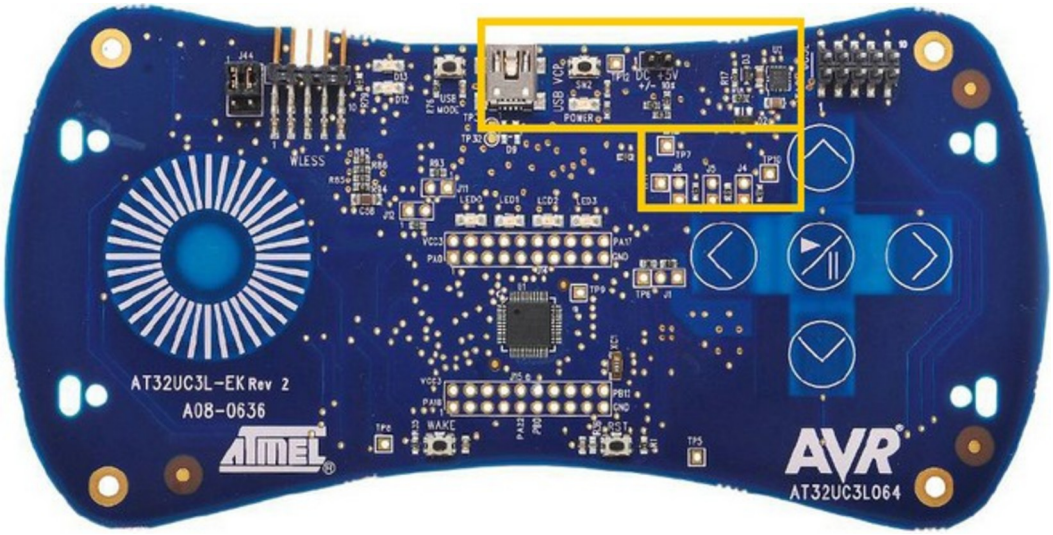
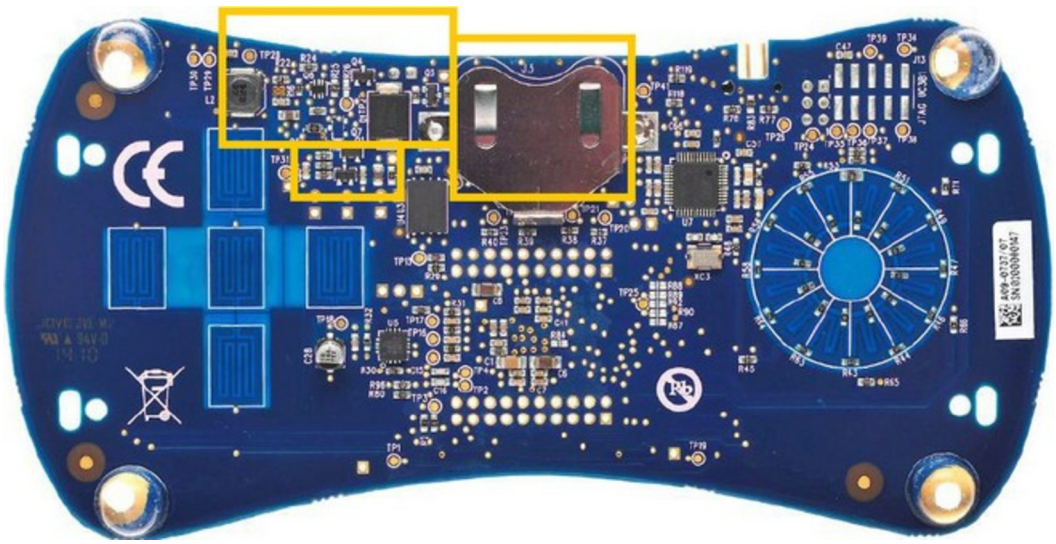


Figure 2-3 AT32UC3L-EK Bottom View Power Supply Location



2.1.2. Schematics

The schematic of the power supply block is on page 2 of the schematics document found here: http://www.atmel.com/Images/AT32UC3L-EK_Schematics.zip document.

2.1.3. UC3L-specific Information

2.1.3.1. Atmel AT32UC3L064 Power Supply Mode

Of the three power supply configurations supported by the AT32UC3L064, this board implements the 3.3V single power supply mode configuration. Refer to the figure, "3.3V single power supply mode", in the AVR UC3 L0 Series datasheet for schematics of this mode: this is how it is implemented on this board.

2.1.3.2. Atmel AT32UC3L064 Pinout for the Power Supply Block

Table 2-1 UC3L Pinout for the Power Supply Block

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
1	N.A.	N.A.	GND
4	PA03	GPIO[3]	The Power-Off signal from the AT32UC3L064 to the power supply block.
17	N.A.	N.A.	VDDIN
18	N.A.	N.A.	VDDCORE
19	N.A.	N.A.	GND
33	N.A.	N.A.	GNDANA
34	N.A.	N.A.	ADVREFP
35	N.A.	N.A.	VDDANA
42	N.A.	N.A.	VDDIO
48	N.A.	N.A.	VDDIO

2.1.4. Configurations and Test Points

2.1.4.1. Hardware Configurations

The default hardware configuration of the power supply block implies that:

- The power supply sources are the battery or the USB plug (thus the dotted-lines on the J2 plug in the block diagram, figure AT32UC3L-EK Power Supply Logical View and Figure 1-1 AT32UC3L-EK Block Diagram on page 4
- The power-off signal from the AT32UC3L064 is not connected to the on-board power supply block (thus the dotted arrow in the block diagram)

To enable the power supply through the J2 connector, mount the R5 resistor (solder patch) and remove the R6 resistor.

To activate the Power-Off signal, remove the R17 resistor and mount the R26 resistor (solder patch).

To locate the resistors mentioned here above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.1.4.2. Test Points

A few test points covering the power supply block have been placed on the AT32UC3L-EK for the verification of important signals.

Table 2-2 Power Supply Block Test Points

Designation	Feature
TP7	Input voltage level after D1 when the J2 external power supply is used
TP8	Input voltage for all boards' components except the AT32UC3L064. Should be 3.3V nominal.
TP9	Input voltage for the AT32UC3L064 VDDIO pin. Should be 3.3V nominal.
TP10	Output voltage out of the external regulator

Designation	Feature
TP11	Input voltage for the AT32UC3L064 VDDIN pin. Should be 3.3V nominal
TP12	GND

To locate the test points mentioned above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

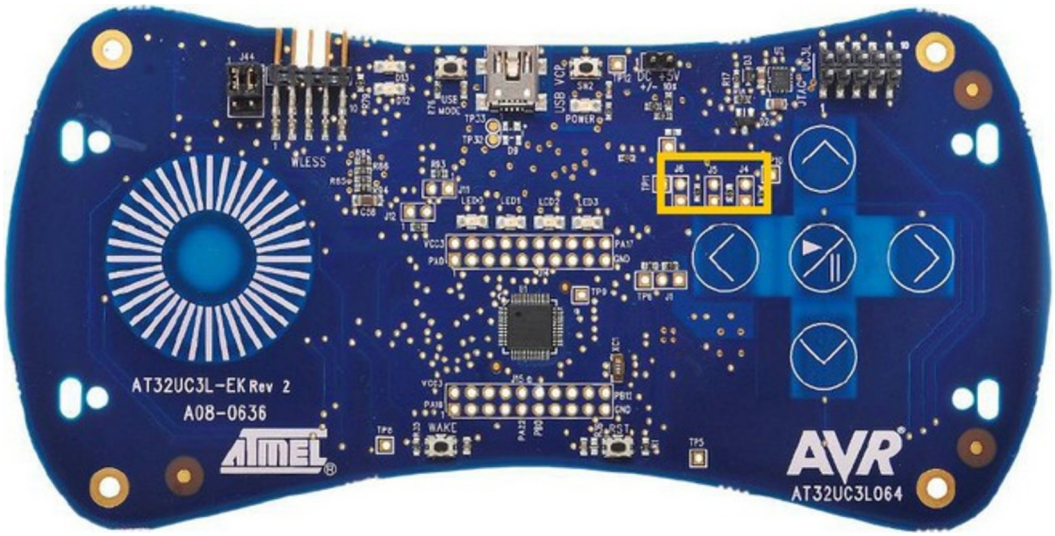
2.1.5. Power Consumption Measurement

To measure the power consumption of the overall board minus the AT32UC3L064, remove the 0Ω R11 resistor and measure the current over the J4 2-pin header (not mounted by default).

To measure the power consumption on the AT32UC3L064 VDDIO, remove the 0Ω R14 resistor and measure the current over the J5 2-pin header (not mounted by default).

To measure the power consumption on the AT32UC3L064 VDDIN, remove the 0Ω R19 resistor and measure the current over the J6 2-pin header (not mounted by default).

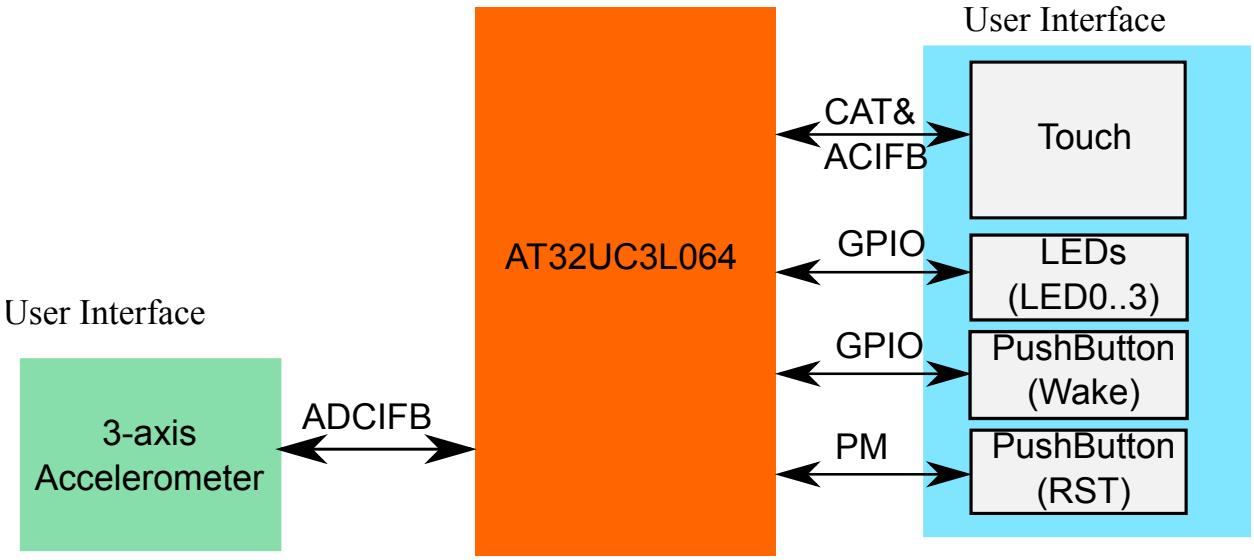
Figure 2-4 AT32UC3L-EK Power Consumption Measurement Headers Location



The above figure points to the location of the power consumption measurement area. To accurately locate the components mentioned above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.2. User Interface

Figure 2-5 AT32UC3L-EK User Interface Logical View



The main user interface offered by the kit is the touch user interface consisting of the wheel sensor and the five button sensors. The touch sensors are implemented by using the QMatrix method (X=6, Y=2). The CAT IP of the AT32UC3L064 is used, as is the ACIFB IP (implied by the use of the QMatrix method). Applications running on the AT32UC3L064 need to use the QTouch library for optimal touch events management.

Four general purpose LEDs (labeled LED0, LED1, LED2, and LED3) are connected to the AT32UC3L064.

The WAKE pushbutton can be used as a general purpose pushbutton, and is connected to the special purpose WAKE_N pin.

The RST pushbutton is used to generate an external reset to the AT32UC3L064. A three-axis accelerometer is connected to three channels of the AT32UC3L064's ADCIFB IP.

Note that there are other user interface components in the kit, and these are related to:

- The USB Interface, presented in Section USB Interface on page 23 of this document
- The power supply interface, presented in Section Power Supply on page 7 of this document

Figure 2-6 AT32UC3L-EK Top View User Interface Location

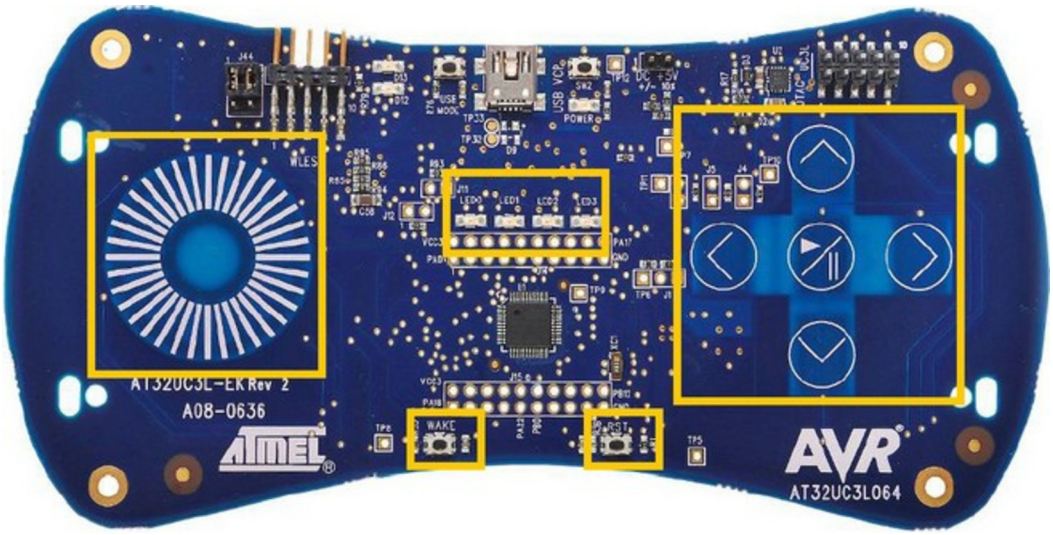
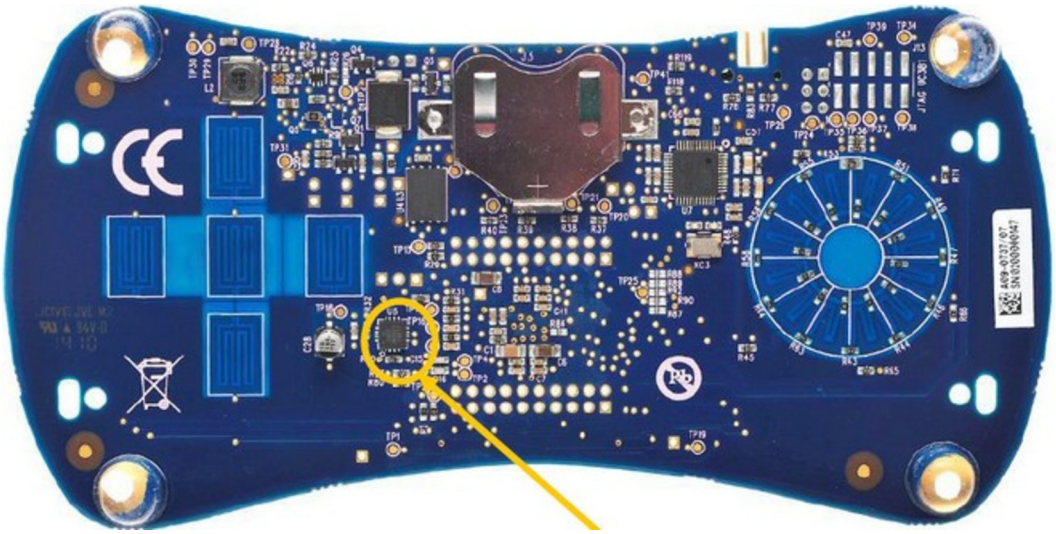


Figure 2-7 AT32UC3L-EK Bottom View User Interface Location



2.2.1. User Interface Schematics

In the Schematic document, the components of the user interface are found:

- On page 1 for the RST pushbutton
- On page 3 for the three-axis accelerometer
- On page 4 for the touch sensors, LEDs, and WAKE pushbutton

2.2.2. UC3L-specific Information

2.2.2.1. Atmel AT32UC3L064 Pinout for the Interface Block

Table 2-3 UC3L Pinout for the Touch Sensors Interface

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
46	PA10	CAT-CSA[5]	QMatrix Y2
47	PA12	CAT-CSB[5]	QMatrix YK2

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
5	PB12	CAT-CSA[15]	QMatrix Y7
29	PB09	CAT-CSB[15]	QMatrix YK7
36	PA14	CAT-CSA[6]	QMatrix X6
37	PA15	CAT-CSB[6]	QMatrix X7
40	PA19	CAT-CSA[10]	QMatrix X10
9	PA22	CAT-CSB[10]	QMatrix X11
21	PB04	CAT-CSA[14]	QMatrix X14
20	PB05	CAT-CSB[14]	QMatrix X15
38	PA16	ACIFB-ACREFN	ACREFN, connected to GNDANA.
39	PA17	CAT-SMP	SMP

Table 2-4 UC3L Pinout for the LEDs and Push-Buttons Interfaces

QFP48 pin	GPIO	GPIO Alternate functions	Feature
24	PA21	GPIO[21] or TC0-B1 or PWMA[21] or SCIF-GCLK[0]	LED0
23	PB10	GPIO[42] or GLOC-OUT[1] or PWMA[33]	LED1
7	PB02	GPIO[34] or TC0-A2 or PWMA[25] or SCIF-GCLK[1]	LED2
8	PB03	GPIO[35] or TC0-B2 or PWMA[26] or TC1-A2	LED3
27	PA11	GPIO[11] controls the pin	WAKE pushbutton
22	N.A.	N.A.	RST pushbutton, connected to the RESET_N pin

Table 2-5 UC3L Pinout for the Accelerometer Interface

QFP48 pin	GPIO	GPIO Alternate functions	Feature
30	PB06	ADCIFB-AD[6]	Ouput VoutX of the accelerometer acquired by ADC channel 6
31	PB07	ADCIFB-AD[7]	Ouput VoutY of the accelerometer acquired by ADC channel 7
32	PB08	ADCIFB-AD[8]	Ouput VoutZ of the accelerometer acquired by ADC channel 8

2.2.3. Hardware Configuration and Test Points

2.2.3.1. Hardware Configuration

The default hardware configuration of the user interface block implies that:

There is no hardware to support debounce on the RST pushbutton: R36 is not mounted, so C4 has no effect. This was done to support the aWire programming and debugging interface (refer to Section Programming and Debug Interface on page 14). To enable the hardware debounce support on the RST pushbutton, mount the 0Ω R36 resistor (solder patch).

To locate the R36 resistor mentioned above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.2.3.2. Test Points

A few test points covering the user interface block have been placed on the AT32UC3L-EK for the verification of important signals.

Table 2-6 User Interface Block Test Points

Designation	Feature
TP1	Input voltage on the AT32UC3L064 RESET_N pin, depending on the state of the RST pushbutton
TP18	Input voltage for the accelerometer. Should be 1.8V nominal
TP15	Output voltage on the accelerometer VoutZ pin
TP16	Output voltage on the accelerometer VoutY pin
TP17	Output voltage on the accelerometer VoutX pin
TP19	Input voltage on the AT32UC3L064 WAKE_N pin, depending on the state of the WAKE pushbutton
TP20	Voltage level on LED0
TP21	Voltage level on LED1
TP22	Voltage level on LED2
TP23	Voltage level on LED3

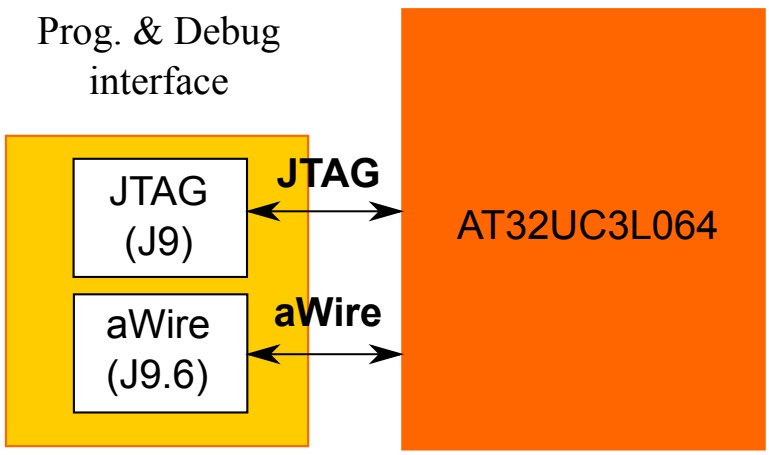
To locate the test points mentioned here above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.3. Programming and Debug Interface

The programming and debugging interface block of the AT32UC3L-EK provides the developer with a means to debug an application running on the AT32UC3L064.

2.3.1. Overview

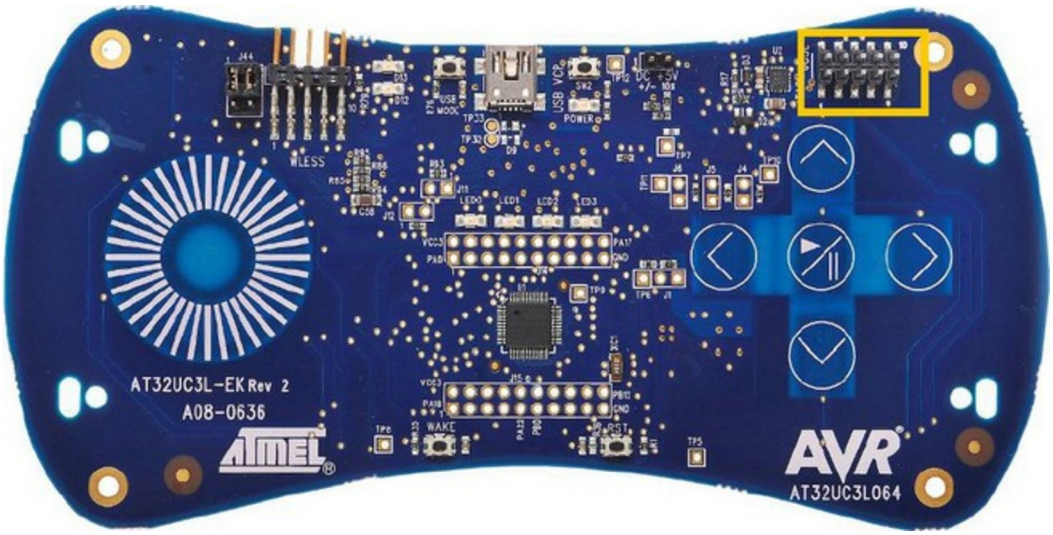
Figure 2-8 AT32UC3L-EK Programming and Debugging Interface Logical View



The main programming and debugging interface of the AT32UC3L-EK is meant to program and debug the AT32UC3L064. There are two debug interfaces available on the AT32UC3L064: the JTAG interface and the aWire interface (single pin debug system), both accessible through the J9 connector.

Note that there is another programming and debugging interface block on the kit, but it is related to the AT32UC3B1256 chip in charge of USB communication (refer to USB Interface on page 23).

Figure 2-9 AT32UC3L-EK Programming and Debugging Interface Location



2.3.2. Schematics

In the Schematics document, the programming and debugging interface is on page 5.

2.3.3. UC3L-specific Information

2.3.3.1. Atmel AT32UC3L064 Pinout for Programming and Debugging Interface

Table 2-7 Atmel AVR UC3L Pinout for Programming and Debugging Interface

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
11	PA00	None	JTAG.TCK
14	PA01	None	JTAG.TMS
13	PA02	None	JTAG.TDO
4	PA03	None	JTAG.TDI
22	N.A.	N.A.	RESET_N pin. Used when enabling/disabling the JTAG or the aWire interface. Also, the aWire data is multiplexed on this pin.

2.3.4. Configuration and Test Points

2.3.4.1. Special Considerations for the RESET_N Pin and the JTAG Pins

On the AVR UC3 L0 series, the RESET_N pin is used to enable/disable the JTAG interface or the aWire interface. For this reason, the RESET_N pin should not be connected to an external reset circuit to avoid drive contention and speed problems. To avoid this issue with the RST pushbutton, the 0Ω R36 resistor is not mounted by default.

On the AVR UC3 L0 series, the JTAG TMS, TDI, TDO, and TCK pins are multiplexed with I/O lines. While using these multiplexed JTAG lines, all normal peripheral activity on these lines is disabled. The user must make sure that no external peripheral is blocking the JTAG lines while debugging.

Conflict conditions over the debugging pins, highlights the components on the AT32UC3L-EK that might interfere with the multiplexed JTAG pins. These components must not be used while debugging with the JTAG interface. Another way to say this is that debugging over the JTAG interface will not work if there is any external signal activity over these components.

Table 2-8 Conflict Conditions over the Debugging Pins

QFP48 pin	GPIO	Conflict conditions
11	PA00	If the WLESS J8 connector is configured with a jumper on J44.3-5, signal activities over J8.1 will conflict with JTAG.TCK
14	PA01	If the WLESS J8 connector is configured with a jumper on J44.4-6, signal activities over J8.2 will conflict with JTAG.TMS
13	PA02	No possible conflicts with JTAG.TDO
4	PA03	• Signal activities over J8.5 will conflict with JTAG.TDI • If the Power-Off signal is enabled (refer to Section Hardware Configurations on page 9, in the Power supply interface chapter), the power supply hardware block or any software activity on the PA03 pin will conflict with JTAG.TDI
22	N.A.	If the 0Ω R36 resistor is mounted, the effect of C4 will conflict with the RESET_N pin

To summarize, debugging will not work if:

- The WLESS connector is used
- The Power-Off signal is enabled by hardware (refer to Section Hardware Configurations on page 9) and the software running on the AT32UC3L064 toggles PA03

2.3.4.2. Test Points

A few test points covering the programming and debugging interface block have been placed on the AT32UC3L-EK for the verification of important signals.

Table 2-9 Programming and Debugging Interface Block Test Points.

Designation	Feature
TP24	JTAG.TCK
TP25	JTAG.TDO
TP26	JTAG.TMS
TP27	JTAG.TDI
TP28	GND
TP29	VCC3
TP30	RESET_N

To locate the test points mentioned above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.3.4.3. Using the aWire

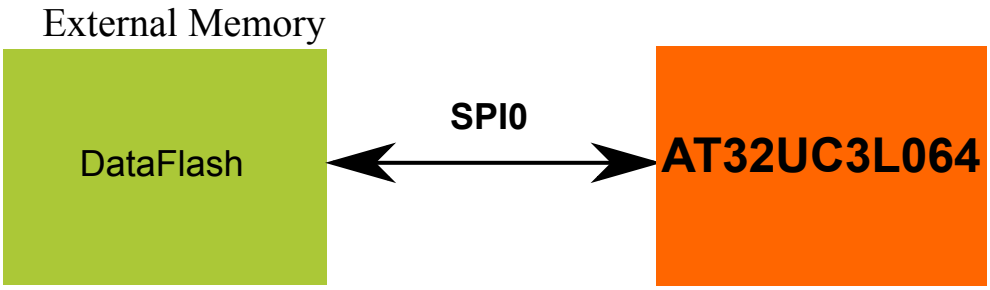
The AVR ONE! and JTAGICE mkII tools can interface with the AVR UC3 L0 series using the single-wire aWire interface. Check the documentation of these tools to know the recommended pinout to connect to an aWire target.

2.4. External Memory

The external memory on the AT32UC3L-EK provides extra memory to the AT32UC3L064.

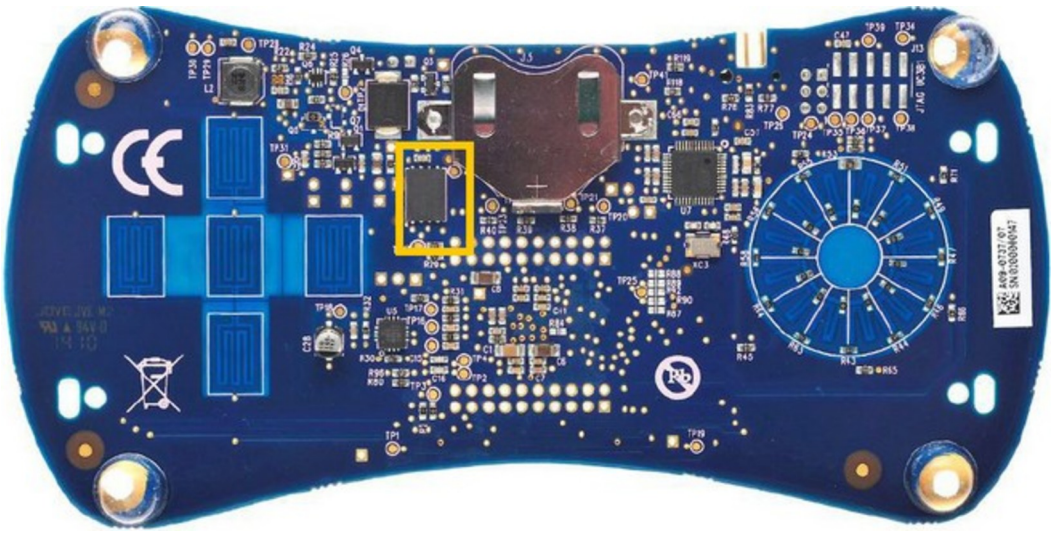
2.4.1. Overview

Figure 2-10 AT32UC3L-EK External Memory Logical View



The AT32UC3L-EK contains a 64Mbit Atmel DataFlash device (AT45DB642D-CNU) that is connected to the SPI0 interface of the AT32UC3L064.

Figure 2-11 AT32UC3L-EK External Memory Logical View



2.4.2. Schematics

In the Schematics document, the external memory is described on page 3.

2.4.3. UC3L-specific Information

2.4.3.1. Atmel AT32UC3L064 Pinout for the Atmel DataFlash

Table 2-10 UC3L Pinout for the Atmel DataFlash

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
28	PA04	SPI0.MISO	DataFlash SO
12	PA05	SPI0.MOSI	DataFlash SI
10	PA06	SPI0.SCK	DataFlash SCK
15	PA07	SPI0.NPCS	DataFlash #CS
22	N.A.	N.A. RESET_N pin	DataFlash #RESET

2.4.4. Configuration and Test Points

2.4.4.1. Special Considerations when using the DataFlash

The pins PA05, PA06, and PA07 are multiplexed with other components on the AT32UC3L-EK.

The following table highlights the components on the AT32UC3L-EK that might interfere with the DataFlash pins. These components must not be used while using the DataFlash.

Table 2-11 Conflict Conditions with the DataFlash

QFP48 pin	GPIO	DataFlash signal	Conflict conditions
28	PA04	DataFlash SO	If the WLESS J8 connector is configured with a jumper on J44.2-4, signal activities over J8.2 will conflict with the DataFlash SO signal.
12	PA05	If the WLESS J8 connector is configured with a jumper on J44.1-3, signal activities over J8.1 will conflict with the DataFlash SI signal.	

To summarize, the DataFlash cannot be used when using an external module on the WLESS connector configured with a jumper on J44.2-4 and/or with a jumper on J44.1-3.

2.4.4.2. Test Points

Two test points covering the Atmel DataFlash have been placed on the AT32UC3LEK for the verification of important signals.

Table 2-12 Atmel Dataflash Test Points

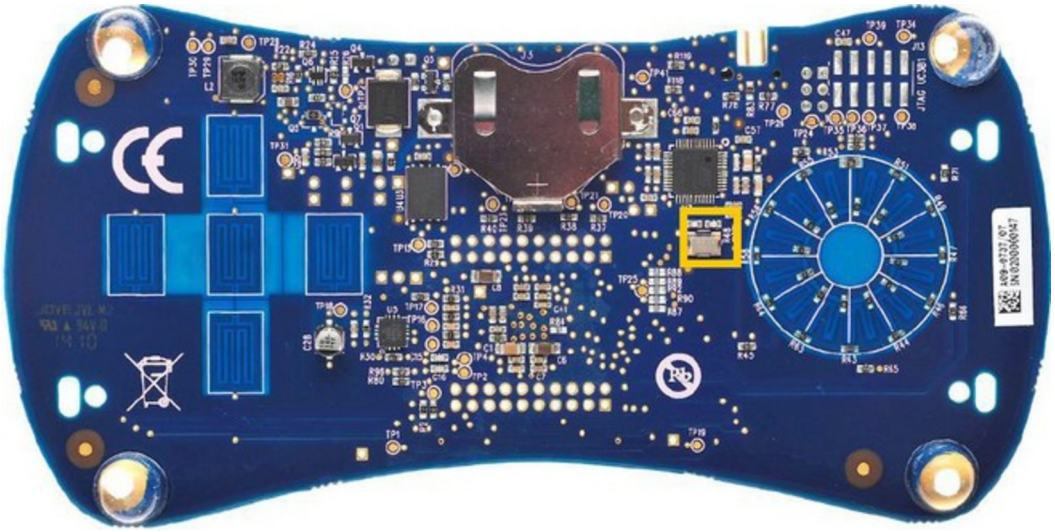
Designation	Feature
TP13	DataFlash #CS
TP14	DataFlash #WP

To locate the test points mentioned above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.5. Real Time Clock

The RTC block on the AT32UC3L-EK provides a 32kHz oscillating crystal to the AT32UC3L064.

Figure 2-12 AT32UC3L-EK Bottom View 32kHz Crystal Location



The AT32UC3L-EK contains a 32kHz crystal connected to the AT32UC3L064.

2.5.1. UC3L-specific Information

2.5.1.1. AT32UC3L064 Pinout for the RTC Clock

Table 2-13 UC3L Pinout for the 32kHz Crystal Connections

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
26	PA13	N.A. XIN32_2	32kHz crystal input
25	PA20	N.A. XOUT32_2	32kHz crystal output

2.5.2. Test Points

Two test points covering the RTC block have been placed on the AT32UC3L-EK for the verification of important signals.

Table 2-14 RTC Block Test Points

Designation	Feature
TP2	32kHz crystal output
TP4	32kHz crystal input

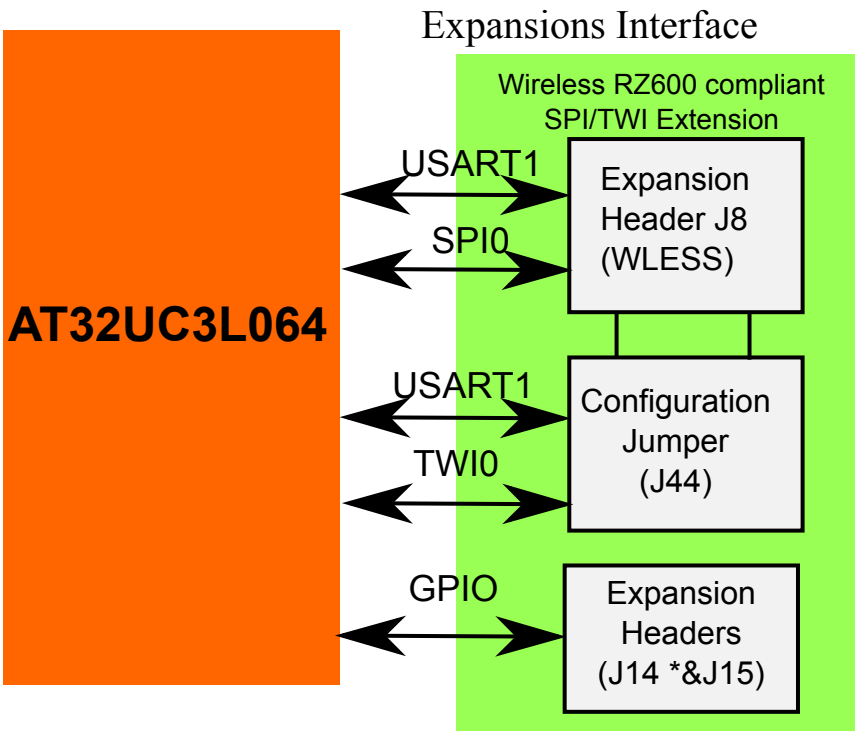
To locate the test points mentioned above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.6. Expansion Interface

The expansion interface on the AT32UC3L-EK offers the possibility to connect various external devices to the AT32UC3L064.

2.6.1. Overview

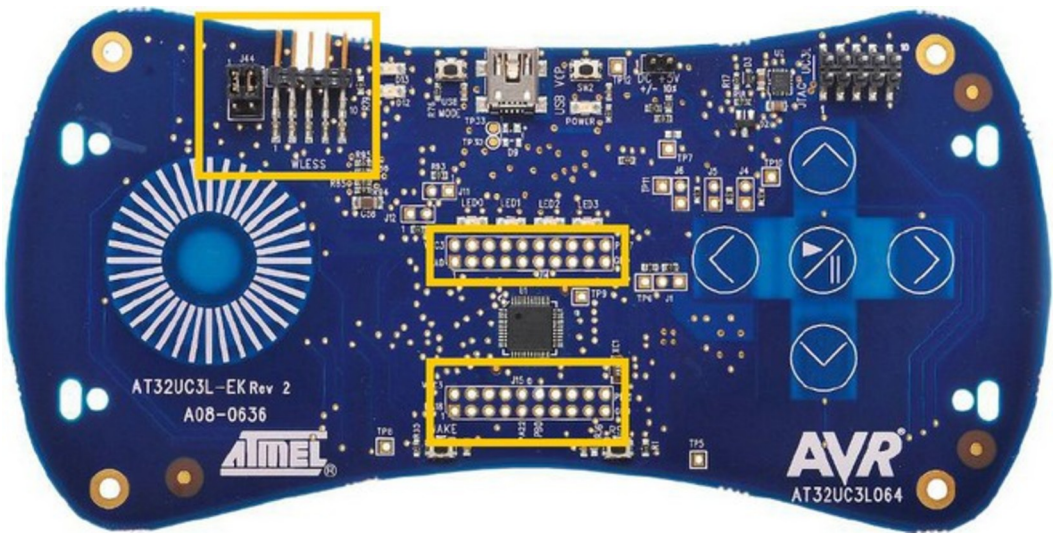
Figure 2-13 AT32UC3L-EK Expansion Interface Logical View



There are two expansion headers on the AT32UC3L-EK:

- The J8 header (labeled WLESS on the PCB) connects the Atmel RZ600 AT86RF231 radio board to provide wireless communication capabilities to the kit. Signals on J8.1 and J8.2 are configurable with the J44 header. The AT32UC3L064 modules available on J8 are USART1 and SPI0. Depending on the J44 configuration, TWI0 is available too.
- The J14 and J15 headers provide access to the AT32UC3L064's GPIOs, ground, and VCC3. This offers the possibility to check signals and/or to expand the board with additional hardware.

Figure 2-14 AT32UC3L-EK Top View Expansion Headers Location



2.6.2. Schematics

In the Schematics document, the expansion headers are described:

- On page 4 for the wireless J8+J44 headers
- On page 7 for the J14 and J15 headers

2.6.3. UC3L-specific Information

2.6.3.1. Atmel AT32UC3L064 Pinouts for the Expansion Headers

Table 2-15 UC3L Pinouts for the J8 and J44 Headers

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
11	PA00	USART1.RTS or GPIO[0] Provides access to the USART1.RTS signal or to the RZ600.RST feature. Available on J8.1 if J44 is configured with a jumper connecting J44.3 to J44.5.	
14	PA01	USART1.CTS or GPIO[1] Provides access to the USART1.CTS signal or to the RZ600.MISC feature. Available on J8.2 if J44 is configured with a jumper connecting J44.4 to J44.6.	
4	PA03	SPI0.NPCS[1] RZ600 SPI chip select. Available on J8.5.	
28	PA04	SPI0.MISO RZ600.MISO signal. Available on J8.7.	
28	PA04	TWI0.TWCK Provides access to the TWI0 TWCK signal. Available on J8.2 if J44 is configured with a jumper connecting J44.2 to J44.4.	
12	PA05	SPI0.MOSI RZ600.MOSI signal. Available on J8.6.	
12	PA05	TWI0.TWD Provides access to the TWI0 TWD signal. Available on J8.1 if J44 is configured with a jumper connecting J44.1 to J44.3.	
10	PA06	SPI0.SCK RZ600 SPI clock. Available on J8.8. 3 PA08 USART1.TX or GPIO[8] Provides access to the RZ600.SLP_TR feature or to the USART1.TX signal. Available on J8.4.	
2	PA09	USART1.RX or GPIO[9] Provides access to the RZ600.IRQ feature or to the USART1.RX signal. Available on J8.3.	
N.A.	N.A.	N.A.	GND. Available on J8.9.
N.A.	N.A.	N.A.	VCC3. Available on J8.10.

Table 2-16 UC3L Pinouts for the J14 Header

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
11	PA00	Software-dependent	J14.1
14	PA01	Software-dependent	J14.3
13	PA02	Software-dependent	J14.5
4	PA03	Software-dependent	J14.7

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
28	PA04	Software-dependent	J14.9
12	PA05	Software-dependent	J14.11
10	PA06	Software-dependent	J14.13
15	PA07	Software-dependent	J14.15
3	PA08	Software-dependent	J14.17
-	-	-	GND on J14.19
-	-	-	VCC3 on J14.2
2	PA09	Software-dependent	J14.4
46	PA10	Software-dependent	J14.6
27	PA11	Software-dependent	J14.8
47	PA12	Software-dependent	J14.10
26	PA13	Software-dependent	J14.12
36	PA14	Software-dependent	J14.14
37	PA15	Software-dependent	J14.16
38	PA16	Software-dependent	J14.18
39	PA17	Software-dependent	J14.20

Table 2-17 UC3L Pinouts for the J15 Header

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
41	PA18	Software-dependent	J15.1
40	PA19	Software-dependent	J15.3
25	PA20	Software-dependent	J15.5
24	PA21	Software-dependent	J15.7
9	PA22	Software-dependent	J15.9
6	PB00	Software-dependent	J15.11
16	PB01	Software-dependent	J15.13
7	PB02	Software-dependent	J15.15
8	PB03	Software-dependent	J15.17
-	-	-	GND on J15.19
-	-	-	VCC3 on J15.2
21	PB04	Software-dependent	J15.4
20	PB05	Software-dependent	J15.6
30	PB06	Software-dependent	J15.8

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
31	PB07	Software-dependent	J15.10
32	PB08	Software-dependent	J15.12
29	PB09	Software-dependent	J15.14
23	PB10	Software-depenent	J15.16
44	PB11	Software-depenent	J15.18
5	PB12	Software-dependent	J15.20

2.6.4. Configuration and Test Points

2.6.4.1. Configuration

The J8.1 and J8.2 pins are configurable through the J44 header. Refer to Table Table 2-15 UC3L Pinouts for the J8 and J44 Headers on page 21, for a description of the possible configurations.

2.6.4.2. Test Points

None.

2.6.4.3. Special Considerations when using the Expansion Headers

The J8+J44 expansion headers gather signals multiplexed with the JTAG signals on J8.1, J8.2, and J8.5. For this reason, JTAG debugging is not possible when an external component is connected to these pins of the WLESS header. See also Section Special Considerations for the RESET_N Pin and the JTAG Pins on page 15.

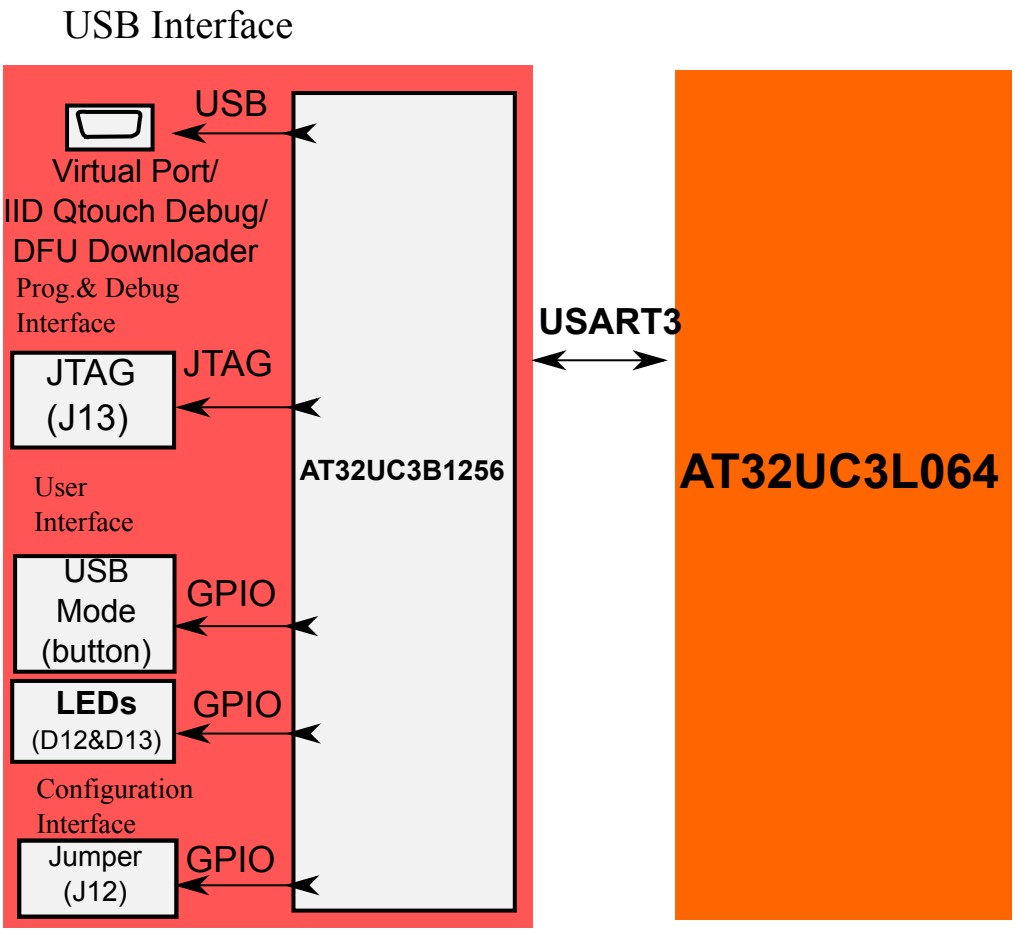
The J14 and J15 headers gather all GPIO signals of the AT32UC3L064. Obvious care should be taken when accessing pins that are being used by another component of the kit.

2.7. USB Interface

The USB interface on the AT32UC3L-EK offers USB communication capabilities to the AT32UC3L064 through the on-board AT32UC3B1256 device.

2.7.1. Overview

Figure 2-15 AT32UC3L-EK USB Interface Logical View



The USB interface provides two features to the AT32UC3L-EK kit:

- USB communication
- Power supply (see Section Power Supply on page 7 for a description of that feature)

The USB controller is the AT32UC3B1256.

The AT32UC3B1256 comes pre-loaded with several firmware components:

- A USB DFU boot loader [accessible upon power up when the J12 header is closed (see Figure 2-16 AT32UC3L-EK Top View USB Interface Location on page 25, for the location of the J12 header)] to re-program the AT32UC3B1256
- A USB CDC-USART bridge (a USB CDC virtual com port) where every data character received from the USB is sent to the AT32UC3L064's USART3, and every character received from the AT32UC3L064's USART3 is sent to the USB
- A HID QTouch Debug firmware acting as a USB HID-USART bridge between AVR QTouch Studio (Reference Materials on page 6) and the AT32UC3L064's USART3
- A tiny boot selector allowing the user to choose (using the USB MODE pushbutton) upon power up between running the virtual com port firmware or the HID QTouch Debug firmware. By default the HID QTouch Debug firmware will be running. See also Reference Materials on page 6.

The source code of this firmware is available in the AVR Software Framework (Reference Materials on page 6).

The user interface of the USB interface block is made of:

- Two LEDs, D12 and D13, [with the default firmware (except the USB DFU boot loader) these LEDs are blinking, depending on the activity over the USB]
- The USB MODE pushbutton on the PCB. With the default pre-loaded firmware, this button is used at power up to choose between the virtual com port firmware or the HID QTouch Debug firmware (see Configuration and Test Points on page 26 for the AT32UC3B1256 default firmware configuration).

The AT32UC3B256 can be programmed:

- Through the JTAG interface J13 header (see Figure Figure 2-17 AT32UC3L-EK Bottom View USB Interface Location on page 26 for the location of the J13 header)
- Through the USB DFU boot loader running on the AT32UC3B, accessible upon power up when the J12 header is closed

Attention:
Programming the AT32UC3B1256 will overwrite the default firmware. The AT32UC3B256 can be programmed and debugged through the JTAG interface J13 header.

The AT32UC3B1256 is connected to the AT32UC3L064's USART3 TX and RX pins.

Figure 2-16 AT32UC3L-EK Top View USB Interface Location

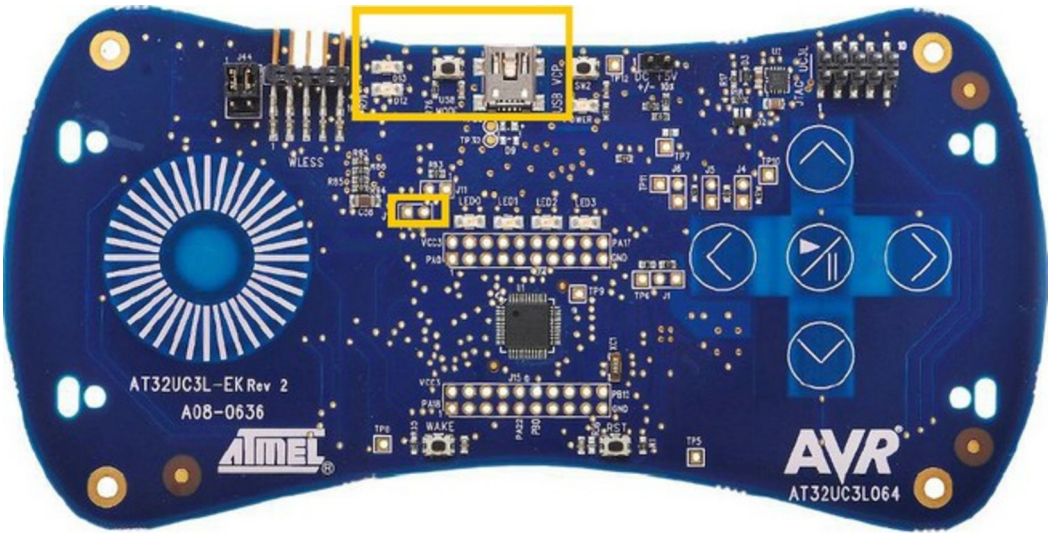
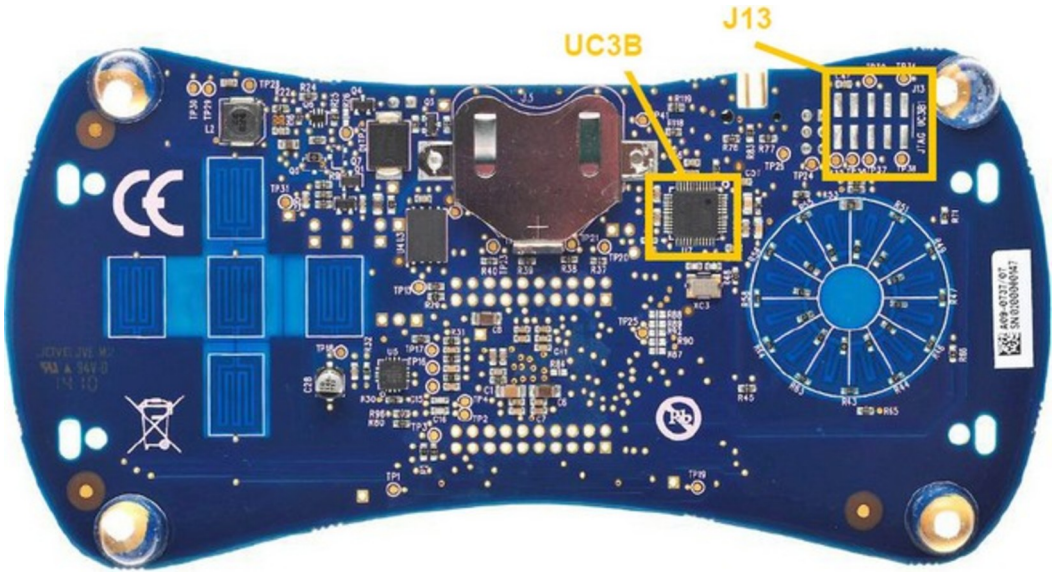


Figure 2-17 AT32UC3L-EK Bottom View USB Interface Location



2.7.2. Schematics

In the Schematics document, the USB interface block is described on page 6.

2.7.3. UC3L-specific Information

2.7.3.1. Atmel AT32UC3L064 Pinout for the USB Interface Block

Table 2-18 UC3L Pinouts for the J15 Header

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
6	PB00	USART3.TXD	USART3 TX line
16	PB01	USART3.RXD	USART3 RX line

2.7.4. Configuration and Test Points

2.7.4.1. Atmel AT32UC3LB1256 Default Firmware Configuration

The default firmware pre-loaded on the AT32UC3B1256 is dynamically configurable upon power up:

- The USB DFU boot loader can be enabled by closing the J12 jumper. Use flip/batchisp to read/write resources on the AT32UC3B1256 through the boot loader.

Attention:
Programming the AT32UC3B1256 will overwrite the default firmware.

- If the USB MODE pushbutton is pressed at power up, the USB virtual com port firmware will execute. Otherwise, the USB HID QTouch Debug firmware will execute.

2.7.4.2. Test Points

A few test points covering the USB interface block have been placed on the AT32UC3L-EK for the verification of important signals.

Table 2-19 USB Block Test Points

Designation	Feature
TP31	VBUS
TP32	D-
TP33	D+
TP34	GND
TP35	JTAG.TCK.UC3B
TP36	JTAG.TDO.UC3B
TP37	JTAG.TMS.UC3B
TP38	JTAG.TDI.UC3B
TP39	RESET_N.UC3B
TP41	USB MODE pushbutton state

To locate the test points mentioned here above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

2.8. AT32UC3L064

The AT32UC3L064 is the central point of the AT32UC3L-EK.

2.8.1. Overview

See Figure 1-1 AT32UC3L-EK Block Diagram on page 4, for a logical view of the AT32UC3L064 in the kit.

The AT32UC3L064 is powered from the power supply block. It can read the current battery voltage (through an ADCIFB channel), and may control the power supply block through the Power-Off signal. For a detailed presentation of the power supply block, see Section Power Supply on page 7.

The AT32UC3L064 is in charge of the main user interface block:

- The touch sensors
- The LEDs LED0-4
- The WAKE pushbutton
- The RST pushbutton
- The three-axis accelerometer

For a detailed presentation of the user interface block, see Section User Interface on page 11.

The AT32UC3L064 can be programmed and debugged through the programming and debugging interface block that provides JTAG or aWire access. For a detailed presentation of the programming and debugging interface block, see Section Programming and Debug Interface on page 14.

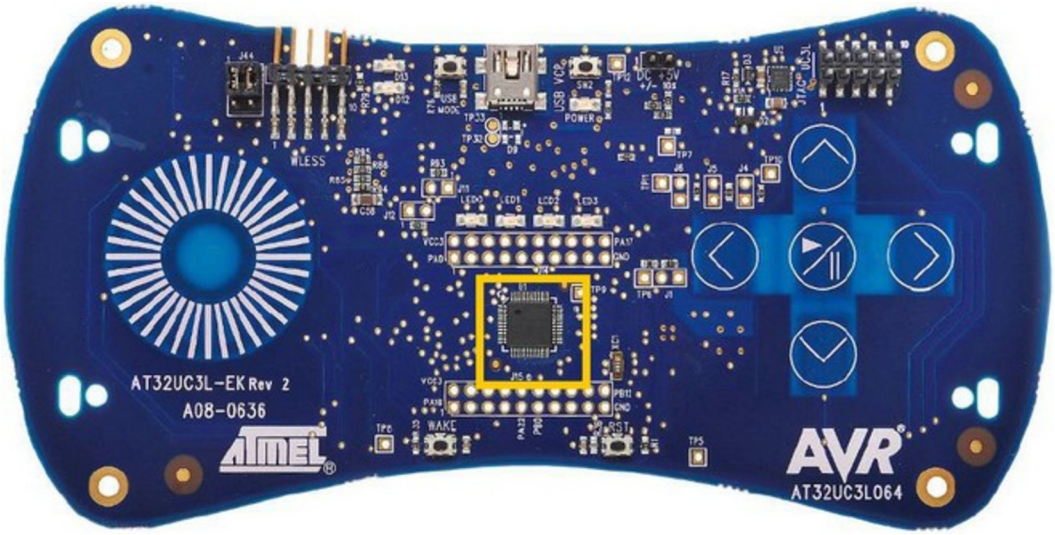
The AT32UC3L064 has access to one external on-board Atmel DataFlash 64Mb memory. For a detailed presentation of the external memory block, see Section External Memory on page 17.

A 32kHz crystal is connected to the AT32UC3L064 to support the lowest sleep modes and to provide the RTC feature. For a detailed presentation of the RTC block, see Section Real Time Clock on page 19.

The expansion interface offers the possibility to connect various external devices to the AT32UC3L064. The J8 header (labeled WLESS on the PCB) connects the RZ600 AT86RF231 radio board (provided with this board) to provide wireless capabilities to the kit. Obviously, dedicated firmware must be running on the AT32UC3L064 to support this feature. The J14 and J15 headers provide access to all of the AT32UC3L064's GPIOs. For a detailed presentation of the expansion interface block, see Section Expansion Interface on page 19.

To provide USB communication capabilities to the kit, the AT32UC3L064 accesses the USB interface block through the USART3 RX and TX signals. The USB interface block main component is the AT32UC3B1256 device, pre-loaded with several default firmware components providing added features to the kit. For a detailed presentation of the USB interface block, see Section USB Interface on page 23.

Figure 2-18 AT32UC3L-EK Top View AT32UC3L064 Location



2.8.2. Schematics

In the Schematics document, the AT32UC3L064 is described on page 1.

2.8.3. AT32UC3L064 Pinout

Table 2-20 UC3L Pinout

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
33	N.A.	N.A.	GNDANA
34	N.A.	N.A.	ADVREFP
1	N.A.	N.A.	GND
19	N.A.	N.A.	GND
43	N.A.	N.A.	GND
45	N.A.	N.A.	GND
22	N.A.	N.A.	RESET_N
35	N.A.	N.A.	VDDANA
17	N.A.	N.A.	VDDIN
18	N.A.	N.A.	VDDCORE

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
48	N.A.	N.A.	VDDIO
42	N.A.	N.A.	VDDIO
11	PA00	JTAG.TCK/USART1.RTS/GPIO[0]	JTAG_TCK/WZ_U1_RTS/ WZ_RZ600_RST
14	PA01	JTAG.TMS/USART1.CTS/GPIO[1]	JTAG_TMS/WZ_U1_CTS/ WZ_RZ600_MISC
13	PA02	JTAG.TDO	JTAG_TDO
4	PA03	JTAG.TDI/GPIO[3]/SPI.NPCS[1]	JTAG_TDI/POWER_OFF/WZ_RZ600_CS
28	PA04	SPI.MISO/TWIMS0.TWCK	DF_MISO/WZ_MISO/WZ_TW0CK
12	PA05	SPI.MOSI/TWIMS0.TWD	DF_MOSI/WZ_MOSI/WZ_TW0D
10	PA06	SPI.SCK	DF_SCK/WZ_RZ600_SCK
15	PA07	SPI.NPCS[0]	DF_CS
3	PA08	USART1.TXD/GPIO[8]	WZ_U1_TX/WZ_RZ600_SLPTR
2	PA09	USART1.RXD/GPIO[9]	WZ_U1_RX/WZ_RZ600_IRQ
46	PA10	CAT.CSA[5]	TOUCH_Y2
27	PA11	GPIO[11]	WAKEPush button
47	PA12	CAT.CSB[5]	TOUCH_YK2
26	PA13	XIN32_2	RTC
36	PA14	CAT.CSA[6]	TOUCH_X6
37	PA15	CAT.CSB[6]	TOUCH_X7
38	PA16	ACIFB.ACREFN	TOUCH_ACREFN
39	PA17	CAT.SMP	TOUCH_SMP
41	PA18	ADCIFB[4]	VBAT
40	PA19	CAT.CSA[10]	TOUCH_X10
25	PA20	XOUT32_2	RTC
24	PA21	GPIO[21]/TC0.B1/PWMA[21]/ SCIF.GCLK0	LED_0
9	PA22	CAT.CSB[10]	TOUCH_X11
6	PB00	USART3.TXD	USBGW_UC3L_TX
16	PB01	USART3.RXD	USBGW_UC3L_RX
7	PB02	GPIO[34]/TC0.A2/PWMA[25]/ SCIF.GCLK1	LED_2
8	PB03	GPIO[35]/TC0.B2/PWMA[26]/TC1.A2	LED_3
21	PB04	CAT.CSA[14]	TOUCH_X14

QFP48 pin	GPIO	GPIO Alternate Functions	Feature
20	PB05	CAT.CSB[14]	TOUCH_X15
30	PB06	ADCIFB[6]	ACC_X
31	PB07	ADCIFB[7]	ACC_Y
32	PB08	ADCIFB[8]	ACC_Z
29	PB09	CAT.CSA[15]	TOUCH_YK7
23	PB10	GPIO[42]/GLOC.OUT[1]/PWAM[33]	LED_1
44	PB11	CAT.VDIVEN	CAT-VDIVEN
5	PB12	CAT.CSA[15]	TOUCH_Y7

Note: Some pins offer multiple GPIO alternate function configuration, while others do not. For example, for LED1 (PB10), it is possible to drive the intensity of the LED through a regular GPIO function or through the PWMA function multiplexed on this pin. However, for TOUCH_Y7 (PB12), if the GPIO function configuration is different than CAT.CSA[15], the touch interface of this board won't be functional.

2.8.4. Configuration and Test Points

2.8.4.1. Configuration

A UART boot loader is pre-loaded on the AT32UC3L064. To enter this boot loader mode, the WAKE pushbutton must be pressed upon reset and then released. It is then possible to program the AT32UC3L064 through the UART boot loader. Note also that if the AT32UC3B1256 is running the pre-loaded virtual com port firmware, it is possible to program the AT32UC3L064 with the UART boot loader through the USB. For detailed information on the AVR UC3 UART boot loader, check Reference Materials on page 6.

2.8.4.2. Test Points

A few test points covering the AT32UC3L064 have been placed on the AT32UC3LEK for the verification of important signals.

Table 2-21 AT32UC3L064 Test Points

Designation	Feature
TP3	GNDANA
TP5	GND
TP6	VDDANA

To locate the test points mentioned here above, use the assembly top/bottom views provided within the AT32UC3L-EK schematics package.

3. UC3L-EK Schematics

Schematics (AT32UC3L-EK schematics package) are available on the Atmel website www.atmel.com.

4. Errata and Troubleshooting

While using the touch sensors, if the bottom side is touched, the touch events are wrong.

Workaround: when demonstrating the touch feature on the kit, the bottom side of the PCB must not be in contact with fingers or any external object.

The pin-through holes near the touch sensors may cause spurious touch events.

On some AT32UC3L-EK kits, the pin-through holes are not protected, causing spurious touch events when the fingers are not exactly on the touch sensors.

Workaround: when demonstrating the touch feature on this kit, the user must make sure to touch the sensor-delimited PCB areas only and nowhere else on the PCB.

The kit will not operate if power-hungry add-ons are connected to the expansion headers.

Workaround: the kit must not be used with external add-ons consuming more than 100mA. Note that the RZ600 radio board provided with this kit has very low power consumption and can be used with this kit safely.

5. Evaluation Board/kit Important Notice

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Mailing Address:

Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA

6. Revision History

Doc. Rev	Date	Comments
32150C	06/2015	New template and some minor corrections
32150B	03/2012	
32150A	08/2010	Initial document release

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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