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Specification

Part Number:	MC144032A6WC-SPTLY
Version:	1
Date:	01/09/2011

Revision

No.	Date	Description	Item	Page

DOC.	DATASHEET STATEMENT

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Midas 2006 version logo.Midas is an integrated manufacturer of flat panel display (FPD). Midas supplies TN, HTN, STN, FSTN monochrome LCD panel; COB, COG, TAB LCD module; and all kinds of LED backlight.

FAST RESPONSE TIME
This icon on the cover indicates the product is with high response speed; Otherwise not.

PROTECTION CIRCUIT
This icon on the cover indicates the product is with protection circuit; Otherwise not.

HIGH CONTRAST
This icon on the cover indicates the product is with high contrast; Otherwise not.

LONG LIFE VERSION
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Vlcm = 3.0V
This icon on the cover indicates the product can work at 3.0V exactly; otherwise not.

N SERIES TECHNOLOGY (2008 developed)
New structure, new craft, new technology and new materials inside both LCD module and LCD panel to improve the "RainBow"

Contents

		Page
2.	General Specification	4
3.	Module Coding System	5
4.	Interface Pin Function	6
5.	Outline dimension & Block Diagram	7
6.	Function Description	8
7.	Display Control Instruction	24
8.	Optical Characteristics	32
9.	Absolute Maximum Ratings	33
10.	Electrical Characteristics	33
11.	Backlight Information	34
12.	Reliability	35
13.	Inspection specification	36
14.	Precautions in use of LCD Modules	40
15.	Material List of Components for RoHs	41
16.	Recommendable storage	41

2. General Specification

The Features is described as follow:

- Module dimension: 85.0x36.0x13.2(MAX)mm3
- View area: 66.0 x 16.0 mm2
- Active area: 60.44x 13.4 mm2
- Number of Dots: 144x 32
- Dot size: 0.38 x 0.38 mm2
- Dot pitch: 0.42 x 0.42mm2
- LCD type: STN Positive, Yellow Green ，Transflective,
- Duty: 1/32
- View direction: 6 o'clock
- Backlight Type: LED, Yellow Green

Midas LCD Part Number System

MC	COG	132033	A	*	6	W	*	*	-	S	N	T	L	W	*	*
1	2	3	4	5	6	7	8	9	-	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **Blank:** COB (chip on board) **COG**: chip on glass

3 = **No of dots** (e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)

4 = **Series**

5 = **Series Variant:** A to Z **– see addendum**

6 = **3:** 3 o'clock **6:** 6 o'clock **9**: 9 o'clock **12**: 12 o'clock

7 = S: Normal (0 to + 50 deg C) **W:** Wide temp. (-20 to + 70 deg C) **X:** Extended temp (-30 + 80 Deg C)

8 = **Character Set**

Blank: Standard (English/Japanese)
C: Chinese Simplified (Graphic Displays only)
CB: Chinese Big 5 (Graphic Displays only)
H: Hebrew
K: European (std) (English/German/French/Greek)
L: English/Japanese (special)
M: European (English/Scandinavian)
R: Cyrillic
W: European (English/Greek)
U: European (English/Scandinavian/Icelandic)

9 = **Bezel Height** (where applicable /available)

	Top of Bezel to Top of PCB	LED Connection Common (via pins 1 and 2)	Array or Edge Lit
Blank	9.5mm / not applicable	via pins 15+ 16-	Array
2	8.9 mm	Common	Array
3	7.8 mm	Separate	Array
4	7.8 mm	Common	Array
5	9.5 mm	Separate	Array
6	7 mm	Common	Array
7	7 mm	Separate	Array
8	6.4 mm	Common	Edge
9	6.4 mm	Separate	Edge
A	5.5 mm	Common	Edge
B	5.5 mm	Separate	Edge
D	6.0mm	Separate	Edge
E	5.0mm	Separate	Edge
F	4.7mm	Common	Edge
G	3.7mm	Separate	EL
H	7 mm	Separate	Edge

10 = **T:** TN S: STN **B:** STN Blue **G:** STN Grey **F:** FSTN **F2:** FFSTN **V:** VA (Vertically Aligned)

11 = **P:** Positive **N**: Negative

12 = **R:** Reflective **M**: Transmissive **T:** Transflective

13 = **Backlight: Blank:** Reflective **L:** LED

14 = **Backlight Colour: Y:** Yellow-Green **W:** White **B:** Blue **R:** Red **A:** Amber **O:** Orange **G:** Green **RGB:** R.G.B.

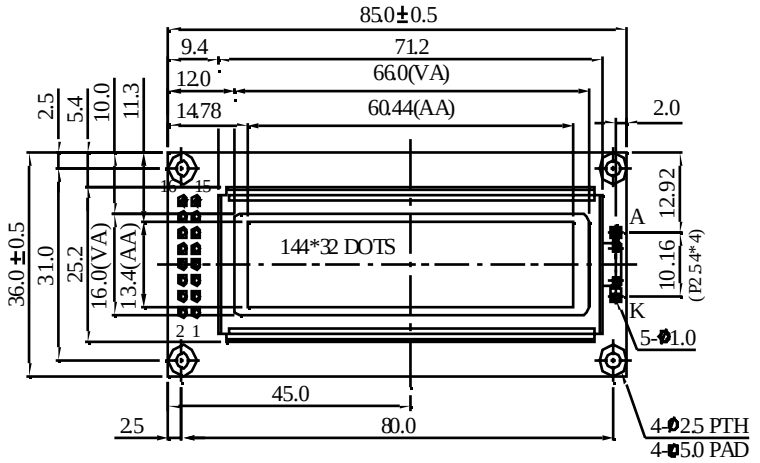
15 = **Driver Chip:** **Blank:** Standard **I:** I²C S: SPI **T:** Toshiba T6963C **A:** Avant SAP1024B **R:** Raio RA6963

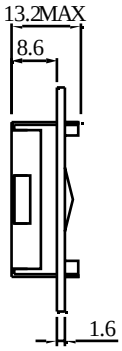
16 = **Voltage Variant**: e.g. **3** = 3v

4. Interface Pin Function

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	5.0V	Supply voltage for logic
3	Vo		Supply voltage for LCD
4	RS		H: Data , L : Instruction
5	R/W	H/L	H: Read (MPU←Module) , L: Write (MPU→Module)
6	E	H/L	ENABLE SIGNAL
7	DB0	H/L	Data bus line
8	DB1	H/L	Data bus line
9	DB2	H/L	Data bus line
10	DB3	H/L	Data bus line
11	DB4	H/L	Data bus line
12	DB5	H/L	Data bus line
13	DB6	H/L	Data bus line
14	DB7	H/L	Data bus line
15	Vout		Positive voltage output
16	NC		NC

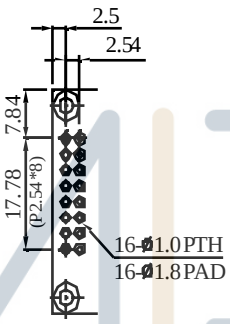
5. Outline Dimension & Block Diagram



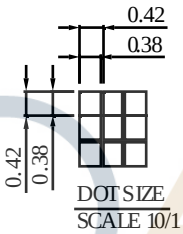


LED B/L

PIN NO.	SYMBOL
1	Vss
2	Vdd
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	Vout
16	NC

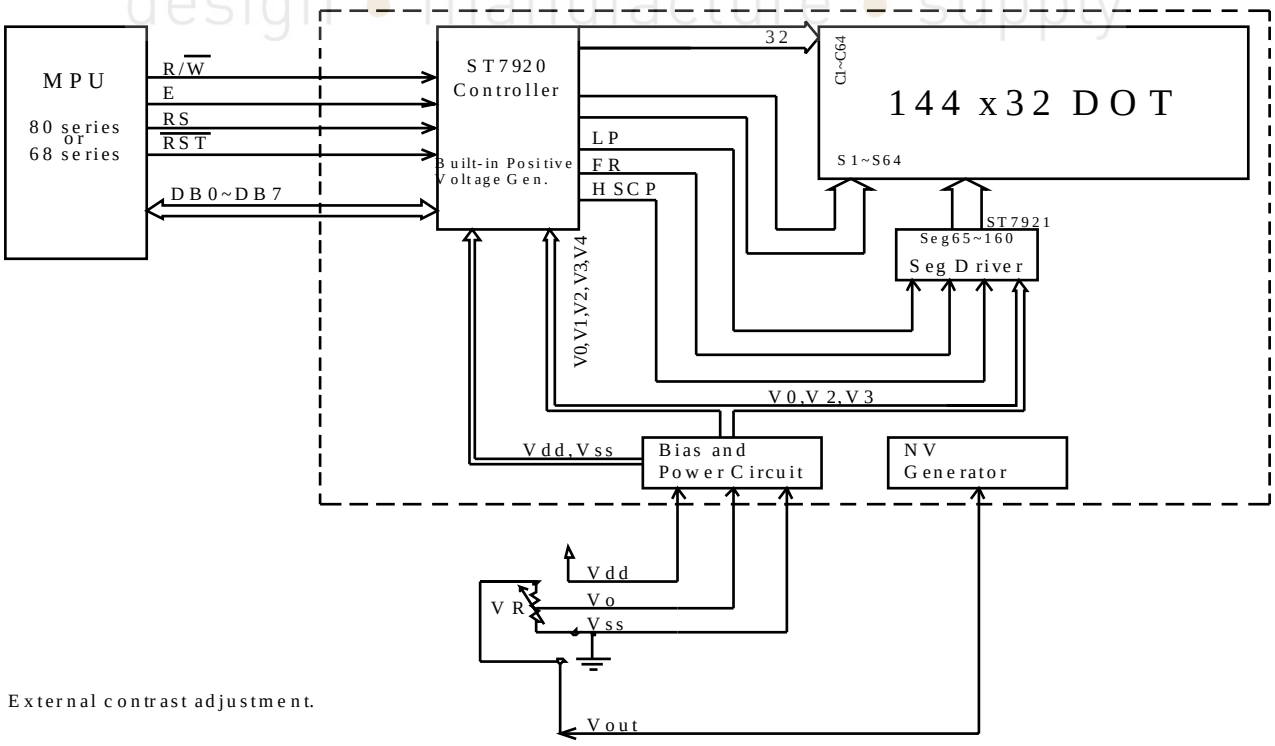


PIN DETAIL



DOT SIZE
SCALE 10/1

The non-specified tolerance of dimension is ±0.3 mm.



External contrast adjustment.

6. Function Description

Function Description：

System interface

ST7920 supports 3 kinds of bus interface to MPU. 8 bits parallel, 4 bits parallel and clock synchronized serial interface. Parallel interface is selected by PSB="I" and serial interface by PSB="0". 8 bit / 4 bit interface is selected by function set instruction DL bit.

Two 8 bit registers (data register DR, instruction register IR) are used in ST7920's write and read operation. Data Register (DR) can access DDRAM/CGRAM/GDRAM and IRAM's data through the address pointer implemented byAddress Counter (AC). Instruction Register (IR) stores the instruction by MPU to ST7920.

4 modes of read/write operation specified by RS and RW：

RS	RW	description
L	L	MPU write instruction to instruction register (IR)
L	H	MPU read busy flag (BF) and address counter (AC)
H	L	MPU write data to data register (DR)
H	H	MPU read data from data register (DR)

Busy Flag (BF)

Internal operation is in progress when BF="I", ST7920 is in busy state. No new instruction will be accepted until BF="0". MPU must check BF to determine whether the internal operation is finished and new instruction can be sent.

Address counter (AC)

Address counter(AC)is used for address pointer of DDRAM/CGRAM/IRAM/GDRAM. (AC) can be set by instruction and after data read or write to the memories (AC) will increase or decrease by 1 according to the setting in "entry mode set". When RS="0" and RW= "1" and E="1" the value of (AC) will output to DB6~DB0.

16x16 character generation ROM (CGROM) and 8x16 half height ROM (HCGROM)

ST7920 provides character generation ROM supporting 8192 16 x 16 character fonts and 126 8 x 16 alphanumeric characters. It is easy to support multi languages application such as Chinese and English. Two consecutive bytes are used to specify one 16x16 character or two 8x16 half-height characters. Character codes are written into DDRAM and the corresponding fonts are mapped from CGROM or HCGROM to the display drivers.

Character generation RAM (CGRAM)

ST7920 provides RAM to support user-defined fonts. Four sets of 16x16 bit map area are available. These user-defined fonts are displayed the same ways as CGROM fonts through writing character cod data to DDRAM

ICON RAM (IRAM)

ST7920 provides 240 ICON display. It consists of 15 sets of IRAM address. Each IRAM address has 16 bits data IRAM address should be set first before writing to the IRAM. Two bytes for each address. First higher byte (D15~D8) and then lower byte (D7~D0).

Display data RAM (DDRAM)

There are 64x2 bytes for display data RAM area. Can store display data for 16 characters(16x16) by 4 lines or 32 characters(8x16) by 4 lines. However, only 2 lines can be displayed at a time. Character codes stored in DDRAM point to the fonts specified by CGROM, HCGROM and CGRAM. ST7920 display half height HCGROM fonts, user-defined CGRAM fonts and full 16x16 CGROM fonts. Data codes 0000H~0006H are for CGRAM user-defined fonts. Data codes 02H~7FH are for half height alpha numeric fonts. Data codes (A140--~D75F) are for BIG5 code and (A1A0~F7FF) are for GB code.

1. display HCGROM fonts: Write 2 bytes data to DDRAM to display two 8x16 fonts. Each byte represents 1 character font. The data of each byte is 02H~7FH.
2. display CGRAM fonts: Write 2 bytes data to DDRAM to display one 16x16 font. Only 0000H, 0002H, 0004H, 0006H are allowed.
3. display CGROM fonts: Write 2 bytes data to DDRAM to display one 16x16 font. A140H~D75FH are for (BIG5) code, A1A0H~F7FFH are for (GB) code.

Higher byte (D15--, D8) are written first and then lower byte (D7~DO) .
Refer to Table 5 for address map

CGRAM fonts and CGROM fonts can only be displayed in the start position of each address. (Refer to Table 4)

80

	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L
S I	t r	o n	I x	S	T 7	9 2	0								
矽	創	電	子	•	中	文	編	碼	(	正	確	)			
矽	創	電	子		中	文	編	碼							

Table 4

Incorrect position

Graphic RAM (GDRAM)

Graphic display RAM supports 64x256 bits bit-mapped memory space. GDRAM address is set by writing 2 consecutive bytes for vertical address and horizontal address. Two-bytes data write to GDRAM for one address. Address counter will automatically increase by one for the next two-byte data. The procedure is as followings.

1. Set vertical address (Y) for GDRAM
2. Set horizontal address (X) for GDRAM
3. Write D 15~ D8 to GDRAM (first byte)
4. Write D7~D0 to GDRAM (second byte)

Graphic display memory map please refer to Table-8

LCD driver

LCD driver have 33 common and 64 segments to drive the LCD panel. Segment data from CGRAM /CGROM/HCGROM are shifted into the 64 bits segment latches to display. Extended segment driver ST7921 can be used to extend the segment drivers to 256.

DDRAM data (char. code)					CGRAM Addr.						CGRAM data (higher byte)								CGRAM data (lower byte)							
B15~ B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00	X	00	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
					0	0	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
					0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0
					0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0
					0	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	0	0	0	1	0	0
					0	1	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0	0
					0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	0
					0	1	1	1	1	0	1	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0
					1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
					1	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
					1	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
					1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0
					1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
					1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
					1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
					1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01	X	01	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
					0	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0
					0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0
					0	0	1	1	0	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	0
					0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0
					0	1	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0
					0	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	1	0	0
					0	1	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0
					1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	1	0	0
					1	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0
					1	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0
					1	0	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0
					1	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	0	0
					1	1	0	1	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	0	0
					1	1	1	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0
					1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5：**DDRAM data**（**character code**），**CGRAM data / address map**

Note

1. DDRAM data (character code) bit1 and bit2 are the same as CGRAM address bit4 and bit5.
2. CGRAM address bit0 to bit3 specify total 16 rows. Row16 is for cursor display. The data in row 16 will be logical OR to the cursor.
3. CGRAM data for each address is 16 bits.
4. DDRAM data to select CGRAM bit4 to bit15 must be “0”. Bit0 and bit3 value are “don’t care”.

ICON RAM address Set SR "0",and then set IRAM address AC3…AC0				ICON RAM data														
				Higher byte							Lower byte							
AC3	AC2	AC1	AC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
0	0	0	1	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31
0	0	1	0	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40	SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47
0	0	1	1	SEG48	SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63
0	1	0	0	SEG64	SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72	SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79
0	1	0	1	SEG80	SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88	SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95
0	1	1	0	SEG96	SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104	SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111
0	1	1	1	SEG112	SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
1	0	0	0	SEG128	SEG129	SEG130	SEG131	SEG132	SEG133	SEG134	SEG135	SEG136	SEG137	SEG138	SEG139	SEG140	SEG141	SEG142	SEG143
1	0	0	1	SEG144	SEG145	SEG146	SEG147	SEG148	SEG149	SEG150	SEG151	SEG152	SEG153	SEG154	SEG155	SEG156	SEG157	SEG158	SEG159
1	0	1	0	SEG160	SEG161	SEG162	SEG163	SEG164	SEG165	SEG166	SEG167	SEG168	SEG169	SEG170	SEG171	SEG172	SEG173	SEG174	SEG175
1	0	1	1	SEG176	SEG177	SEG178	SEG179	SEG180	SEG181	SEG182	SEG183	SEG184	SEG185	SEG186	SEG187	SEG188	SEG189	SEG190	SEG191
1	1	0	0	SEG192	SEG193	SEG194	SEG195	SEG196	SEG197	SEG198	SEG199	SEG200	SEG201	SEG202	SEG203	SEG204	SEG205	SEG206	SEG207
1	1	0	1	SEG208	SEG209	SEG210	SEG211	SEG212	SEG213	SEG214	SEG215	SEG216	SEG217	SEG218	SEG219	SEG220	SEG221	SEG222	SEG223
1	1	1	0	SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239
1	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 6 ICON RAM address,data and segment pins

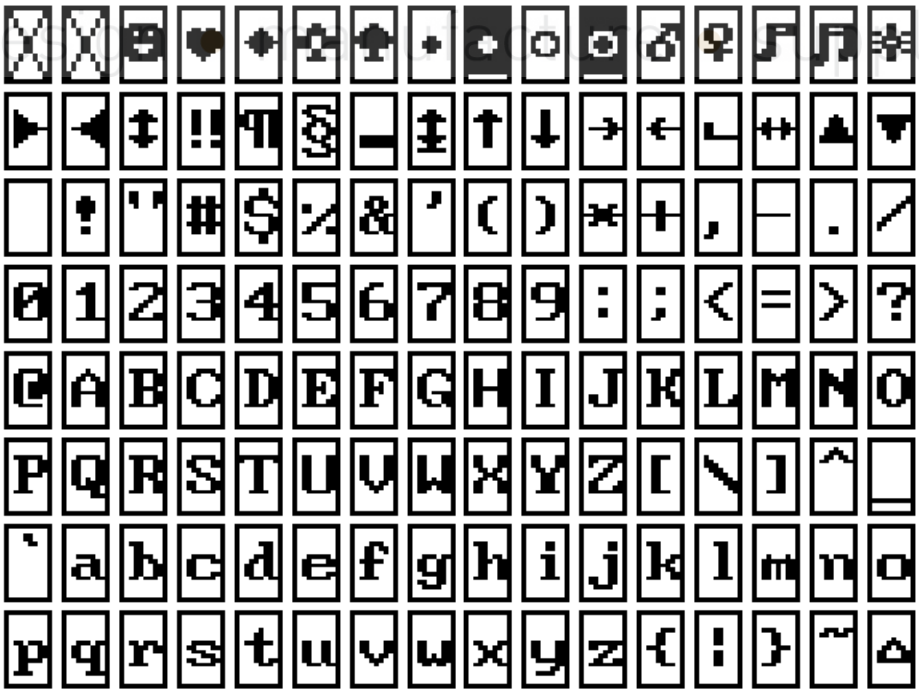


Table 6 16x8 half-height characters

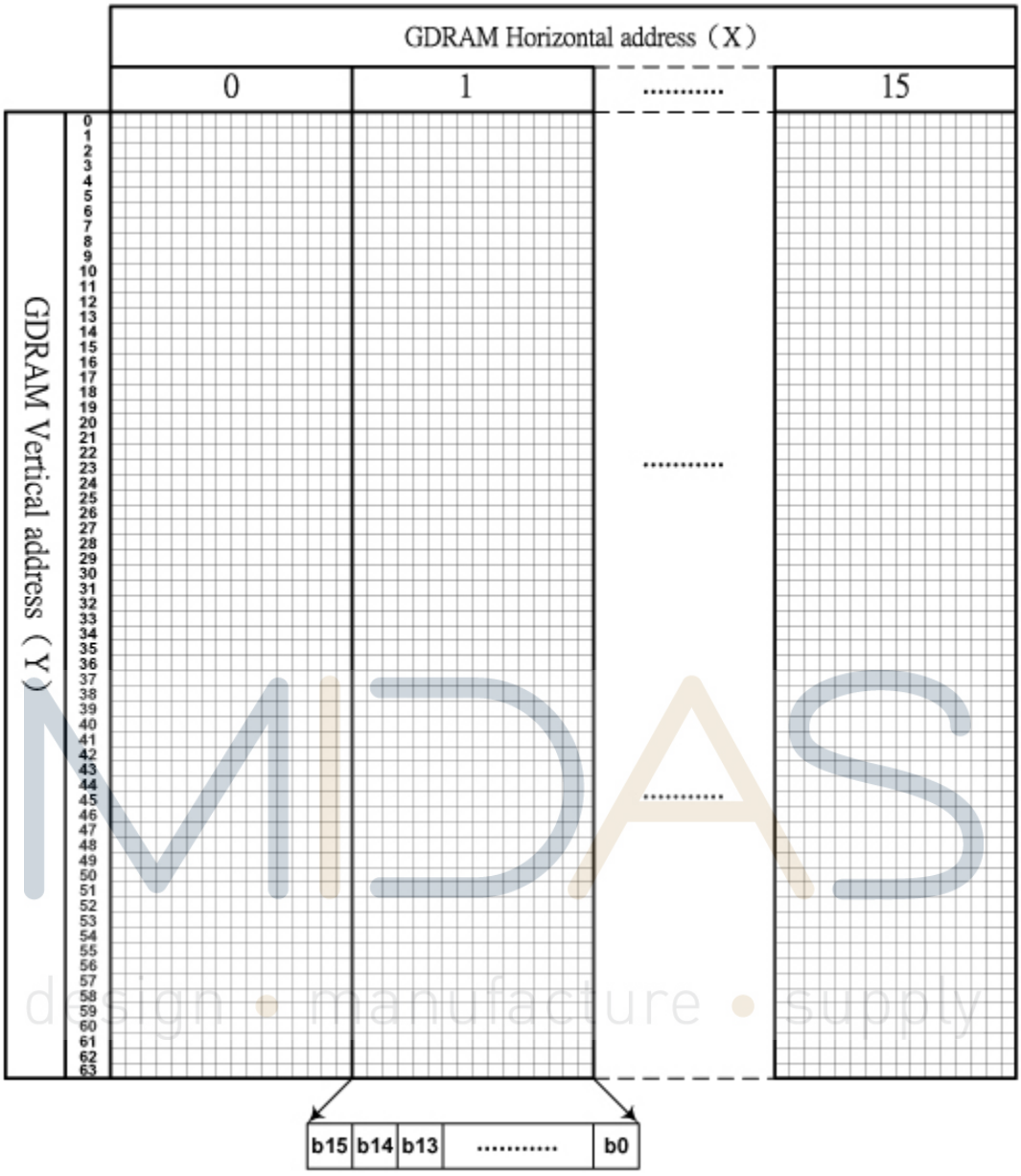
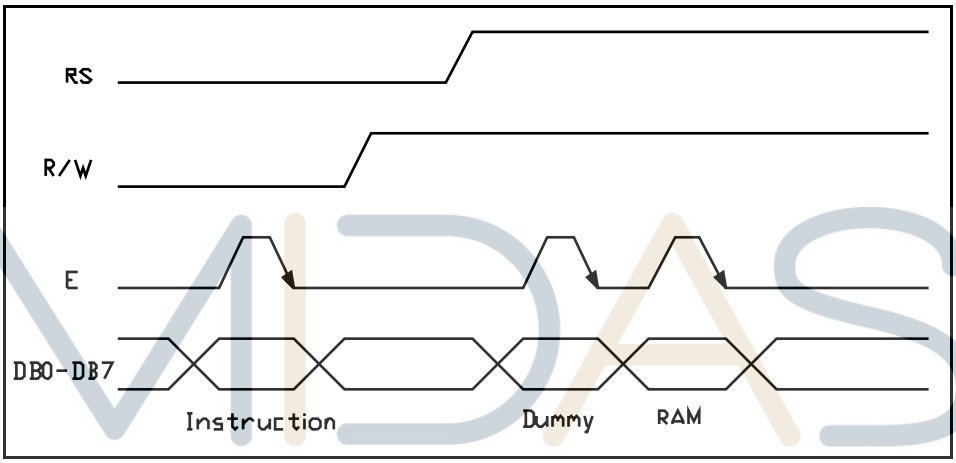


Table 8 GDRAM display coordinates and corresponding address

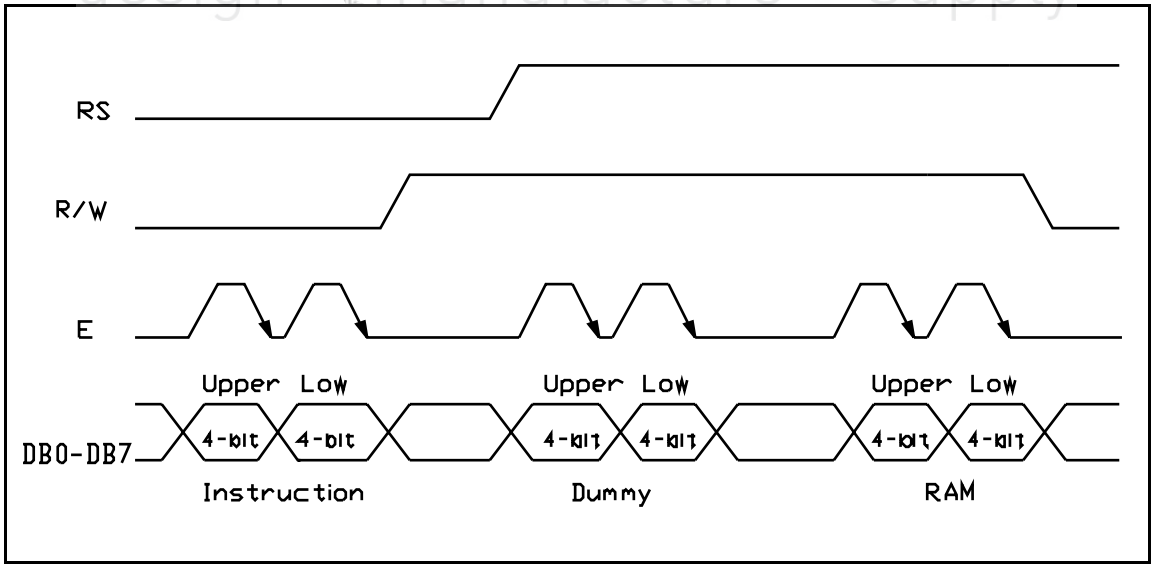
Parallel interface

ST7920 is in parallel mode by pulling up PSB pin. And can select 8 bit or 4-bit bus interface by function set instruction DL control bit. MPU can control (RS , RW , E , and DB0..DB7) pins to complete the data transmission.

In 4-bit transfer mode, every 8 bits data or instruction is separated into 2 parts. Higher 4 bits DB7~DB4 data will transfer.
First and placed into data pins (DB7~DB4). Lower 4 bits (DB3~DB0) data will transfer second and placed into data pins (DB7~DB4). (DB3~DB0) data pins are not used.



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer



Timing Diagram of 4-bit Parallel Bus Mode Data Transfer

Serial interface :

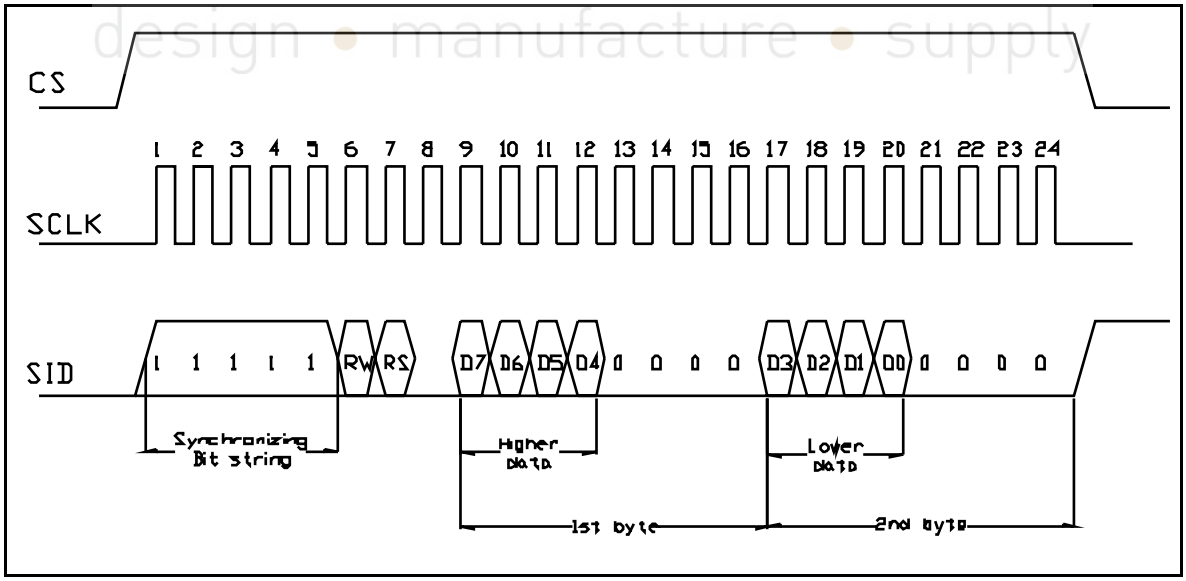
ST7920 is in serial interface mode when pull down PSB pin. Two pins (SCLK and SID) are used to complete the data transfer. Only write data is available.

When connecting several ST7920, chip select (CS) must be used. Only when (CS) is high the serial clock (SCLK) can be accepted. On the other hand, when chip select (CS) is low ST7920 serial counter and data will be reset. Transmission will be terminated and data will be cleared. Serial transfer counter is set to the first bit. For a minimal system with only one ST7920 and one MPU,
only SCLK and SID pins are necessary. CS pin should pull to high.

ST7920's serial clock SCLK is asynchronous to the internal clock and is generated by MPU. When multiple instruction/data is transferred instruction execution time must be considered. Must wait for the previous instruction to finish before sending the next. ST7920 has no internal instruction buffer area.

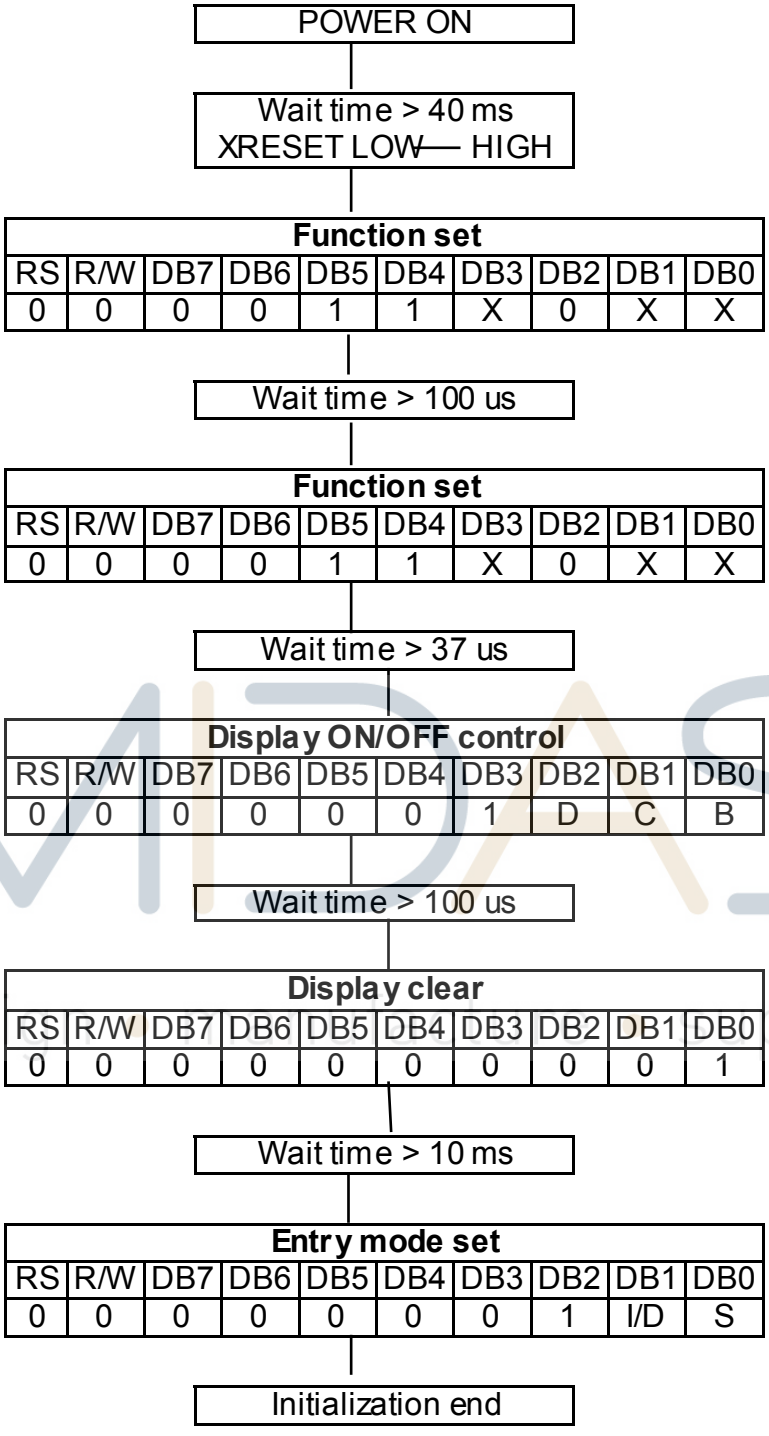
When starting a transmission a start byte is required. It consists of 5 consecutive "1"(sync character). Serial transfer counter will be reset and synchronized. Following 2 bits for read/write (RW) and register/data select (RS). Last 4 bits is filled by "0"

After receiving the sync character and RW and RS bits, every 8 bits instruction/data will be separated into 2 groups. Higher 4 bits (DB7~DB4) will be placed in first section followed by 4 "0". And lower 4 bits DB3~DB0 will be placed in second section followed by 4 "0".

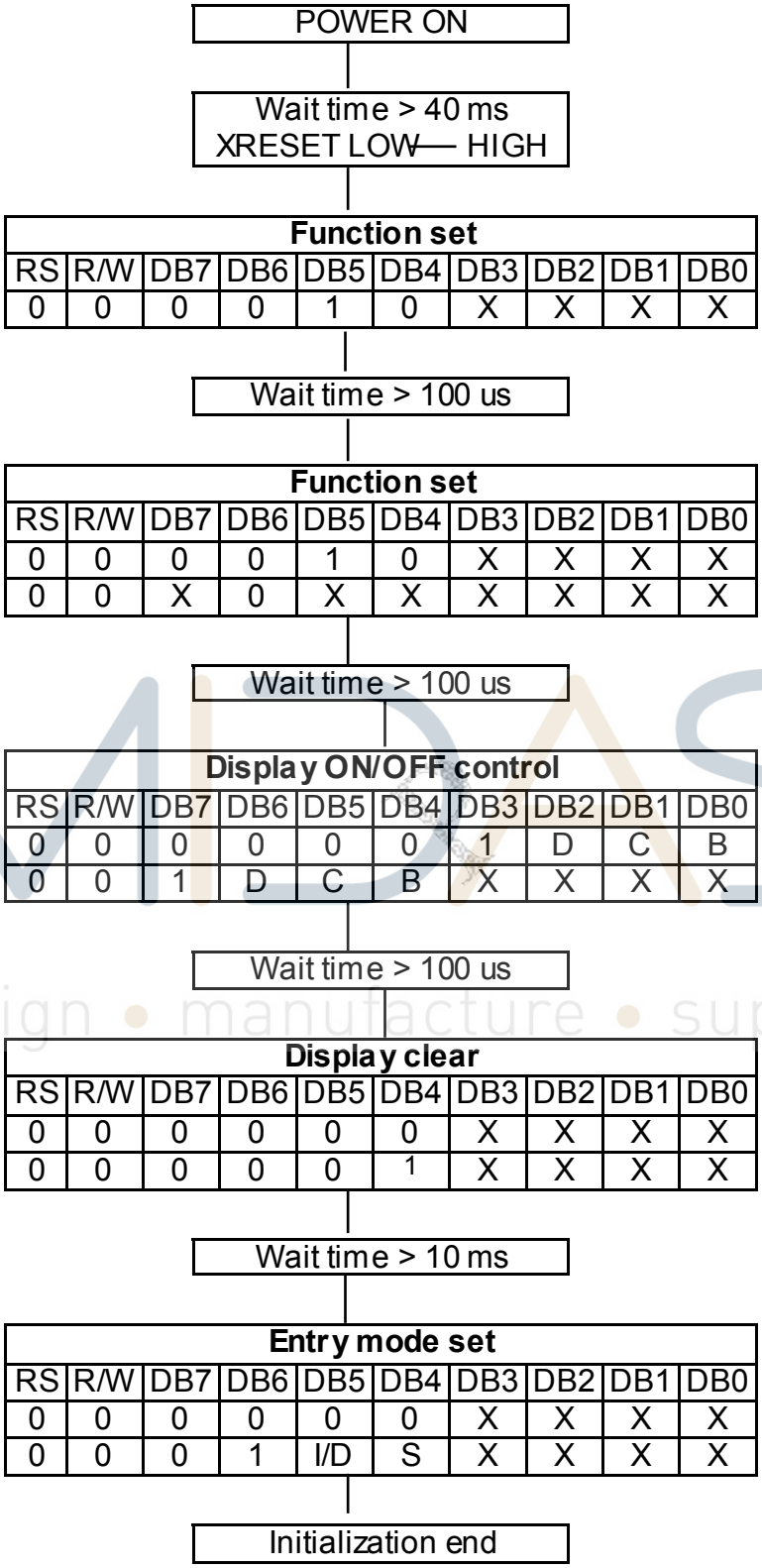


Timing Diagram of Serial Mode Data Transfer

8 bit interface :

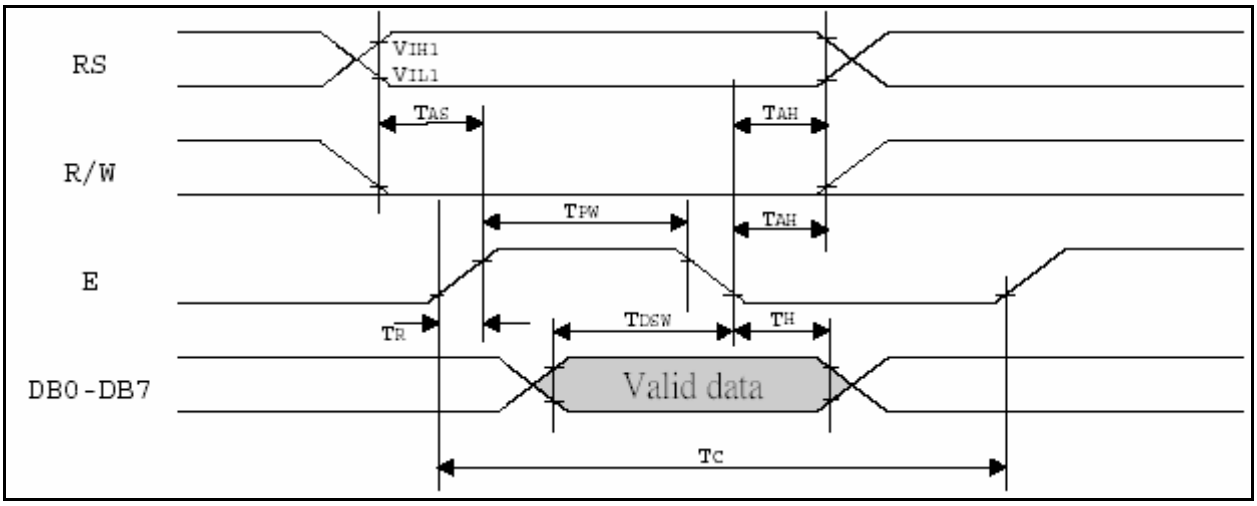


4 bit interface :

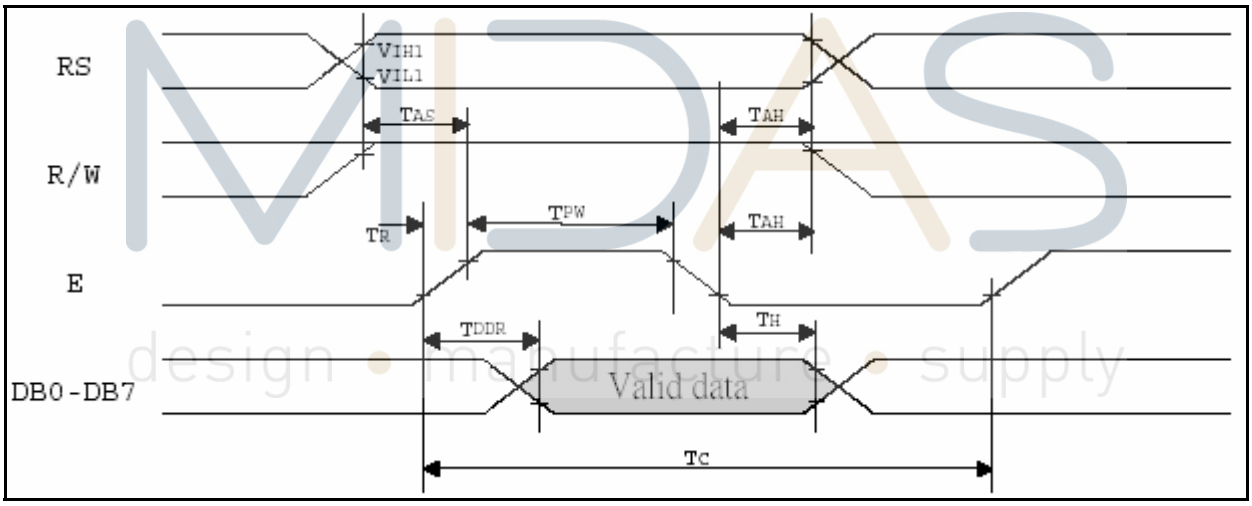


8 bit interface timing diagram

● MPU write data to ST7920

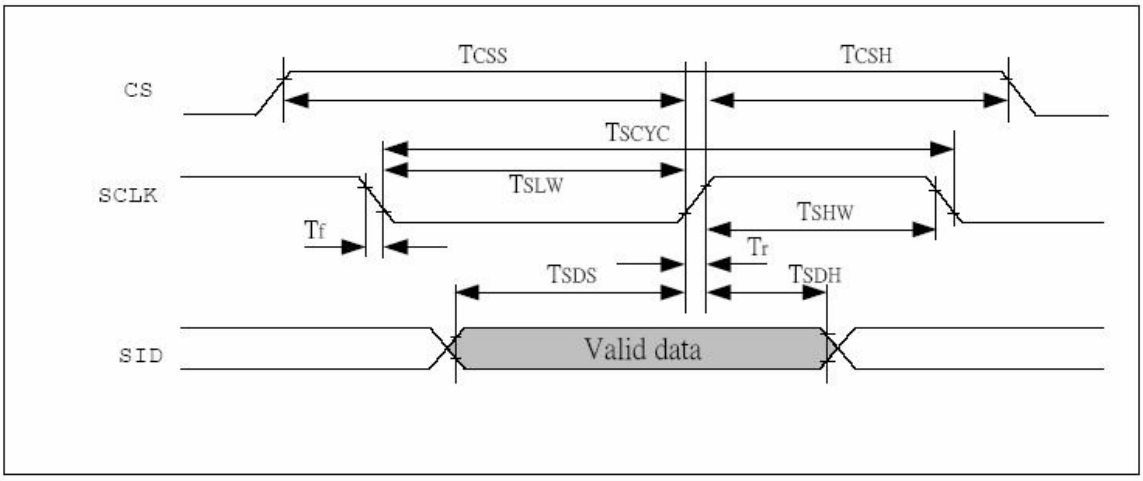


● **MPU read data from ST7920**



Serial interface timing diagram

● **MPU write data to ST7920**



Absolute Mazimum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{DD}	-0.3V to +5.5V
LCD Driver Voltage	V_{LCD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD}+0.3V
Operating Temperature	T_A	-20°C to +85°C
Storage Temperature	T_{STO}	-55°C to +125°C

DC Characteristics (T_A=25°C, V_{DD}=2.7V – 4.5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.7	—	5.5	V
V_{LCD}	LCD Voltage	V0 – Vss	3.0	—	5.5	V
Icc	Power Supply Cruuent	f_{OSC} = 530KHz, V_{DD} = 3.0V Rf = 18 kΩ	—	0.20	0.45	mA
V_{IH1}	Input High Voltage (Except OSC1)	—	0.7 V_{DD}	—	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	—	-0.3	—	0.6	V
V_{IH2}	Input High Voltage (OSC1)	—	V_{DD}-1	—	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	—	—	—	1.0	V
V_{OH1}	Output High Voltage (DB0 – DB7)	I_{OH} = -0.1 mA	0.8V_{DD}	—	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 – DB7)	I_{OL} = 0.1 mA	—	—	0.1	V
V_{OH2}	Output High Voltage (Except DB0 – DB7)	I_{OH} = -0.04 mA	0.8 V_{DD}	—	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 – DB7)	I_{OL} = 0.04 mA	—	—	0.1 V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V TO V_{DD}	-1	—	1	µa
I_{PUP}	Pull Up MOS Current	V_{DD} = 3V	22	27	32	µA

DC Characteristics (T_A = 25°C, V_{DD} = 4.5 V – 5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	4.5	—	5.5	V
V_{LCD}	LCD Voltage	V0 – Vss	3.0	—	5.5	V
Icc	Power Supply Cruuent	f_{OSC} = 540KHz, V_{DD} = 5 V Rf = 33kΩ	—	0.45	0.75	mA
V_{IH1}	Input High Voltage (Except OSC1)	—	0.7 V_{DD}	—	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	—	-0.3	—	0.6	V
V_{IH2}	Input High Voltage (OSC1)	—	V_{DD}-1	—	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	—	—	—	1.0	V
V_{OH1}	Output High Voltage (DB0 – DB7)	I_{OH} = -0.1 mA	0.8V_{DD}	—	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 – DB7)	I_{OL} = 0.1 mA	—	—	0.4	V
V_{OH2}	Output High Voltage (Except DB0 – DB7)	I_{OH} = -0.04 mA	0.8 V_{DD}	—	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 – DB7)	I_{OL} = 0.04 mA	—	—	0.1 V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V TO V_{DD}	-1	—	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 5 V	75	80	85	µA

AC Characteristics (T_A = 25°C, V_{DD} = 4.5V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	LCD Voltage	V0 – Vss	3.0	—	7	V
f_{EX}	Power Supply Cruuent	f_{OSC} = 540KHz, V_{DD} = 5 V Rf = 33kΩ	—	0.45	0.75	mA
V_{IH1}	Input High Voltage (Except OSC1)	—	0.7 V_{DD}	—	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	—	-0.3	—	0.6	V
V_{IH2}	Input High Voltage (OSC1)	—	V_{DD}-1	—	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	—	—	—	1.0	V
V_{OH1}	Output High Voltage (DB0 – DB7)	I_{OH} = -0.1 mA	0.8V_{DD}	—	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 – DB7)	I_{OL} = 0.1 mA	—	—	0.4	V
V_{OH2}	Output High Voltage (Except DB0 – DB7)	I_{OH} = -0.04 mA	0.8 V_{DD}	—	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 – DB7)	I_{OL} = 0.04 mA	—	—	0.1 V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V TO V_{DD}	-1	—	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 5 V	75	80	85	µA

AC Characteristics (T_A = 25°C, V_{DD} = 4.5V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R=33kΩ	480	540	600	KHz
External Clock Operation						
f_{EX}	External Frequency	—	480	540	600	KHz
	Duty Cycle	—	45	50	55	%
T_R,T_F	Rise/Fall Time	—	—	—	0.2	μS
Write Mode (Writing data from MPU to ST7920)						
Tc	Enable Cycle Time	Pin E	1200	—	—	nS
T_{PW}	Enable Pulse Width	Pin E	140	—	—	nS
T_R,T_F	Enable Rise/Fall Time	Pin E	—	—	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	—	—	nS`
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	—	—	nS
T_{DSW}	Data Setup Time	Pins : DB0-DB7	40	—	—	nS
T_H	Data Hold Time	Pins : DB0-DB7	20			nS
Read Mode (Reading Data from ST7920 to MPU)						
Tc	Enable Cycle Time	Pin : E	1200	—	—	nS
T_{PW}	Enable Pulse Width	Pin : E	140	—	—	nS
T_R,T_F	Enable Rise/Fall Time	Pin : E	—	—	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	—	—	nS
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	—	—	nS
T_{DDR}	Data Delay Time	Pins : DB0-DB7	—	—	100	nS
T_H	Data Hold Time	Pins : DB0-DB7	20	—	—	nS
Interface Mode with LCD Driver (ST7921)						
T_{CWH}	Clock Pulse with High	Pins : CL1, CL2	800	—	—	nS
T_{CWL}	Clock Pulse With Low	Pins : CL1, CL2	800	—	—	nS
T_{CST}	Clock Setup time	Pins : CL1, CL2	500	—	—	nS
T_{SU}	Data Setup Time	Pin : D	300	—	—	nS
T_{DM}	Data Hold Time	Pin : D	300	—	—	nS
T_{PW}	Enable Pulse Width	Pin : M	-1000	—	1000	nS

AC Characteristics (T_A = 25°C, V_{DD} = 2.7V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R=18kΩ	470	530	590	KHz
External Clock Operation						
f_{EX}	External Frequency	—	470	530	590	KHz
	Duty Cycle	—	45	50	55	%
T_R,T_F	Rise/Fall Time	—	—	—	0.2	μS
Write Mode (Writing data from MPU to ST7920)						
Tc	Enable Cycle Time	Pin E	1800	—	—	nS
T_{PW}	Enable Pulse Width	Pin E	160	—	—	nS
T_R,T_F	Enable Rise/Fall Time	Pin E	—	—	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	—	—	nS`
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	—	—	nS
T_{DSW}	Data Setup Time	Pins : DB0-DB7	40	—	—	nS
T_H	Data Hold Time	Pins : DB0-DB7	20			nS
Read Mode (Reading Data from ST7920 to MPU)						
Tc	Enable Cycle Time	Pin : E	1800	—	—	nS
T_{PW}	Enable Pulse Width	Pin : E	320	—	—	nS
T_R,T_F	Enable Rise/Fall Time	Pin : E	—	—	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	—	—	nS
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	—	—	nS
T_{DDR}	Data Delay Time	Pins : DB0-DB7	—	—	260	nS
T_H	Data Hold Time	Pins : DB0-DB7	20	—	—	nS
Interface Mode with LCD Driver (ST7921)						
T_{CWH}	Clock Pulse with High	Pins : CL1, CL2	800	—	—	nS
T_{CWL}	Clock Pulse With Low	Pins : CL1, CL2	800	—	—	nS
T_{CST}	Clock Setup time	Pins : CL1, CL2	500	—	—	nS
T_{SU}	Data Setup Time	Pin : D	300	—	—	nS
T_{DM}	Data Hold Time	Pin : D	300	—	—	nS
T_{PW}	Enable Pulse Width	Pin : M	-1000	—	1000	nS

7. Display Control Instruction

Instructions

ST7920 offers basic instruction set and extended instruction set:

Ins	code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CLEAR	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H", and set DDRAM address counter (AC) to "00H"	1.6 ms
HOME	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin; to content of DDRAM are not changed.	72 us
ENTRY MODE	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and shift when doing write or read operation.	72 us
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1：display ON C=1：cursor ON B=1：blink ON	72 us
CURSOR DISPLAY CONTROL	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control；the content of DDRAM are not changed.	72 us
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1： extended instruction** **RE=0： basic instruction**	72 us
SET CGRAM ADDR.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter (AC) **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
SET DDRAM ADDR.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter(AC) AC6 is fixed to 0	72 us
READ BUSY FLAG(BF) & ADDR.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) for completion of internal operation, also Read out the value of address counter(AC)	0 us
WRITE RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/IRAM/GDRAM)	72 us
READ RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/IRAM/GDRAM)	72 us

Instruction set 2：(RE=1： extended instruction)

Ins	code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
STAND BY	0	0	0	0	0	0	0	0	0	1	Enter stand by mode, any other instruction can terminate (Com1..32 halted, only Com33 ICON can display)	72 us
SCROLL or RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	SR=1：enable vertical scroll position SR=0：enable IRAM address **(extended instruction)** SR=0：enable CGRAM address **(basic instruction)**	72 us
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction. **R1, R0 initial value is 00**	72 us
SLEEP	0	0	0	0	0	0	1	SL	X	X	SL=1： leave sleep mode SL=0： enter sleep mode	72 us
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1：extended instruction** **RE=0：basic instruction** G=1： graphic display ON G=0： graphic display OFF	72 us
SET IRAM or SCROLL ADDR	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1： AC5~AC0 the address of vertical scroll SR=0：AC3~AC0 the address of ICON RAM	72 us
SET GRAPHIC RAM ADDR.	0	0	1	0 AC6	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set CGRAM address to address counter (AC) First set vertical address and the horizontal address by consecutive writing. Vertical address range AC6..AC0 Horizontal address range AC3..AC0	72 us

Note：

1. Make sure that ST7920 is not in busy state by reading the busy flag before sending instruction or data. If use delay loop instead please make sure the delay time is enough. Please refer to the instruction execution time.
2. “RE” is the selection bit of basic and extended instruction set. Each time when altering the value of RE it will remain. There is no need to set RE every time when using the same group of instruction set.

Initial setting(Register flag) (RE=0: basic instruction)

Ins	code										Description
	RS	RW	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	
ENTRY MODE SET	0	0	0	0	0	0	0	1	I/D	S	Cursor move to right, DDRAM address counter (AC) plus 1
									1	**0**	
DISPLAY STATUS	0	0	0	0	0	0	1	D	C	B	Display, cursor and blink ALL OFF
								0	**0**	**0**	
CURSOR DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	X	X	No cursor or display shift operation
							X	**X**			
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	**8 BIT** MPU interfce, basic instruction set
						1		**0**			

Initial setting(Register flag) (RE=1：extended instruction set)

Ins	code										Description
	RS	RW	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	
SCROLL OR RAM ADDR. SELECT	0	0	0	0	0	0	0	1	1	SR	Allow IRAM address or set CGRAM address
										0	
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Begin with normal and toggle to reverse
									0	**0**	
SLEEP	0	0	0	0	0	0	1	SL	X	X	Not in sleep mode
								1			
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	0 RE	G	X	Graphic display OFF
									0		

Description of basic instruction set

● CLEAR

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	0	1

Fill DDRAM with "20H"(space code). And set DDRAM address counter （AC to"00H". Set entry mode I/D bit to be "1".

Cursor moves right and AC adds 1 after write or read operation.

● HOME

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	X

Set DDRAM address counter AC to "00H". Cursor moves to origin. Then content of DDRAM is not changed.

● ENTRY MODE SET

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	1	I/D	S

Set the cursor movement and display shift direction when doing write or read operation.

I/D :address counter increase / decrease

When I/D = "1", cursor moves right, DRAM address counter AC add by 1.

When I/D = "0", cursor moves left, DRAM address counter AC subtract by 1.

S: Display shift

S	I/D	DESCRIPTION
H	H	Entire display shift left by 1
H	L	Entire display shift right by 1

● DISPLAY STATUS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	1	D	C	B

Controls display, cursor and blink ON/OFF.

D : Display ON/OFF control bit

When D = "1", display ON

When D = "0",display OFF，the content of DDRAM is not changed

C : Cursor ON/OFF control bit

When C = "1", cursor ON.

When C = "0", cursor OFF.

B : Blink ON/OFF control bit

When B = "1", cursor position blink ON. Then display data in cursor position will blink.

When B = "0", cursor position blink OFF

● **CURSOR AND DISPLAY SHIFT CONTROL**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	1	S/C	R/L	X	X

Instruction to move the cursor or shift the entire display. The content of DDRAM is not changed.

S/C	R/L	Description	AC Value
L	L	Cursor moves left by 1	AC=AC-1
L	H	Cursor moves right by 1	AC=AC+1
H	L	Display shift left by 1, cursor also follows to shift.	AC=AC
H	H	Display shift right by 1, cursor also follows to shift.	AC=AC

● **FUNCTION SET**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	1	DL	X	RE	X	X

DL : 4/8 BIT interface control bit

When DL = "1", **8 BIT** MPU bus interface

When DL = "0", **4 BIT** MPU bus interface

RE : extended instruction set control bit

When RE = "1", extended instruction set

When RE = "0", basic instruction set

In same instruction cannot alter DL and RE at once. Make sure that change DL first then RE.

● **SET CGRAM ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to address counter AC

AC range is 00H..3FH

Make sure that in extended instruction SR=0 (scroll address or RAM address select)

● SET DDRAM ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to address counter (AC) .
First line AC range is 80H..8FH
Second line AC range is 90H..9FH
Third line AC range is A0H..AFH
Fourth line AC range is B0H..BFH
Please note that only 2 lines can be display at a time.

● READ BUSY FLAG (BF) AND ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read busy flag BF can check whether internal operation is finished. At the same time the value of address counter (AC) is also read. When BF = “1” new instruction will not be accepted. Must wait for BF = “0” for new instruction.

● WRITE DATA TO RAM

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write data to internal RAM and alter the (AC) by 1
Each RAM address (CGRAM,DDRAM,IRAM…..) must write 2 consecutive bytes for 16 bit data. After the second byte the address counter will add or subtract by 1 according to the entry mode set control bit.

● READ RAM DATA

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read data from internal RAM and alter the (AC) by 1
After address set to read (CGRAM,DDRAM,IRAM…..)a DUMMY READ is required.
There is no need to DUMMY READ for the following bytes unless a new address set instruction is issued.

Description of extended instruction set

- **STAND BY**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	0	1

Instruction to enter stand by mode. Any other instruction follows this instruction can terminate stand by.
The content of DDRAM remain the same.

- **VERTICAL SCROLL OR RAM ADDRESS SELECT**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	SR

When SR = "1", the vertical scroll address set is enabled.
When SR = "0", the IRAM address set **(extended instruction)** and CGRAM address set**(basic instruction)** is enabled.

- **REVERSE**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	1	R1	R0

Select 1 out of 4 lines to reverse the display and to toggle the reverse condition by repeating this instruction.
R1,R0 initial vale is 00. When set the first time the display is reversed and set the second time the display become normal.

R1	R0	Description
L	L	First line normal or reverse
L	H	Second line normal or reverse
H	L	Third line normal or reverse
H	H	Fourth line normal or reverse

Please note that only 2 lines out of 4 line display data can be displayed.

- **SLEEP**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	1	SL	0	0

SL=1: leave sleep mode
SL=0: enter sleep mode

- **EXTENED FUNCTION SET**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	1	DL	X	RE	G	X

DL : 4/8 BIT interface control bit

When DL = "1", **8 BIT** MPU interface

When DL = "0", **4 BIT** MPU interface

RE : extended instruction set control bit

When RE = "1", extended instruction set

When RE = "0", basic instruction set

G : Graphic display control bit

When G = "1", graphic display ON

When G = "0", Graphic display OFF

In same instruction cannot alter DL, RE and G at once. Make sure that change DL or G first and then RE.

- **SET IRAM OR SCROLL ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

SR=1: AC5~AC0 is vertical scroll displacement address

SR=0: AC3~AC0 is ICON RAM address

- **SET GRAPHIC RAM ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set GDRAM address to address counter AC .

First set vertical address and then horizontal address(write 2 consecutive bytes to complete vertical and horizontal address set)

Vertical address range is AC6...AC0

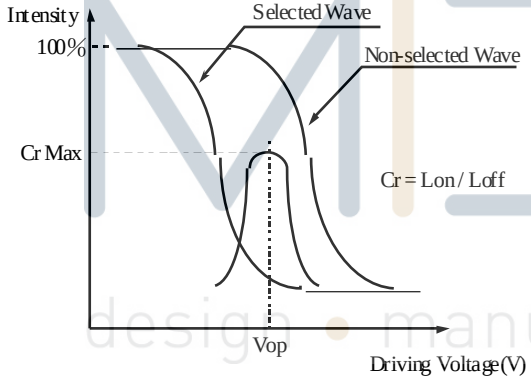
Horizontal address range is AC3…AC0

The address counter AC of graphic RAM(GRAM) only increment after write for horizontal address. After horizontal address=0FH it will automatically back to 00H. However, the vertical address will not increase as the result of the same action.

8. Optical Characteristics

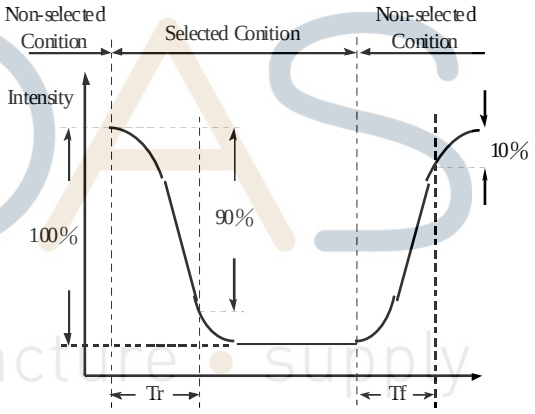
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧2	20	—	40	deg
	(H)φ	CR≧2	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	200	300	ms
	T fall	—	—	200	300	ms

Definition of Operation Voltage (Vop)



[positive type]

Definition of Response Time (Tr , Tf)



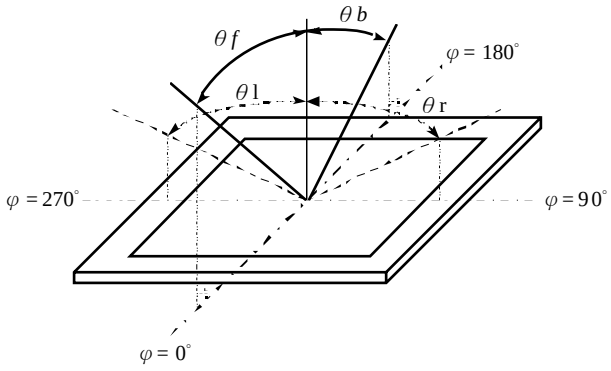
[positive type]

Conditions :

Operating Voltage : Vop　　Viewing Angle(θ ， φ) : 0°， 0°

Frame Frequency : 64 HZ　　Driving Waveform : 1/N duty , 1/a bias

Definition of viewing angle(CR≧2)



9. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Input Voltage	V_I	0	—	V_{DD}	V
Supply Voltage For Logic	V_{DD}	0	—	6.7	V
Supply Voltage For LCD	V_{DD}-V_{SS}	0	—	7.0	V

10. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	4.5	5.0	5.5	V
Supply Voltage For LCD *Note	V_O-V_{SS}	Ta=-20℃	—	—	—	V
		Ta=25℃	4.1	4.3	4.5	V
		Ta=+70℃	—	—	—	V
Input High Volt.	V_{IH}	—	0.7V_{DD}	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	-0.3	—	0.6	V
Output High Volt.	V_{OH}	—	0.8V_{DD}	—	V_{DD}	V
Output Low Volt.	V_{OL}	—	0	—	0.4	V
Supply Current	I_{DD}	—	—	1.5	3.0	mA

11. Backlight Information

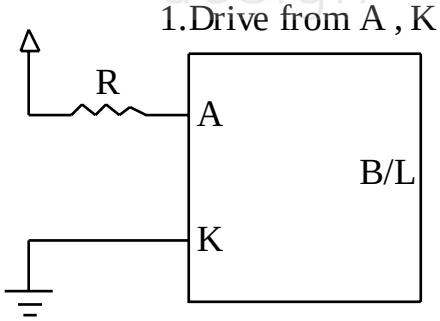
Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	80	100	150	mA	V=4.2V
Supply Voltage	V	4.0	4.2	4.4	V	—
Reverse Voltage	VR	—	—	8	V	—
Luminous Intensity	IV	80	95	—	cd/m2	ILED=100mA
Wave Length	λ p	563	568	573	nm	ILED=100mA
LED Life Time	—	—	100K	—	Hr.	ILED≦100mA
Color	Yellow Green					

Note: The LED of B/L is drive by current only, drive voltage is for reference only. drive voltage can make driving current under safety area (current between minimum and maximum).

LED B\L Drive Method

1.Drive from A , K



12. Reliability

Content of Reliability Test (wide temperature, -20℃~70℃)

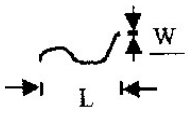
Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃ 30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 15mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

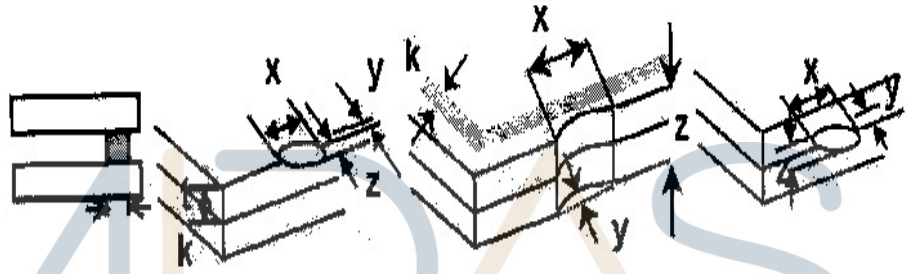
Note3: Vibration test will be conducted to the product itself without putting it in a container.

13. Inspection specification

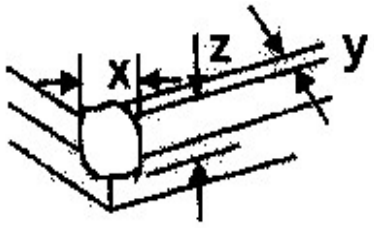
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

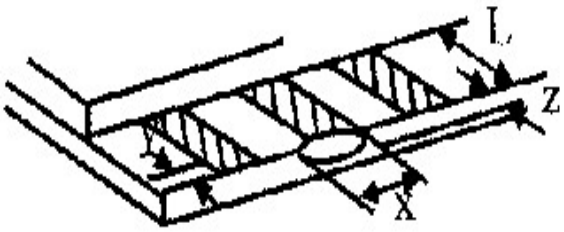
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length:

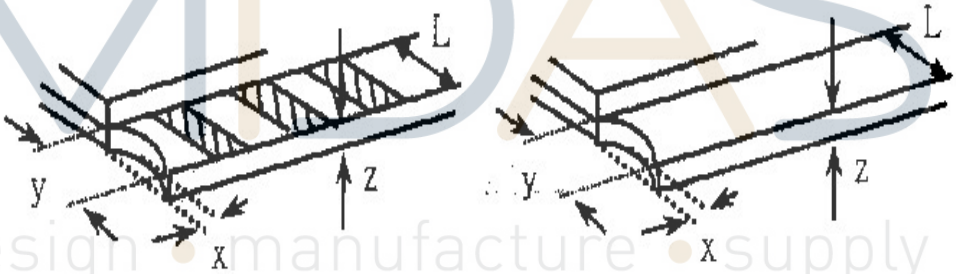
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:
 

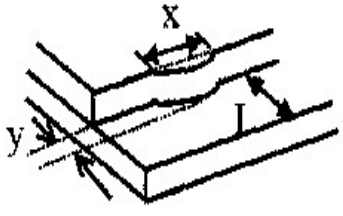
<table><tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:
 

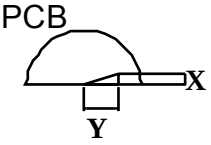
<table><tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is the total length of each chip.</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of PCB  **X * Y<=2mm^2**	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icide. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 LCD pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

14. Precautions in use of LCD Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.

(3)Don't disassemble the LCM.

(4)Don't operate it above the absolute maximum rating.

(5)Don't drop, bend or twist LCM.

(6)Soldering: only to the I/O terminals.

(7)Storage: please storage in anti-static electricity container and clean environment.

(8). Midas have the right to change the passive components
(Resistors,capacitors and other passive components will have different appearance and color caused by the different supplier.)

(9). Midas have the right to change the PCB Rev.

15. Material List of Components for RoHs

1. Midas Components Ltd. hereby declares that all of or part of products, including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

   Exhibit A：The Harmful Material List

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2. Process for RoHS requirement：
   (1) Use the Sn/Ag/Cu soldering surface; the surface of Pb-free solder is rougher than we used before.
   (2) Heat-resistance temp.：
   Reflow：250℃,30 seconds Max.；
   Connector soldering wave or hand soldering：320℃, 10 seconds max.
   (3) Temp. curve of reflow, max. Temp.：235±5℃；
   Recommended customer's soldering temp. of connector：280℃, 3 seconds.

16. Recommendable storage

1. Place the panel or module in the temperature 25°C±5°C and the humidity below 65% RH
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module