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Package Application Note for QFN and DFN Packages

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INTRODUCTION

This package application note provides the guidelines for the handling and assembly of Microchip QFN and DFN packages during the Printed Circuit Board (PCB) assembly. In addition, it provides general information for the PCB land pattern design and component rework guidelines.

SCOPE

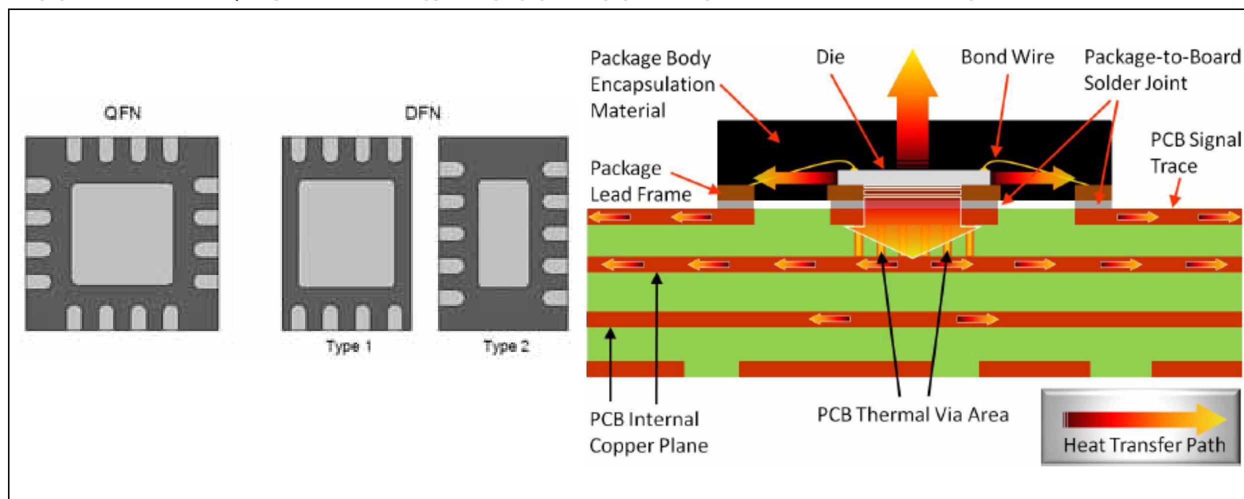
This application note contains generic information for various Microchip QFN and DFN packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.microchip.com or contact your local Microchip sales office.

PACKAGE DESCRIPTION AND CONSTRUCTION

QFN and DFN packages are plastic encapsulated lead-frame-based packages, which are near Chip Scale Package (CSP) with a low profile (≤1.0 mm). This package type uses perimeter lands/pins on the bottom of the package to provide electrical contacts to the PCB. Perimeter pins can be arranged in dual-in-line (DFN) or quad (QFN) configuration. Pins in DFN packages, when rectangular, can be arranged on the short side (Type 1), or on the long side (Type 2), see Figure 1. The package also has an exposed center pad (ePAD) as a thermal enhancement at the bottom of the package. The ePAD needs to be soldered directly to the PCB for an efficient thermal path from the die to the board (see Figure 1). The center pad also enables stable ground through use of down-bonds and electrical connections through conductive die attach material. The QFN and DFN packages are offered in various pincounts and body sizes, and have the following features:

- Small overall dimensions, compared to leaded packages, which helps maximize board space
- Thermally enhanced plastic package
- Very high design flexibility due to the etching process of the leadframe
- Easy accommodation of multi die assemblies, where separated pads are required
- Standard SMT performance characteristics

FIGURE 1: QFN/DFN LEADS/PINS CONFIGURATION AND HEAT TRANSFER



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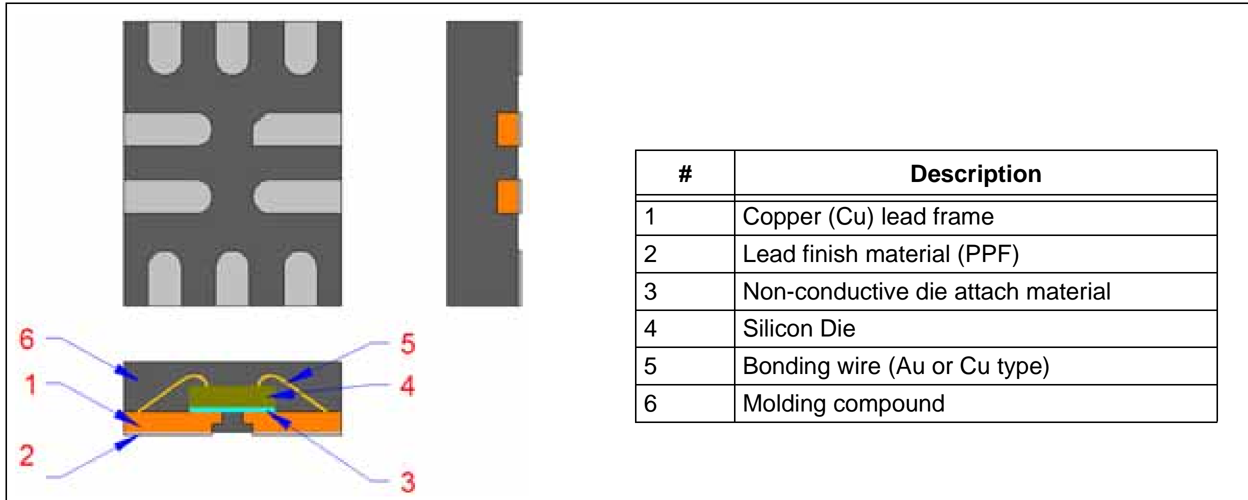
In some cases of very small QFN or DFN packages, the center exposed pad is not present and the die is mounted directly on the leads, which is called a Chip-on-Lead (COL) design. See Figure 2 for a typical leads/pins configuration and a cross section view of a QFN-COL design.

FIGURE 2: QFN-COL PACKAGE CONSTRUCTION

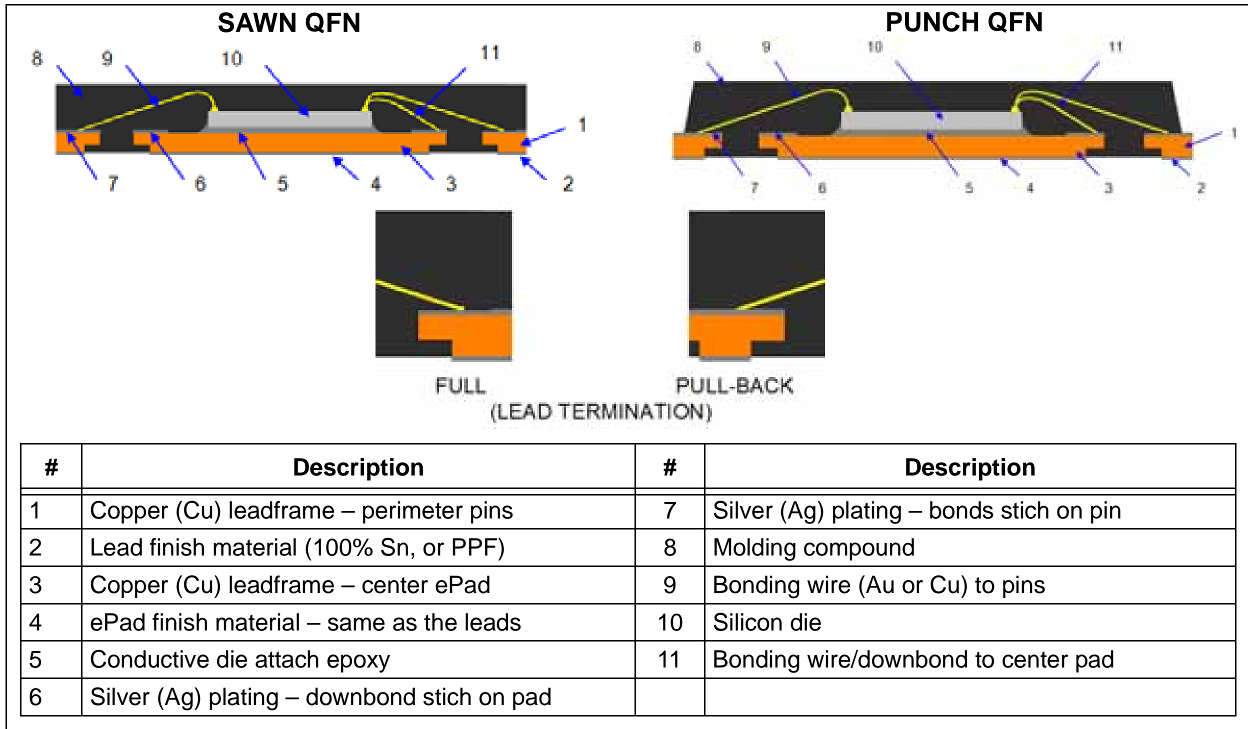


#	Description
1	Copper (Cu) lead frame
2	Lead finish material (PPF)
3	Non-conductive die attach material
4	Silicon Die
5	Bonding wire (Au or Cu type)
6	Molding compound

A typical QFN package with exposed pad construction (cross-section) is shown in Figure 3. These packages are punch or saw singulated high density, leadframe strip-assembled with “die up” configuration. A standard wirebond technology with Cu or Au type wire is used for the electrical connection between the die and package.

The QFN packages are processed in integrated assembly and test lines from die attach through tape and reel. Each perimeter lead/pin, either in punch or sawn QFN, is a full or pull-back lead termination design, and they are arranged in dual-in-line or quad configuration.

FIGURE 3: QFN PACKAGE CONSTRUCTION



#	Description	#	Description
1	Copper (Cu) leadframe – perimeter pins	7	Silver (Ag) plating – bonds stich on pin
2	Lead finish material (100% Sn, or PPF)	8	Molding compound
3	Copper (Cu) leadframe – center ePad	9	Bonding wire (Au or Cu) to pins
4	ePad finish material – same as the leads	10	Silicon die
5	Conductive die attach epoxy	11	Bonding wire/downbond to center pad
6	Silver (Ag) plating – downbond stich on pad		

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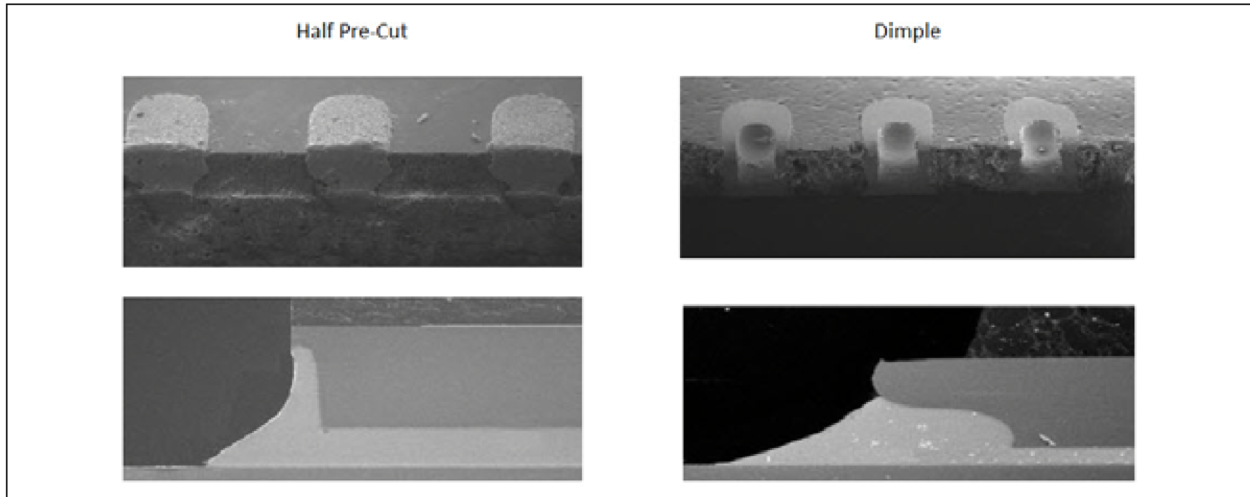
Special perimeter pin designs are available to further enhance the solderability of the pin edge. The dimple design is mostly used for pitches down to 0.5 mm. The half pre-cut design can also be used for smaller pitches and for sawn singulated QFNs, refer to Figure 4.

FIGURE 4: PIN DESIGNS WITH ENHANCED SOLDERABILITY



TYPICAL QFN/DFN CONFIGURATIONS AND DIMENSIONS

Microchip offers wide range of QFN/DFN packages ranging from 1.5x1.5 to 12x12 mm in size with standard pitches of 0.4, 0.5, 0.65 and 0.8 mm. The actual package outlines are provided on the Microchip website as a separate document. To obtain the complete set of QFN package dimensions and tolerances, refer to the "*Packaging Specification*" (DS00000049).

PCB LAND PATTERN GUIDELINES

The QFN/DFN is a surface mountable package with bottom termination of its external connections (pins). The land pattern design for all QFN type packages is based on the IPC-7093 and IPC-7351 standards. A Non-Solder-Mask Defined (NSMD) pad design is suggested for all perimeter pins, as shown in Figure 5. The solderable area of the center pad, as defined by the solder mask (SMD) or NSMD, should match the size of the ePAD of the component. An array of solid vias should be incorporated in the PCB center pad design in order to achieve maximum thermal and electrical performance of the device. Examples of typical QFN PCB land pattern guidelines and dimensions are provided in Figure 6.

FIGURE 5: NSMD AND SMD BOARD PAD DEFINITION

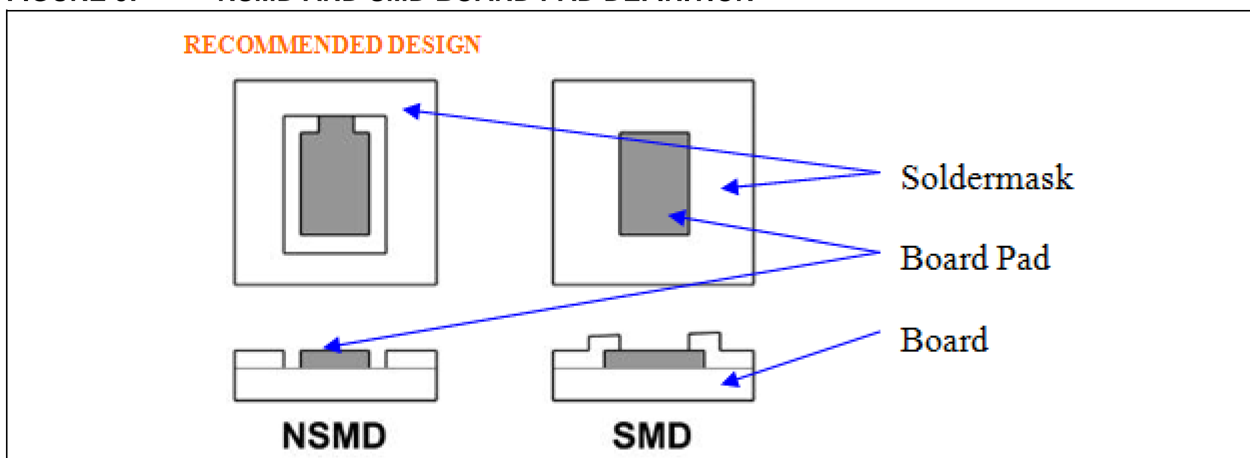
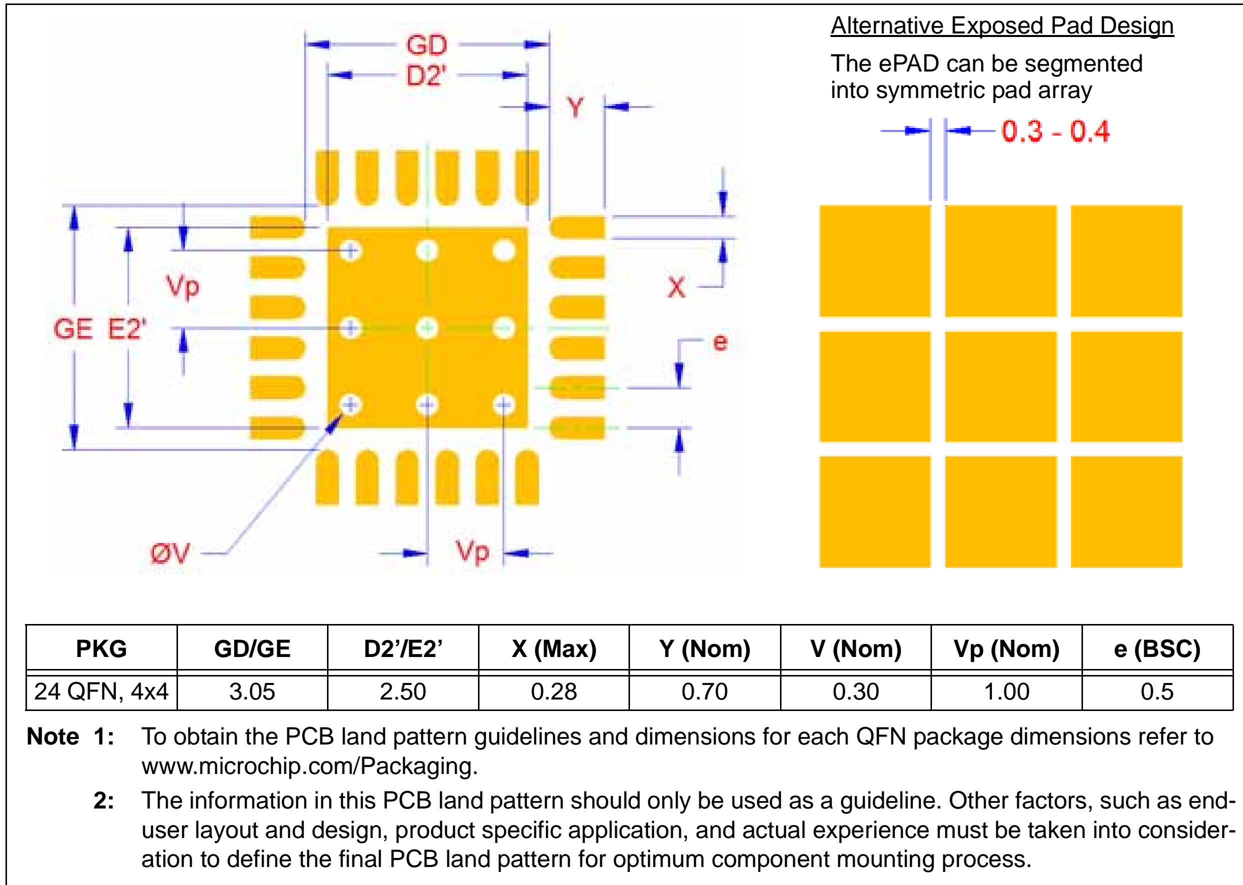


FIGURE 6: TYPICAL QFN PCB LAND PATTERN



PKG	GD/GE	D2'/E2'	X (Max)	Y (Nom)	V (Nom)	Vp (Nom)	e (BSC)
24 QFN, 4x4	3.05	2.50	0.28	0.70	0.30	1.00	0.5

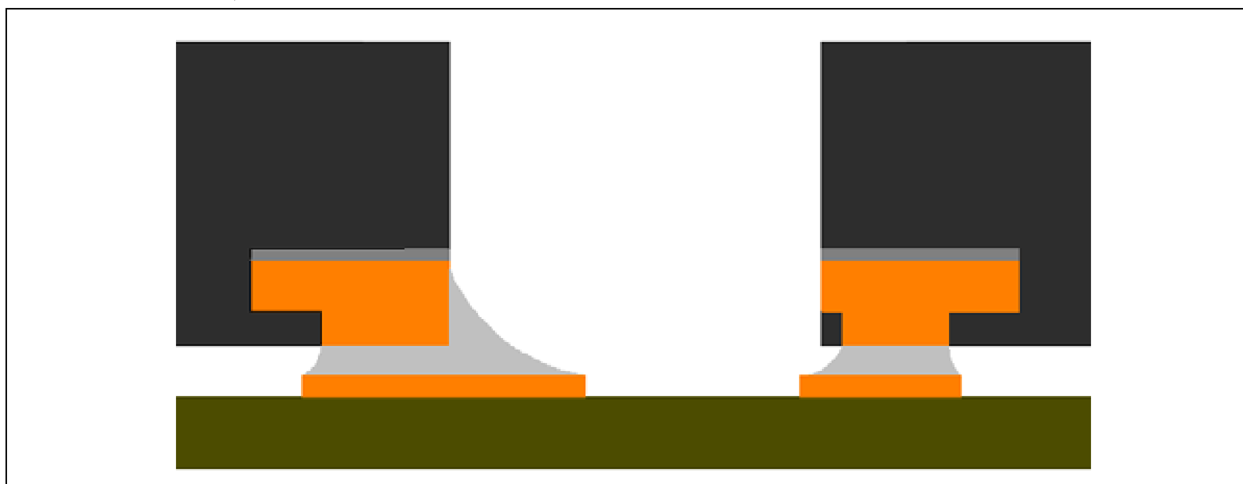
Note 1: To obtain the PCB land pattern guidelines and dimensions for each QFN package dimensions refer to www.microchip.com/Packaging.

2: The information in this PCB land pattern should only be used as a guideline. Other factors, such as end-user layout and design, product specific application, and actual experience must be taken into consideration to define the final PCB land pattern for optimum component mounting process.

STENCIL DESIGN GUIDELINES

The optimum and reliable solder joints on the perimeter pins should have 50-75 um standoff height and good side fillet at the pins edges, in the case of full terminated pin design. The pull-back pin design will not have side fillet, refer to Figure 7.

FIGURE 7: QFN/DFN STENCIL DESIGN



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Microchip recommends that the user follows the guidelines of industry specification IPC-7525 in designing the optimum stencil for the given board.

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern. A 0.101 (4.0 mils) and 0.127 mm (5.0 mil) thick stainless steel stencil is recommended for 0.40 and 0.50 mm pitch packages respectively. Package pitches ≥ 0.65 mm can accommodate a 0.150 mm (6 mil) thick stencil. Since QFN/DFN are (most likely) not the only package on the actual production PCB, the recommended stencil thickness for this package may be thinner than desired. For such a case, a step-down stencil is recommended, where most of the stencil for the PCB has a typical thickness, but the area for the DFN/QFN would be reduced to 0.127 to 0.150 mm (5 to 6 mils), depending on the package pitch.

REFLOW SOLDERING AND PROFILING

As with all SMT components, it is important that furnace profiles be monitored on all new board designs. Additionally, if there are multiple package types on the board, the thermal profile should be measured at multiple locations. Component temperature may vary because of surrounding components, location of the device on the board, and package densities. To maximize the self-alignment effect of the QFN component, it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded.

Microchip recommends that the user follows the guidelines of industry specifications IPC-7093 and J-STD-020 in developing the optimum reflow profile for the Pb-free QFN components with a given board.

HANDLING

The following information details handling procedures that should be used with product packed in desiccant bags and intended for surface mount applications. Following these handling guidelines will ensure that components maintain their as-shipped, dry state, alleviating package cracking and other moisture-related, stress-induced concerns that may be associated with the surface mount process.

1. Incoming Inspection

   Upon receipt, shipments should be inspected for bag integrity. There should not be holes, gouges, tears or punctures of any kind that expose either the contents or the inner layer of the bag.

2. Storage Conditions/Shelf Life

   The sealed Moisture Barrier Bag (MBB) and enclosed desiccant have been designed to provide a minimum of 12 months of storage from the seal date in an environment as specified in JEDEC specification J-STD-033.

   If the worst-case storage conditions (time, temperature, or relative humidity) are exceeded and there is a need to verify whether inventory has been affected, a bag can be opened and the Humidity Indicator Card (HIC) can be checked for expiration. If the HIC has not expired (there is no failed dot discoloration), then new desiccant can be added and the bag resealed. If the HIC has expired, then the devices should either be rebaked and used in the SMT, or rebaked and resealed in an new MBB with fresh desiccant, or rebaked and stored in an environment of ≤20% RH before they are used in an SMT.

3. Opening an MBB

   To open an MBB when the containers are ready to be used or inspected, simply cut across the top of the bag, being careful not to damage the enclosed materials. Once the bag has been opened, please follow the guidelines for ambient exposure time in the following section to ensure that devices are maintained below the critical moisture level.

4. Manufacturing Conditions/Floor Life

   Microchip classifies surface mount components into levels of moisture sensitivity. The labels on the MBB list the moisture sensitivity level and the allowable floor life. Once the MBB has been opened, Microchip recommends that components from the bag be surface mounted and reflowed within the time indicated on the MBB label. This time is based on a manufacturing environment not more extreme than 30ºC/60% RH, and a maximum component body temperature during solder reflow of 260 ºC. If the component cannot be mounted within this timeframe, then they should be put into a dry storage environment immediately, or sealed into an MBB with fresh desiccant as soon as possible. In either case, the remaining allowable ambient exposure time must be reduced by the time the units are out of the MBB or dry storage environment.

5. In-Process Storage

   Microchip highly recommends having dry storage capability available for units that will not be used within the allowable exposure time. A desiccator with dry nitrogen or air (≤5% RH source) is suggested for such storage.

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6. Rebaking

   QFN/DFN components should be rebaked if they have been exposed to excessive moisture by exceeding the recommended ambient exposure time or by expiration of the HIC. Rebaking should be performed prior the use of the parts in the SMT line at 125ºC for at least 8 hours. Each part should not be rebaked more than twice.

7. Resealing an MBB

   If there is a need to reseal an MBB for any reason, Microchip recommends the following guidelines to ensure that the seal does not allow moisture into the bag. The seal area must not exhibit any separation when subjected to the load and temperature conditions detailed in the JEDEC J-STD-033 specification. The integrity of the seal is vital to the storage life of the devices.

REWORK

Guidelines for Hot Gas Convention and Manual Rework

Since solder joints are not fully exposed in the case of QFN/DFN packages, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Since QFN/DFN packages are smaller and are mounted on thinner and denser boards, one of the areas of concern is thermal separation of adjoining components during the rework process. To address this concern, the following should be considered in the QFN/DFN rework process:

- A special design hot gas nozzle to maintain the keep-out zone around the reworked component
- Using a micro stencil and squeegee, specially designed for small component rework
- Using a beam-splitting imaging system for component placement

Component Removal

It is highly recommended to bake (125ºC for 4 hours) the board prior to the rework to reduce the risk of delaminating either the board or the component/part. In general, the reflow profile for part removal should be the same as the one used for part attachment. Once the thermal profile is optimized, the process parameters are used to remove the part.

The application of flux is recommended for QFN/DFN removal. The gas nozzle surrounds the part and seals against the board. The QFN/DFN is heated from the top side with hot gas. Excessive gas flow should be avoided since this may cause the QFN/DFN to skew. Gas velocity of 15-20 liters/minute is a good starting point. The board (entire assembly) is also heated from the bottom side with an under-board convective heater to help prevent warpage. Preheating the board to a fixed temperature before the component is heated also helps to ensure process repeatability. Once the joints have reflowed, the vacuum lift-off (nozzle cup) is automatically activated during the transition from reflow to cool-down, and the component is slowly lifted off the pads. The vacuum cup should be designed (vacuum pressure less than 15 inch of Hg) to disengage if the part has not fully reflowed for any reason. Generic guidelines to remove QFN packages mounted on a 1.42 mm FR4 board are shown in Table 1.

TABLE 1: PB-FREE SOLDER COMPONENT REMOVAL

Step #	Process Step Description	Parameters	Remark
1	Apply flux to component	—	No-clean flux used by manufacturer
2	Align nozzle over part to be removed	—	
3	Lower gas nozzle over the part	—	Maintain nozzle 1.27 mm over part
4	Preheat board	90-100°C	
5	Nozzle warm-up (20% air flow)	125°C	Perform during step 4
6	Soak stage (20% air flow)	225°C, 90 sec	
7	Ramp stage (20% air flow)	335°C, 30 sec	
8	Reflow stage (25% air flow)	370°C, 65 sec	
9	Vacuum activation	<15 inch Hg	At the end of step 8
10	Lower vacuum nozzle & part removal	—	
11	Cool-down stage (40% air flow)	25°C, 50 sec	
12	Turn off vacuum and part removal from nozzle	—	Do not use metal tweezers
13	Do not re-use the removed part/s (unless needed for failure analysis)		

Note 1: It is recommended to modify the heating profile for different board thickness and equipment use. Part must not exceed the peak temperature as listed on the MSL label.

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Site Redress

Once the QFN/DFN has been removed, the residual solder that remains on the board pads must be removed. Perform the site redress process carefully because the QFN/DFN pads are small and fragile. Perform the site redress in the following order:

1. Apply no-clean flux to the site after part removal.
2. Use a low-temperature-controlled soldering iron.
3. Choose a blade-style conductive tool/tip and desoldering braid, where the width matches the maximum width of the footprint area of the QFN/DFN.
4. Presoak the braid in no-clean flux and gently apply it to the site until the solder is removed.
5. If any residual flux is still present on the site, remove it with solvent/alcohol and a lint-free swab.
6. Inspect the cleaned site to make sure it is ready for the component replacement process. The clean site should not have any foreign material and area with excessive solder.

Solder Paste Deposition

Since the QFN/DFN is a land area type package, application of solder paste/material is required to ensure proper solder joint formation after rework. Use the same type of solder paste as in the initial component reflow process. Depending on the application (board density and surrounding components), one of the following two methods can be used to apply the solder paste/material:

1. Applying the solder material on the PCB.
2. Applying the solder material on the component.

Both methods require the use of a mini stencil specific to the component. Mini stencil apertures and thickness should be identical to the stencil apertures and thickness of this component during the initial part placement on the board.

Component Placement and Reflow

QFN/DFN packages are expected to have superior self-centering ability due to their small mass and, therefore, the placement of this package should be similar to that of a BGA. The QFN/DFN rework station should have a pick and place feature for accurate placement and alignment, with the capability for fine adjustment in X, Y and rotation axes. Also, the rework station should have a beam-splitting imaging system for accurate component placement. Manual pick and place, with only eye-ball alignment, is not recommended. The alignment should be done on the rework station, and at 50-100X magnification to guarantee placement within 0.1mm. When the QFN/DFN part is correctly aligned, the X-Y table is locked to prevent further movement. The gas nozzle is lowered until it lightly contacts the board. The nozzle vacuum is automatically deactivated and the thermal/reflow cycle begins. Once the cool-down cycle is complete, the nozzle is raised and the assembly is removed for inspection. Inspect the reworked component at the appropriate magnification and/or through x-ray to ensure an acceptable mounting. Generic guidelines to reflow QFN packages mounted on a 1.42 mm FR4 board are shown in Table 2.

TABLE 2: QFN REFLOW GUIDELINES

Step #	Process Step Description	Parameters	Remark
1	Align part over pads	—	
2	Place part on board	—	Do not over-travel the part
3	Raise nozzle	1.27 mm	Over the part
4	Preheat board	110-140°C	
5	Nozzle warm-up (20% air flow)	125°C	Perform during step 5
6	Soak stage (20% air flow)	225°C, 90 sec	
7	Ramp stage (20% air flow)	335°C, 30 sec	
8	Reflow stage (25% air flow)	370°C, 65 sec	
9	Cool-down stage (40% air flow)	25°C, 50 sec	
10	Remove the nozzle	—	
11	Reworked assembly inspection	—	10-30X magnification

Note 1: It is recommended to modify the heating profile for different board thickness and equipment use. Part must not exceed the peak temperature as listed on the MSL label.

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