

# NCP81151

## VR12.5 Compatible Synchronous Buck MOSFET Driver

The NCP81151 is a high performance dual MOSFET gate driver optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. It can drive up to 3 nF load with a 25 ns propagation delay and 20 ns transition time.

Adaptive anti-cross-conduction and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook systems.

The UVLO function guarantees the outputs are low when the supply voltage is low.

### Features

- Faster Rise and Fall Times
- Adaptive Anti-Cross-Conduction Circuit
- Zero Cross Detection function
- Output Disable Control Turns Off Both MOSFETs
- Undervoltage Lockout
- Power Saving Operation Under Light Load Conditions
- Direct Interface to NCP6131 and Other Compatible PWM Controllers
- Thermally Enhanced Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Power Management Solutions for Notebook Systems



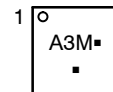
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



DFN8  
CASE 506AA

### MARKING DIAGRAM



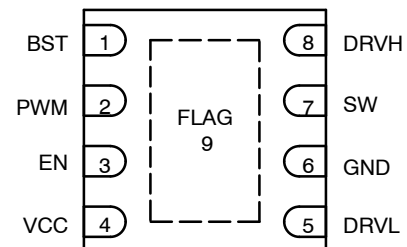
A3 = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

### PINOUT DIAGRAM



### ORDERING INFORMATION

Device	Package	Shipping†
NCP81151MNTAG	DFN8 (Pb-Free)	3000 / Tape & Reel
NCP81151MNTBG	DFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP81151

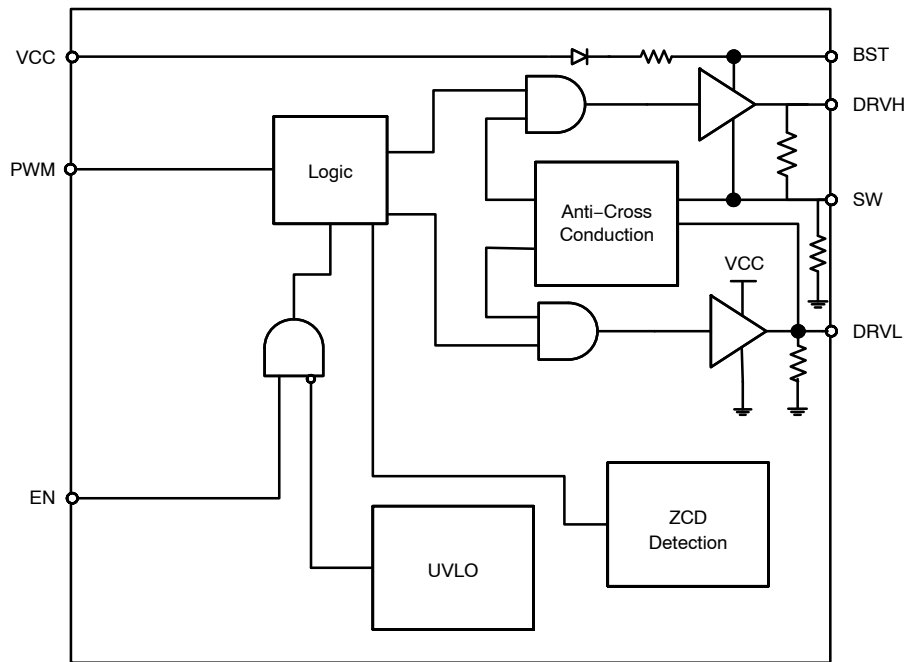


Figure 1. Block Diagram

## PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2	PWM	Control input. The PWM signal has three distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled.
3	EN	Logic input. A logic high to enable the part and a logic low to disable the part. Three states logic input: EN = High to enable the gate driver; EN = Low to disable the driver; EN = Mid to go into diode mode (both high and low side gate drive signals are low)
4	VCC	Power supply input. Connect a bypass capacitor (0.1 $\mu$ F) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node.
7	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
8	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.



# NCP81151

## ABSOLUTE MAXIMUM RATINGS

### ELECTRICAL INFORMATION

Symbol	Pin Name	V <sub>MAX</sub>	V <sub>MIN</sub>
V <sub>CC</sub>	Main Supply Voltage Input	6.5 V	-0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 6.5 V wrt/ SW 7.7 V < 50 ns wrt/ SW	-0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	-5 V -10 V (200 ns)
DRVH	High Side Driver Output	BST + 0.3 V	-0.3 V wrt/SW -2 V (< 200 ns) wrt/SW
DRVL	Low Side Driver Output	V <sub>CC</sub> + 0.3 V	-0.3 V DC -5 V (< 200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	-0.3 V
EN	Enable Pin	6.5 V	-0.3 V
GND	Ground	0 V	0 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

\*All signals referenced to AGND unless noted otherwise.

### THERMAL INFORMATION

Symbol	Parameter	Value	Unit
R <sub>θJA</sub>	Thermal Characteristic QFN Package (Note 1)	119	°C/W
T <sub>J</sub>	Operating Junction Temperature Range (Note 2)	-40 to 150	°C
T <sub>A</sub>	Operating Ambient Temperature Range	-40 to +100	°C
T <sub>STG</sub>	Maximum Storage Temperature Range	-55 to +150	°C
MSL	Moisture Sensitivity Level - QFN Package	1	

\*The maximum package power dissipation must be observed.

1. 1 in<sup>2</sup> Cu, 1 oz. thickness.

2. JESD 51-7 (1S2P Direct-Attach Method) with 1 LFM.

# NCP81151

**NCP81151 ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} < T_A < +100^{\circ}\text{C}$ ;  $4.5\text{ V} < V_{\text{CC}} < 5.5\text{ V}$ ,  $4.5\text{ V} < \text{BST-SWN} < 5.5\text{ V}$ ,  $4.5\text{ V} < \text{BST} < 30\text{ V}$ ,  $0\text{ V} < \text{SWN} < 21\text{ V}$ , unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
-----------	-----------------	-----	-----	-----	------

## SUPPLY VOLTAGE

VCC Operation Voltage		4.5		5.5	V
-----------------------	--	-----	--	-----	---

## UNDERVOLTAGE LOCKOUT

VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV

## SUPPLY CURRENT

Shutdown Mode	$I_{\text{CC}} + I_{\text{BST}}$ , EN = GND		11	20	$\mu\text{A}$
Normal Mode	$I_{\text{CC}} + I_{\text{BST}}$ , EN = 5 V, PWM = OSC		4.7		mA
Standby Current	$I_{\text{CC}} + I_{\text{BST}}$ , EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		0.9		mA
Standby Current	$I_{\text{CC}} + I_{\text{BST}}$ , EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		1.1		mA

## BOOTSTRAP DIODE

Forward Voltage	$V_{\text{CC}} = 5\text{ V}$ , forward bias current = 2 mA	0.1	0.4	0.6	V
-----------------	--	-----	-----	-----	---

## PWM INPUT

PWM Input High		3.4			V
PWM Mid-State		1.3		2.7	V
PWM Input Low				0.7	V
ZCD Blanking Timer			350		ns

## HIGH SIDE DRIVER

Output Impedance, Sourcing Current	$V_{\text{BST}} - V_{\text{SW}} = 5\text{ V}$		0.9	1.7	$\Omega$
Output Impedance, Sinking Current	$V_{\text{BST}} - V_{\text{SW}} = 5\text{ V}$		0.7	1.7	$\Omega$
DRVH Rise Time $t_{\text{rDRVH}}$	$V_{\text{CC}} = 5\text{ V}$ , 3 nF load, $V_{\text{BST}} - V_{\text{SW}} = 5\text{ V}$		16	25	ns
DRVH Fall Time $t_{\text{fDRVH}}$	$V_{\text{CC}} = 5\text{ V}$ , 3 nF load, $V_{\text{BST}} - V_{\text{SW}} = 5\text{ V}$		11	18	ns
DRVH Turn-Off Propagation Delay $t_{\text{pd}1\text{DRVH}}$	$C_{\text{LOAD}} = 3\text{ nF}$	10		30	ns
DRVH Turn-On Propagation Delay $t_{\text{pd}h\text{DRVH}}$	$C_{\text{LOAD}} = 3\text{ nF}$	10		40	ns
SW Pulldown Resistance	SW to PGND		45		k $\Omega$
DRVH Pulldown Resistance	DRVH to SW, BST-SW = 0 V		45		k $\Omega$

## LOW SIDE DRIVER

Output Impedance, Sourcing Current			0.9	1.7	$\Omega$
Output Impedance, Sinking Current			0.4	0.8	$\Omega$
DRVL Rise Time $t_{\text{rDRVL}}$	$C_{\text{LOAD}} = 3\text{ nF}$		16	25	ns
DRVL Fall Time $t_{\text{fDRVL}}$	$C_{\text{LOAD}} = 3\text{ nF}$		11	15	ns
DRVL Turn-Off Propagation Delay $t_{\text{pd}1\text{DRVL}}$	$C_{\text{LOAD}} = 3\text{ nF}$	10		30	ns
DRVL Turn-On Propagation Delay $t_{\text{pd}h\text{DRVL}}$	$C_{\text{LOAD}} = 3\text{ nF}$	5.0		25	ns
DRVL Pulldown Resistance	DRVL to PGND, $V_{\text{CC}} = \text{PGND}$		45		k $\Omega$

# NCP81151

**NCP81151 ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} < T_A < +100^{\circ}\text{C}$ ;  $4.5\text{ V} < V_{\text{CC}} < 5.5\text{ V}$ ,  $4.5\text{ V} < \text{BST-SWN} < 5.5\text{ V}$ ,  $4.5\text{ V} < \text{BST} < 30\text{ V}$ ,  $0\text{ V} < \text{SWN} < 21\text{ V}$ , unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>EN INPUT</b>					
Input Voltage High		3.3			V
Input Voltage Mid		1.35		1.8	V
Input Voltage Low				0.6	V
Input bias current		-1.0		1.0	$\mu\text{A}$
Propagation Delay Time			20	40	ns

## SW NODE

SW Node Leakage Current				20	$\mu\text{A}$
Zero Cross Detection Threshold Voltage			-6.0		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

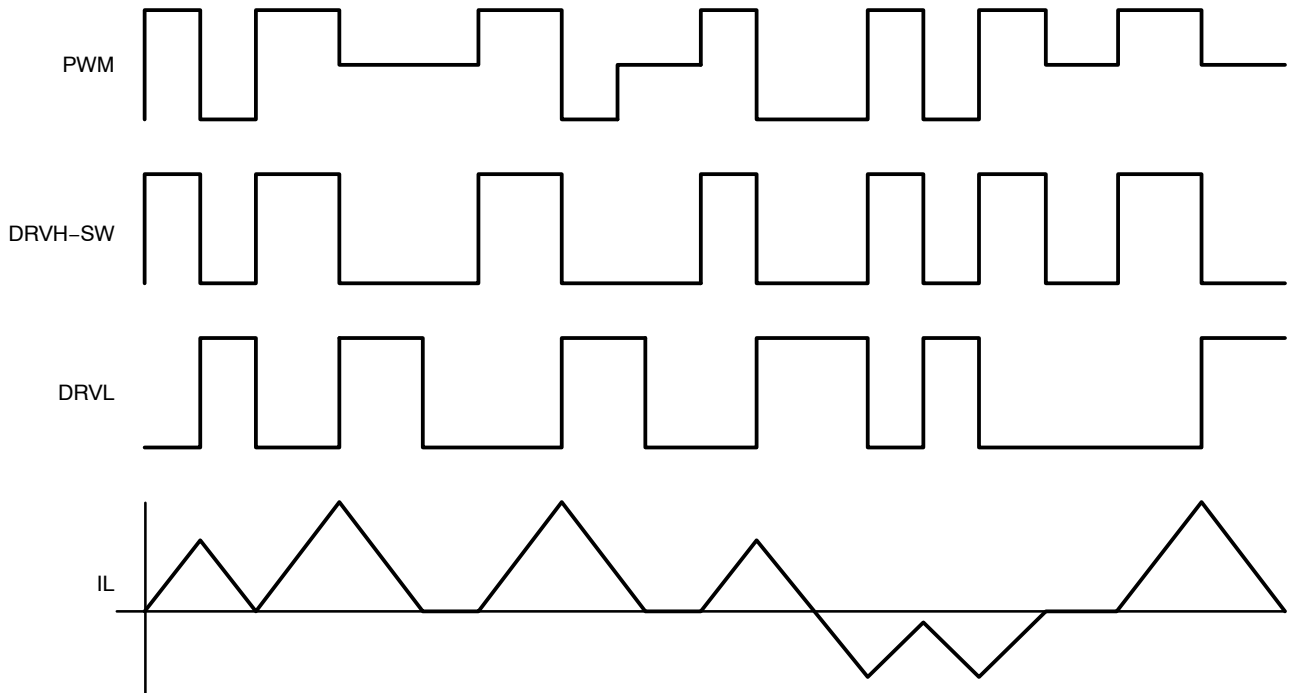
# NCP81151

**Table 1. DECODER TRUTH TABLE**

Input	ZCD	DRVL	DRVH
PWM High (Enable High)	ZCD Reset	Low	High
PWM Mid (Enable High)	Positive Current Through the Inductor	High	Low
PWM Mid (Enable High)	Zero Current Through the Inductor	Low	Low
PWM Low (Enable High)	ZCD Reset	High	Low
Enable at Mid	X	Low	Low



**Figure 3.**



**Figure 4. Timing Diagram**

## APPLICATION INFORMATION

The NCP81151 gate driver is a single phase MOSFET driver designed for driving N-channel MOSFETs in a synchronous buck converter topology. The NCP81151 is designed to work with ON Semiconductor's NCP6131 multi-phase controller. This gate driver is optimized for notebook applications.

**Undervoltage Lockout**

DRVH and DRVL are held low until VCC reaches 4.5 V during startup. The PWM signal will control the gate status when VCC threshold is exceeded.

**Three-State EN Signal**

When EN is set to the mid state, both DRVH and DRVL are set low, to force diode mode operation.

**PWM Input and Zero Cross Detect (ZCD)**

The PWM input, along with EN and ZCD, control the state of DRVH and DRVL.

When PWM is set high, DRVH will be set high after the adaptive non-overlap delay. When PWM is set low, DRVL will be set high after the adaptive non-overlap delay.

When PWM is set to the mid state, DRVH will be set low, and after the adaptive non-overlap delay, DRVL will be set high. DRVL remains high during the ZCD blanking time. When the timer has expired, the SW pin will be monitored for zero cross detection. After the detection, DRVL will be set low.

**Adaptive Non-overlap**

Adaptive dead time control is used to avoid shoot-through damage of the power MOSFETs. When the PWM signal pulls high, DRVL will be set low and the driver will monitor the gate voltage of the low side MOSFET. When the DRVL voltage falls below the gate threshold, DRVH will be set to

high after the  $t_{pdhDRVH}$  delay. When PWM is set low, the driver will monitor the gate voltage of the high side MOSFET. When the DRVH-SWN voltage falls below the top gate drive threshold, DRVL will be set to high after the  $t_{pdhDRVL}$  delay.

**Layout Guidelines**

The layout for a DC-DC converter is very important. The bootstrap and VCC bypass capacitors should be placed close to the driver IC.

Connect the GND pin to a local ground plane. The ground plane can provide a good return path for gate drives and reduce the ground noise. The thermal slug should be tied to the ground plane for good heat dissipation. To minimize the ground loop for the low side MOSFET, the driver GND pin should be close to the low-side MOSFET source pin. The gate drive trace should be routed to minimize its length. The minimum width is 20 mils.

**Gate Driver Power Loss Calculation**

The gate driver power loss consists of the gate drive loss and quiescent power loss.

The equation below can be used to calculate the power dissipation of the gate driver.  $Q_{GMF}$  is the total gate charge for each main MOSFET and  $Q_{GSF}$  is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[ \frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC} \right] \times V_{CC} \quad (\text{eq. 1})$$

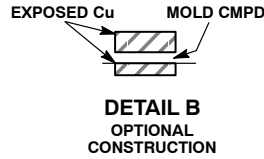
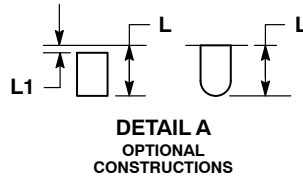
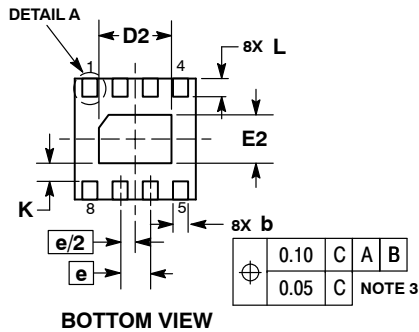
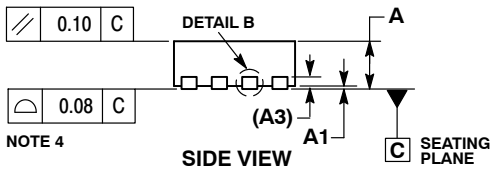
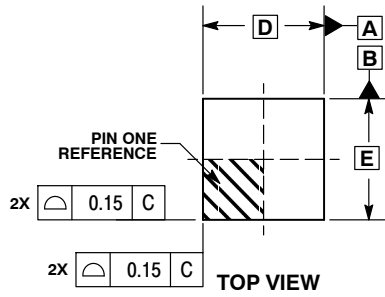
Also shown is the standby dissipation factor ( $I_{CC} \times V_{CC}$ ) of the driver.



# NCP81151

## PACKAGE DIMENSIONS

DFN8 2x2  
CASE 506AA  
ISSUE E

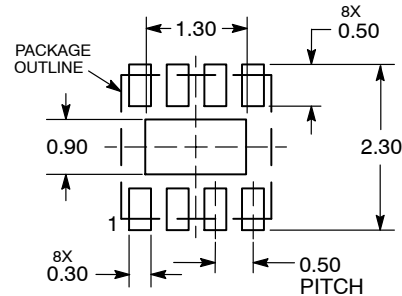


NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1	---	0.10

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative