BGSA14GN10

Single-Pole Quad Throw Antenna Tuning Switch

Data Sheet

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Power Management & Multimarket

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Revision History

Document No.: BGSA14GN10.pdf	
Revision History: 2.0	
Previous Version: 1.2 - 2015-08-04	
Page	**Subjects (major changes since last revision)**
6	added on Table. 3 Absolute Maximum RF Voltage
9	deleted RF Operating Voltage on Table. 7
12	Package Dimensions Drawing figure updated (Figure3)

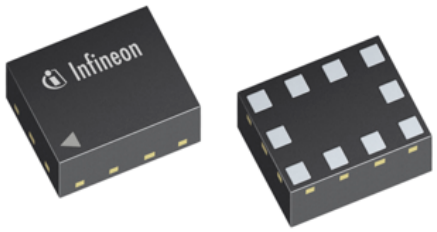
Contents

List of Figures

List of Tables

BGSA14GN10 Single-Pole Quad Throw Antenna Tuning Switch

1 Features



- High-linearity SP4T for antenna aperture switching applications
- Ultra-Low R_{ON} of 1.6 Ω in ON state
- Ultra-Low C_{OFF} of 120 *fF* in OFF state
- High max RF voltage state handling
- Low harmonic generation
- No DC decoupling components required, if no external DC is applied on RF ports
- Supply voltage range: 1.8 to 3.6 V
- No insertion loss change within supply voltage range
- No linearity change within supply voltage range
- Suitable for EDGE / C2K / LTE / WCDMA Applications
- 0.1 to 5.0 GHz coverage
- Small form factor 1.1 mm x 1.5 mm
- 400 μm pad pitch
- RoHS and WEEE compliant package

2 Product Description

The BGSA14GN10 is a Single Pole Quad Throw (SP4T) RF antenna aperture switch optimized for low C_{off} enabling applications up to 5.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Table 1: Ordering Information

Type	Package	Marking	Chip
BGSA14GN10	TSNP10-1/-2	A4	BGSA14GN10

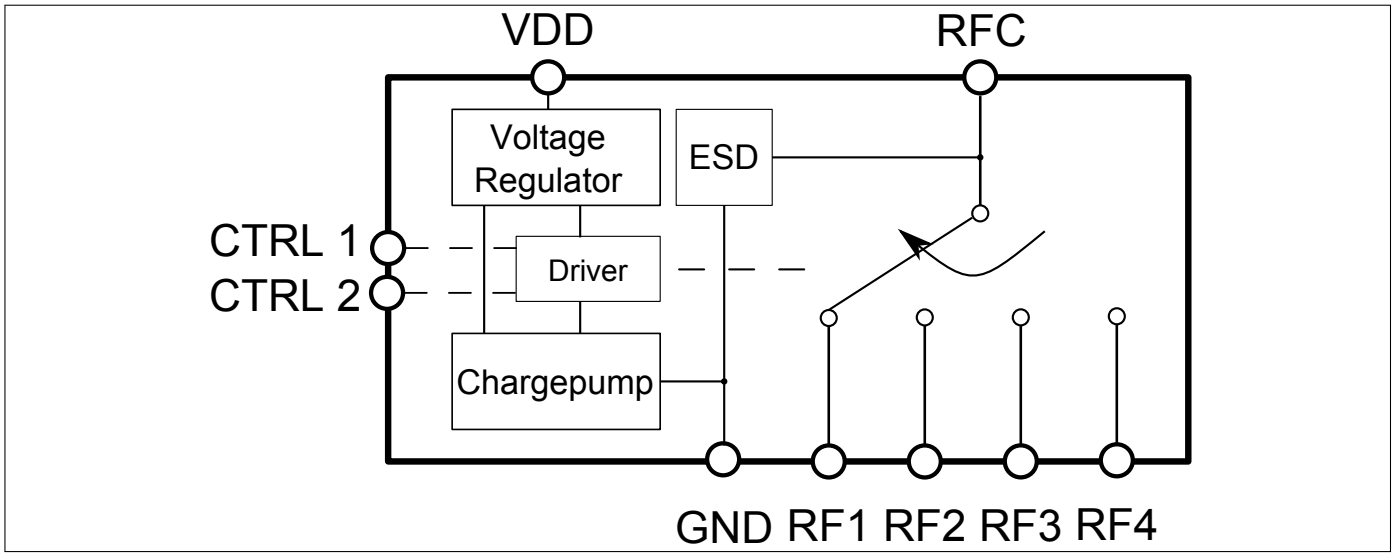


Figure 1: BGSA14GN10 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	–	GHz	[1]
Supply voltage [2]	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_TRx}	–	–	39	dBm	25 % Duty Cycle
RF voltage[3]	V_{RF_max}	–	–	48	V	All switch throws operated in isolation mode.
ESD capability, CDM [4]	$V_{ESD_{CDM}}$	-1.5	–	+1.5	*kV*	
ESD capability, HBM [5]	$V_{ESD_{HBM}}$	-1	–	+1	*kV*	
ESD capability, system level (RFC port) [6]	$V_{ESD_{ANT}}$	-8	–	+8	*kV*	RFC vs system GND, with 27 nH shunt inductor
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has no highpass response. There is also a high ohmic DC to the RF path. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{DD}. A high RF ripple at the V_{DD} can exceed the maximum ratings by $V_{DD} = V_{DC} + V_{Ripple}$.
[3] 1000h over 8 years lifetime-short pulse duration
[4] Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[5] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
[6] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{CTRL}	-0.7	–	3.3	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.8	2.85	3.6	V	–
Supply current[1)]	I_{DD}	–	80	150	μA	–
Control voltage low	$V_{Ctrl,low}$	0		0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} \ll V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	μA	–
Control current high	$I_{Ctrl,high}$	-1	0	1	μA	$V_{Ctrl,high} \ll V_{DD}$
Ambient temperature	T_A	-30	25	85	°C	–
RF switching time	t_{sw}	2	5	7	μs	–
Startup time	t_{sw}		20	30	μs	–

[1)] T_A = -30 °C – +85 °C, V_{VDD} = 1.8 – 3.6 V

5 Logic Table

Table 5: Logic Table

CTRL 1	CTRL 2	Mode
0	0	RF1 connected to RFC
0	1	RF2 connected to RFC
1	0	RF3 connected to RFC
1	1	RF4 connected to RFC

6 RF small signal parameter

Table 6: RF small signal parameter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	5.0	GHz	–
Switch ON resistance	R_{ON}	–	1.6		Ω	RFx to RFC
Switch OFF capacitance	C_{OFF}	–	120		fF	RFx to RFC
Parasitic RF shunt capacitance	$C_{SH,PAR}$	–	42		fF	RFx to GND, extracted value for 2 GHz
Switch series inductance	L_{SER}	–	0.1		nH	
Insertion Loss [1,2,3]						
698 - 960 MHz	*IL*	0.16	0.26	0.36	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω
1710 - 1980 MHz		0.23	0.37	0.47	dB	
1980 - 2170 MHz		0.29	0.39	0.49	dB	
2170 - 2690 MHz		0.36	0.46	0.59	dB	
Return Loss[1,2,3]						
All Ports @ 698 - 960 MHz	*RL*	19	22	26	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω
All Ports @ 1710 - 2690 MHz		17	21	25	dB	
Isolation RFx to RFC[1,2,3]						
698 - 960 MHz	*ISO*	28	31	38	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω
1710 - 1980 MHz		21	25	35	dB	
1980 - 2170 MHz		20	23	35	dB	
2170 - 2690 MHz		17	20	27	dB	

[1] Valid for all RF power levels, no compression behavior
[2] Network analyser input power: $P_{IN} = -20\,dBm$
[3] On application board without any matching components

7 RF large signal parameter

Table 7: RF large signal specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation up to 12.75 GHz[1,2,3]						
All RF Ports - Second Order Harmonics	P_{H2}	–	105	–	dBc	25 dBm, 50Ω, f_0 = 786 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	115	–	dBc	25 dBm, 50Ω, f_0 = 786 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	93	–	dBc	33 dBm, 50Ω, f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	94	–	dBc	33 dBm, 50Ω, f_0 = 824 MHz
All RF Ports	P_{Hx}	105	–	–	dBc	25 dBm, 50Ω
Intermodulation Distortion IMD2 [1,2,3]						
IIP2, low	IIP2,l	–	110	–	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	–	120	–	dBm	
Intermodulation Distortion IMD3 [1,2,3]						
IIP3	IIP3	–	75	–	dBm	IIP3 conditions table 9
SV LTE Intermodulation [1,2,3]						
IIP3,SVLTE	IIP3,SV	–	75	–	dBm	SV-LTE conditions table 10

[1] Terminating Port Impedance: Z_0 = 50 Ω
[2] Supply Voltage: V_{DD} = 1.8 – 3.6 V
[3] On application board without any matching components

Table 8: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 9: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 10: SV-LTE conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

8 Package Outline and Pin Configuration

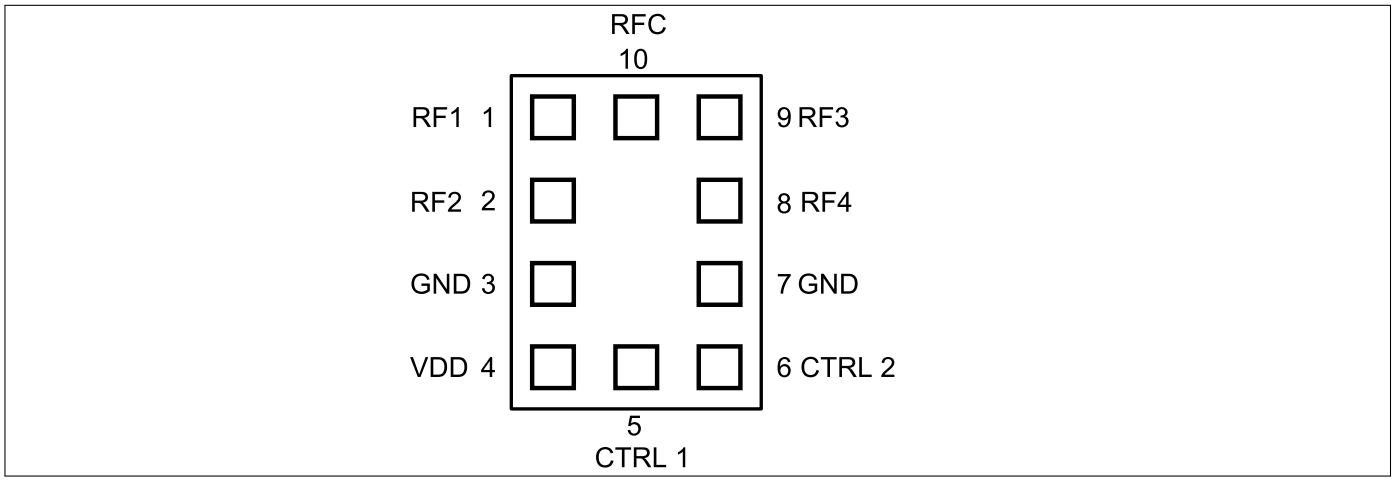


Figure 2: Pinout (top view)

Table 11: Pin Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	RF1	I/O		RF1
2	RF2	I/O		RF2
3	GND	GND		Ground
4	VDD	PWR		Supply voltage
5	CTRL1	I		Control 1 Pin
6	CTRL2	I		Control 2 Pin
7	GND	GND		Ground
8	RF4	I/O		RF4
9	RF3	I/O		RF3
10	RFC	I/O		Common RF

Table 12: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	*X*	1.1 ± 0.05	*mm*
Y-Dimension	*Y*	1.5 ± 0.05	*mm*
Size	*Size*	1.65	mm^2
Height	*H*	0.375	*mm*

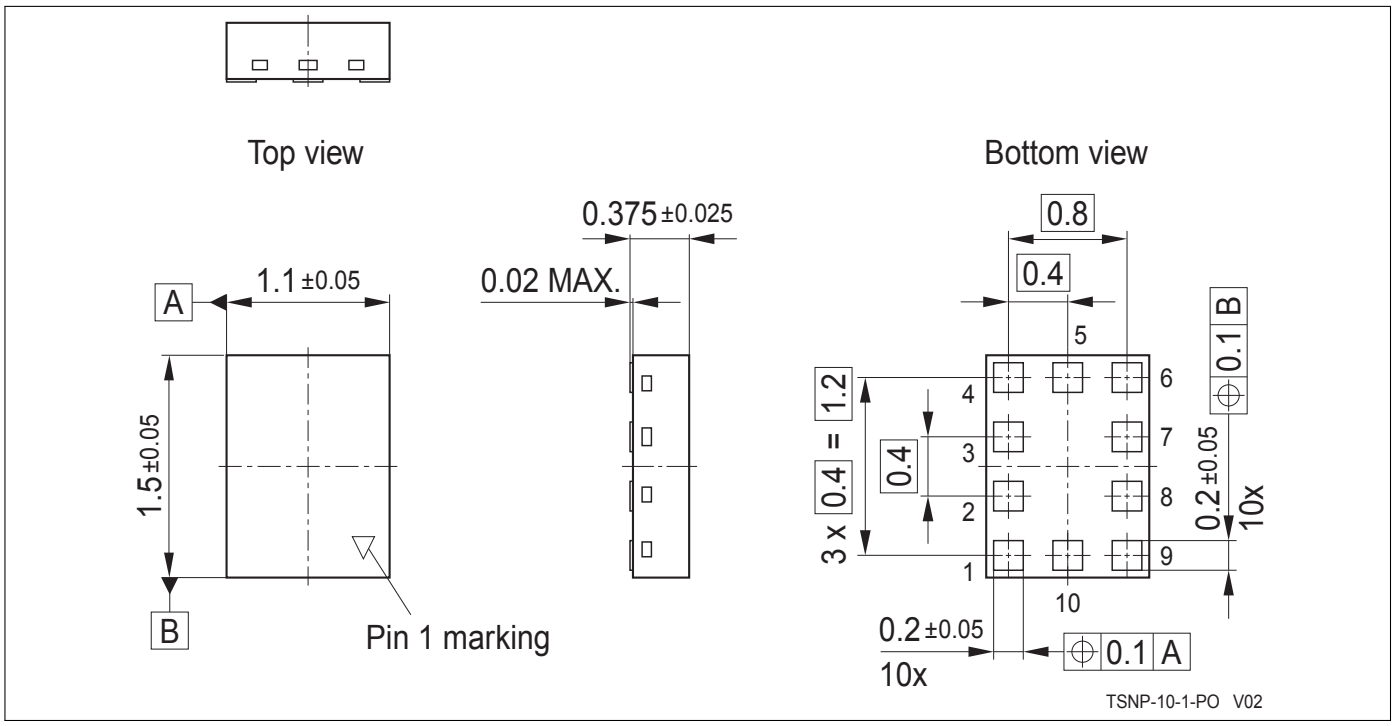


Figure 3: Package Dimensions Drawing (TSNP-10-1)

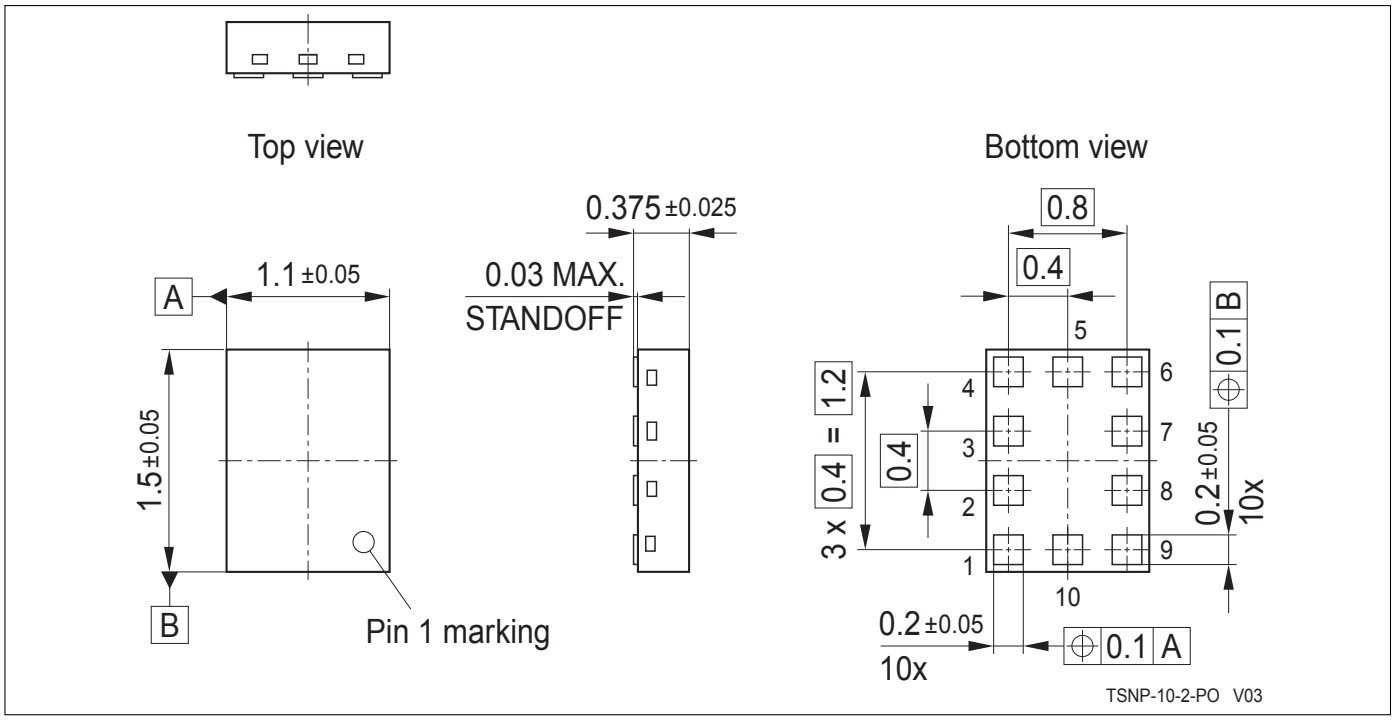


Figure 4: Package Dimensions Drawing (TSNP-10-2)

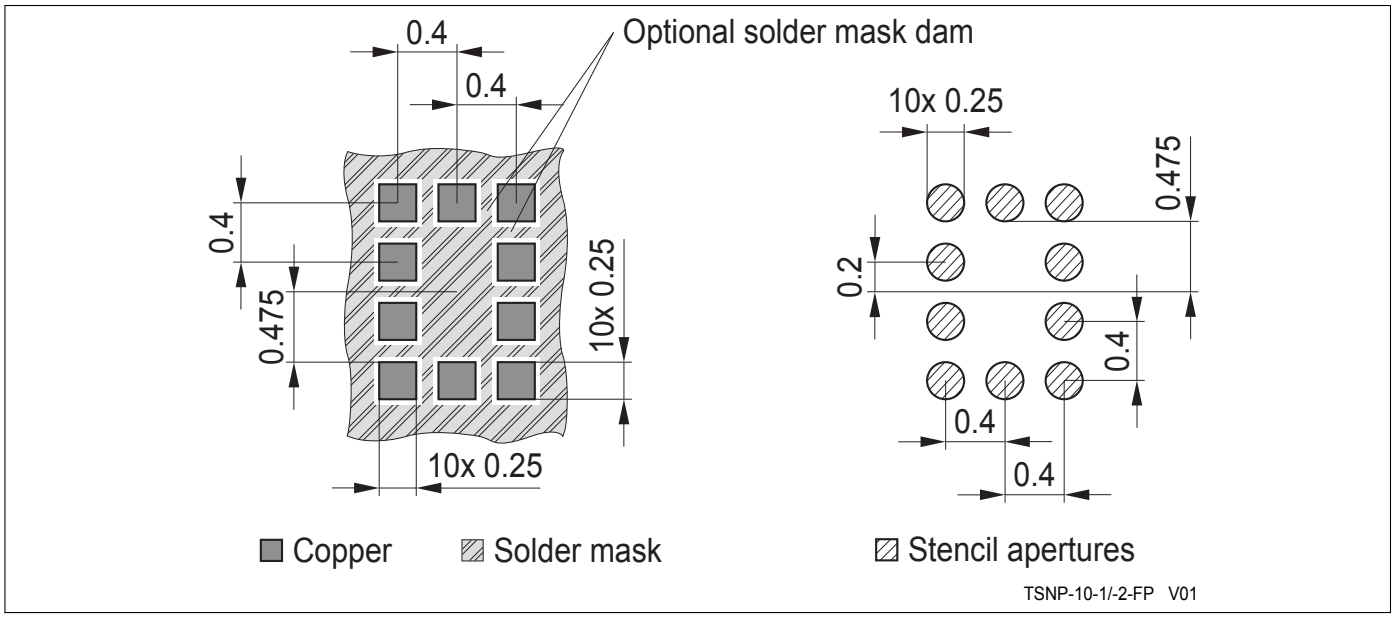


Figure 5: Land pattern and stencil mask (TSNP-10-1/-2)

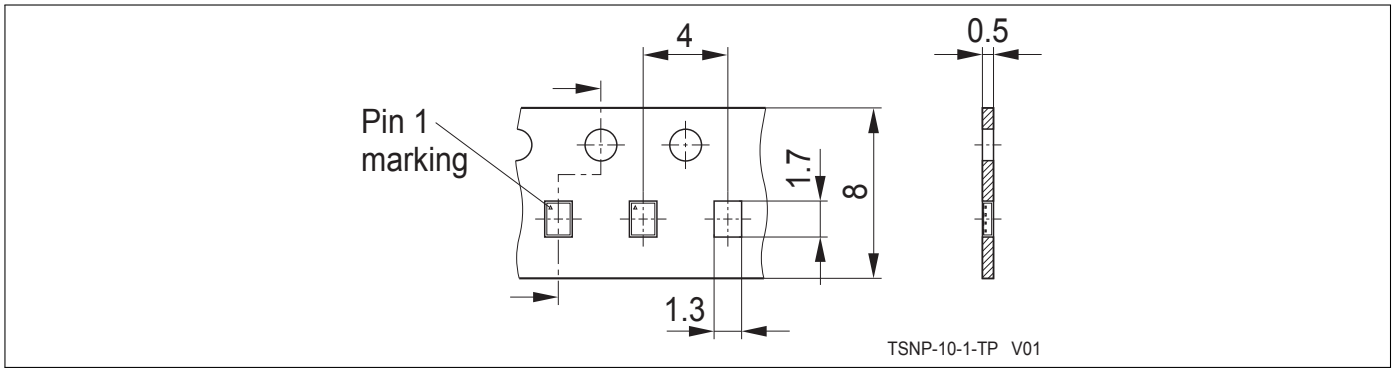


Figure 6: Tape drawing (TSNP-10-1)

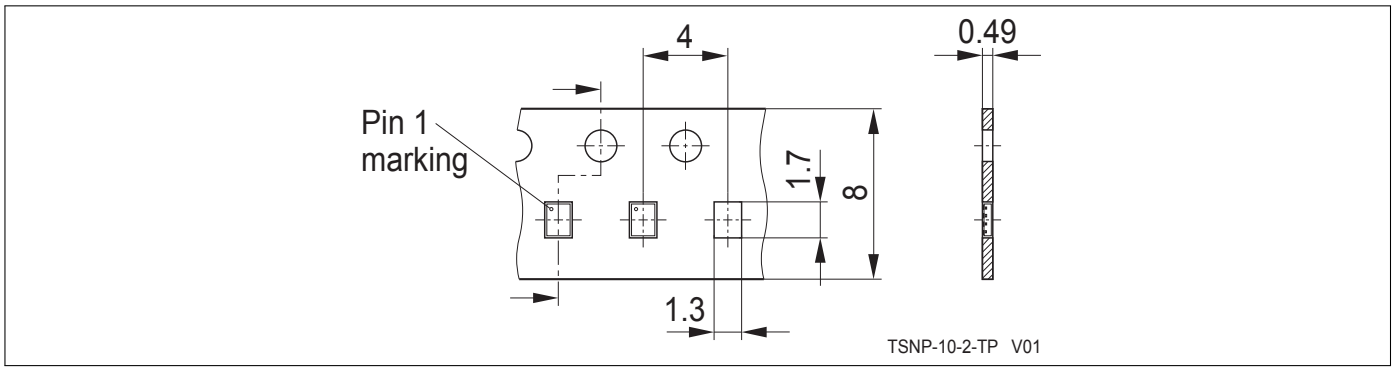


Figure 7: Tape drawing (TSNP-10-2)

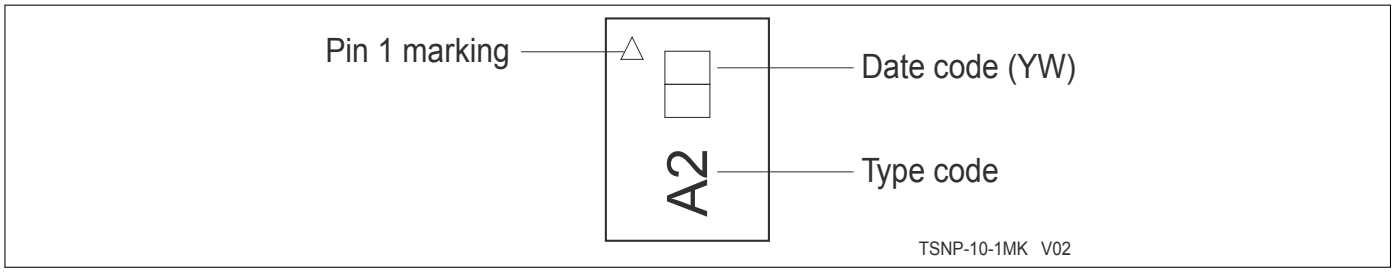


Figure 8: Package marking (TSNP-10-1): Date code digits Y and W are found in Table 13/14

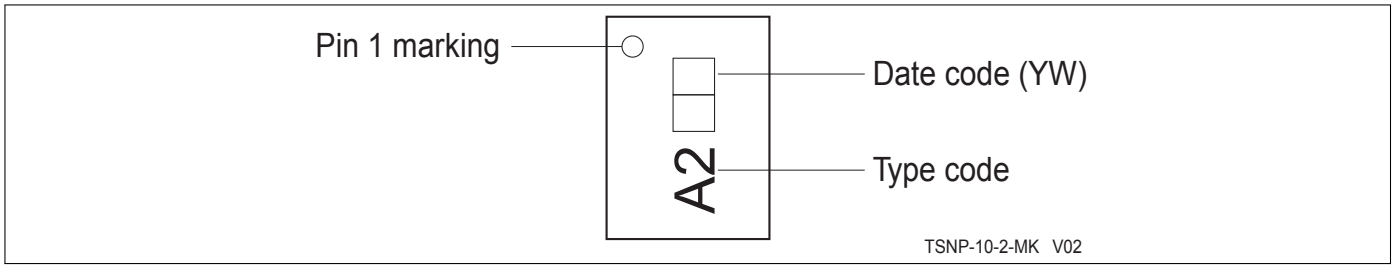


Figure 9: Package marking (TSNP-10-2): Date code digits Y and W are found in Table 13/14

Table 13: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 14: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

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