Kintex-7 FPGA Connectivity Kit

Getting Started Guide

Vivado Design Suite 2014.3

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/26/2012	1.0	Initial Xilinx release.
08/23/2012	1.1	Updated Figure 7, Figure 27, Figure 28, Figure 30, Figure 31, Figure 33, and Figure 35 with v1.1 screen captures. Changed ISE Design Suite Logic Edition Tools "v14.1" to "v14.1 or later" under Hardware Test Setup Requirements. Clarified step 3 through step 6 under Hardware Setup. Clarified step 2 through step 5 and step 3 under Installing Linux Device Drivers. Added Next Steps.
01/07/2013	2.0	Replaced reference to USB stick with link to design files (under Hardware Test Setup Requirements and Installing Linux Device Drivers). Added Note preceding Hardware Setup. Replaced reference to ISE Design Suite user guide with references to Vivado® Design Suite user guides in Appendix A, Additional Resources.
04/17/2013	3.0	Updated title page for Vivado Design Suite 2013.1. Changed "32-bit" to "32-bit and 64-bit" in last paragraph under Introduction. Added Notes 2 and 3 following Figure 1. Updated "UG477" to "PG054", "UG773" to "PG072", and "UG692" to "PG068" user guide references throughout document.
11/19/2013	4.0	Updated for Vivado Design Suite 2013.3. Strengthened the description in the power connection caution note on page 18. Revised all links and references in Appendix A, Additional Resources and revised links to websites and documents throughout document to conform to latest linking style convention.
03/07/2013	4.0.1	Tech pubs update. Technical content not affected.
05/14/2014	5.0	Updated for Vivado Design Suite 2014.1. The ZIP file name changed to `rdf0282-k7-connectivity-trd-2014-1.zip`.
12/16/2014	6.0	Updated for Vivado Design Suite 2014.3. The ZIP file name changed to `rdf0282-k7-connectivity-trd-2014-3.zip`. Updated Figure 13 and Figure 14.

Table of Contents

Getting Started with the Kintex-7 FPGA Connectivity Kit

The Kintex®-7 FPGA connectivity kit provides a comprehensive, high-performance development and demonstration platform using the Kintex-7 FPGA family for high-bandwidth and high-performance applications in multiple market segments. The kit enables designing with DDR3, I/O expansion through FMC, and common serial standards, such as PCI Express® and 10GBASE-R through the FMC interface.

This Getting Started Guide is divided into two sections:

- Hardware Setup and Testing with the KC705 Built-in Self-test

  This section on the built-in self-test (BIST) familiarizes users with the KC705 board, the various switch positions, the sequence to program the FPGA, and provides a sanity check on the board's hardware components.

- Connectivity System Setup with the Targeted Reference Design

  This section provides the steps required to setup the connectivity targeted reference design (TRD) hardware, program the FPGA, load the application driver, and become familiar with the GUI.

Hardware Setup and Testing with the KC705 Built-in Self-test

The built-in self-test (BIST) tests many of the features offered by the Kintex-7 FPGA KC705 evaluation kit. The test is stored in the nonvolatile BPI Linear Flash memory, and configures the FPGA when the mode and upper flash address pins on the board are set for Master BPI.

Figure 1 provides an overview of the board features used by the BIST.

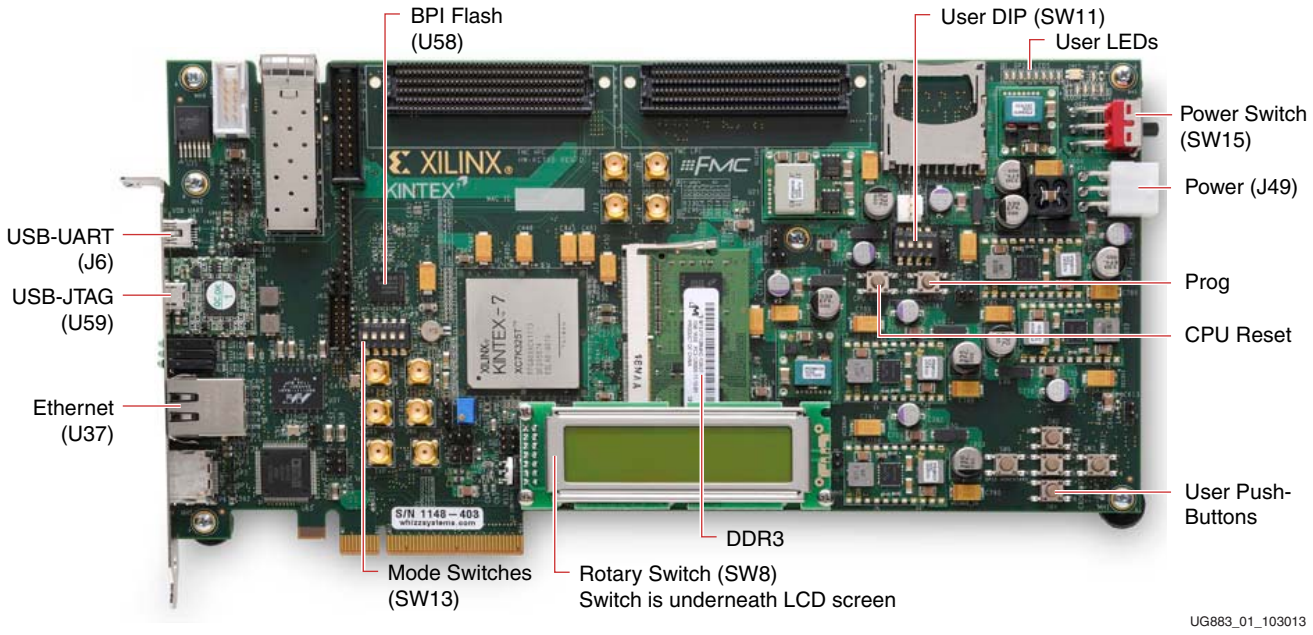

Figure 1: **KC705 Board Features**

Note: For a diagram of all the features on the KC705, see *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810) [Ref 1].

Hardware Test Setup Requirements

The prerequisites for testing the design in hardware are:

- KC705 Evaluation board with the Kintex-7 FPGA XC7K325T-2FFG900C device
- USB Type-A to Mini-B cable (for UART)
- AC power adapter (12 VDC)
- TeraTerm Pro terminal program [Ref 2]

  Note: The Tera Term Pro program is used for illustrative purposes. Other terminal programs can be used.
- CP210x USB to UART Bridge VCP Drivers from Silicon Labs [Ref 3]

Hardware Test Board Setup Requirements

This section details the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

KC705 Evaluation Board Setup

1. Set the jumpers and switches on the KC705 board as follows:
   - The mode switches (SW13) are set for Master BPI mode 010.
   - The upper flash address switches (SW13) are set to 11.
2. Verify the switch and jumper settings are set as shown in Table 1 and Figure 2.

Note: For this application, the board should be set up as a stand-alone system, with power coming from the cord and brick that comes with the KC705 evaluation kit.

Table 1: **Switch and Jumper Settings**

Switch	Setting	
SW15	Board Power slide-switch	
	N/A	Off
SW11	User GPIO DIP switch	
	4	Off
	3	Off
	2	Off
	1	Off
SW13	Configuration Mode switch	
	5	Off
	4	On
	3	Off
	2	On
	1	On

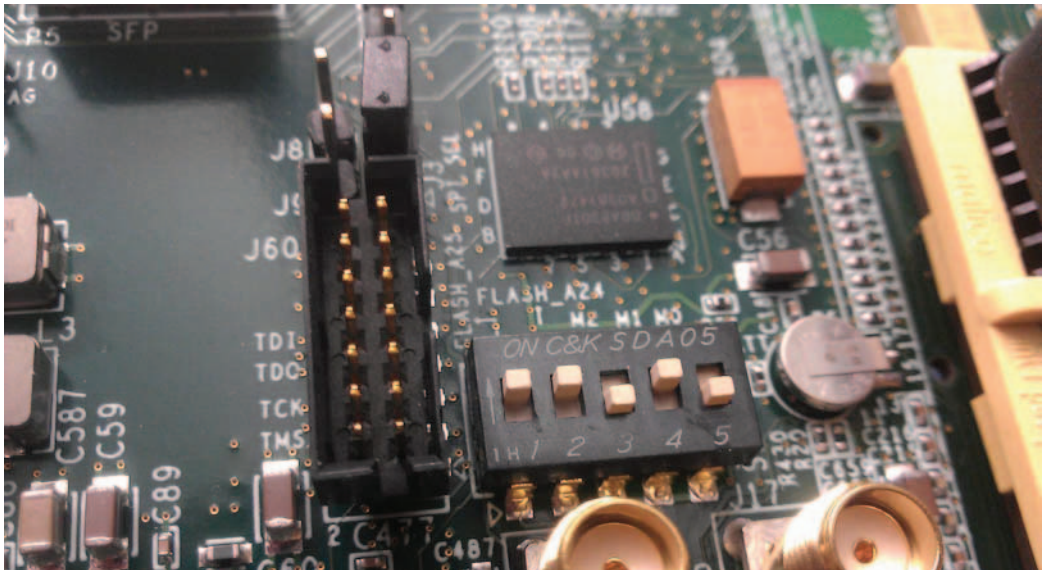

Figure 2: **BIST Switch and Jumper Settings**

Hardware Bring-Up

This section details the steps for hardware bring-up:

1. With the board switched off, plug a USB-to-Mini-B cable into the UART port of the KC705 board and the PC (see Figure 3).
2. Install the power cable.
3. Switch the KC705 board power to ON.

Figure 3: **KC705 with the UART and Power Cable Attached**

Install the UART Driver

1. Run the downloaded executable UART-USB driver file listed in Hardware Test Setup Requirements, page 8. This enables UART-USB communications with a host PC (see Figure 4).

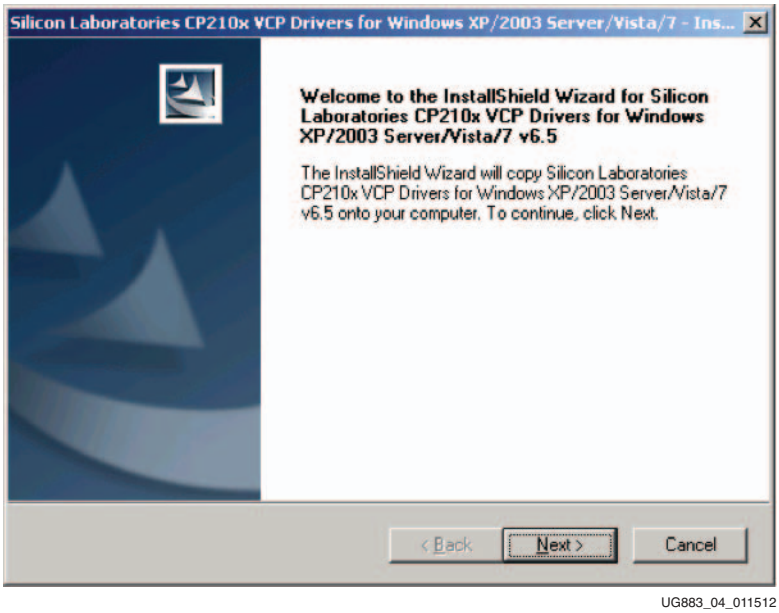

Figure 4: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known port in the Device Manager as follows:
   - Right-click **My Computer** and select **Properties**.
   - Select the **Hardware** tab, then click the **Device Manager** button.
   - Find and right-click the Silicon Labs device in the list. Then select **Properties**.
   - Click the **Port Settings** tab and the **Advanced...** button.
   - Select an open COM port between COM1 and COM4.

Figure 5 shows the steps needed to set the USB-UART port.

Note: Steps and diagrams refer to use with a Windows host PC with the Windows XP or Windows 7 operating system.

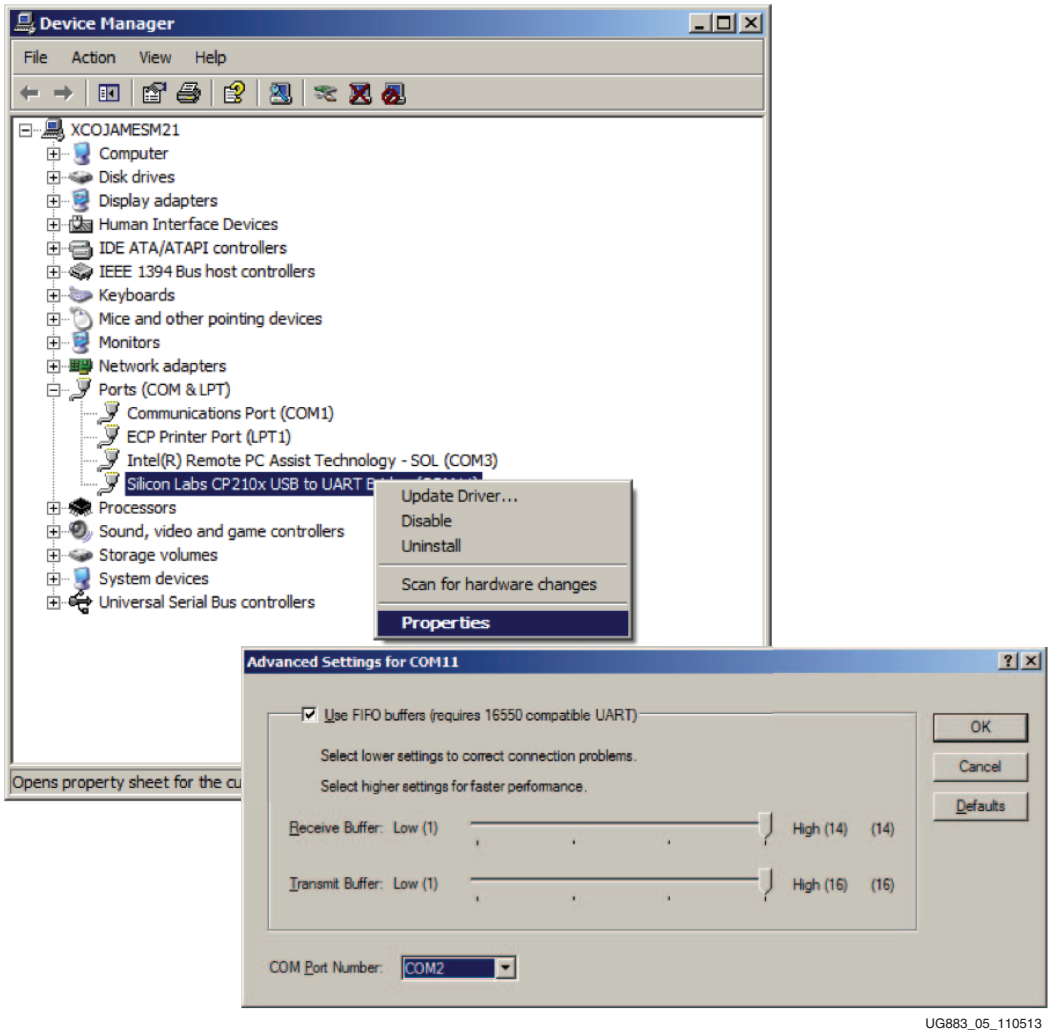

Figure 5: **Port Selection on the Device Manager Screen**

Run the BIST Application

1. Start the installed terminal program.
2. Press PROG (SW14) on the KC705 board, and view the BIST output on the terminal window (see Figure 6).

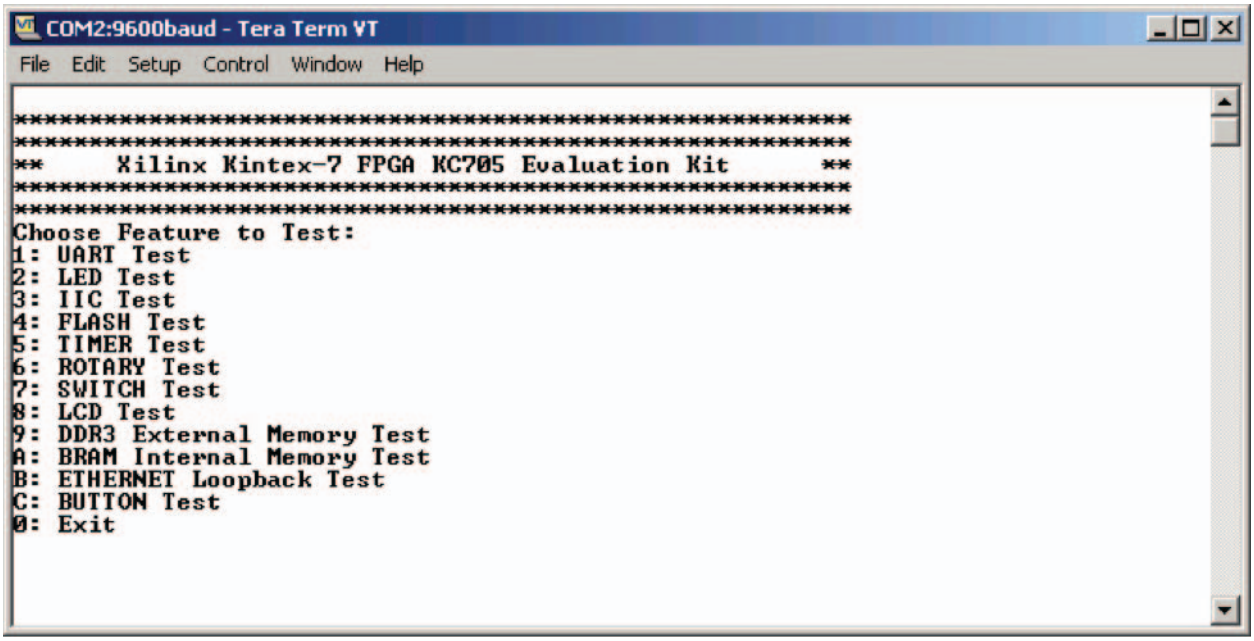

Figure 6: **BIST Main Menu**

3. Select the relevant tests to run, and observe the results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the Kintex-7 FPGA KC705 Evaluation Kit website.

Connectivity System Setup with the Targeted Reference Design

Introduction

Figure 7 depicts the block level overview of the Kintex-7 connectivity TRD which delivers up to 20 Gb/s of performance per direction.

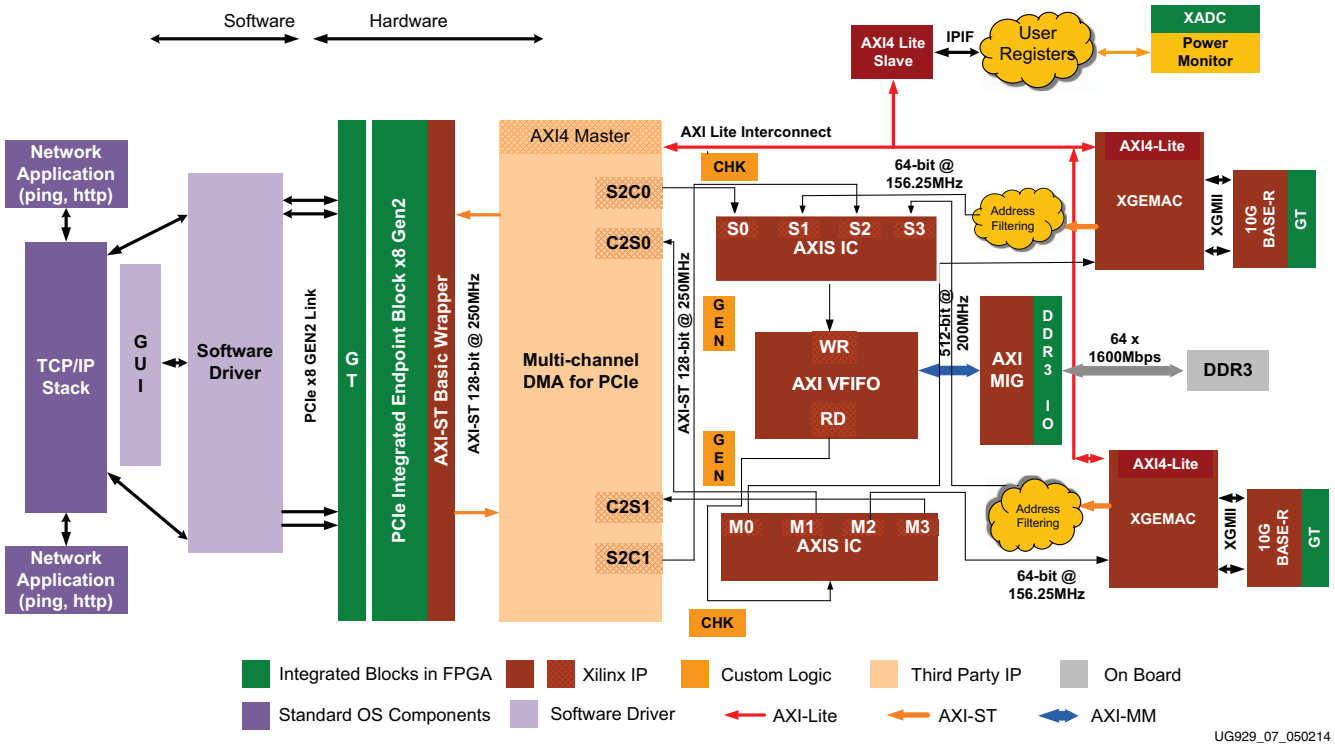

Figure 7: **Kintex-7 Connectivity TRD Block Diagram**

Notes:

1. The arrows in Figure 7 indicate AXI interface directions from master to slave. They do not indicate data flow directions.
2. The DMA netlist shipped along with this core is an evaluation netlist. For full version netlist, contact Northwest Logic [Ref 4].
3. The DMA used in the TRD is configured for x8Gen2 PCIe interface. For other supported configurations, contact Northwest Logic [Ref 4].

The design is a dual Network Interface Card (NIC) with an x8 GEN2 PCIe® Endpoint, a multi-channel packet DMA from Northwest Logic, DDR3 memory for buffering, 10-Gigabit Ethernet MAC and 10GBASE-R standard compatible physical layer interface. The PCIe-DMA together is responsible for movement of data between a PC system and FPGA (S2C implies data movement from PC system to FPGA and C2S implies data movement from FPGA to PC system).

DDR3 SDRAM (64-bit, 1,600 Mb/s or 800 MHz) is used for packet buffering – a virtual FIFO layer facilitates the use of DDR3 as multiple FIFOs. The virtual FIFO layer is built using the AXI Stream interconnect and AXI Virtual FIFO controller CoreGEN IPs.

Dual NIC application is built over this by use of 10- Gigabit Ethernet MAC and 10-Gigabit PCS/PMA (10GBASE-R PHY) IPs. The 10G MAC connects to the 10G BASE-R PHY over 64-bit, SDR XGMII parallel interface. Additionally, the design provides power monitoring capability based on a PicoBlaze™ processor engine.

For software, the design provides 32-bit and 64-bit Linux drivers for all modes of operation listed and a graphical user interface (GUI) that controls the tests and monitors the status.

Features

The Kintex-7 FPGA connectivity TRD features these components:

- PCI Express v2.1 compliant GEN2 x8 Endpoint operating at 5 Gb/s per lane per direction
  - PCIe transaction interface utilization engine
  - MSI and legacy interrupt support
- Bus mastering scatter-gather DMA to offload processor
- Multi-channel DMA
- AXI4 streaming interface for data
- AXI4 interface for register space access
- DMA performance engine
- Full duplex operation
  - Independent transmit and receive channels
- 10-Gigabit Ethernet MAC with 10G BASE-R PHY
  - Address filtering
  - Inter-frame gap control
  - Jumbo frame support up to 16,383 bytes in size
  - Ethernet statistics engine
  - Management interface for configuration (MDIO)
- PicoBlaze processor-based PVT monitoring
  - Engine in hardware to monitor power by reading the TI UCD9248 power controller chip on-board KC705
  - Engine in hardware to monitor die temperature via Xilinx analog-to-digital converter
- Application demand driven power management
  - Option to change PCIe link width and link speed for reduced power consumption in lean traffic scenario

Hardware Test Setup Requirements

The prerequisites for testing the design in hardware are:

- KC705 evaluation board with XC7K325T-2FFG900 FPGA
- Design files
  - Design source files
  - Device driver files
  - Board design files

  - Documentation

    Design files are available at the Kintex-7 FPGA Connectivity Kit Documentation website.

- Vivado® Design Suite Logic Edition Tools 2014.3 or later
- 4-pin to 6-16 12V PCIe adapter cable
- Micro USB cable
- FM-S14 FMC card with 4 SFP+ cages from Faster Technology, LLC [Ref 5]
- Two 10G MMF SFP+ SR optical transceivers from Avago Technologies [Ref 6]
- LC to LC OM3 10G fiber optic patch cable from Amphenol Corporation [Ref 7]
- Fedora 16 LiveCD from Fedora Project [Ref 8]
- PC with PCIe v2.0 slot. Recommended PCI Express Gen2 PC system motherboards are ASUS P5E (Intel X38), ASUS Rampage II Gene (Intel X58) and Intel DX58SO (Intel X58). Note that the Intel X58 chipsets tend to show higher performance. This PC could also have Fedora Core 16 Linux OS installed on it. Note that the PC is not part of the Kintex-7 connectivity kit.

Note: This document refers to the initially released TRD version (v1_0). For subsequent releases, the design version will be upgraded but the change will not be reflected in this document.

Hardware Setup

This section details the hardware setup and use of provided application and control GUI to help the user get started quickly with the hardware. It provides a step-by-step explanation on hardware bring-up, software bring-up, and use of the application GUI.

All procedures listed in the following sections require super user access on a Linux machine. When using Fedora 16 LiveCD provided with the kit, super user access is granted by default due to the way the kernel image is built; if LiveCD is not used, contact the system administrator for super user access.

1. With the power supply turned off, ensure that switches P1 and P2 on the FM-S14 FMC card are in the ON position, as shown in Figure 8.

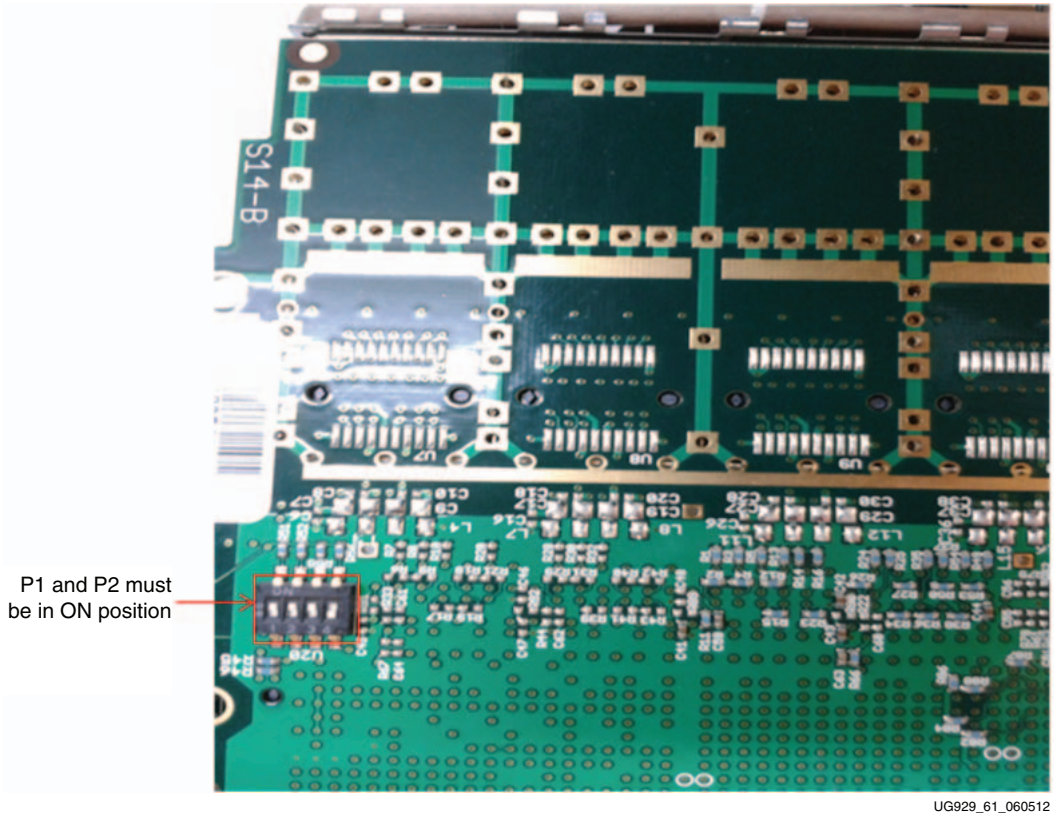

Figure 8: **DIP Switch Position on FMC Card**

2. Insert SFP+ connectors to channel 2 and channel 3 positions as shown in Figure 9.

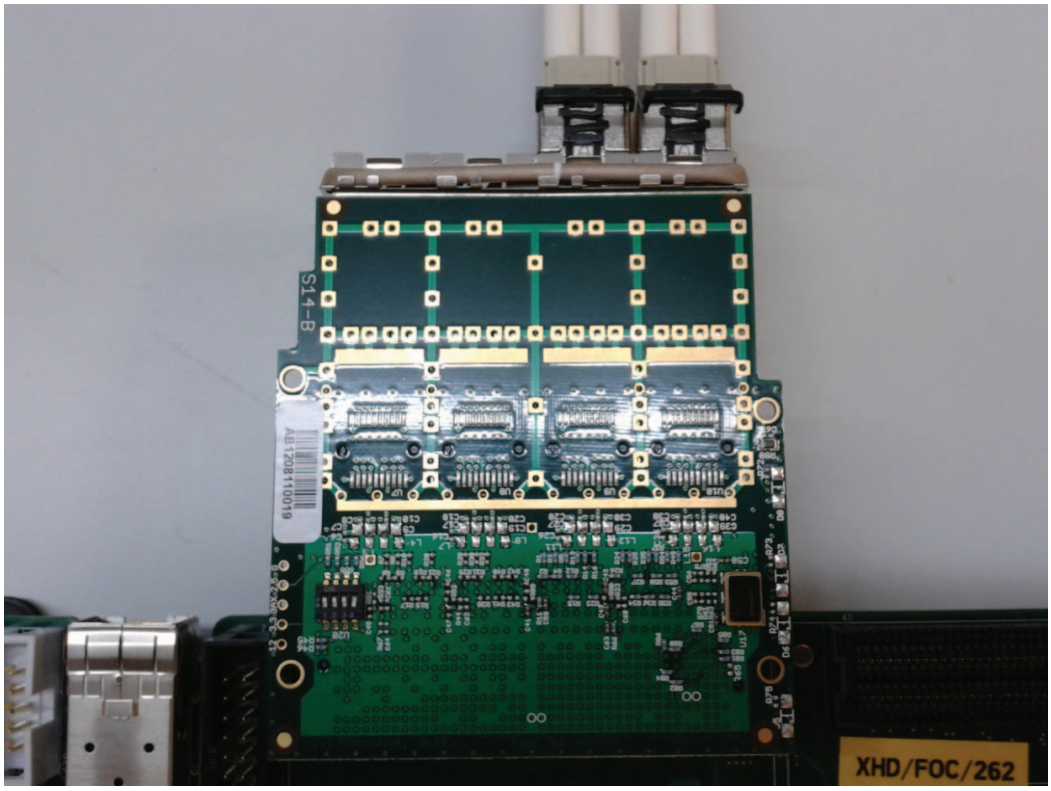

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Figure 9: **SFP+ Connector Position on FMC Card**

3. Insert the FM-S14 FMC card in the HPC slot of the KC705 board as shown in Figure 10. Remove the cap from the fiber optic cables and connect the fiber optic cables in a loopback fashion as shown in the figure.

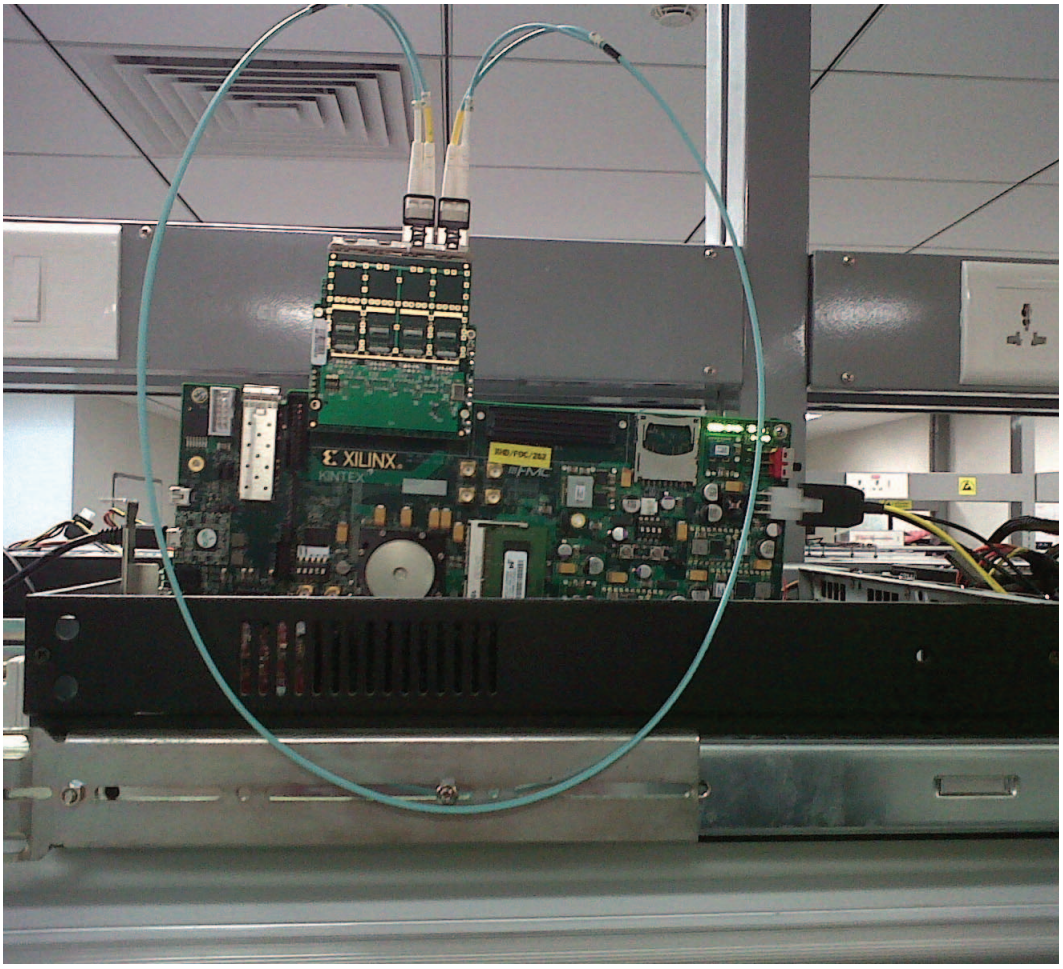


Figure 10: **Setup with Fiber Optic Cable**

4. Connect the 12V ATX power supply 4-pin disk drive type connector to the board. Note that the 6-pin ATX supply cannot be connected directly to the KC705 board and the 6-pin adapter is required.

   Caution! Do NOT plug a PC ATX power supply 6-pin connector into J49 on the KC705 board The ATX 6-pin connector has a different pinout than J49. Connecting an ATX 6-pin connector into J49 will damage the KC705 board and void the board warranty.

5. With the host system powered off, insert the KC705 board in the PCI Express slot through the PCI Express x8 edge connector.
6. Ensure that the connections are secure to avoid loose contact problems. Power on the KC705 board and then the system.
7. The GPIO LEDs are located in the top right corner of the KC705 board. These LED indicators illuminate to provide the following status (LED positions are marked from left to right):

   LED position 1 – DDR3 link up

   LED position 2 – 10GBASE-R link 1 ready

LED position 3 – 10GBASE-R link 2 ready

LED position 4 – 156.25 MHz clock heart beat LED

LED position 5 – PCIe x8 link stable

LED position 6 – PCIe 250 MHz clock

LED position 7 – PCIe link up

LED positions on the KC705 board are shown in Figure 11.

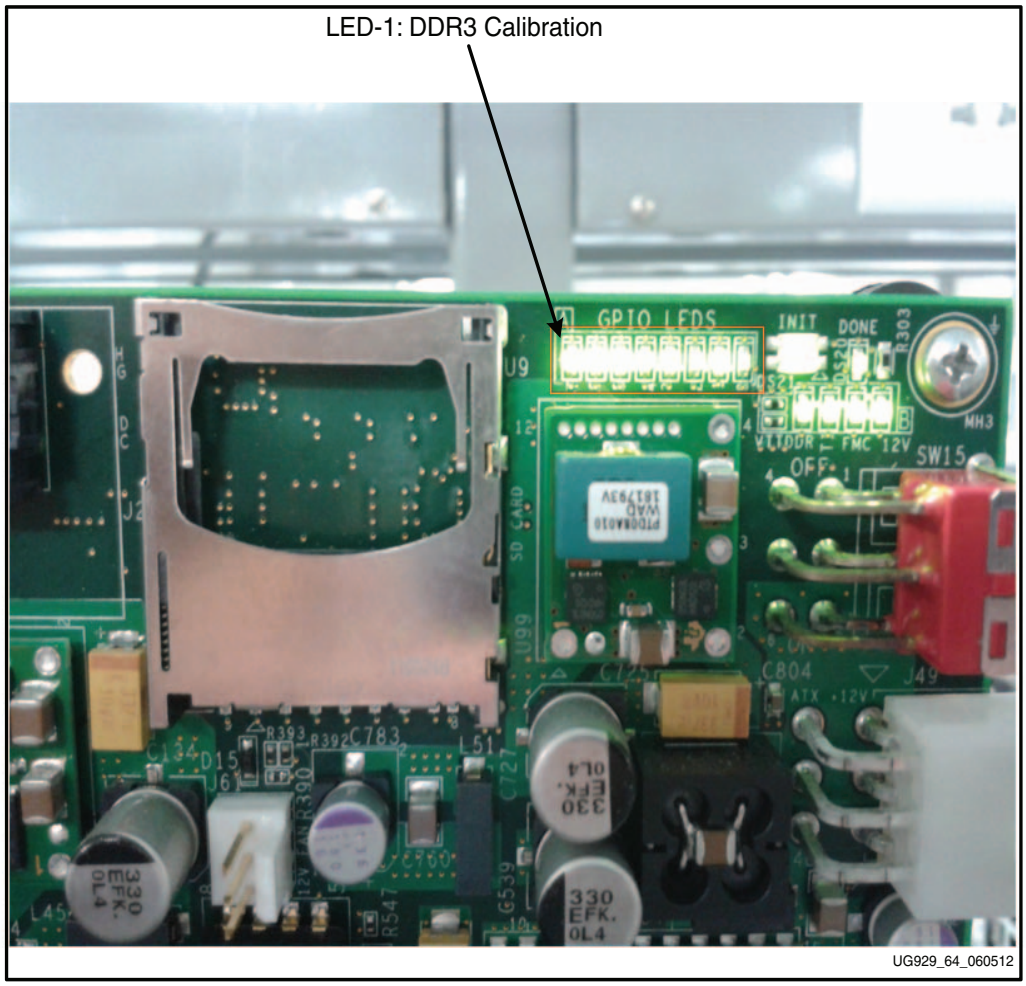


Figure 11: **LED Position on the FMC Card**

8. The LEDs on the FMC card (note that these are on the bottom side) indicate the following status:

   LED position top – FM-S14 is connected on the correct FMC connector on KC705 board

   LED position bottom – indicates clock generator on FMC is programmed to generate 312.5 MHz as required by the TRD

Installing Linux Device Drivers

This sections describes the steps to install the device drivers for the Kintex-7 connectivity TRD after completion of the above hardware setup steps.

1. If Fedora 16 is installed on the PC system's hard disk, boot as a root-privileged user, proceed to step 3. Otherwise continue with step 2.
2. To boot from the Fedora 16 Live DVD provided in the kit, place the DVD in the PC's CD-ROM drive. The Fedora 16 Live Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. The PC boots from the CD-ROM drive and logs into a liveuser account. This account has kernel development root privileges required to install and remove device driver modules.

   Note: Users might have to adjust BIOS boot order settings to ensure that the CD-ROM drive is the first drive in the boot order. To enter the BIOS menu to set the boot order, press the DEL or F2 key when the system is powered on. Set the boot order and save the changes. (The DEL or F2 key is used by most PC systems to enter the BIOS setup. Some PCs might have a different way to enter the BIOS setup.)

   The PC should boot from the CD-ROM drive. The images in Figure 12 are seen on the monitor during boot up. (Booting from the Fedora 16 Live DVD takes few minutes and the user needs to wait for until the Fedora 16 menu pops up on the screen as shown in Figure 12.)

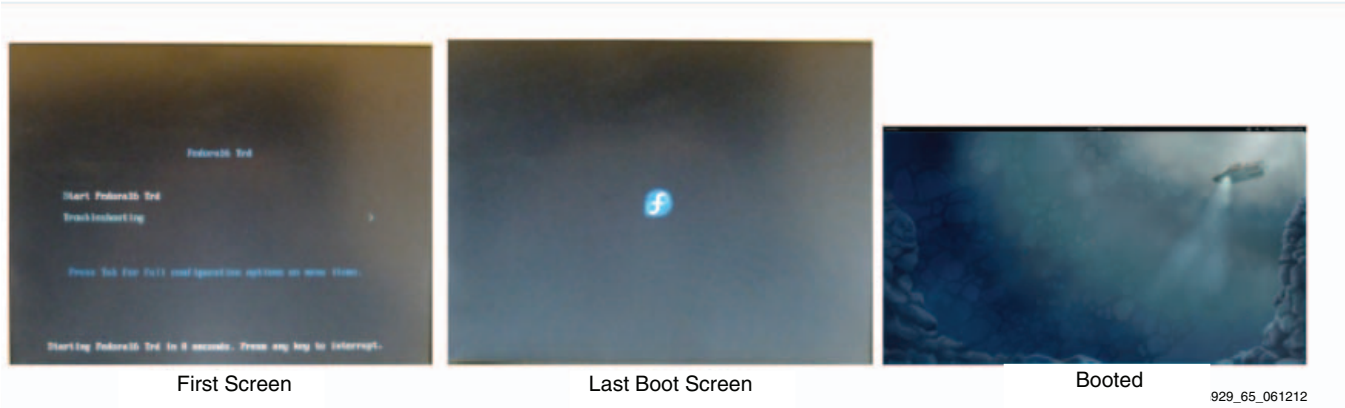


Figure 12: **Fedora 16 LiveCD Boot Sequence**

3. Copy the `k7_connectvity_trd_v1_0` folder to the home directory (or a folder of choice). Note that the user must be a root-privileged user. Connectivity kit design files are available at the Kintex-7 FPGA Connectivity Kit Documentation website.

4. Double-click the copied `k7_connectivity_trd_v1_0` folder. The screen capture in Figure 13 shows the content of the `k7_connectivity_trd_v1_0` folder. The user needs to browse through the "Activities" tab after Fedora 16 boots up to access the "Home" directory.

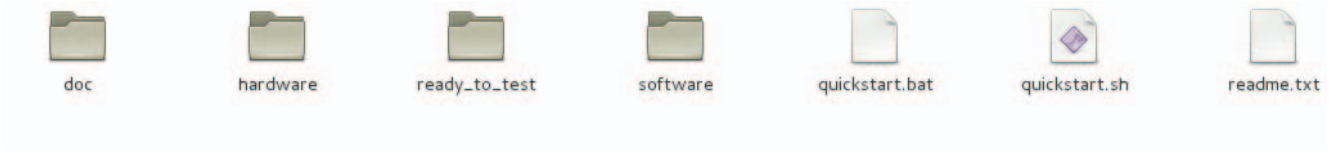


Figure 13: **Directory Structure of k7_connectivity_trd**

5. Ensure that the TRD package has the proper "execute" permission. Double-click `quickstart.sh` script (see Figure 14). This script invokes the driver installation GUI. Click **Run in Terminal**.

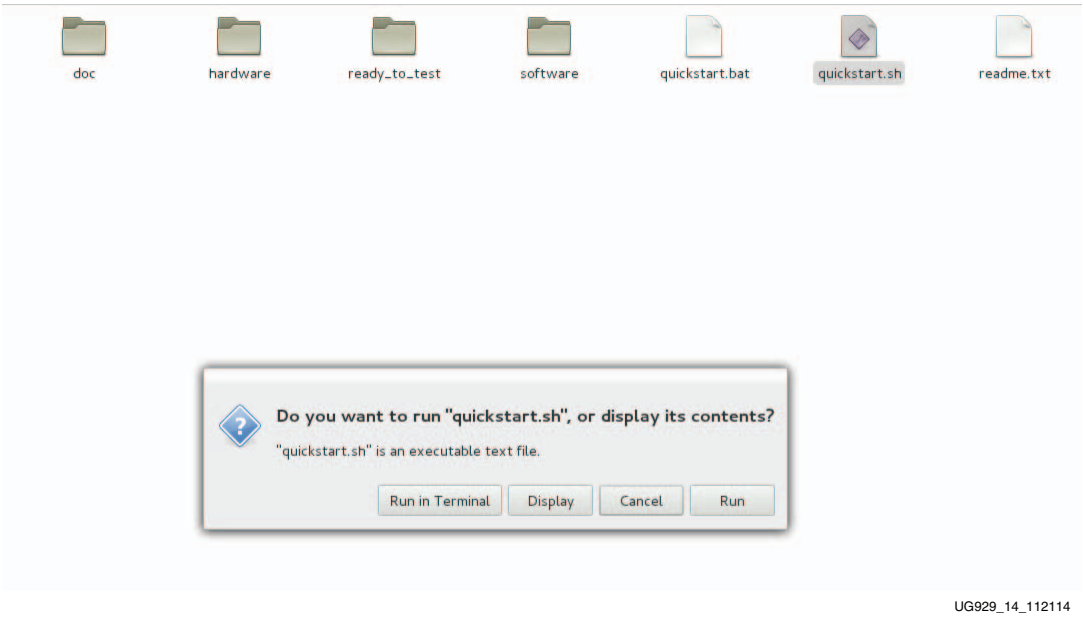


Figure 14: **Running the Quickstart Script**

6. The GUI with driver installation option pops up as shown in Figure 15. The next steps demonstrate all modes of design operation by installing and un-installing various drivers.

   Select **GEN/CHK** performance mode driver mode as shown in Figure 15 and click **Install.**

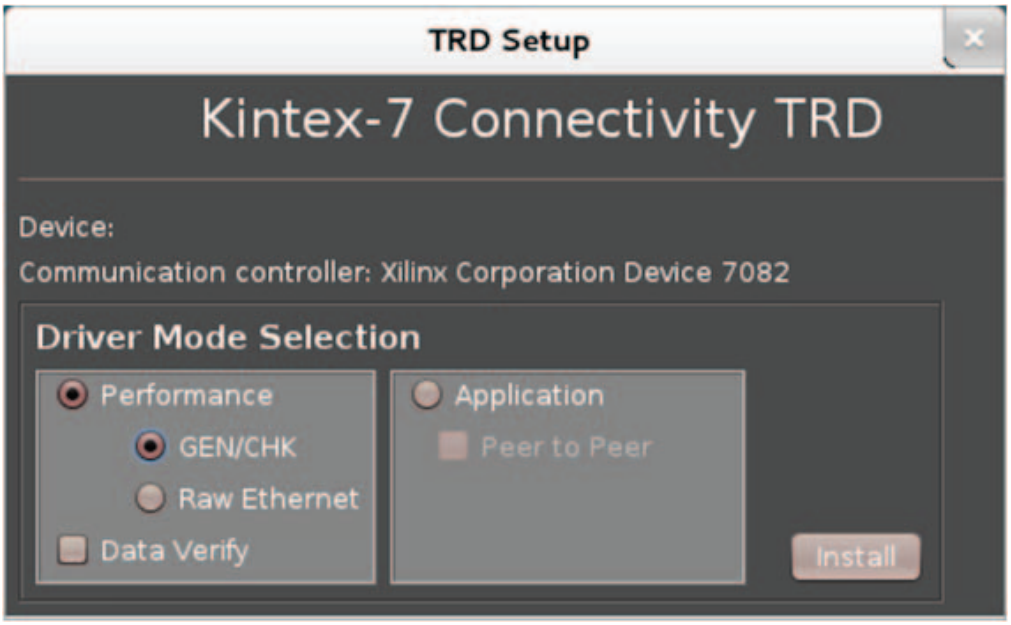


Figure 15: **Landing Page of Kintex-7 Connectivity TRD**

Installing the Windows Device Driver

PC requirements for installing the Windows device drivers:

- Operating System: Windows 7 (32-bit or 64-bit)
- Java installation: Java SE Development Kit 7u5 [Ref 9] and Java SE Runtime Environment 7u5 [Ref 10]
- Hardware Setup, page 15 has been completed

To install the drivers:

1. Restart the computer. During bootup, select **Windows 7** from the boot menu, and press the **F8** key to go to the Advanced Boot Options menu (Figure 16).

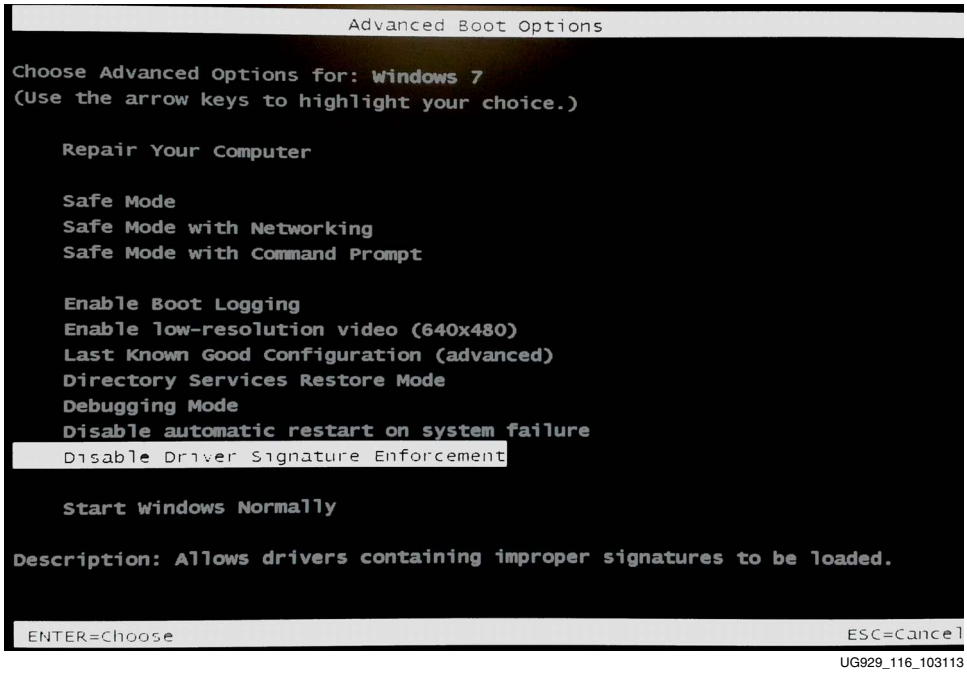


Figure 16: **Windows 7 Advanced Boot Menu**

2. Select **Disable Driver Signature Enforcement** (Figure 16) and press **Enter** to boot Windows.
3. Download `rdf0282-k7-connectivity-trd-2014-3.zip` from the Kintex-7 FPGA Connectivity Kit Documentation website to the desktop (or a folder of choice).
4. Double-click the `rdf0282-k7-connectivity-trd-2014-3.zip` file and unzip and navigate to the `k7_connectivity_trd` folder.
5. Execute the `quickstart.bat` file using administrative privileges by selecting **Run as Administrator** in the right-click menu.

6. When the User Account Control window opens, select **YES** to invoke the InstallShield wizard shown in Figure 17.
7. Click **Next** (Figure 17) to open the Customer Information window (Figure 18).

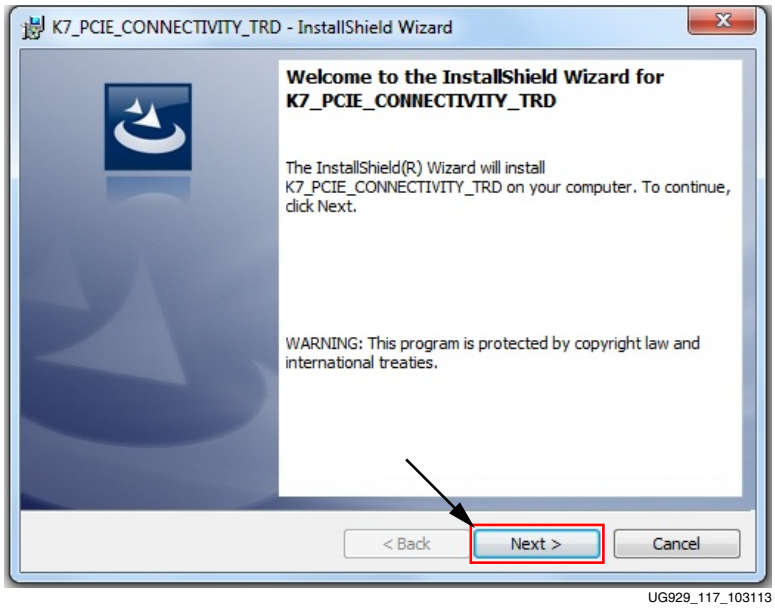


Figure 17: **InstallShield Wizard First Window**

8. Enter your user name and organization. Click **Next** (Figure 18) to open the Destination Folder window (Figure 19).

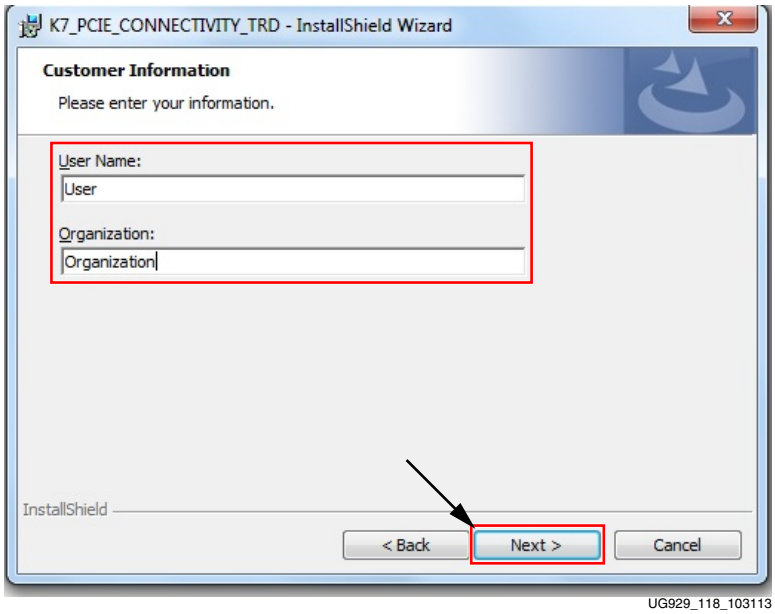


Figure 18: **Customer Information Window**

9. Do one of the following:
   a. Click **Next** (Figure 19) to copy the driver files, Java GUI, user guides, and source files to their default installation locations:
      - `C:\ProgramFiles(x86)\Xilinx\K7_PCIE_CONNECTIVITY_TRD` (for 64-bit machines)
      - `C:\ProgramFiles\Xilinx\K7_PCIE_CONNECTIVITY_TRD` (for x86 machines)
   b. Click **Change...** (Figure 19) to copy the driver files, Java GUI, user guides, and source files to a custom installation directory.

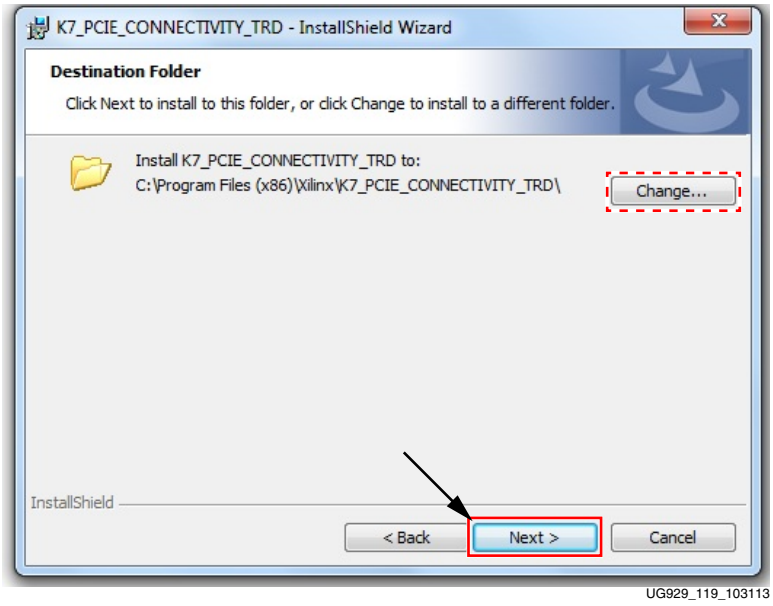


Figure 19: **Destination Folder Window**

10. Click **Install** (Figure 20) to begin installation.

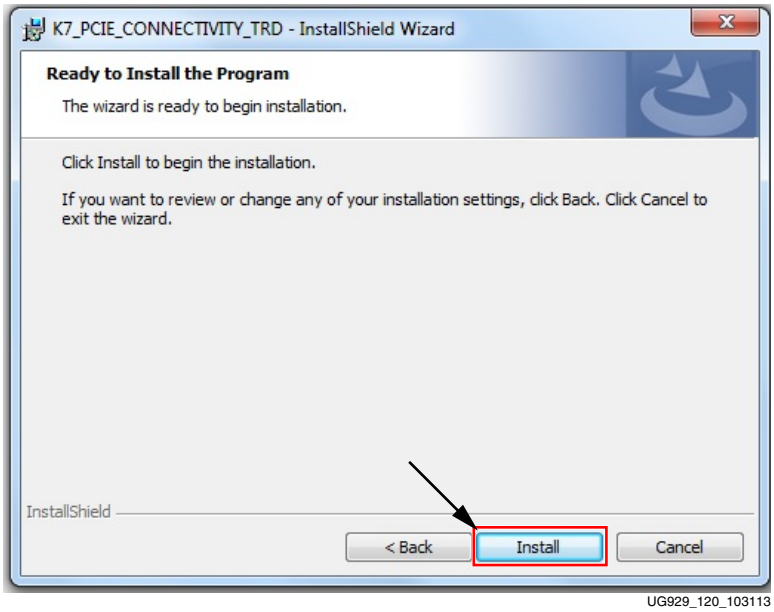


Figure 20: **Install Button**

11. When the Windows Security Window opens, Select **Install this driver software anyway** (Figure 21). This warning is seen because the drivers are unsigned.

Note: This step is repeated two more times because this driver package contains three drivers.

Figure 21: **Windows Security Window**

12. When the installation is complete, Figure 22 is displayed. Click **Finish** to close the wizard.

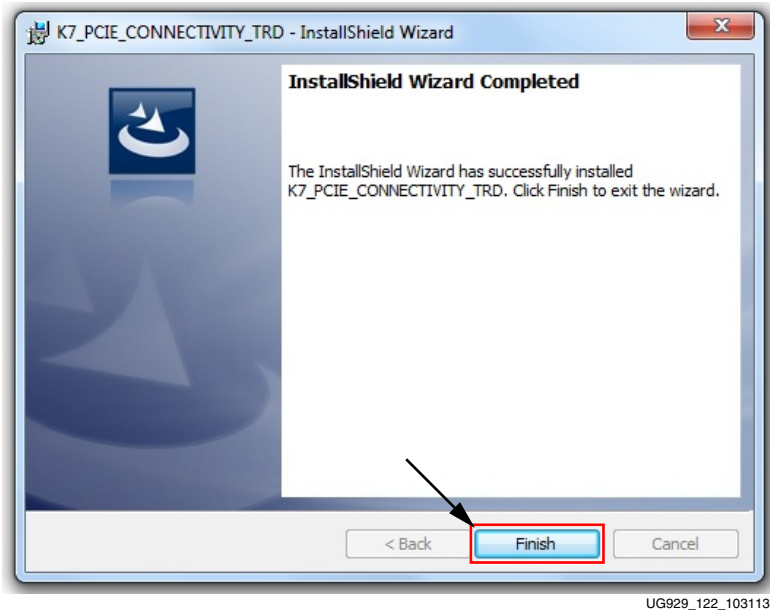


Figure 22: **Finish Button**

Verify Installation

After the installation is successful, verify the installed drivers are properly mapped as described here:

1. Open Device Manager (Figure 23). Click **Start**, click **Control Panel**, and then click **Device Manager**.

2. Right-click on the computer name and select **Scan for hardware changes** (Figure 23).

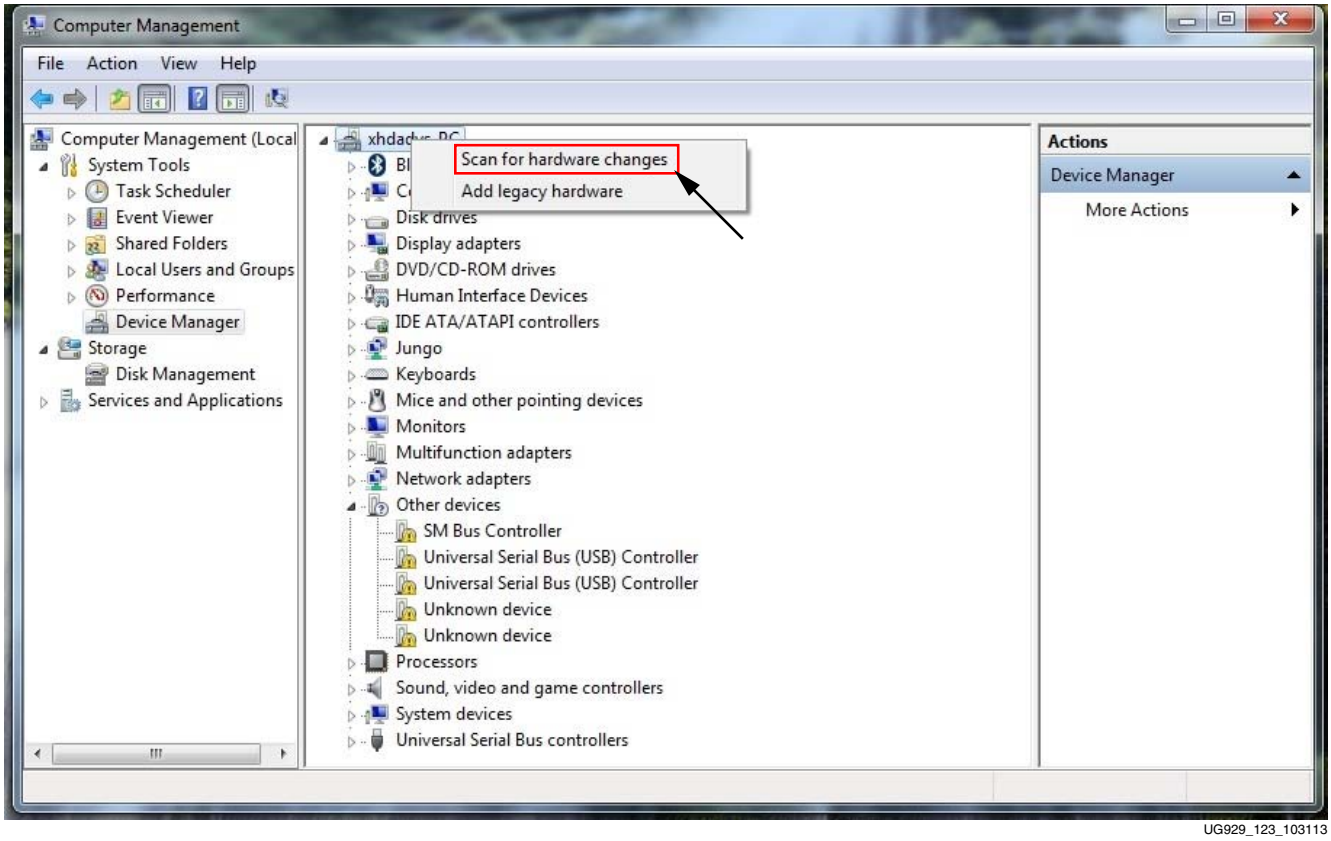


Figure 23: **Initiating Scan for Hardware Changes in Device Manager**

3. Figure 24 shows that the Xilinx devices associated with the design have been detected after the scan.

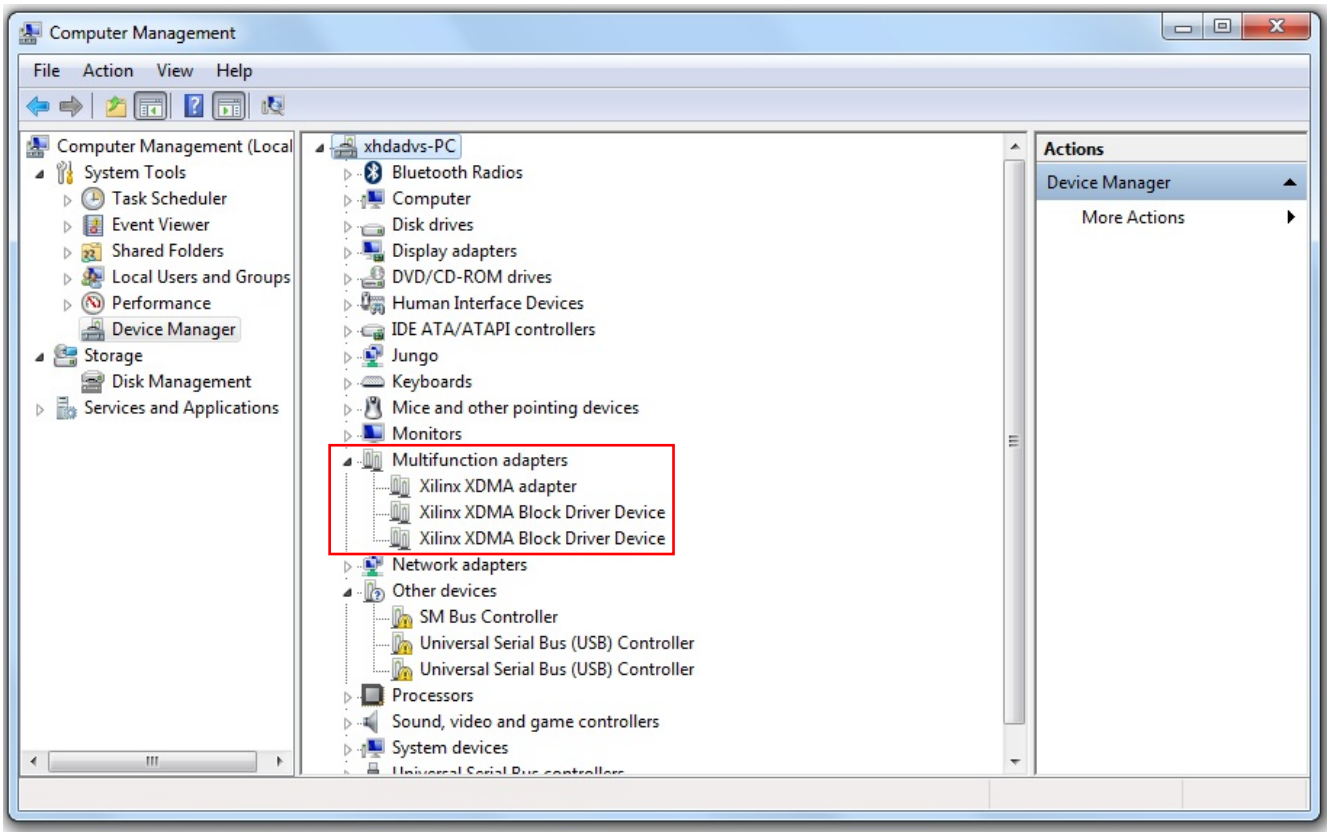


Figure 24: **Xilinx XDMA Adapter and Two Block Driver Devices are Detected**

4. Open a command terminal with administrative privileges. Click **Start**, enter **cmd**, and press **Enter**.
5. Navigate to the installation directory, and then to the `gui` directory. Execute **`rungui.bat`** to invoke the GUI (Figure 25).

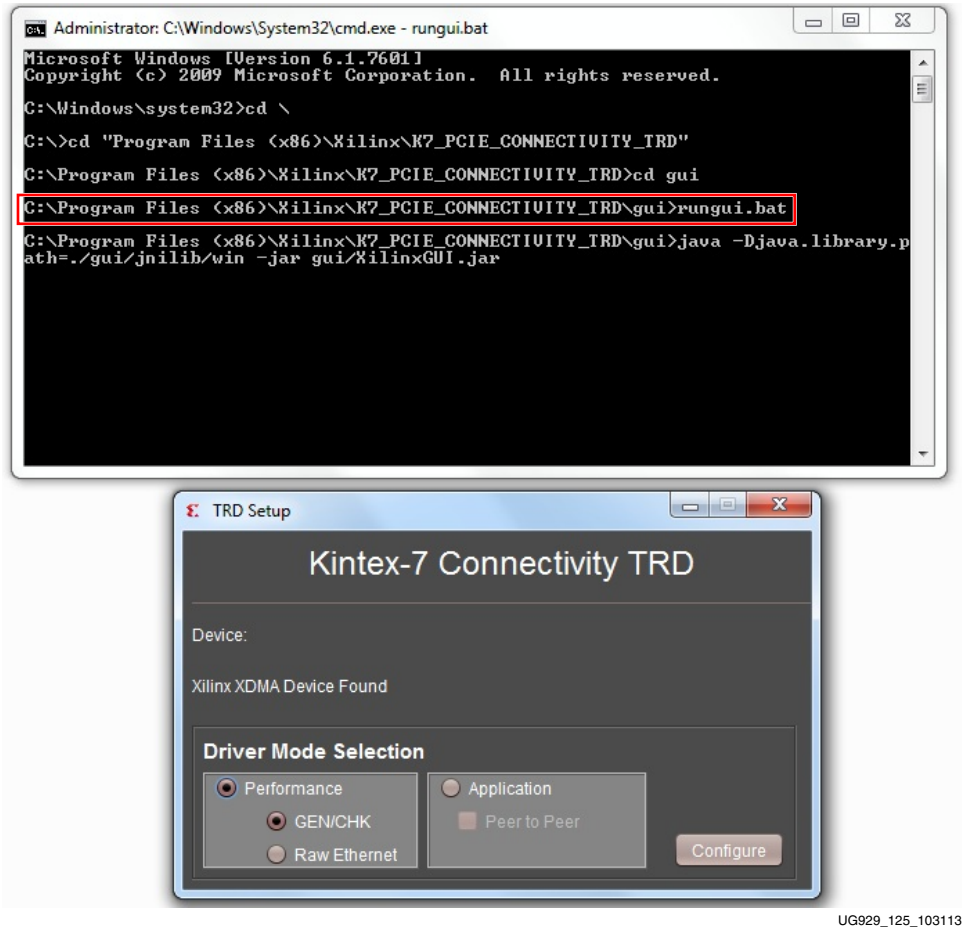


Figure 25: **Invoking the GUI**

6. If **application mode** is selected in the GUI, two new local area networks are displayed in device manager, and the NDIS drivers in place of the Xilinx block drivers (Figure 26).

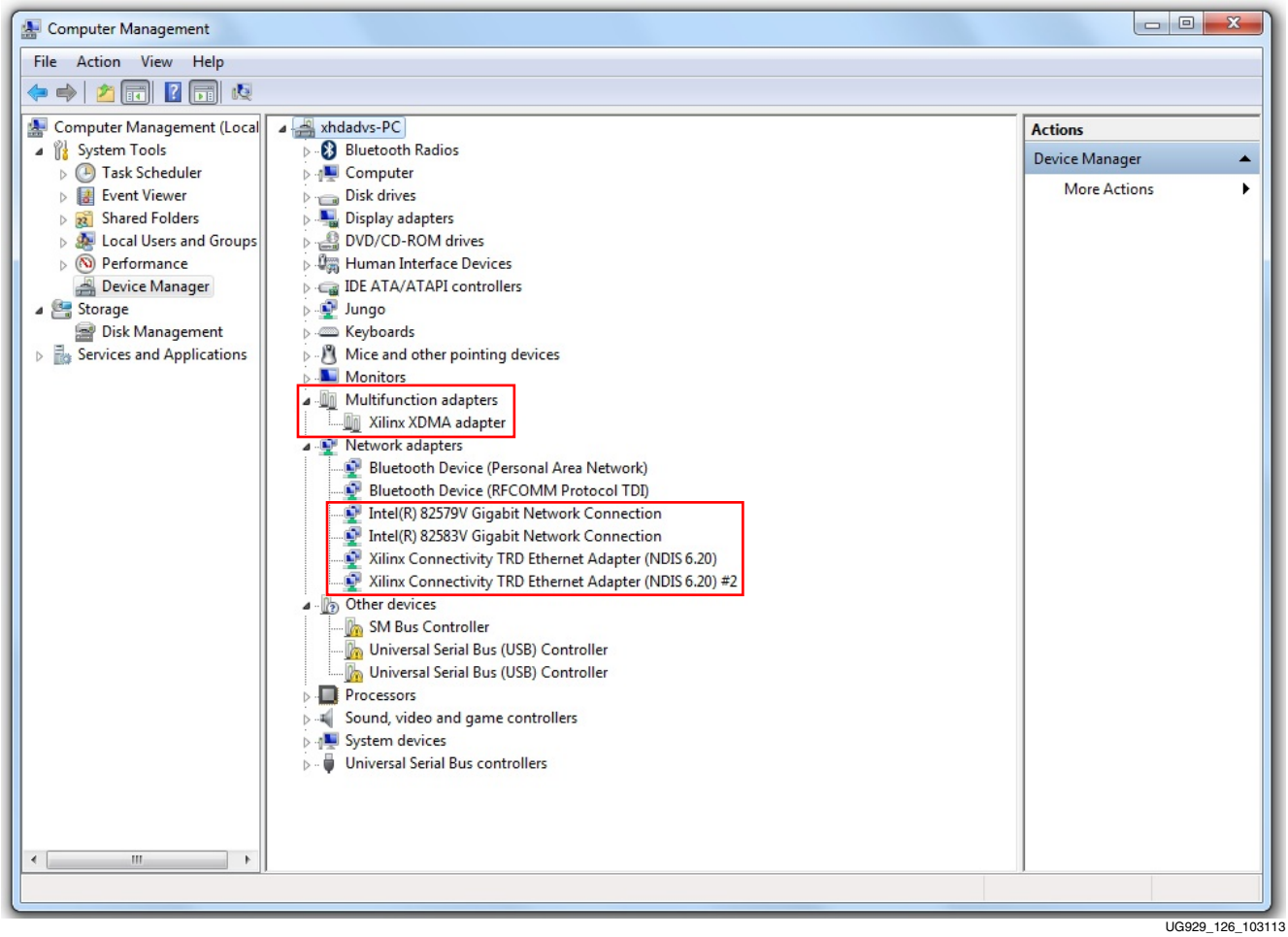


Figure 26: **NDIS 6.20 Ethernet Drivers for the KC705 Design**

GEN/CHK Performance Mode

1. After installing the GEN/CHK performance mode driver, the control and monitor user interface pops up as shown in Figure 27. The control pane shows control parameters such as test mode (loopback, generator, or checker) and packet length. The user can select PCIe link width and speed while running a test if the host machine supports link width and speed configuration capability. The System Monitor tab in the GUI also shows system power and temperature. DDR3 ready status and 10GBASE-R link status are displayed on the top left corner of the GUI.

UG929_69_121712

Figure 27: **GEN/CHK Performance Mode**

2. Click **Start** on both Data Path-0 and Data Path-1. Go to the Performance Plots tab. The Performance Plots tab shows the system-to-card and card-to-system performance numbers for a specific packet size. The user can vary packet size and see performance variation accordingly (see Figure 28).

Figure 28: **GEN/CHK Performance Mode Plots**

3. Close the GUI. A pop up message asks whether you want to un-install the drivers. Click on **Yes**. This process opens the landing page of the Kintex-7 Connectivity TRD. (Driver un-installation requires the GUI to be closed first.)
4. Select **Raw Ethernet** performance as shown in Figure 29. Click **Install**.

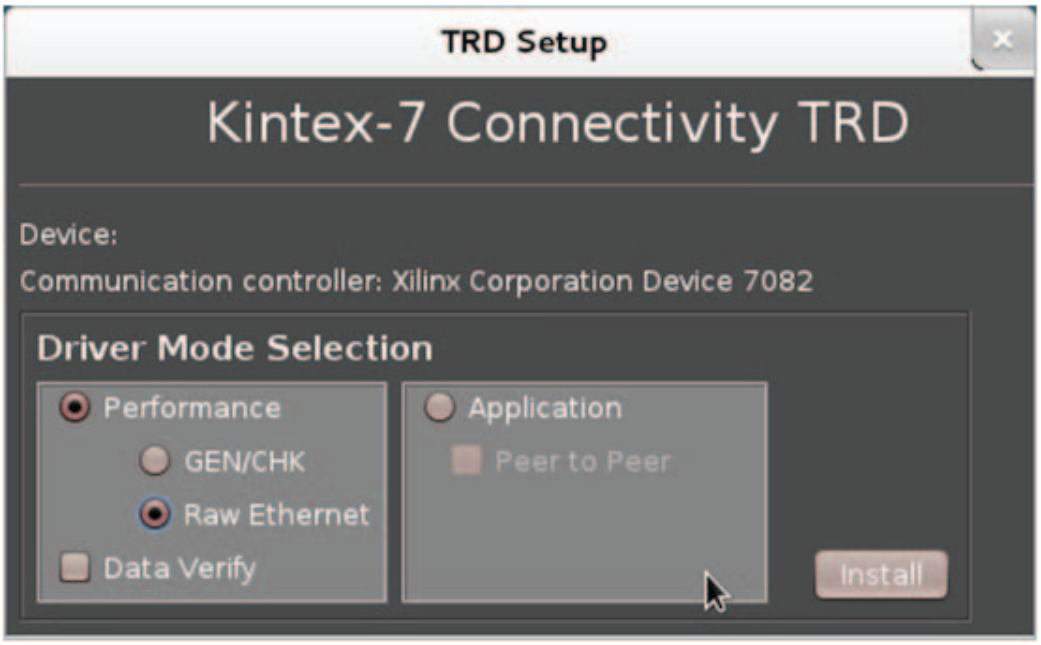


Figure 29: **Raw Ethernet Driver Installation**

5. The GUI for raw Ethernet mode driver is invoked. The user can configure packet size in raw Ethernet mode and can control PCIe link width and speed change if the host machine supports this. The System Monitor tab monitors system power and temperature (see Figure 30).

UG929_72_121712

Figure 30: **Raw Ethernet Driver GUI**

6. Click **Start** on both Data Path-0 and Data Path-1. Navigate to the Performance Plots tab to see performance on system-to-card and card-to-system (see Figure 31).

Figure 31: **Raw Ethernet Driver Performance Plots**

7. Close the GUI. This un-installs driver and opens the Kintex-7 connectivity TRD landing page. Note that driver un-installation requires the GUI to be closed first.
8. Select the Application mode driver as shown in Figure 32. For using the peer to peer option, refer to Appendix 8 of *Kintex-7 FPGA Connectivity Targeted Reference Design User Guide (Vivado Design Suite)* (UG927) [Ref 11]. Click **Install**.

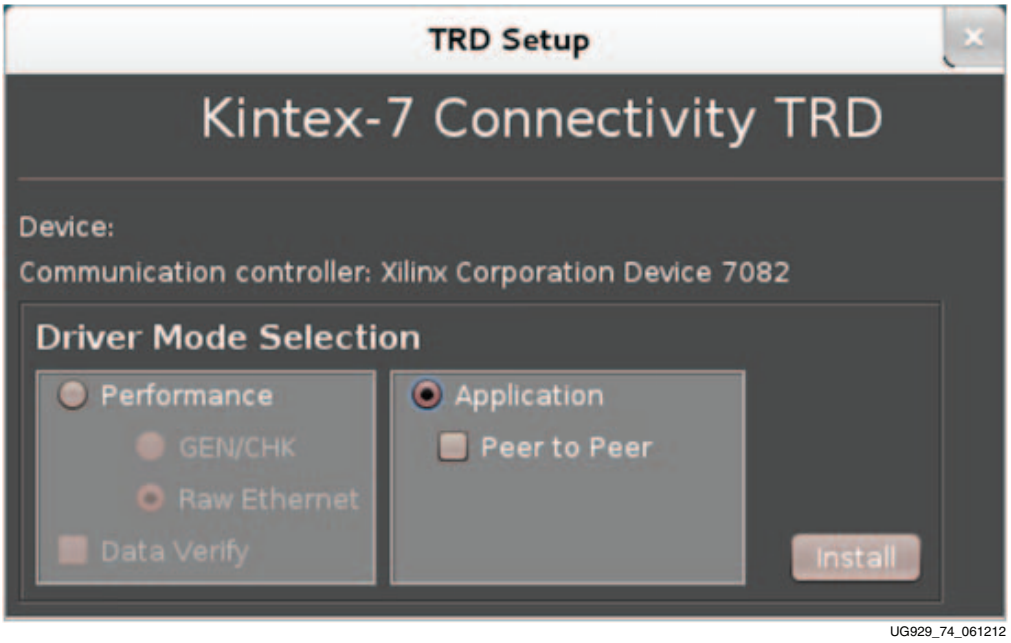
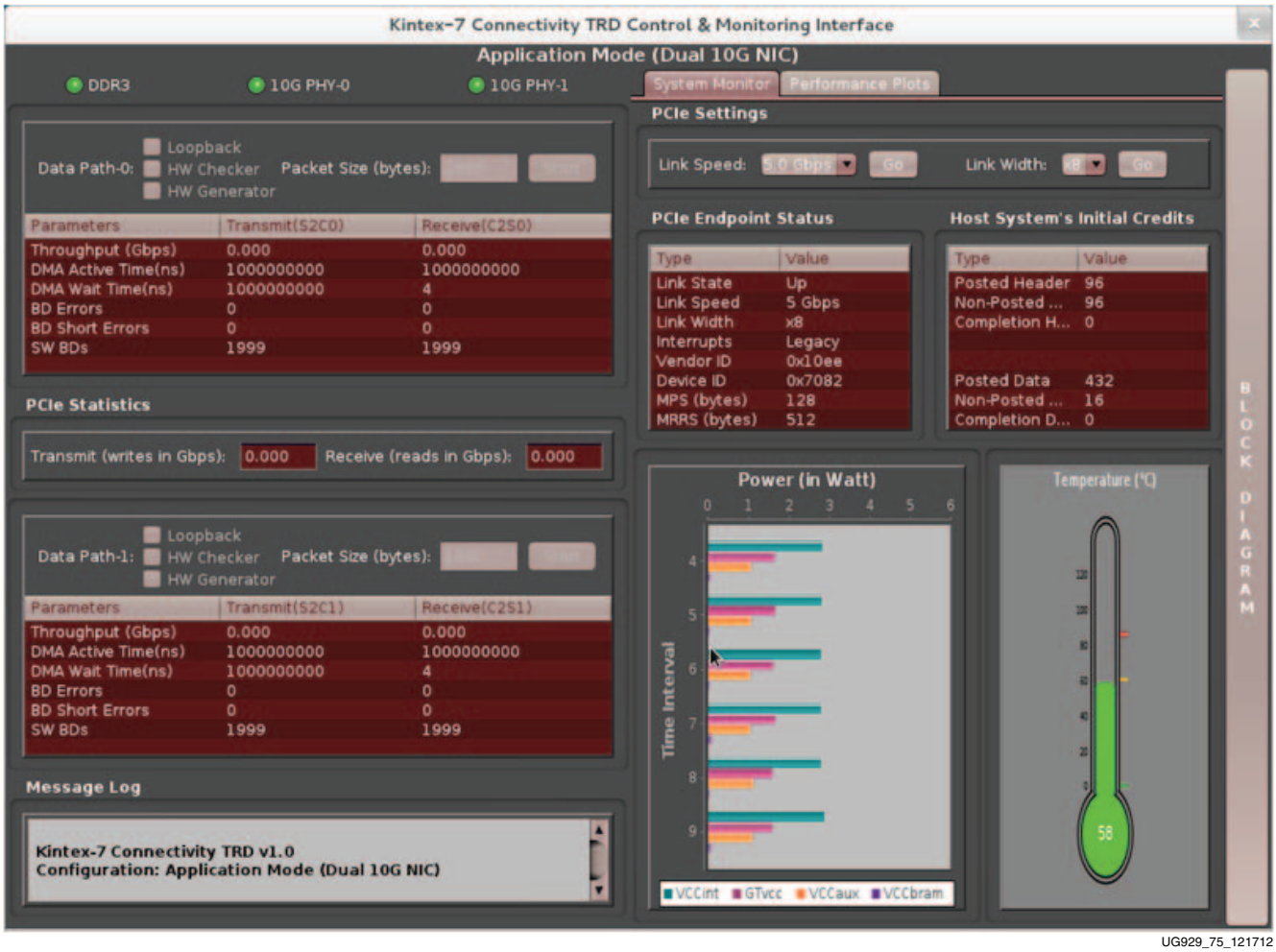


Figure 32: **Application Mode Driver Installation**

9. The GUI is invoked after the driver is installed. However, in application mode, the user cannot start or stop a test – the traffic is generated by the networking stack. The system monitor shows the system power and temperature (see Figure 33).



UG929_75_121712

Figure 33: **Application Mode Driver GUI**

10. Open another terminal on the host machine and run ping (see Figure 34) using the following command:

```
$ ping 10.60.0.1
$ ping 10.60.1.1
```

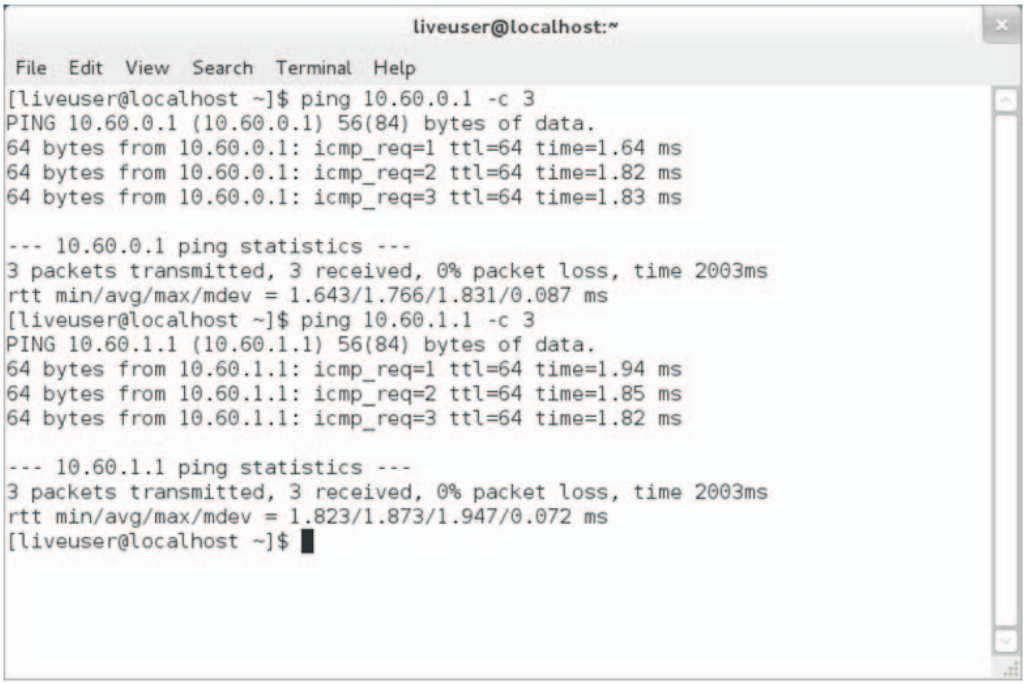


Figure 34: **Ping Application on Application Mode Driver**

Note: In the Windows operating system, only peer to peer mode can be enabled. For enabling peer to peer mode, two PCIe-compatible host PCs are required.

The user can click the Block Diagram option to view the design block diagram as shown in Figure 35.

11. Close the GUI. This un-installs the driver and opens the Kintex-7 connectivity TRD landing page. Note that driver un-installation requires the GUI to be closed first.

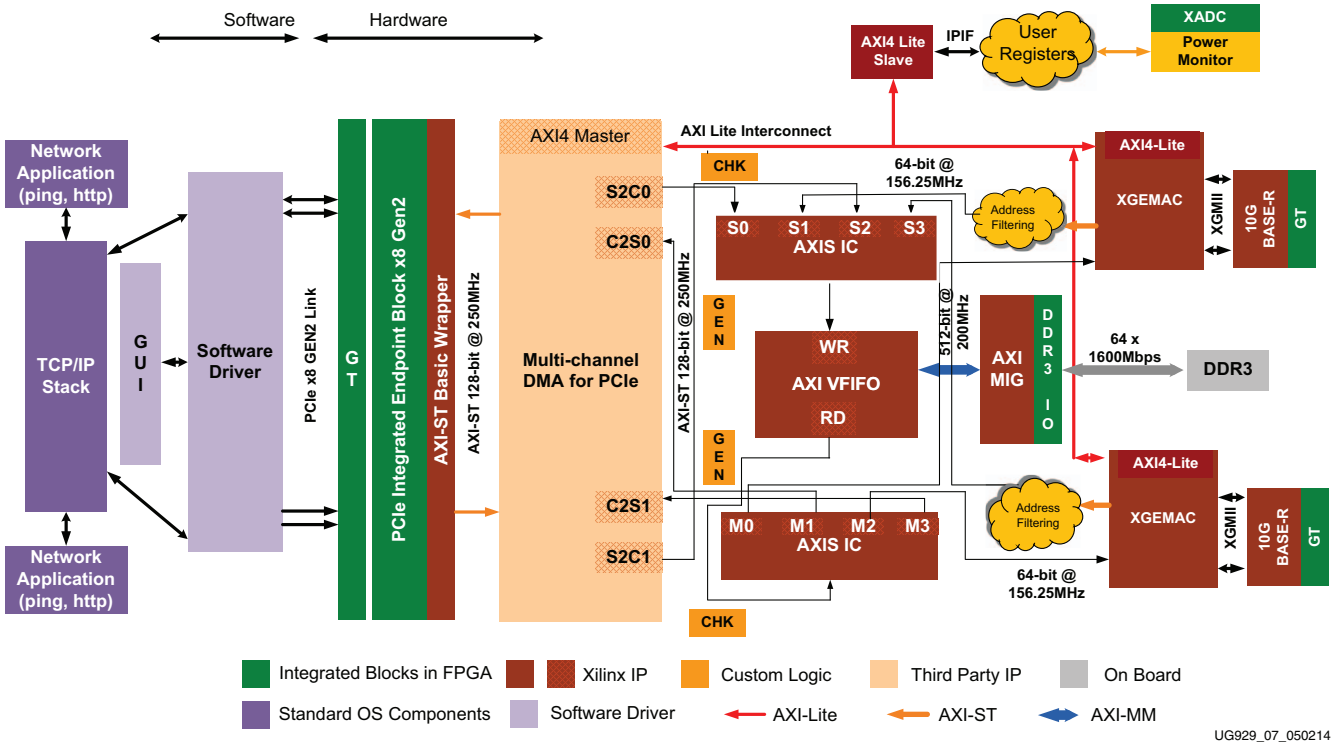


Figure 35: **Design Block Diagram**

Next Steps

With the steps in this getting started guide completed, the user has achieved a simple hardware bring-up of the Kintex-7 connectivity TRD and initial hands-on experience with the connectivity kit.

Users can refer to the *Kintex-7 FPGA Connectivity Targeted Reference Design User Guide (Vivado Design Suite)* (UG927) [Ref 11] to learn how to use this design as a platform to develop their own system.

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Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the Kintex-7 FPGA connectivity kit and its documentation is available on these websites:

Kintex-7 FPGA KC705 Evaluation Kit

Kintex-7 FPGA Connectivity Kit Documentation

Kintex-7 FPGA Connectivity Kit (AR 50555)

These Xilinx documents and sites provide supplemental material useful with this guide:

1. *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810)
2. Ayera Technologies
   TeraTerm Pro Enhanced Telnet/SSH2 Client terminal program
3. Silicon Labs
   CP2103 VCP Drivers
4. Northwest Logic
   PCI Express® Solution IP, including DMA Back-End Core
5. Faster Technology, LLC
   FM-S14 Quad SFP/SFP+ transceiver VITA 57 FMC module
6. Avago Technologies
   AFBR-703SDZ 10 Gb/s Ethernet, 850 nm, 10GBASE-SR, SFP+ Transceiver
7. Amphenol Corporation
   LC-LC Duplex 10 Gb/s Multimode 50/125 OM3 Fiber Optic Patch Cable - 2 x LC Male to 2 x LC Male
8. Fedora Project
   Fedora operating system information and downloads

9. Java SE Development Kit 7u5
10. Java SE Runtime Environment 7u5
11. *Kintex-7 FPGA Connectivity Targeted Reference Design User Guide (Vivado Design Suite)* (UG927)
12. *Vivado Design Suite Migration Methodology Guide* (UG911)
13. *Vivado Design Suite Logic Simulation User Guide* (UG900)
14. *Vivado Design Suite Implementation User Guide* (UG904)
15. *7 Series FPGAs Integrated Block for PCI Express v2.2 Product Guide* (PG054)
16. *Synthesis and Simulation Design Guide* (UG626)
17. *Understanding Performance of PCI Express Systems* (WP350)
18. *7 Series FPGAs GTX Transceivers User Guide* (UG476)
19. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
20. *Kintex-7 FPGA Base Targeted Reference Design Getting Started Guide* (UG883)
21. *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072)
22. *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068)
23. *LogiCORE IP AXI4-Stream Interconnect Product Guide* (PG035)
24. *LogiCORE IP AXI Virtual FIFO Controller Product Guide* (PG038)
25. Xilinx AXI Interconnect IP
    AXI Interconnect IP product page

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Appendix B

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
(i) engineering samples or beta versions of Development Systems (which are provided "AS IS" without warranty); (ii) design defects or errors known as "errata";
(iii) Development Systems procured through unauthorized third parties; and
(iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

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