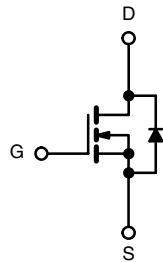
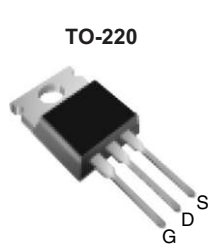


## Power MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	500	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.21
Q <sub>g</sub> (Max.) (nC)	110	
Q <sub>gs</sub> (nC)	33	
Q <sub>gd</sub> (nC)	54	
Configuration	Single	



N-Channel MOSFET

### FEATURES

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low R<sub>DS(on)</sub>
- Compliant to RoHS Directive 2002/95/EC



RoHS\*  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFB20N50KPbF
	SiHFB20N50K-E3
SnPb	IRFB20N50K
	SiHFB20N50K


ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	500	V	
Gate-Source Voltage		V <sub>GS</sub>	± 30		
Continuous Drain Current	V <sub>GS</sub> at 10 V	I <sub>D</sub>	T <sub>C</sub> = 25 °C	20	A
			T <sub>C</sub> = 100 °C	12	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	80		
Linear Derating Factor			2.2	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>		E <sub>AS</sub>	330	mJ	
Repetitive Avalanche Current <sup>a</sup>		I <sub>AR</sub>	20	A	
Repetitive Avalanche Energy <sup>a</sup>		E <sub>AR</sub>	28	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	280	W	
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	10	V/ns	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10		

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- Starting T<sub>J</sub> = 25 °C, L = 1.6 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 20 A.
- I<sub>SD</sub> ≤ 20 A, di/dt ≤ 350 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

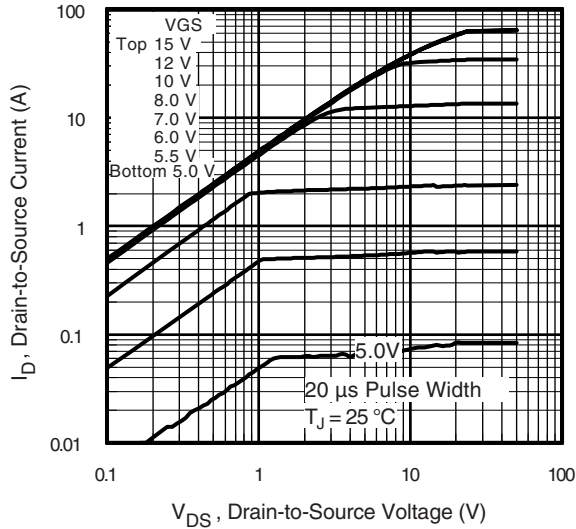
THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	$R_{thJA}$	-	58	°C/W		
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-			
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.45			

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.61	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}^b$	-	0.21	0.25	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 12\text{ A}$	11	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	2870	-	pF
Output Capacitance	$C_{oss}$		-	320	-	
Reverse Transfer Capacitance	$C_{rss}$		-	34	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	3480	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	85	-
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	110	nC
Gate-Source Charge	$Q_{GS}$		-	-	33	
Gate-Drain Charge	$Q_{GD}$		-	-	54	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 20\text{ A}, R_g = 7.5\text{ }\Omega, V_{GS} = 10\text{ V}$ , see fig. 10 <sup>b</sup>	-	22	-	ns
Rise Time	$t_r$		-	74	-	
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	
Fall Time	$t_f$		-	33	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	20	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	80	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 20\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	520	780	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	5.3	8.0	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

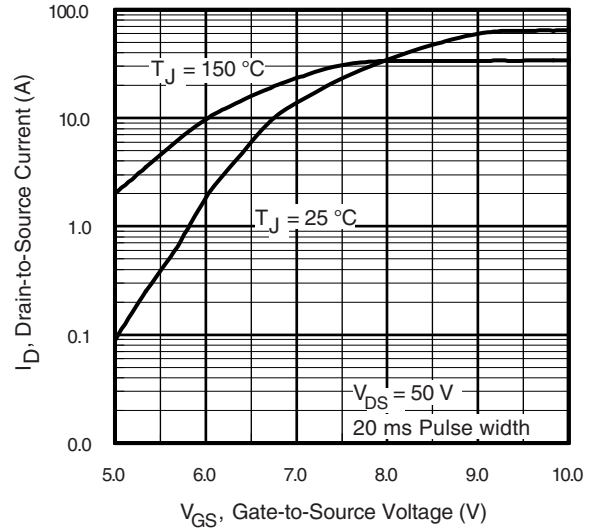
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. Pulse width  $\leq 400\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

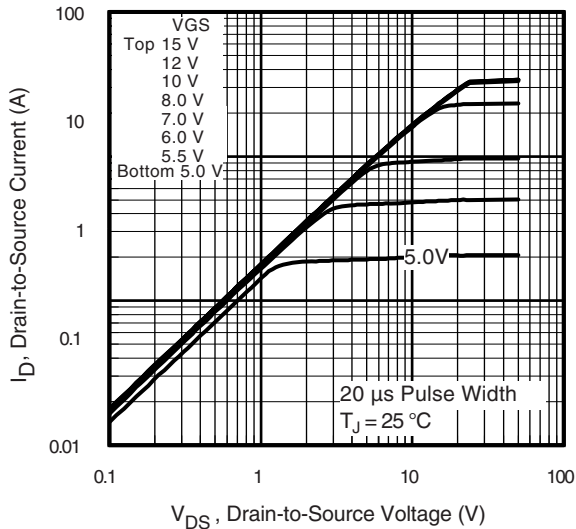
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



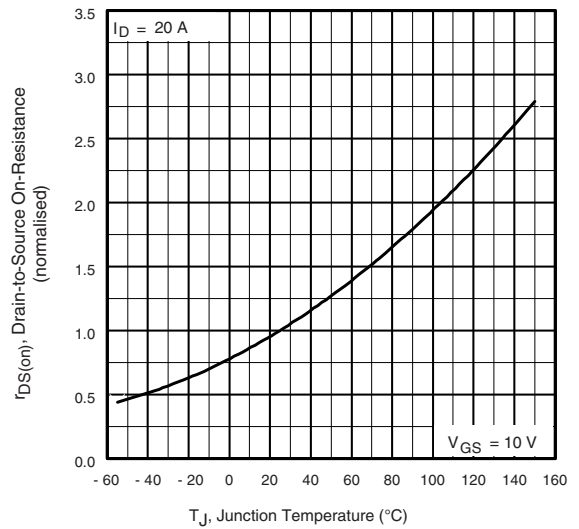
**Fig. 1 - Typical Output Characteristics**



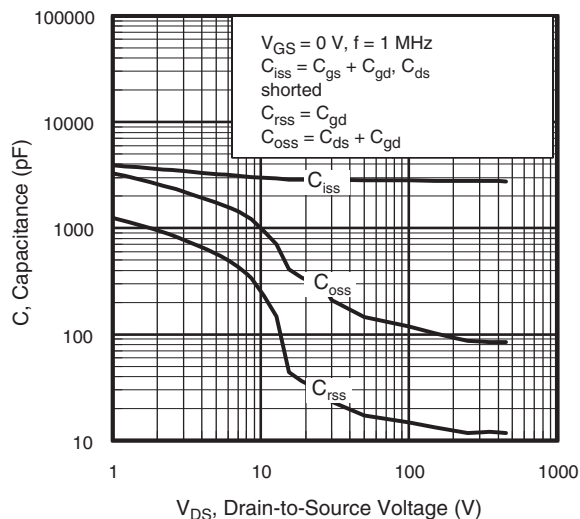
**Fig. 3 - Typical Transfer Characteristics**



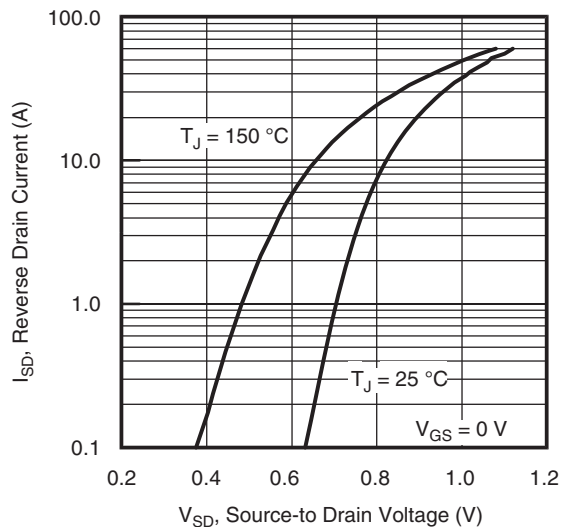
**Fig. 2 - Typical Output Characteristics**



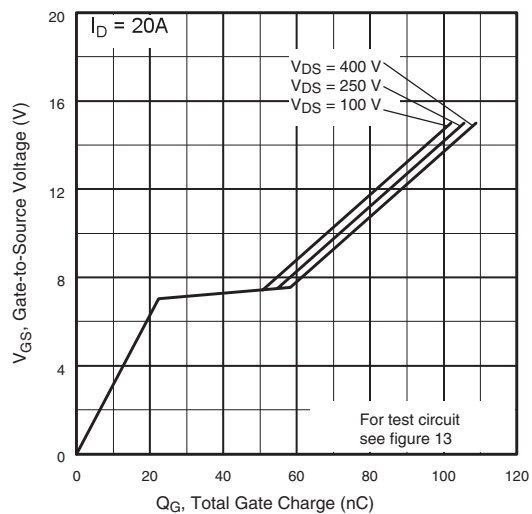
**Fig. 4 - Normalized On-Resistance vs. Temperature**



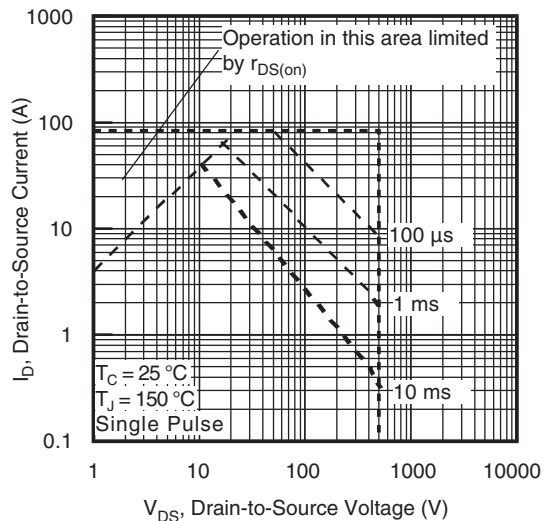
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



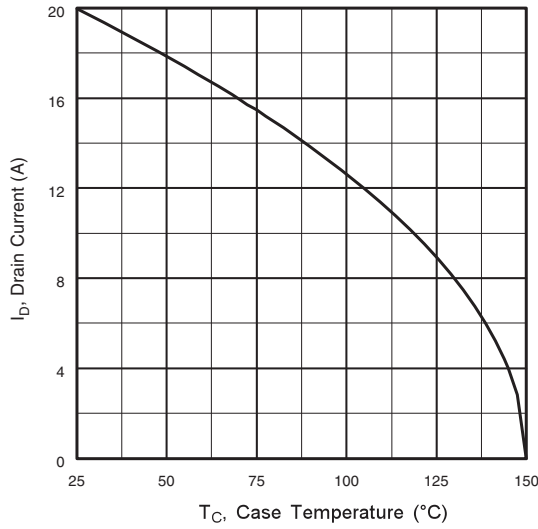
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



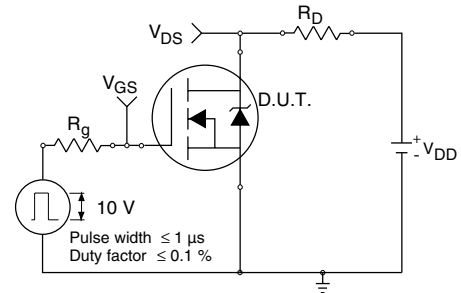
**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



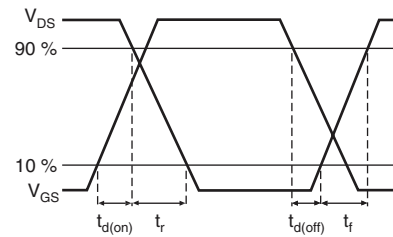
**Fig. 8 - Maximum Safe Operating Area**



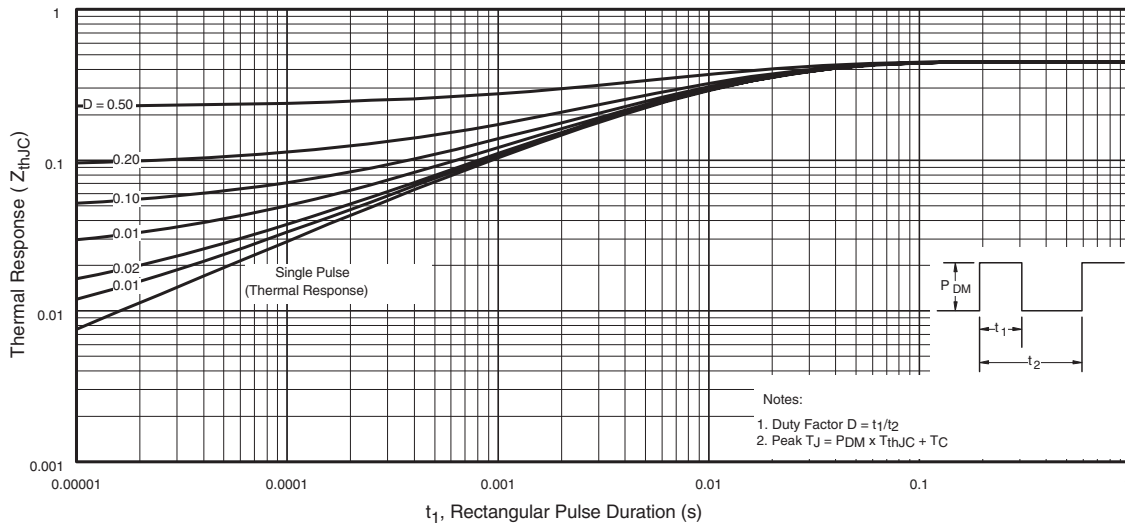
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



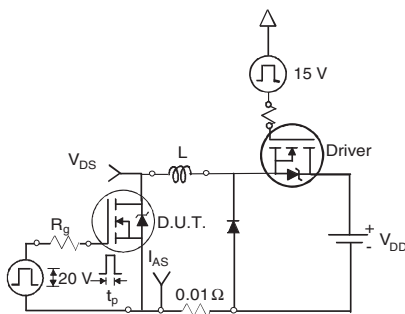
**Fig. 10a - Switching Time Test Circuit**



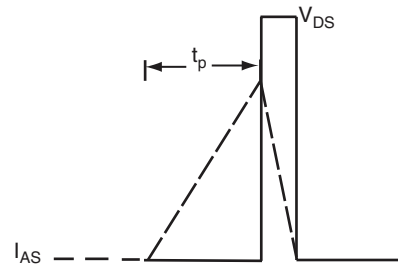
**Fig. 10b - Switching Time Waveforms**



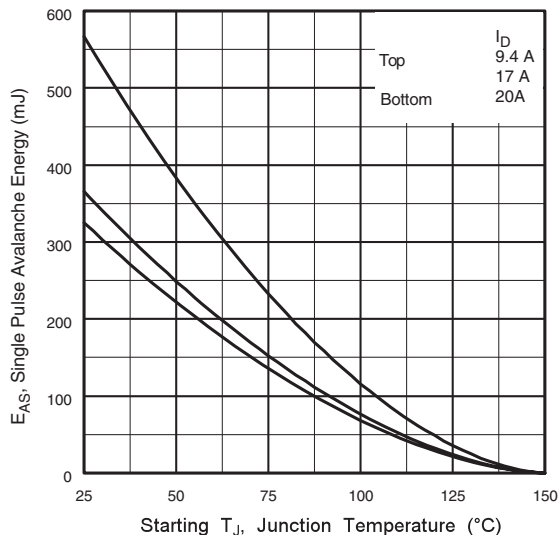
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

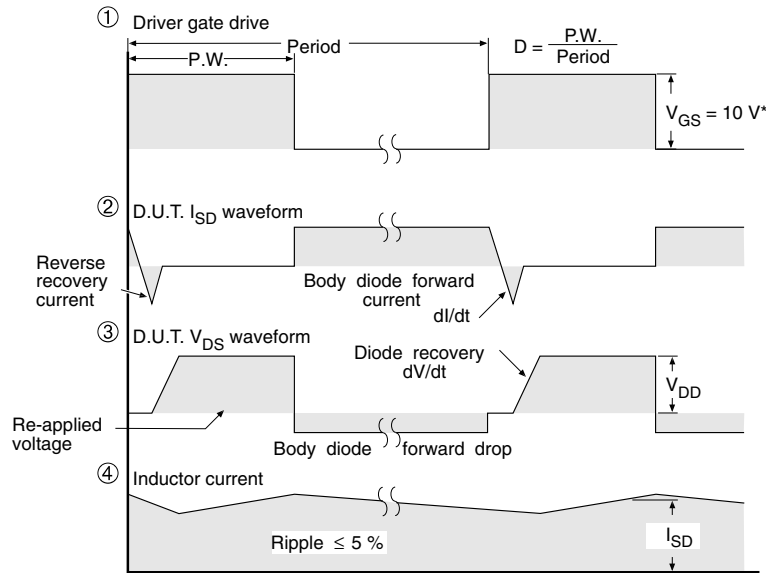
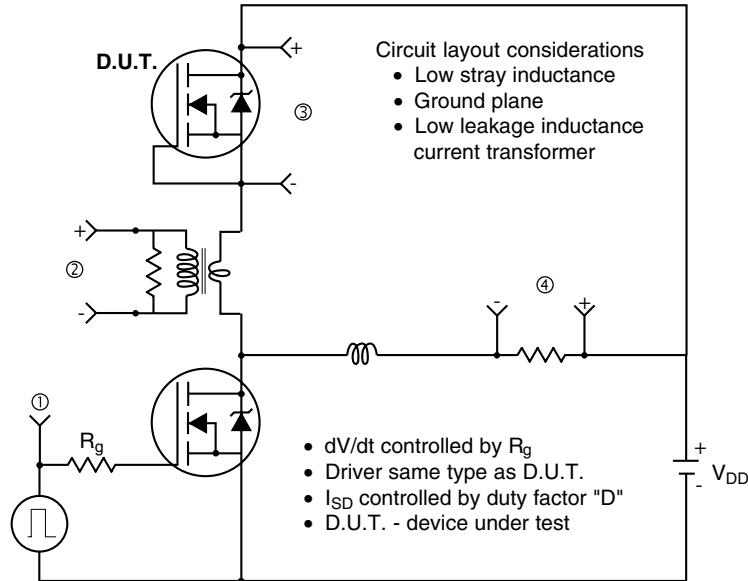


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

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## TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- M\* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM







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