Si53320

1:5 Low Jitter LVPECL Clock Buffer with 2:1 Input Mux

Features

- 5 LVPECL outputs
- Ultra-low additive jitter: 100 fs rms
- Wide frequency range: 1 to 725 MHz
- Input compatible with LVPECL, LVDS, CML, HCSL, LVCMOS
- 2:1 mux
- Glitchless input clock switching
- Synchronous output enable
- 20-TSSOP
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C
- Footprint-compatible with MC100LVEP14, SY100EP14U

Ordering Information:
See page 20.

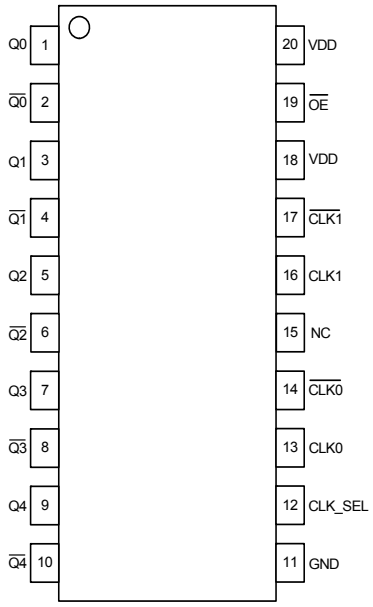
Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Description

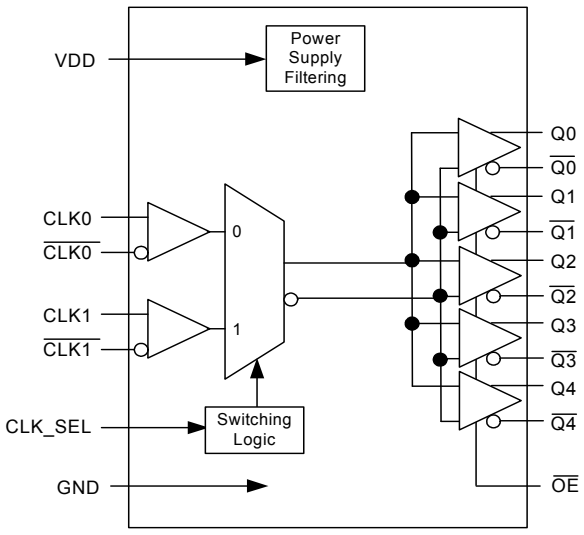
The Si53320 is an ultra low jitter five output LVPECL buffer with synchronous OE. Outputs are enabled/disabled in a low state, ensuring runt pulses are not created when the device is enabled/disabled. The Si53320 features a 2:1 input mux, making it ideal for redundant clocking applications. The Si53320 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53320 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments.

Pin Assignments



Patents pending

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range	V_{DD}		2.38	2.5	2.63	V
			2.97	3.3	3.63	V

Table 2. Input Clock Specifications

(2.5 V ± 5%, or 3.3 V ± 10%, T_A=–40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	0.05	—	—	V
Differential Input Swing (peak-to-peak)	V_{IN}		0.2	—	2.2	V
LVCMOS Input High Voltage	V_{IH}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	V_{DD} x 0.7	—	—	V
LVCMOS Input Low Voltage	V_{IL}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	—	—	V_{DD} x 0.3	V
Input Capacitance	C_{IN}	CLK0/$\overline{\text{CLK0}}$ and CLK1/$\overline{\text{CLK1}}$ pins with respect to GND	—	5	—	pF

Table 3. DC Common Characteristics

(2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}	Includes pull-down current in resistor Rb (see Figure 7)	—	260	—	mA
Input High Voltage	V_{IH}	CLK_SEL/$\overline{\text{OE}}$	0.8 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	CLK_SEL/$\overline{\text{OE}}$	—	—	0.2 x V_{DD}	V
Internal Pull-down Resistor	R_{DOWN}	CLK_SEL/$\overline{\text{OE}}$	—	25	—	kΩ

Table 4. Output Characteristics (LVPECL)

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	V_{COM}		V_{DD} – 1.595	—	V_{DD} – 1.245	V
Single-Ended Output Swing*	V_{SE}		0.55	0.80	1.050	V
***Note:** Unused outputs can be left floating. Do not short unused outputs to ground.						

Table 5. AC Characteristics

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL	1	—	725	MHz
Duty Cycle (50% input duty cycle)	D_C	20/80% T_R/T_F<10% of period (Differential)	48	50	52	%
Minimum Input Clock Slew Rate	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	20/80%	—	—	350	ps
Minimum Input Pulse Width	T_W		500	—	—	ps
Propagation Delay	T_{PLH}, T_{PHL}		700	950	1200	ps
Output Enable Time	T_{EN}	F = 1 MHz	—	1500	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	10	—	ns
Output Disable Time	T_{DIS}	F = 1 MHz	—	2000	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	10	—	ns
Output to Output Skew[1]	T_{SK}		—	60	90	ps
Part to Part Skew[2]	T_{PS}	Differential	—	—	150	ps

Notes:

1. Output-to-output skew specified for outputs with identical configuration.
2. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
3. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DD} (3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

Table 5. AC Characteristics (Continued)
(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Noise Rejection[3]	PSRR	10 kHz sinusoidal noise	—	–67.5	—	dBc
		100 kHz sinusoidal noise	—	–62.5	—	dBc
		500 kHz sinusoidal noise	—	–60	—	dBc
		1 MHz sinusoidal noise	—	–55	—	dBc

Notes:
1. Output-to-output skew specified for outputs with identical configuration.
2. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
3. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DD} (3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

Table 6. Additive Jitter, Differential Clock Input

V_{DD}	Input[1,2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (Single-Ended, Peak-to-Peak)	Differential 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	725	Differential	0.15	0.637	LVPECL	45	65
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
2.5	725	Differential	0.15	0.637	LVPECL	45	65
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185

Notes:
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

Table 7. Additive Jitter, Single-Ended Clock Input

V_{DD}	Input[1,2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (single-ended, peak to peak)	SE 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185

Notes:
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

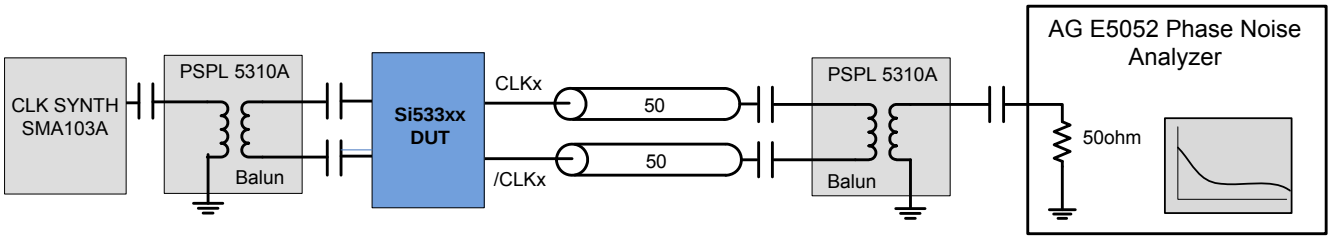


Figure 1. Differential Measurement Method Using a Balun

Table 8. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	93.88	°C/W

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	V_{DD}		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	VDD + 0.3	V
Output Voltage	V_{OUT}		—	—	VDD + 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	2000	—	—	V
ESD Sensitivity	CDM		500	—	—	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53320 is a low jitter, low skew 1:5 differential buffer with an integrated 2:1 input mux. The device has a universal input that accepts most common differential or LVCMOS input signals. A clock select pin is used to select the active input clock. The selected clock input is routed to five high-performance, low-jitter outputs.

2.1. Universal, Any-Format Input

The universal input stage enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 10 and 11 summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended as low slew rates can increased the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

Table 10. LVPECL, LVCMOS, and LVDS Input Clock Options

	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	No	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

Table 11. HCSL and CML Input Clock Options

	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	Yes (3.3 V)	Yes (3.3 V)	Yes	No

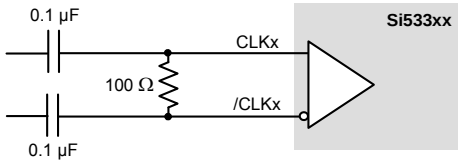


Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination

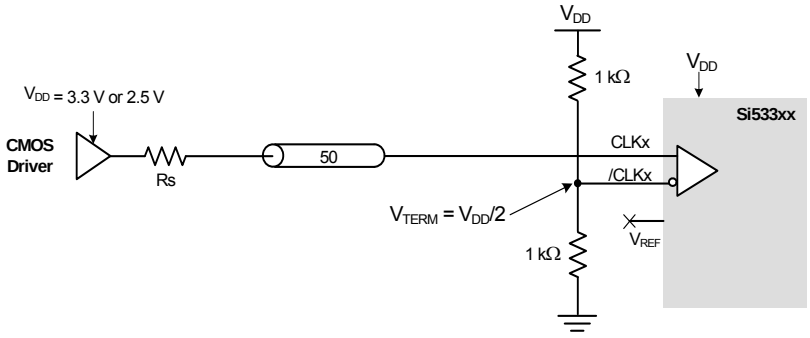
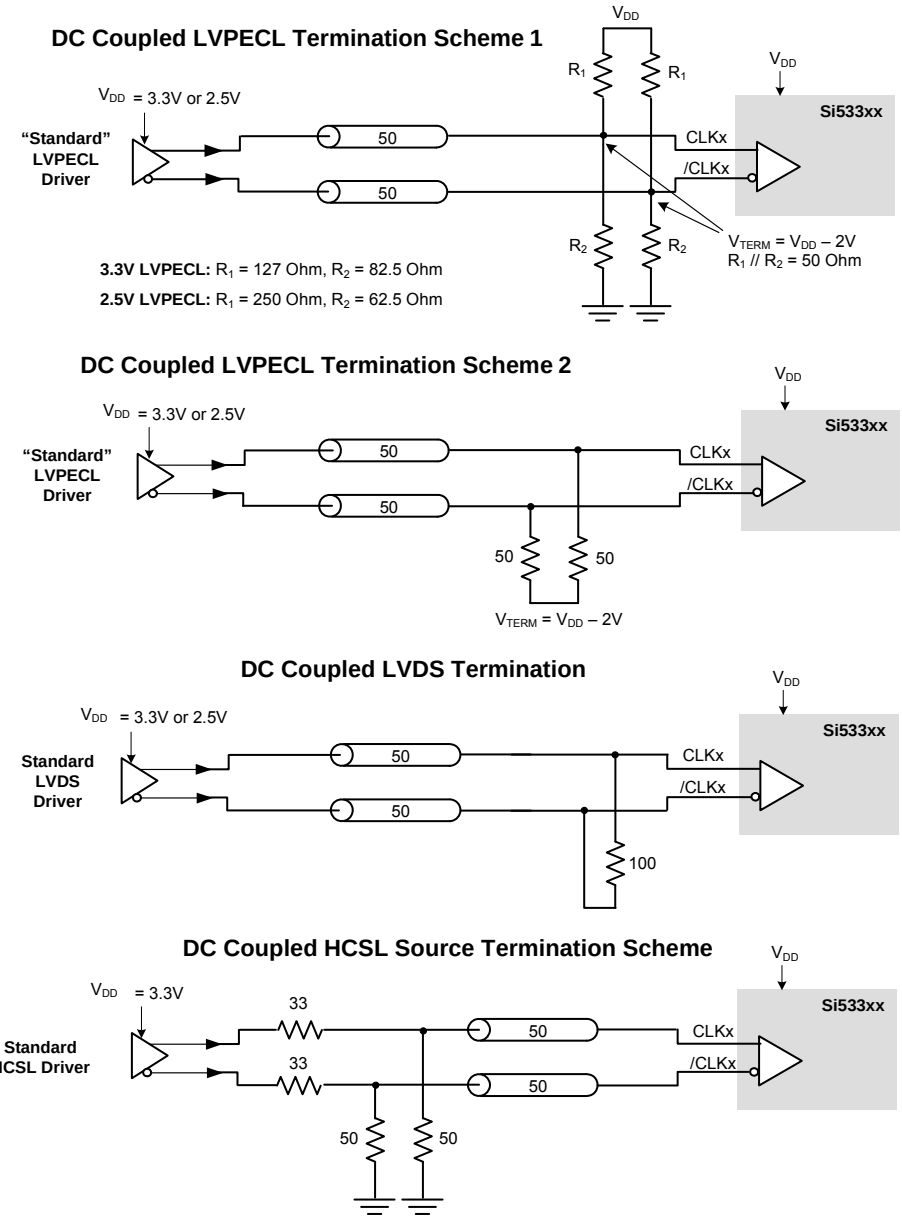


Figure 3. LVCMOS DC-Coupled Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 4. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The non-inverting input is biased with a 18.75 kΩ pull-down to GND and a 75 kΩ pull-up to V_{DD}. The inverting input is biased with a 75 kΩ pull-up to V_{DD}.

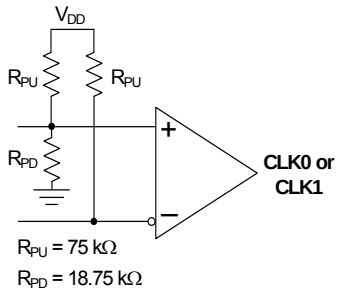
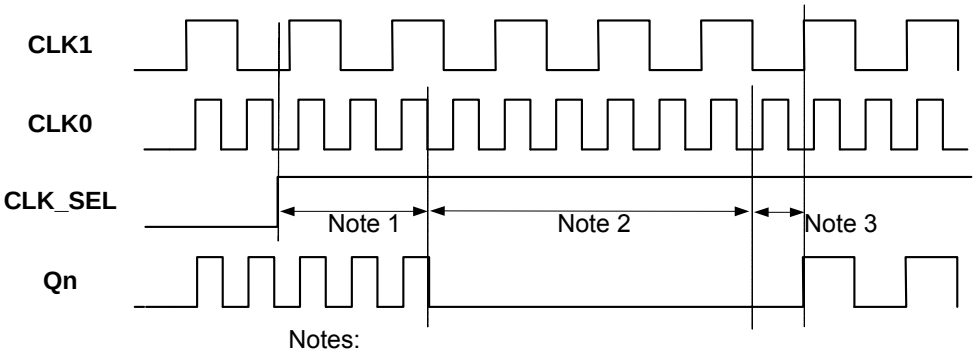


Figure 5. Input Bias Resistors

2.3. Glitchless Clock Input Switching

The Si53320 features glitchless switching between two valid input clocks. Figure 6 illustrates that switching between input clocks does not generate runt pulses or glitches at the output.



Notes:

1. Q_n continues with CLK0 for 2-3 falling edges of CLK0.
2. Q_n is disabled low for 2-3 falling edges of CLK1 .
3. Q_n starts on the first rising edge after 1 + 2.

Figure 6. Glitchless Input Clock Switch

The Si53320 supports glitchless switching between clocks at the same frequency. In addition, the device supports glitchless switching between 2 input clocks that are up to 10x different in frequency. When a switchover to a new clock is made, the output will disable low after two or three clock cycles of the previously-selected input clock. The outputs will remain low for up to three clock cycles of the newly-selected clock, after which the outputs will start from the newly-selected input. In the case a switchover to an absent clock is made, the output will glitchlessly stop low and wait for edges of the newly selected clock. A switchover from an absent clock to a live clock will also be glitchless. Note that the CLK_SEL input should not be toggled faster than 1/250th the frequency of the slower input clock.

2.4. Synchronous Output Enable

The Si53320 features a synchronous output enable (disable) feature. The output enable pin is sampled and synchronized to the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.

When $\overline{OE}$ is high, Q is held low and $\overline{Q}$ is held high. The device features an internal pull-down resistor, so the outputs are enabled when the output enable pin is unconnected. See Table 5, “AC Characteristics,” on page 4 for output enable and output disable times.

2.5. Input Mux and Output Enable Logic

The Si53320 provides two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings.

Table 12. Input Mux and Output Enable Logic

CLK_SEL	CLK0	CLK1	$\overline{OE}$[1]	Q[2]
L	L	X	L	L
L	H	X	L	H
H	X	L	L	L
H	X	H	L	H
X	X	X	H	L[3]

Notes:
1. Output enable active low
2. On the next negative transition of CLK0 or CLK1.
3. Q=low, $\overline{Q}$=high

2.6. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused outputs should be left unconnected.

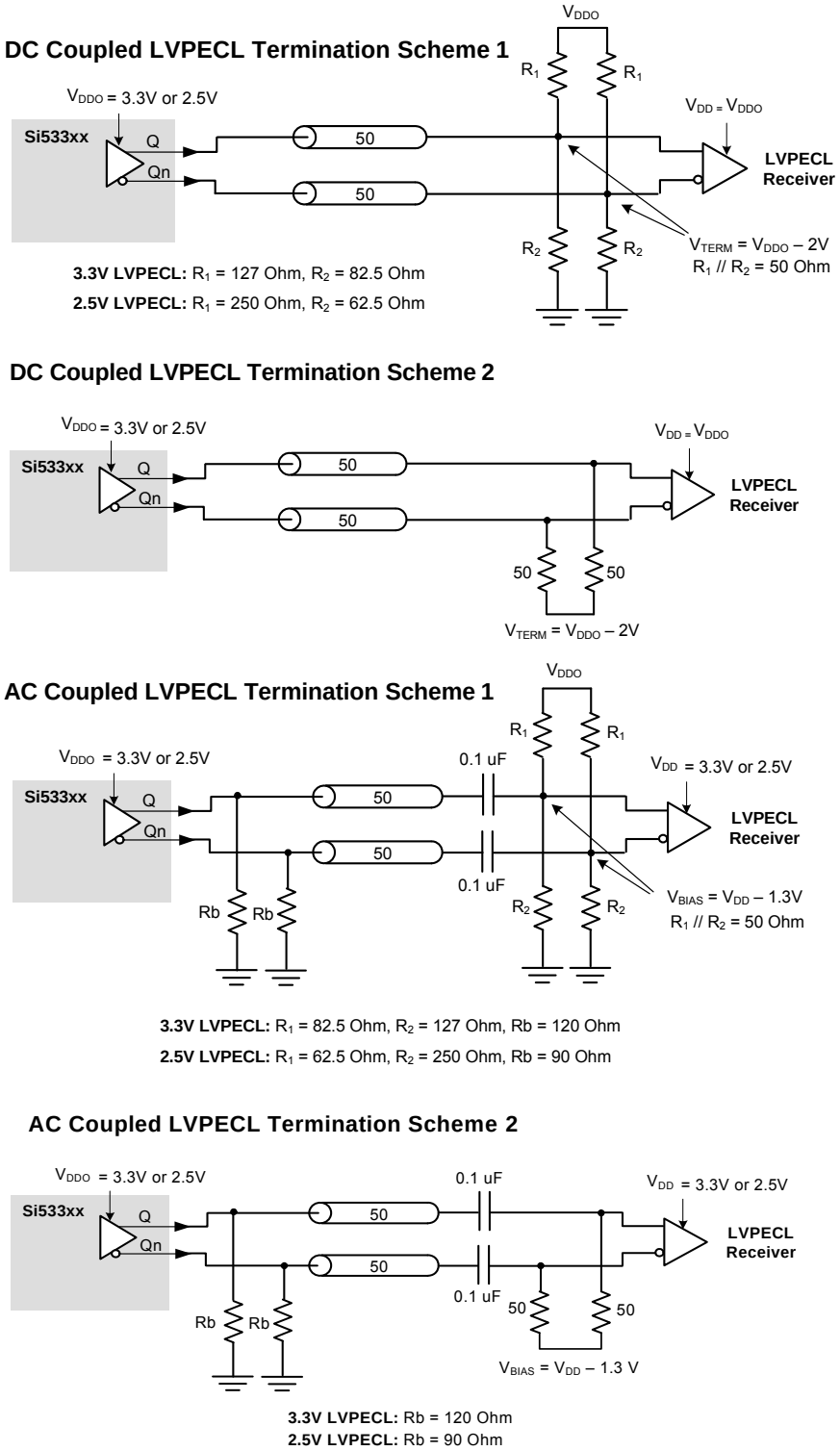


Figure 7. LVPECL Output Termination

2.7. AC Timing Waveforms

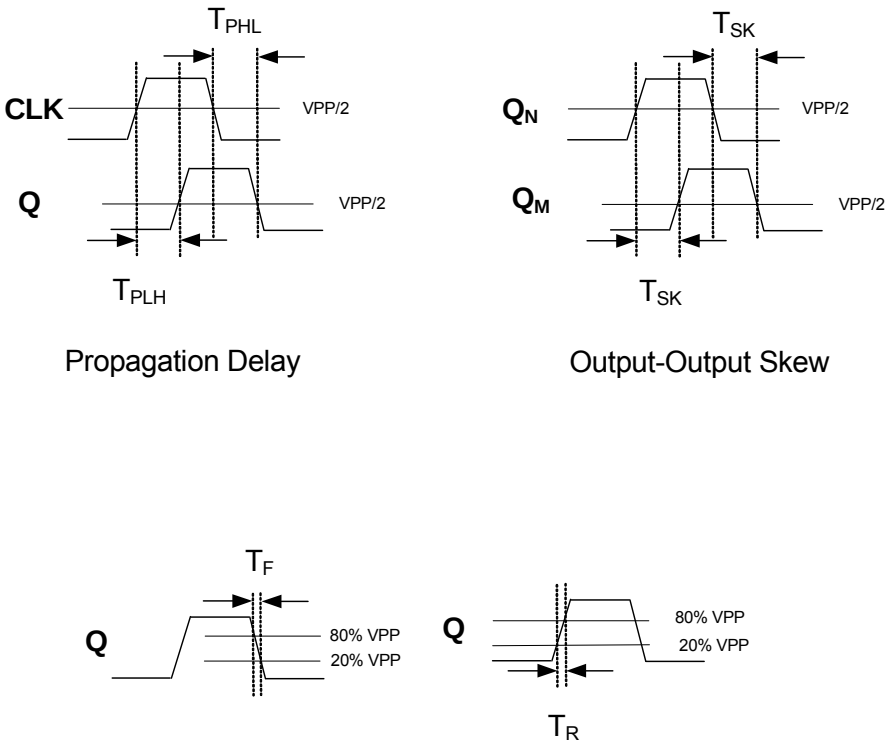


Figure 8. AC Waveforms

2.8. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

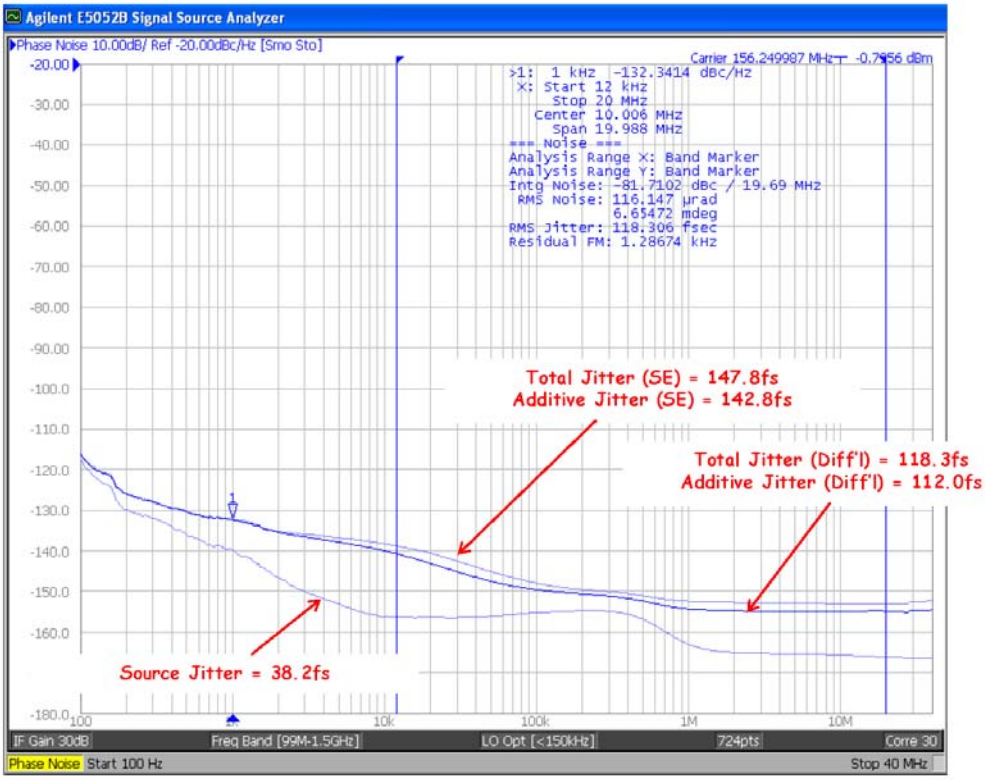
Source Jitter: Reference clock phase noise.

Total Jitter (SE): Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

Total Jitter (Diff): Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 6.

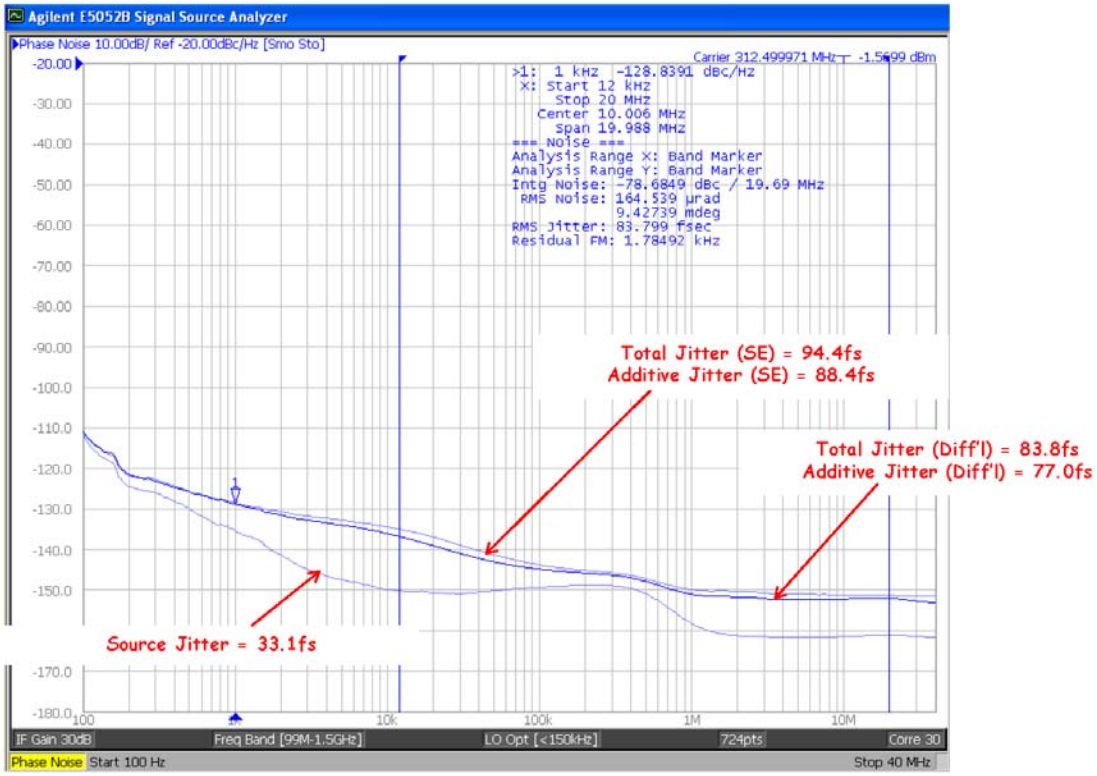
Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



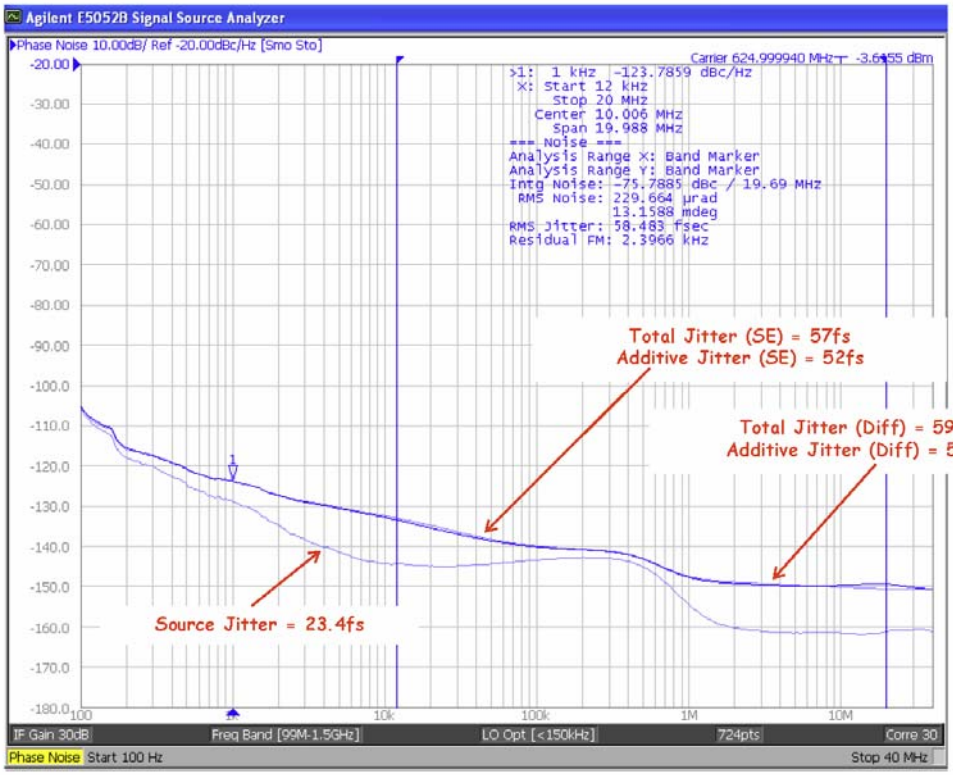
Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

Figure 9. Source Jitter (156.25 MHz)



Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
312.5	1.0	33.10	94.39	88.39	83.80	76.99

Figure 10. Single-Ended Total Jitter (312.5 MHz)



Frequency (MHz)	Diff Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff) (fs)	Additive Jitter (Diff) (fs)
625	1.0	23	57	52	59	54

Figure 11. Differential Total Jitter (625 MHz)

2.9. Input Mux Noise Isolation

The input clock mux is designed to minimize crosstalk between the CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. Figure 12 below is a measurement the input mux's noise isolation.

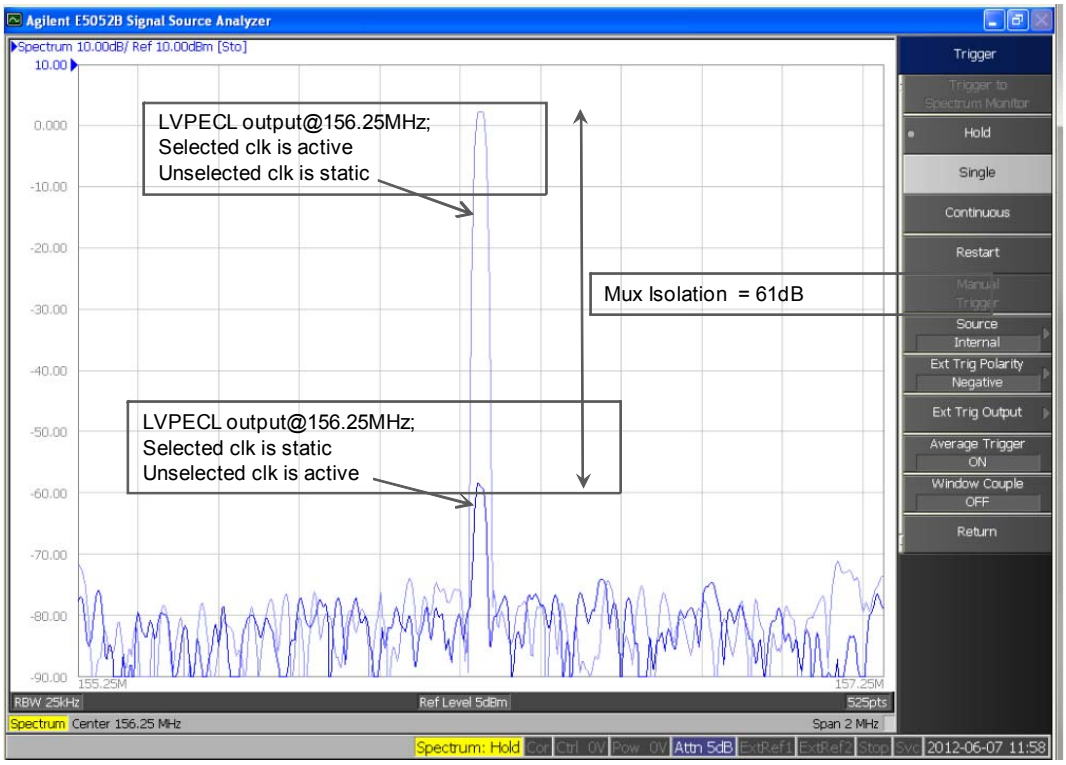


Figure 12. Input Mux Noise Isolation

2.10. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see "AN491: Power Supply Rejection for Low Jitter Clocks".

3. Pin Description: 20-Pin TSSOP

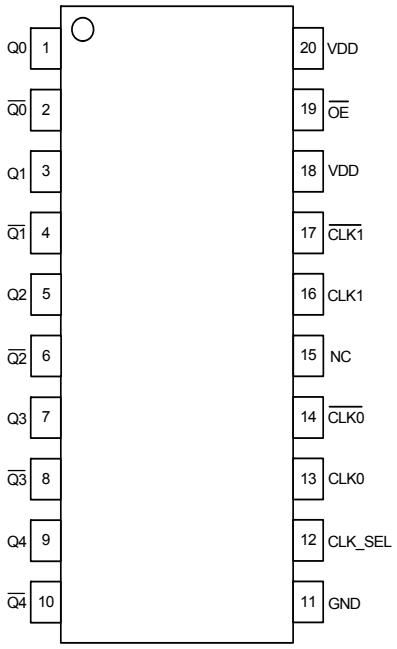


Table 13. Si53320 20-Pin TSSOP Descriptions*

Pin #	Name	Type*	Description
1	Q0	O	Output clock 0.
2	$\overline{Q0}$	O	Output clock 0 (complement).
3	Q1	O	Output clock 1.
4	$\overline{Q1}$	O	Output clock 1 (complement).
5	Q2	O	Output clock 2.
6	$\overline{Q2}$	O	Output clock 2 (complement).
7	Q3	O	Output clock 3.
8	$\overline{Q3}$	O	Output clock 3 (complement).
9	Q4	O	Output clock 4.
10	$\overline{Q4}$	O	Output clock 4 (complement).
11	GND	GND	Ground.
12	CLK_SEL	I	Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
13	CLK0	I	Input clock 0.

Table 13. Si53320 20-Pin TSSOP Descriptions* (Continued)

Pin #	Name	Type*	Description
14	$\overline{\text{CLK0}}$	I	Input clock 0 (complement) When CLK0 is driven by a single-ended input, connect $\overline{\text{CLK0}}$ to an appropriate bias voltage (e.g., for a CMOS input apply $V_{DD}/2$).
15	NC	—	No connect. Leave this pin unconnected.
16	CLK1	I	Input clock 1.
17	$\overline{\text{CLK1}}$	I	Input clock 1 (complement) When CLK1 is driven by a single-ended input, connect $\overline{\text{CLK1}}$ to an appropriate bias voltage (e.g., for a CMOS input apply $V_{DD}/2$).
18	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
19	$\overline{\text{OE}}$	I	Output enable. When $\overline{\text{OE}}$ = low, the clock outputs are enabled. When $\overline{\text{OE}}$ = high, Q is held low and $\overline{\text{Q}}$ is held high. $\overline{\text{OE}}$ features an internal pull-down resistor and may be left unconnected.
20	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
***Note:** Pin types are: I = input, O = output, P = power, GND = ground.			

4. Ordering Guide

Part Number	Package	Pb-Free, ROHS-6	Temperature
Si53320-B-GT	20-TSSOP	Yes	–40 to 85 °C

5. Package Outline

5.1. 20-TSSOP Package Diagram

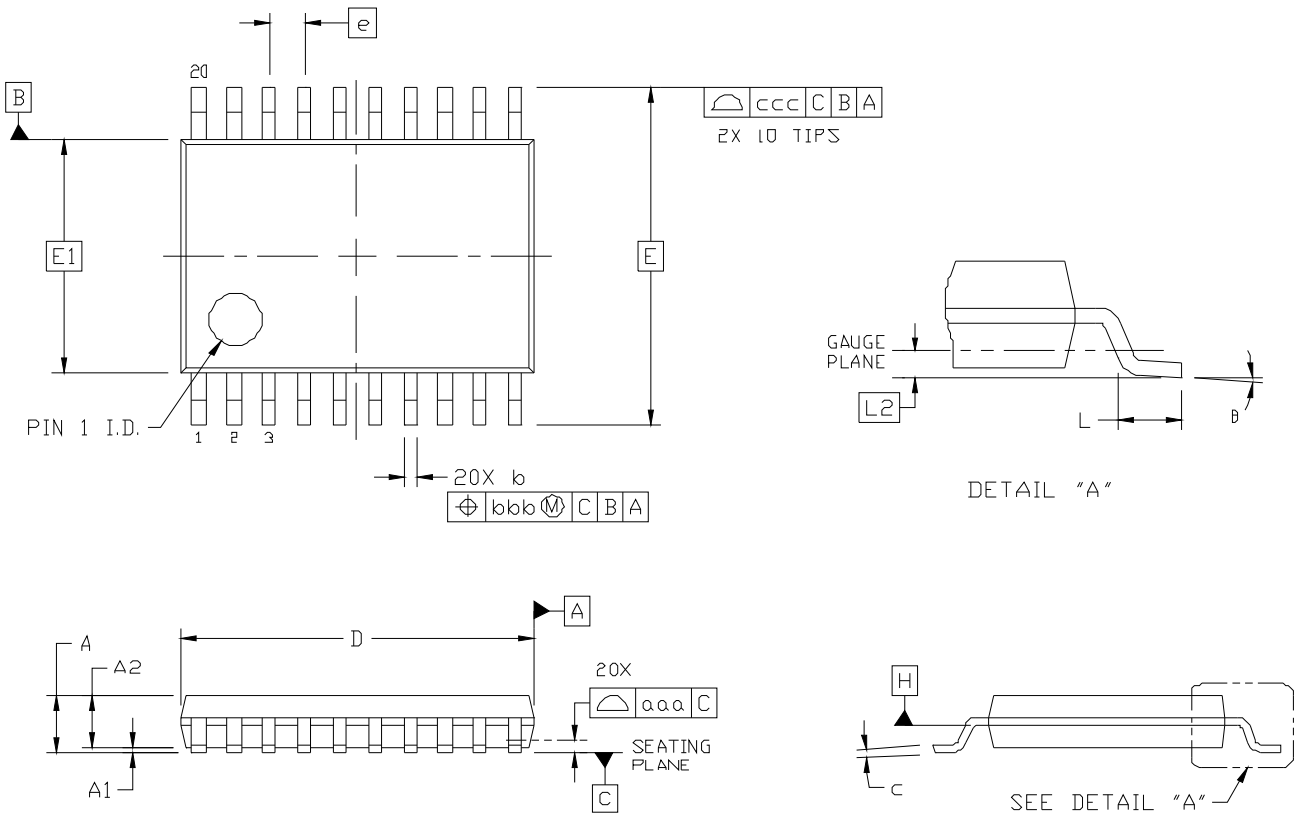


Figure 13. Si53320 20-TSSOP Package Diagram

Table 14. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	6.40	6.50	6.60
E	6.40 BSC		
E1	4.30	4.40	4.50

Dimension	Min	Nom	Max
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.20		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. PCB Land Pattern

6.1. 20-TSSOP Package Land Pattern

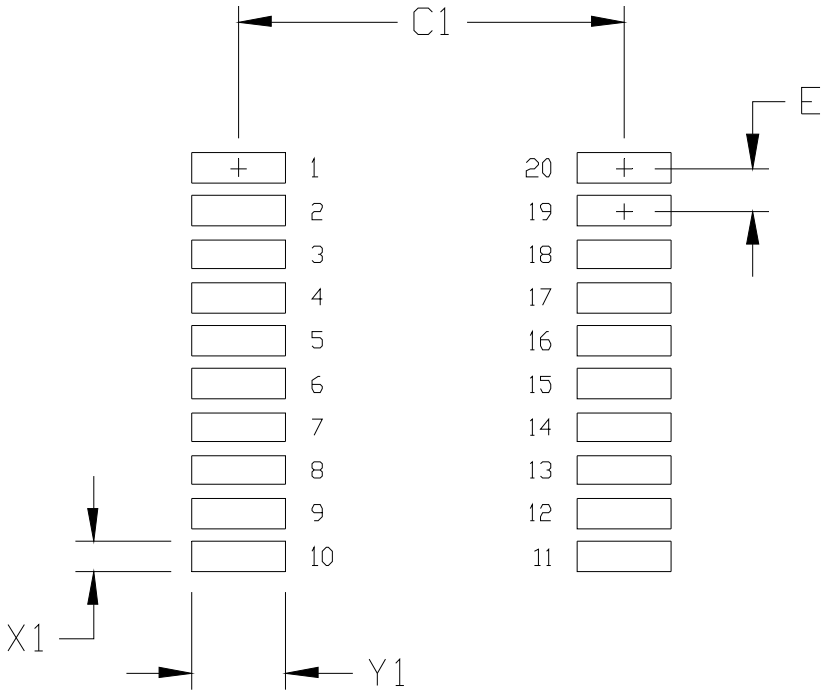


Figure 14. Si53320 20-TSSOP Package Land Pattern

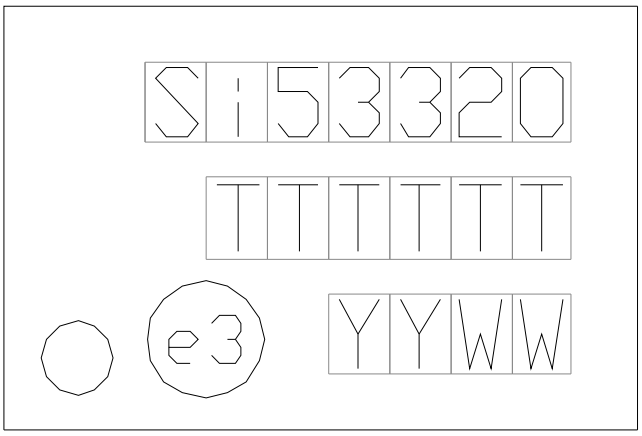
Table 15. PCB Land Pattern

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.80
E	Pad Row Pitch	0.65
X1	Pad Width	0.45
Y1	Pad Length	1.40

Notes:
1. This Land Pattern Design is based on IPC-7351 specifications for Density Level B (Median Land Protrusion)
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7. Top Marking

7.1. Si53320 Top Marking



7.2. Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (0.71 mm) Right-Justified	
Line 1 Marking:	Customer Part Number	**Si53320**
Line 2 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to year and work week of the build date.

Document Change List

Revision 0.4 to 1.0

- Update operating conditions, including LVCMOS and HCSL voltage support.
- Updated Table 2, “Input Clock Specifications,” on page 3.
- Updated Table 3, “DC Common Characteristics,” on page 5.
- Updated Table 4, “Output Characteristics (LVPECL),” on page 6.
- Updated Table 10, “AC Characteristics,” on page 7.
- Updated output voltage specifications
- Improved data for additive jitter specifications.
- Improved typical phase noise plots.
- Updated input/output termination recommendations.
- Improved performance specifications with more detail.
- Removed the voltage reference feature.
- Added pin type description to the pin descriptions table

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com