# Superjunction MOSFET for charger applications

## 600 V/650 V/700 V/800 V CoolMOS™ CE

### About this document

### Scope and purpose

This application note will describe the fundamental differences between a Superjunction MOSFET and a standard MOSFET. Additionally, all features and benefits impacting the target applications will be described. Furthermore, these features will be illustrated from both a theoretical point of view and in hardware measurements. It will also be shown that CoolMOS$^{TM}$ CE is a cost effective alternative compared to standard MOSFETs, which enables reaching higher efficiency levels while offering an attractive price/-performance ratio.

### Intended audience

This document is intended for designers & engineers who wish to design chargers in price sensitive and targeted applications such as consumer, PC silverboxes and lighting where Infineon's CoolMOS™ CE offers the best price-performance ratio on the market while meeting higher efficiency standards.

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# 1 Introduction

The CoolMOS$^{TM}$ CE is a technology platform of Infineon's market leading high voltage power MOSFETs designed according to the revolutionary Superjunction (SJ) principle. After launching the 500 V class in 2012, CE technology is now also available in 600 V, 650 V, 700 V and 800 V. CoolMOS™ CE portfolio provides all benefits of a fast switching SJ MOSFET while keeping ease-of-use and implementation. The complete CE series of MOSFETs achieve very low conduction and switching losses, and can make applications more efficient, more compact, lighter and thermally cooler.

## 1.1 Features and benefits

The following table represents the features and benefits of CoolMOS$^{TM}$ CE in comparison to standard MOSFETs, which will be discussed in depth in the main part of this application note.

**Table 1 Features and benefits**

| Features | Benefits |
|---|---|
| Reduced energy stored in output capacitance ($E_{oss}$) | Reduction of switching losses, improvement of light load efficiency |
| High body diode ruggedness | Higher reliability in critical operating conditions |
| Reduced reverse recovery charge ($Q_{rr}$) | Lower possibility of hard commutation in resonant topologies |
| Reduced gate charge ($Q_g$) | Improvement in light load efficiency |
| | Lower gate drive capability required |

## 1.2 Applications (target market)

The following table represents the target applications and topologies for these new MOSFETs

**Table 2 Target applications and topologies**

| Application | PFC | PWM |
|---|---|---|
| PC silverbox | Boost-Stage | TTF |
| | | LLC |
| LCD / LED / PDP TV | Boost-Stage | LLC |
| Gaming | Boost-Stage | TTF |
| | | LLC |
| Adapter | Boost-Stage | Flyback |
| Charger | | Flyback |
| Lighting | Boost-Stage | Flyback |
| | | LLC |

All the features and benefits of the 500 V CoolMOS™ CE in connection with the target applications and topologies will be analyzed in section 4. The following section will describe the differences between SJ MOSFETs and standard MOSFETs.

# 2 Superjunction (SJ) principle

This chapter is included to understand the difference between SJ MOSFET and standard MOSFET because the consumer market has been dominated in the past by standard MOSFETs.

## 2.1 General description

"All CoolMOS™ series are based on the Superjunction principle, which is a revolutionary technology for high voltage power MOSFETs [1, 2]. Infineon Technologies has been the first company worldwide to commercialize this idea into the market [4]. Where conventional power MOSFETs just command on one degree of freedom to master both on-state resistance and blocking voltage, the superjunction principle allows two degrees of freedom for this task. Therefore conventional MOSFETs are stuck with the limit of silicon, a barrier which marks the optimum doping profile for a given voltage class. This limit line has been theoretically derived by Chen and Hu in the late 80ies [3]. No commercial product has an on-state resistance better than the limit line of silicon." [5]

Figure 1 represents the area-specific on-resistance versus breakdown voltage of a standard MOSFET vs Infineon's SJ MOSFET CoolMOS™

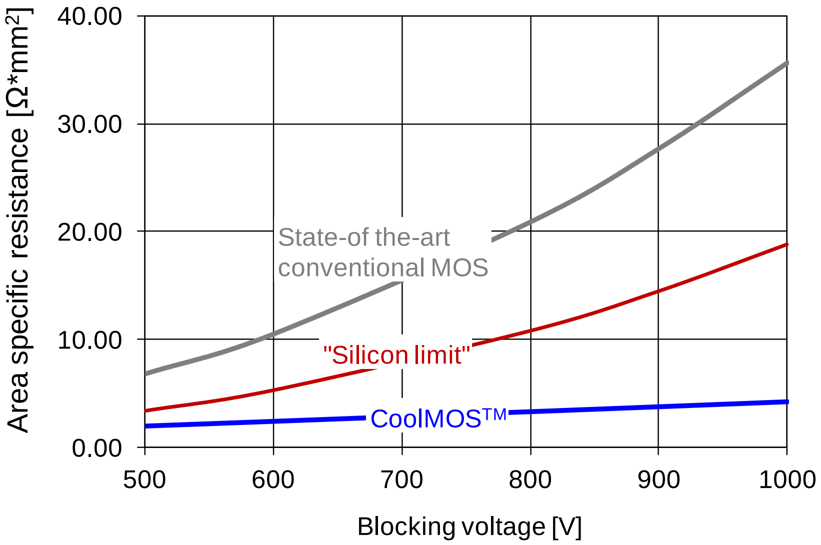


**Figure 1 Comparison of standard MOSFET and CoolMOS™ technology [6]**

"In contrast to that the superjunction principle allows to reduce the on-state resistance of a high voltage MOSFET virtually to zero, limited only by technology efforts and manufacturing capabilities." [5]

"The basic idea is simple: instead of having electrons flowing through a relatively high resistive (high voltage blocking) n-area, we allow them to flow in a very rich doped n-area, which gives naturally a very low on-state resistance. The crucial point for the SJ technology is to make the device block its full voltage, which requires a careful balancing of the additional n-charge by adjacently positioned deep p-columns, which go all the way straight through the device close to the back side n+ contact. This is where manufacturing capability comes in, as the charges within the device needs to be compensated precisely under the constraints of a mass market production line." [5]

Figure 2 shows the cross section of a standard MOSFET (left) and a SJ MOSFET (right).

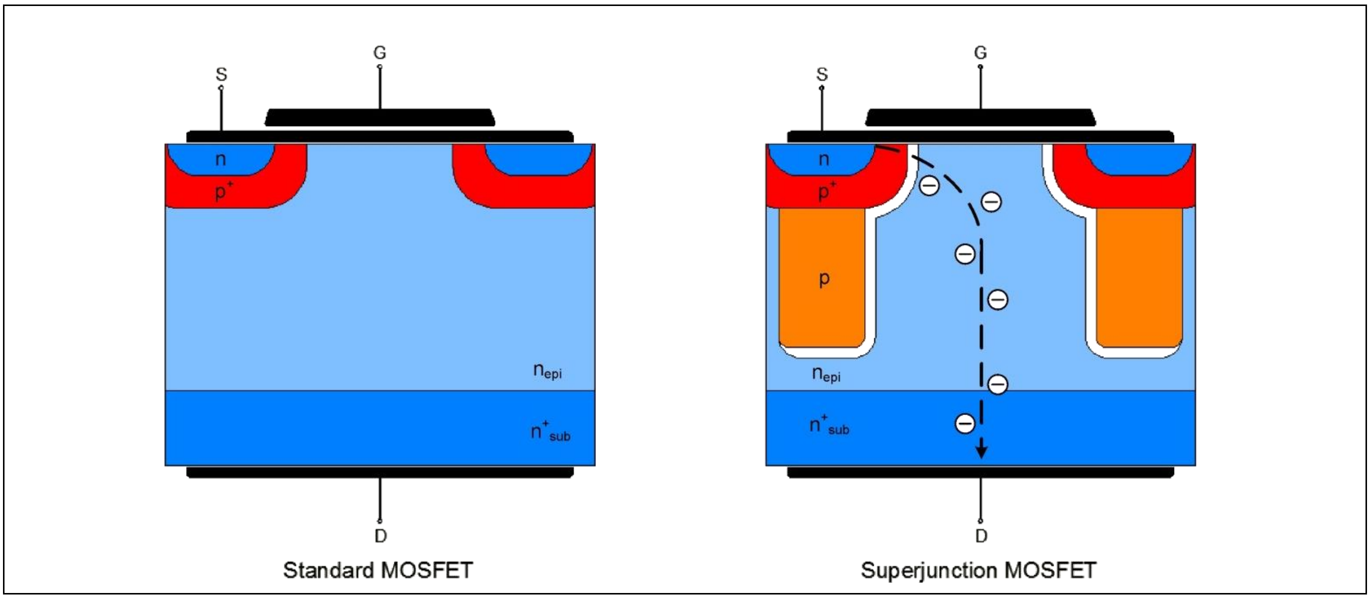


**Figure 2** Cross section of standard MOSFET (left) and SJ MOSFET (right) [5]

“The SJ principle gives us the opportunity to create best-in-class types, which have not been possible before such as a 100 mΩ/600 V part in a TO-220 package. Furthermore it allows making parts with very low capacitances for a given $R_{DS(on)}$ as the silicon chip is much smaller than for a conventional power MOSFET. Both input and high voltage level of the output capacitance scale directly with the chip size, whereas reverse capacitance and to some extent the low voltage level of the output capacitance is technology dependent. Characteristic of all Superjunction devices is a strong non-linearity of the output capacitance with high values at low voltage and low values at high voltage. This behavior can be easily understood if you take into account that the output capacitance is proportional to the area of the blocking pn-junction and inverse proportional to the width of the space charge layer (or the voltage sustaining area). At low voltage the p-columns are not depleted and form a very big surface, furthermore the width of the space charge layer is very narrow (the white area in” Figure 2). ” At high voltage however the p-columns are fully depleted and the space charge layer has reached its full extension of roughly 45µm for a 600 V device. Important is that the non-linearity of the output capacitance allows a quasi zero-voltage-switching (ZVS) turn-off of the device, lowering turn-off losses. Superjunction devices are by nature fast in switching. Very small capacitances together with a low gate charge make rise and fall times of a few nanoseconds a reality.” [5]

For more information on Superjunction devices please read the article “Mastering the Art of Slowness”; see Reference [5].

## 2.2 Superjunction benefit of CoolMOS™ CE

Chapter 2.1 illustrated the general characteristics of a SJ MOSFET in comparison to a standard MOSFET. Now the question arises “What are the benefits for the CoolMOS™ CE?”. This application note will describe one of the most important factors which is the switching speed.

### 2.2.1 Switching speed

As mentioned in the general description the switching speed increases dramatically. This behavior comes from the low parasitic capacitances of a SJ MOSFET in comparison to the standard MOSFET. A SJ MOSFET has about half of the value of input and output capacitance, which brings the benefits for switching losses and driving losses. Figure 3 represents these parasitic capacitances (marked in red) in a simplified schematic.

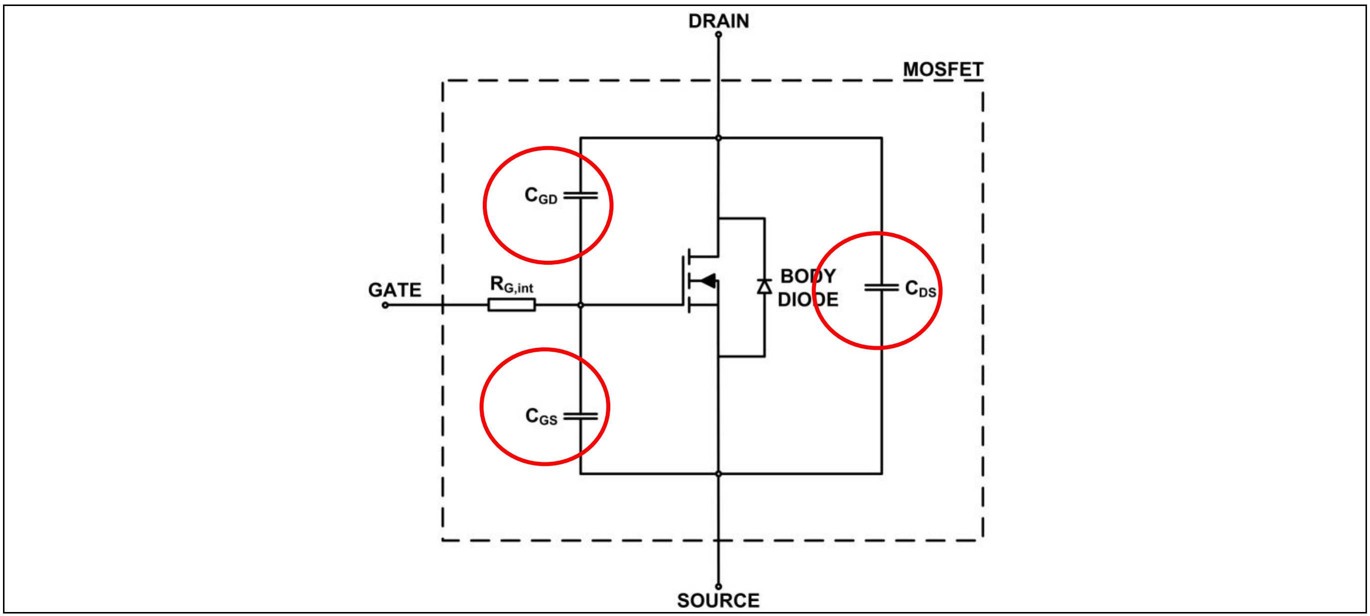


Figure 3 Simplified small signal MOSFET equivalent circuit

Because of this capacitance reduction the $E_{on}$ and $E_{off}$ of the CoolMOS™ CE is about half in comparison to a standard MOSFET. Furthermore this reduction of capacitances results also in a reduced gate charge $Q_g$ which gives the benefit of reduced driving losses, and the possibility to use a lower cost driver with less gate drive capability. Figure 4 represents the capacitance comparison of the 650 V CE (1500 mΩ) vs. a comparable standard MOSFET.

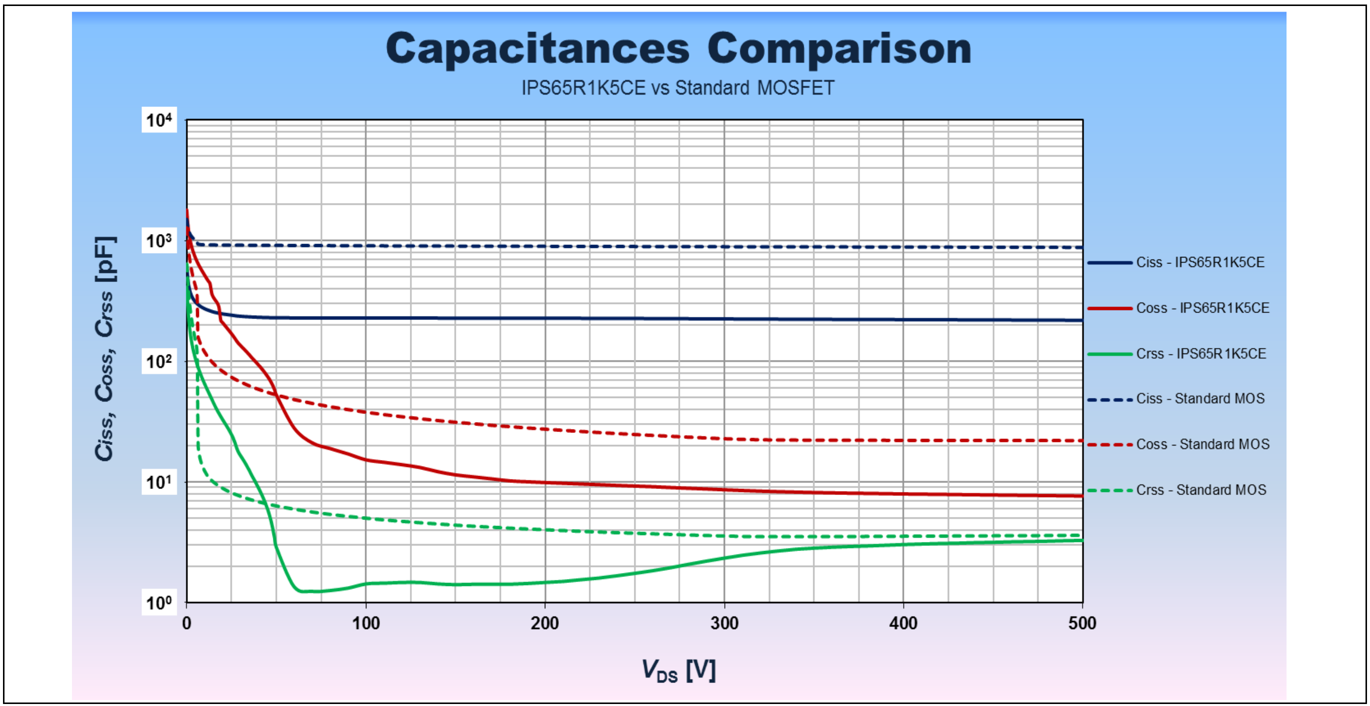


Figure 4 Capacitance comparison 650 V CE vs. standard MOSFET

“A fundamental characteristic of all Superjunction devices is, that both the output and reverse capacitance show a strong non-linearity. The non-linearity in Superjunction capacitance characteristics comes from the fact that at a given voltage – typically in the range of 1/10th of the rated blocking voltage – p- and n-columns deplete each other leading to a fast expansion of the space charge layer throughout the structure. This means that at a voltage beyond 50 V for 500 V rated devices both output and reverse capacitance reach minimum values of a few pF only, resulting in a dv/dt of more than 100V/ns and di/dt of several thousand A/µs if the load current is allowed to fully commute into the output capacitance during turn-off. The output capacitance is charged up to the level of the bus voltage where the voltage rise follows then the formula:

$$^{dv}/_{dt} = \frac{I_{load}}{C_{oss}} \qquad [1]$$

The voltage rise is therefore proportional to the load current Iload and inverse proportional to the value of the output capacitance $C_{oss}$. Because of the decreasing $C_{oss}$ towards higher voltages, the highest dv/dt is reached shortly before reaching the bus voltage. The according di/dt is mainly limited by the inductances of package and PCB circuit. The highest efficiency can now be reached by turning-off the device in this manner, because the occurring switching losses can be ideally reduced down to the level of the stored energy in the output capacitance.” [7]

All these benefits will be clearly visible in the efficiency results, which will be described in chapter 4. Technology parameters

# 3 Technology parameters

## 3.1 Gate charge ($Q_g$)

One of the most important improvements is the $Q_g$ reduction which brings benefits especially in light load conditions due to reduced driving losses. In general the CoolMOS™ CE has about 40% $Q_g$ reduction in comparison to a comparable standard MOSFET over the whole $R_{DS(on)}$ range. Figure 5 shows the $Q_g$ in nC of the 600 V CE against a standard MOSFET over the $R_{DS(on),max}$ range from 400 mΩ to 2100 mΩ.

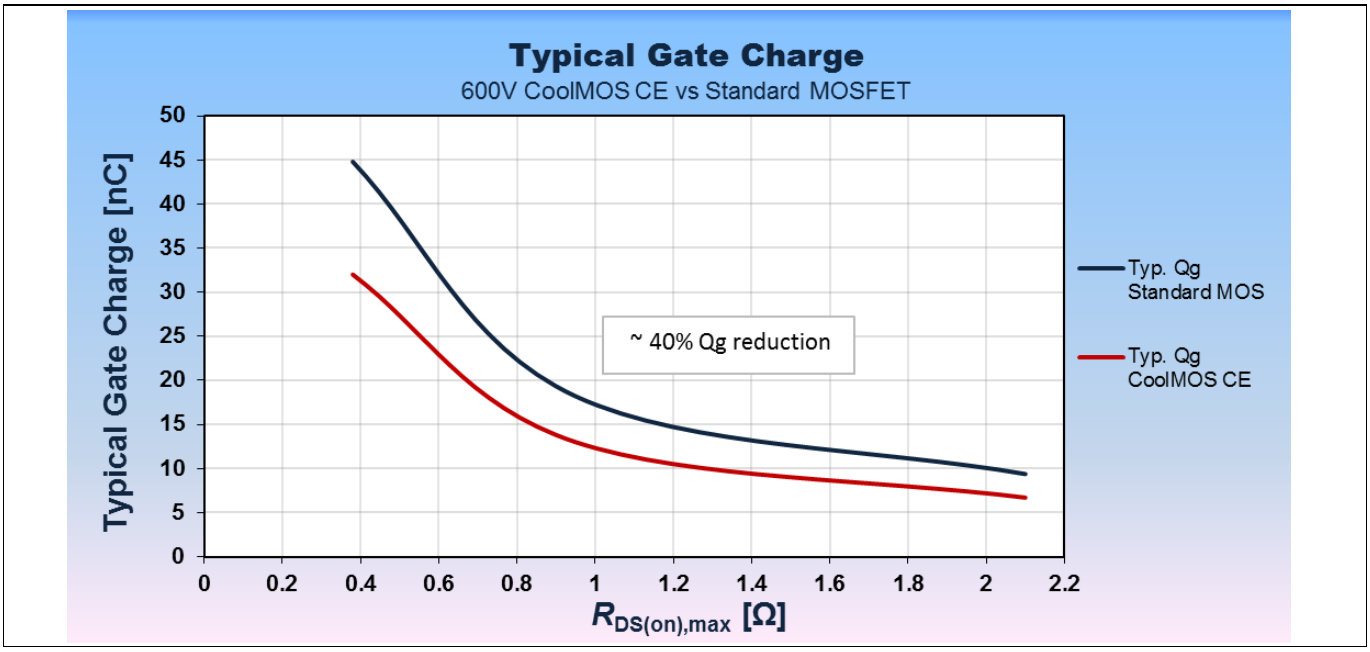


Figure 5 $Q_g$ comparison 600 V CE vs. standard MOSFET

## 3.2 Energy stored in output capacitance ($E_{oss}$)

The reduced energy stored in the output capacitance brings the most important difference in hard switching topologies but nevertheless it affects also the switching losses in a resonant topology. Normally it is possible to choose between zero voltage switching (ZVS) or zero current switching (ZCS). In these two cases it is possible to eliminate the turn-on losses (ZVS) or the turn-off losses (ZCS) but it is not possible to work in these two operation modes at the same time. Normally for MOSFETs the ZVS operation is preferred due to the usual important contribution of the output capacitance to the turn-on losses (if hard switching). Therefore, one part of the switching losses is still always in action, and the reduction of $E_{oss}$ brings a reduction of those switching losses. Figure 6 represents the $E_{oss}$ comparison between the 650 V CE and a comparable standard MOSFET of the 1500 mΩ devices.

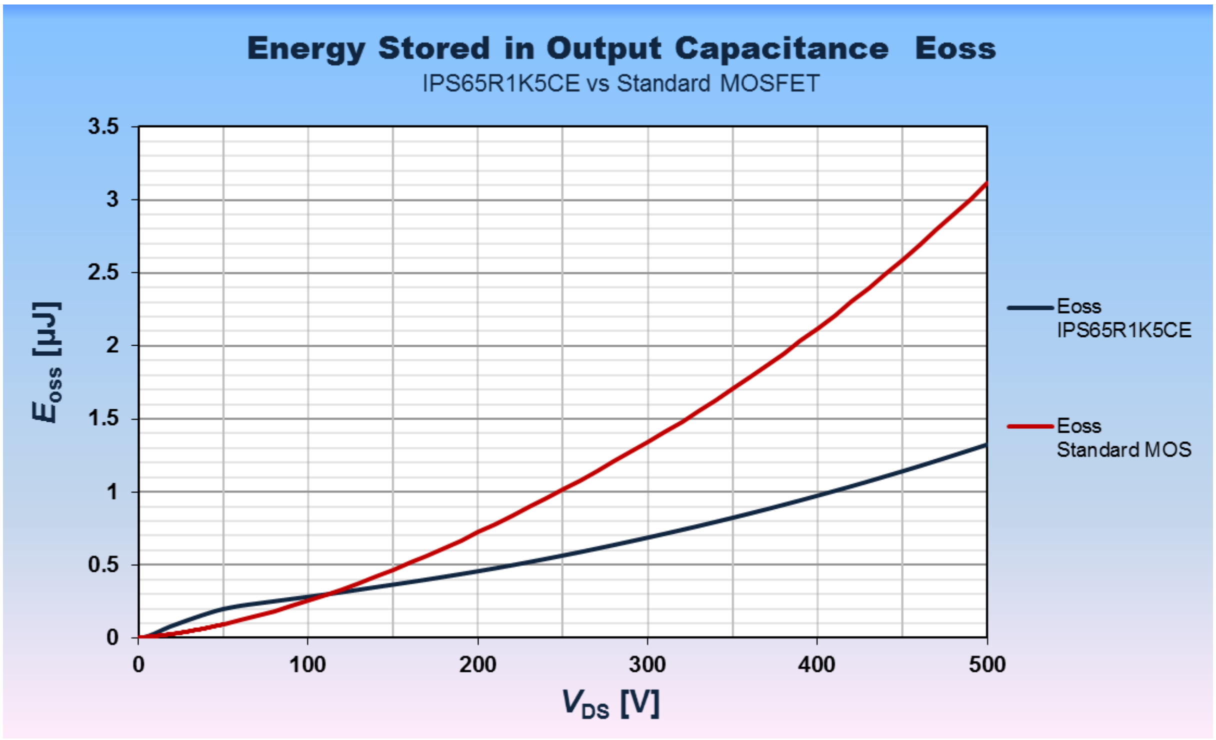


Figure 6 $E_{oss}$ comparison 650 V CE vs. standard MOSFET

The $E_{oss}$ loss is in direct proportion to the output capacitance as a function of drain to source voltage of the MOSFET. In this case the effect of a reduction of $C_{oss}$ is very visible. One further benefit out of this is a faster $V_{DS}$ transition time in resonant topologies, which means that it is possible to reduce the resonant inductance and circulating current loss, because it is possible to completely discharge the $C_{oss}$ with lower currents.

# 4 Measurement results

In order to show the performance of CoolMOS™ CE in charger application, two test platforms have been used. First, a slim-type 10.6 W travel charger design which is typically used in phablet or tablet segment. Next is the small form factor 15 W adapter reference board for catering the demand for fast charger market. Both power supplies are capable to accept universal input and with fixed output voltage.

## 4.1 Efficiency and thermal in charger

In this measurement the 650 V CE is compared to a standard MOSFET in the 1.5 Ω $R_{DS(on)}$ range for 10.6 W charger and the efficiency and thermal performance of 1.0 Ω $R_{DS(on)}$ in 15 W adapter.

### 10.6 W charger

Test setup parameters:

- Topology: Peak current controlled flyback
- $V_{in}$ = 90 $V_{AC}$ – 264 $V_{AC}$
- $V_{out}$ = 5.3 $V_{DC}$
- $I_{out}$ = 0 A to 2 A
- Frequency = 50 kHz @ FL
- Ambient temperature = 25°C
- Plug and play scenario between 650 V CoolMOS™ CE and standard MOSFET
- High voltage MOSFET = IPS65R1K5CE

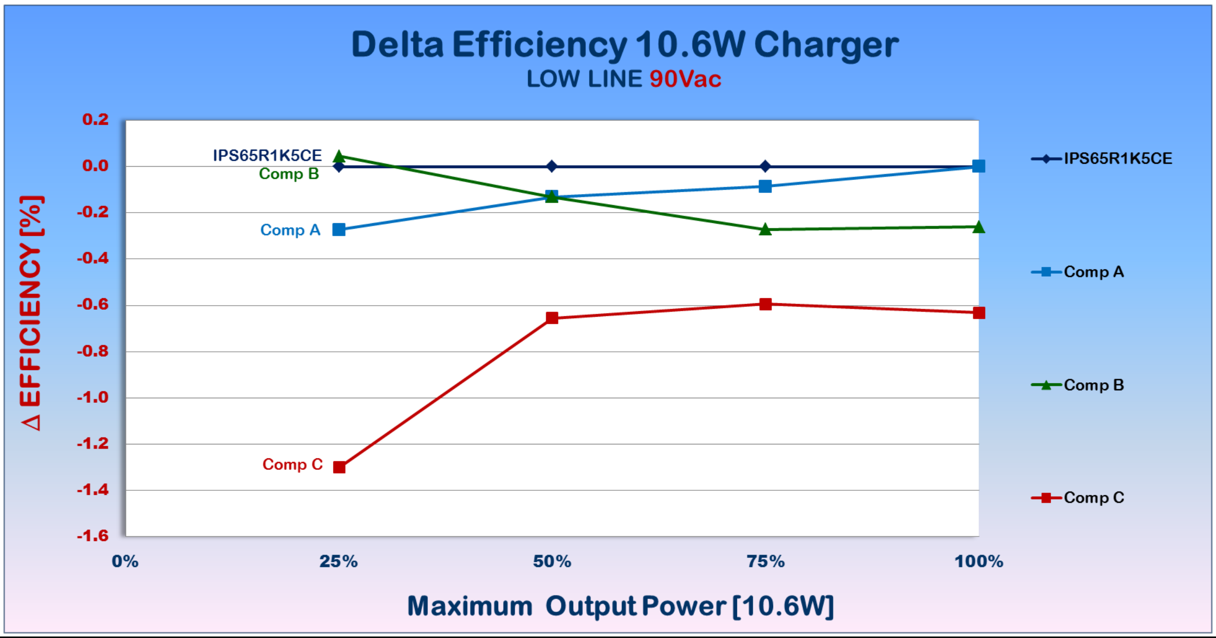


Figure 7 650 V CE vs. standard MOSFET delta efficiency comparison @ $V_{in}$=90 $V_{AC}$

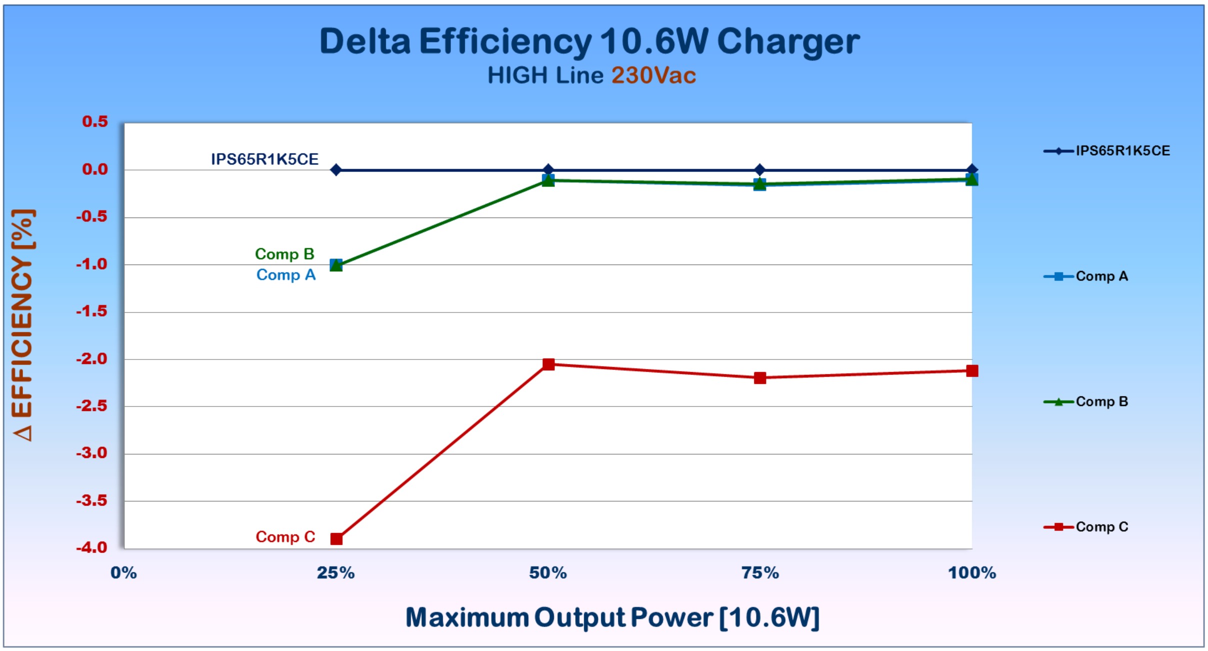


Figure 8 650 V CE vs. standard MOSFET delta efficiency comparison @$V_{in}$=230 $V_{AC}$

This plug and play measurement shows the benefit of a SJ MOSFET in comparison to a standard MOSFET in terms of efficiency and thermals. Due to the $Q_g$ reduction of CoolMOS$^{TM}$ CE a minimum efficiency difference of 1% at 25% load condition, 230 $V_{AC}$ leads to better average efficiency as shown in Figure 7. Hence, future efficiency requirement can be easily achieved with this technology.

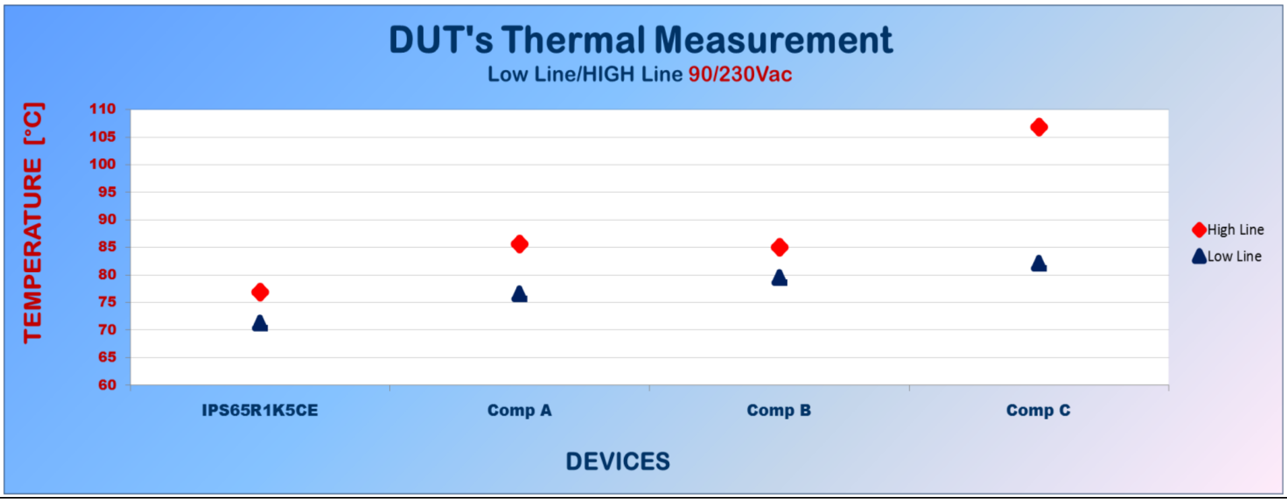


Figure 9 650 V CE vs. standard MOSFET thermal comparison

The thermal behavior of the power devices in charger application is very critical because the heat generated by the components will have very little way to dissipate due to very dense construction and high thermal resistance of the casing. Therefore, power mosfets with improved switching losses will help in ensuring device is below the temperature limit. As presented in Figure 8, IPS65R1K5CE offers 5°C lower than the nearest competition device at low line (worst case) which resulted to enhance design ruggedness due to increase in margin.

15 W charger

Test setup parameters:

- Topology: QR flyback
- $V_{in} = 90\ V_{AC} – 264\ V_{AC}$
- $V_{out} = 5\ V_{DC}$
- $I_{out}$ = 0 A to 3 A
- Frequency = 55-110 kHz
- Ambient temperature = 25°C
- High voltage MOSFET = IPS65R1K0CE
-

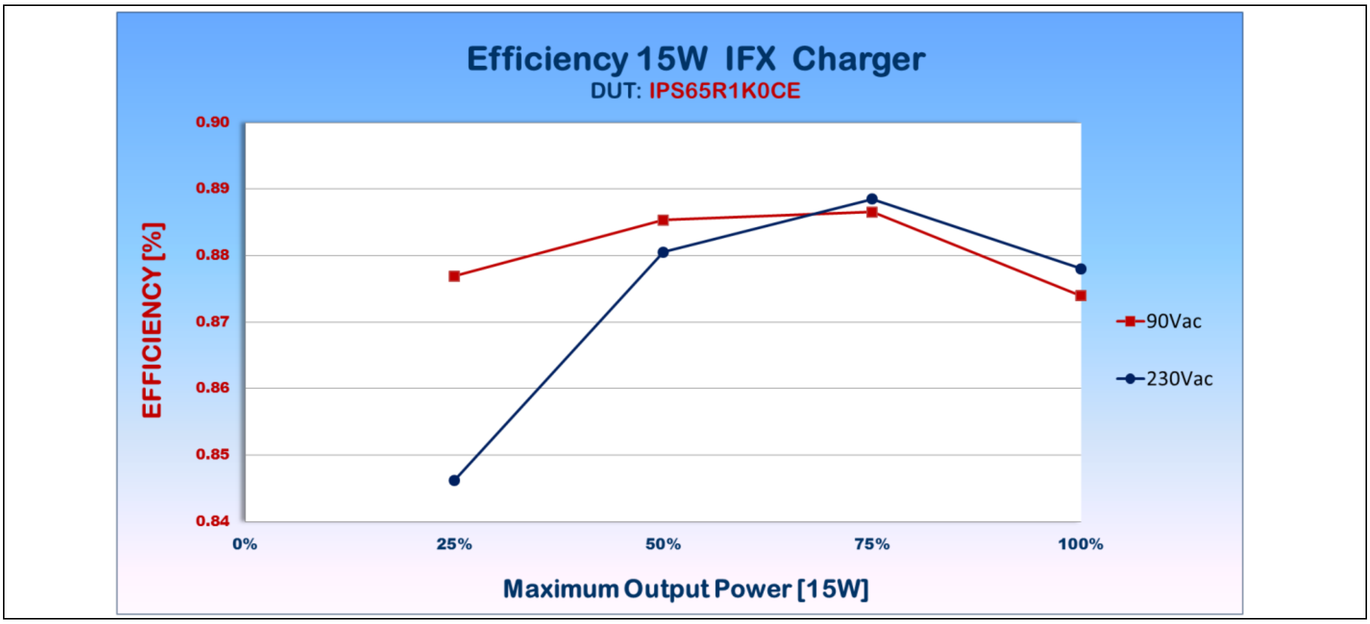


**Figure 10** 1.0 Ω 650 V CE efficiency

Figure 9 indicates the efficiency performance of IPS65R1K0CE. The 15 W charger can easily meet average efficiency specs of EU CoC version 5, Tier 2 and EPS of DOE USA with >5% margins in both input voltages. The solution was able reach high efficiency by reducing the switching losses in the HV switch and conduction losses in the secondary by using a SR MOSFET. Power MOSFET with low $E_{oss}$ and $Q_g$ contributes in minimizing the losses in the primary side.

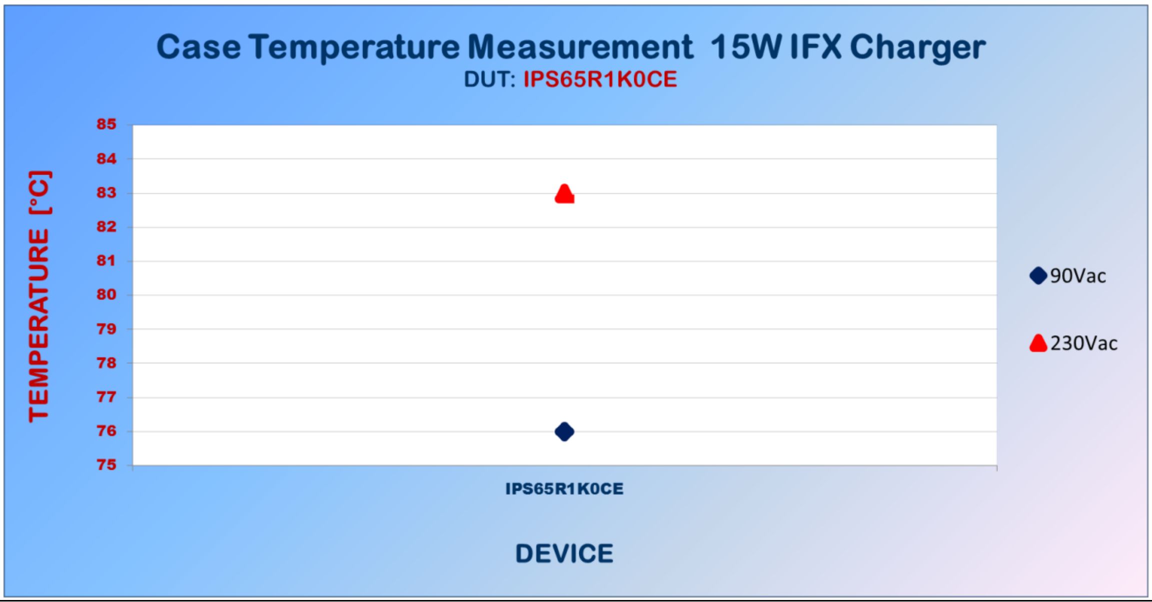


Figure 11 1.0 Ω 650 V CE thermal performance

The case temperature of IPS65R1K0CE is higher at high line compared to low line (Figure 10). And theresult signifies that the converter is a switching loss dominated platform which represents the majority of the solution in the market most especially at power ≥10 W with small form factor. Thus, it is very important to consider the switching characteristic of the power mosfet which is the strongest advantage of SJ MOSFETs in comparison with standard mosfets.

# 5 Design guidelines for CoolMOS™ CE in flyback converter

## 5.1 Breakdown voltage ($V_{(BR)DSS}$)

Proper selection of voltage rating is necessary to ensure safe operation of the device during normal and critical conditions. Transformer's turn ratio and leakage inductance greatly influence the voltage level impressed in the device. Primary MOSFET and secondary rectifier need to be considered in choosing the optimal turn ratio because increasing or decreasing it will deliver opposite results while leakage inductance is mainly attributed to core geometry and winding construction of the transformer. Incidentally, 90% derating can be used as a rule of thumb although it some cases lower derating is required to further improved reliability.

## 5.2 On-state resistance ($R_{DS(on)}$)

The primary consideration of selecting the on-state resistance is the contribution of conduction losses at full load, low input voltage because it is at its highest at this condition. However, mosfet case temperature is more critical at high input voltage which indicates the need for device that will generate lesser switching losses even to the point of choosing higher $R_{DS(on)}$.

## 5.3 $C_{oss}$ stored energy ($E_{OSS}$)

To attain the demand of increasing power density in charger application, it is necessary to increase the switching frequency to lessen the increase in transformer size and output capacitors. Conversely, turn-on losses are proportional to switching frequency and $E_{OSS}$. Device with low $E_{OSS}$ is beneficial in achieving high efficiency particularly at high input voltage.

## 5.4 Total gate charge ($Q_G$)

Gate drive losses and linear losses are influenced by the total gate charge of the MOSFET. The amount of charge required to turn-on the mosfet will be the same amount of charge needed by the driver to dissipate at turn off. The duration of the linear losses is determined by $Q_{GD}$ which is part of switching losses. A low gate charge device is necessary to improve the efficiency and reducing the power consumption of the converter at very light load or no load condition.

# 6 Portfolio

CoolMOS$^{TM}$ CE series follows the same naming guidelines as already established with the previous technology series e.g. IPS65R1K5CE:

| | | |
|---|---|---|
| I | … | Infineon Technologies |
| P | … | power MOSFET |
| S | … | package type (TO-251 SL) |
| 65 | … | voltage class divided by 10 |
| R1K5 | … | on-state resistance in milli Ohms |
| CE | … | name of the series |

Table 3 Portfolio 600 V CoolMOS™ CE

| $R_{DS(on)}$ [mΩ] | TO-220 FullPAK<br> | TO-252 DPAK<br> | TO-251 IPAK SL<br> | TO-251 IPAK<br> | SOT-223<br> | TO-220 FullPAK Wide Creepage<br> |
|---|---|---|---|---|---|---|
| **3300** | | IPD60R3K4CE | IPS60R3K4CE | | IPN60R3K4CE | |
| **2100** | | IPD60R2K1CE | IPS60R2K1CE | IPU60R2K1CE | IPN60R2K1CE | |
| **1500** | IPA60R1K5CE | IPD60R1K5CE | IPS60R1K5CE | IPU60R1K5CE | IPN60R1K5CE | |
| **1000** | IPA60R1K0CE | IPD60R1K0CE | IPS60R1K0CE | IPU60R1K0CE | IPN60R1K0CE | |
| **800** | IPA60R800CE | IPD60R800CE | IPS60R800CE | | | |
| **650/600** | IPA60R650CE | IPD60R650CE | IPS60R650CE | | | IPAW60R600CE |
| **460** | IPA60R460CE | IPD60R460CE | IPS60R460CE | | | |
| **400/380** | IPA60R400CE | IPD60R400CE | IPS60R400CE | | | IPAW60R380CE |
| **280** | | | | | | IPAW60R280CE |
| **190** | | | | | | IPAW60R190CE |

Table 4 Portfolio 650 V CoolMOS™ CE

| $R_{DS(on)}$ [mΩ] | TO-220 FullPAK<br> | TO-252 DPAK<br> | TO-251 IPAK SL<br> | SOT-223<br> |
|---|---|---|---|---|
| **1500** | IPA65R1K5CE | IPD65R1K5CE | IPS65R1K5CE | IPN65R1K5CE |
| **1000** | IPA65R1K0CE | IPD65R1K0CE | IPS65R1K0CE | |
| **650** | IPA65R650CE | IPD65R650CE | IPS65R650CE | |
| **400** | IPA65R400CE | IPD65R400CE | IPS65R400CE | |

Table 5 Portfolio 700 V CoolMOS™ CE

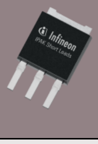
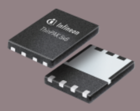
| $R_{DS(on)}$ [mΩ] | TO-262<br>IPAK<br> | TO-252<br>DPAK<br> | TO-251<br>IPAK SL<br> | SOT-223<br> | ThinPAK 5x6<br> |
|---|---|---|---|---|---|
| 2000/2100 | | IPD70R2K0CE | IPS70R2K0CE | | IPL70R2K1CES |
| 1400/1500 | | IPD70R1K4CE | IPS70R1K4CE | IPN70R1K5CE | |
| 950 | IPI70R950CE | IPD70R950CE | IPS70R950CE | | |
| 600 | | IPD70R600CE | IPS70R600CE | | |

Table 6 Portfolio 800 V CoolMOS™ CE

| $R_{DS(on)}$ [mΩ] | TO-220<br>FullPAK<br> | TO-252<br>DPAK<br> | TO-251<br>IPAK<br> |
|---|---|---|---|
| 2800 | | IPD80R2K8CE | IPU80R2K8CE |
| 1400 | IPA80R1K4CE | IPD80R1K4CE | IPU80R1K4CE |
| 1000 | IPA80R1K0CE | IPD80R1K0CE | IPU80R1K0CE |
| 650 | IPA80R650CE | | |
| 460 | IPA80R460CE | | |
| 310 | IPA80R310CE | | |

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## Revision History

### Major changes since the last revision

| Page or Reference | Description of change |
|---|---|
| -- | First Release |
| p. 16/17 | Update of Portfolio |
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## Revision History

### Major changes since the last revision

| Page or Reference | Description of change |
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