Application Note AN 2012-03
V1.1 March 2012

Infineon OptiMOS™ Power MOSFET Datasheet Explanation

Infineon Technologies Austria AG
Power Management and Multimarket
Application Engineer
Alan Huang

Infineon OptiMOS™
Power MOSFET Datasheet Explanation

Edition 2012-03-16
Published by
Infineon Technologies Austria AG
9500 Villach, Austria

Attention please!

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMEN-TATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office. Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

AN 2012-03
Revision History: date (12-03-16) , V1.1
Previous Version: V1.0
Authors: Alan Huang, Power Management & Multimarket

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: [Alan.Huang@infineon.com]

Table of contents

1 Introduction

A datasheet is the most important tool for the electronics engineer to understand a Power MOSFET device and to fully appreciate its intended functionalities. Due to a great amount of information a datasheet offers, it is sometimes deemed to be complicated and a difficult document to comprehend. Furthermore important parameters can be often missed. This could lead to numerous problems, for example, device failure, PCB re-design, project delay, etc. The document provides a general guideline about how to read and understand a datasheet with all its parameters and diagrams.

This application note describes Infineon's OptiMOS™ Power MOSFET datasheets in detail. OptiMOS™ is the trademark for Infineon's low voltage (up to 300V) Power MOSFET product line. This document provides background information on each specification parameter and explanation on each of the specification diagrams. It aims to help the designer to acquire a better understanding of the data sheet.

The parameters and diagrams mentioned in the datasheet provide a complete picture of a MOSFET. With such information, the designer should be able to understand the device's intended operation, to determine the operational limits of the device, and to compare quantitatively against different devices.

This document explains the interaction between the parameters and the influence of temperature or gate voltage on these parameters.

This document is merely aimed to provide clear explanations of the datasheet figures. For design recommendation, please go to www.infineon.com or contact Infineon team.

2 Datasheet Parameters

Datasheets might be deemed hard to analyze due to its large amount of information in a rather compact format. Instead of reading the datasheet line by line, it is suggested for the reader to look at each topic separately. Thus, this section clearly divides datasheets into smaller segments in order to avoid causing confusion for the reader. Each sub-section presents a single datasheet diagram and its relevant parameters.

Note: This document uses diagrams and parameters from IPP029N06N datasheet rev2.0 as examples. For the latest version of Infineon OptiMOS™ datasheets please refer to our OptiMOS™ (20V – 300V) webpage.

2.1 Power dissipation

The first diagram included in the datasheet is the power dissipation versus case temperature chart (Figure1). At a certain case temperature, the maximum allowable power dissipation is governed as illustrated.

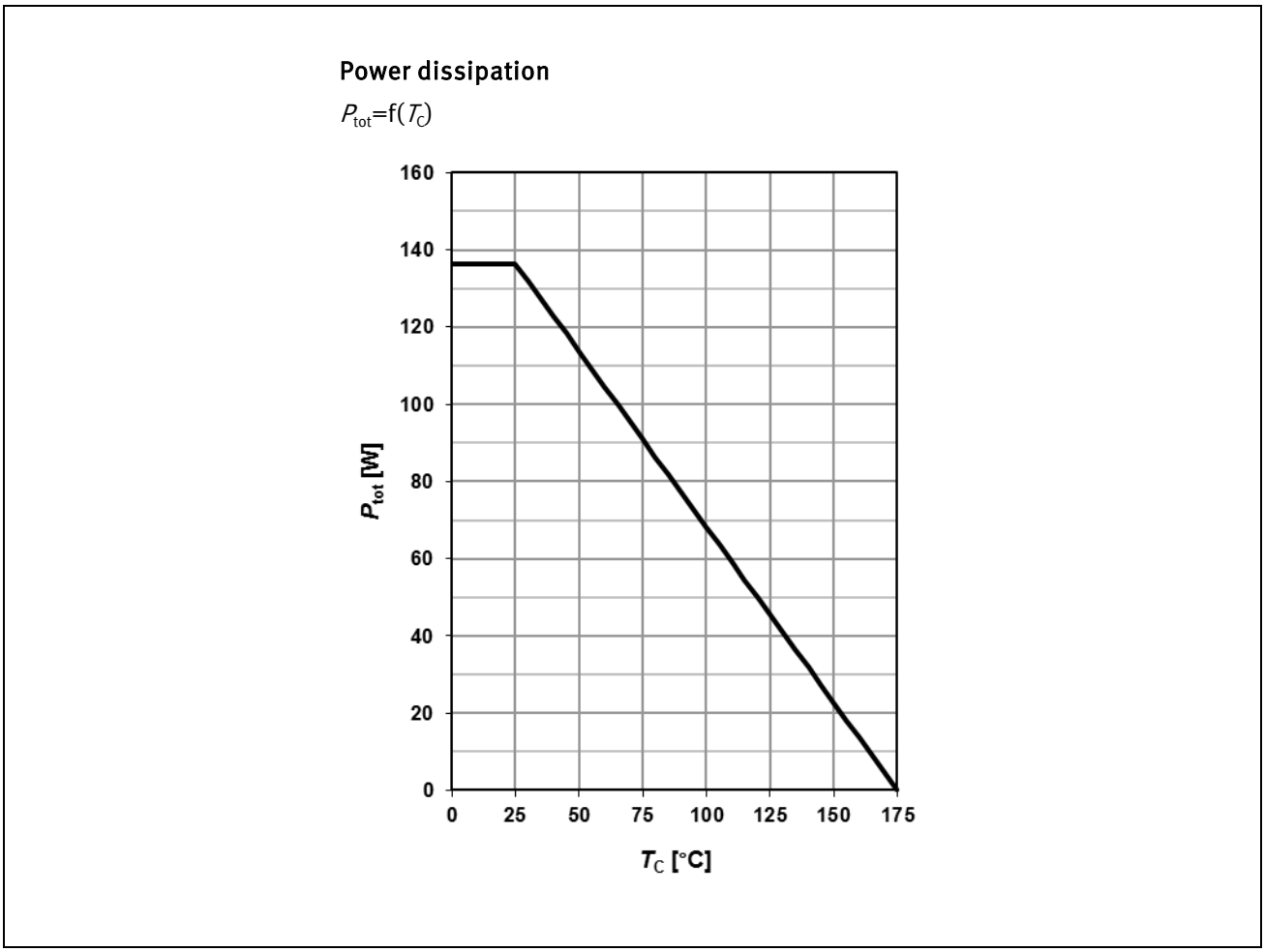


Figure 1 Power dissipation P_{tot} = f(T_C)

There are two power dissipation parameters listed in the datasheet – total junction-to-case and total junction-to-ambient power dissipation. These two numbers can be obtained using eq. (1) and (2).The junction-to-case thermal resistance is material and dimension dependent. With increasing case temperature, the allowable power dissipation decreases

$$(1) \qquad P_{tot}(T_C) = \frac{T_j - T_C}{R_{thJC}}$$

$$(2) \qquad P_{tot}(T_A) = \frac{T_j - T_A}{R_{thJA}}$$

Using these examples, the maximum power dissipation with the highest allowable temperature increase can be calculated. Eq. (3) demonstrates how the numbers in the example (as in Figure 2) were derived.

$$(3) \qquad P_{tot}(T_C)_{\max} = \frac{(175-25)K}{1.1\,K/W} = 136W \qquad P_{tot}(T_A)_{\max} = \frac{(175-25)K}{50\,K/W} = 3.0W$$

Note: The temperature difference in unit K is the same as in unit °C.

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	136	W
		T_A=25 °C, R_{thJA}=50 K/W[2)]	3.0	

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Figure 2 Maximum ratings for P_{tot} (datasheet)

The junction-to-ambient thermal resistance is layout dependent; therefore, in most cases, a footnote regarding the junction-to-ambient thermal resistance is included. It specifies the condition where the specified R_{thJA} rating is estimated.

2.2 Drain current

The datasheet specifies the maximum continuous drain current (I_D) under different operating conditions and the pulsed drain current ($I_{D,pulse}$) as in Figure 3. The maximum pulsed drain current is specified at 4 times the maximum continuous drain current. As the pulse width increases, the pulsed drain current rating decreases due to the thermal characteristics of the device. This can be clearly observed in the safe operating area diagram in Section 2.3.

Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	100	A
		V_{GS}=10 V, T_C=100 °C	100	
		V_{GS}=10 V, T_C=25 °C, R_{thJA} =50K/W [2)]	24	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	400	

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Figure 3 Maximum ratings for I_D (datasheet)

When the maximum continuous drain current depends solely on the maximum power dissipation (Section 2.1), the maximum I_D would be defined by the rearranged Power Law ($P = I^2 * R$). Substituting P in eq. (1) derives eq. (4), where the junction-to-case temperature difference (T_j - T_C), thermal resistance (R_{thJC}), and on-state resistance at maximum junction temperature ($R_{DS(on),Tj(max)}$) come into play.

See Section 2.9 for the temperature dependency of the on-state resistance.

(4)
$$I_D(T_C) = \sqrt{\frac{\frac{T_j - T_C}{R_{thJC}}}{R_{DS(on),Tj(\max)}}} \qquad I_D(25°C) = \sqrt{\frac{\frac{(175-25)K}{0.8\,K/W}}{0.0066\Omega}} = 169A$$

Note: The temperature difference in unit K is the same as in unit °C.

However, in reality, additional boundary conditions, governed by bond wire diameter, chip design and assembly, limit the maximum continuous drain current as illustrated in Figure 4. At T_C = 25°C, I_D is capped at 100 A instead of 169 A as calculated in eq. (4). This diagram illustrates that at low T_C, maximum I_D stays constant; at high T_C, it rolls off with acceleration until reaching zero at $T_C = T_{j(max)}$.

Note: This diagram only presents the limit of the continuous drain current limit. For pulsed current, refer to the safe operating area diagram in Section 2.3.

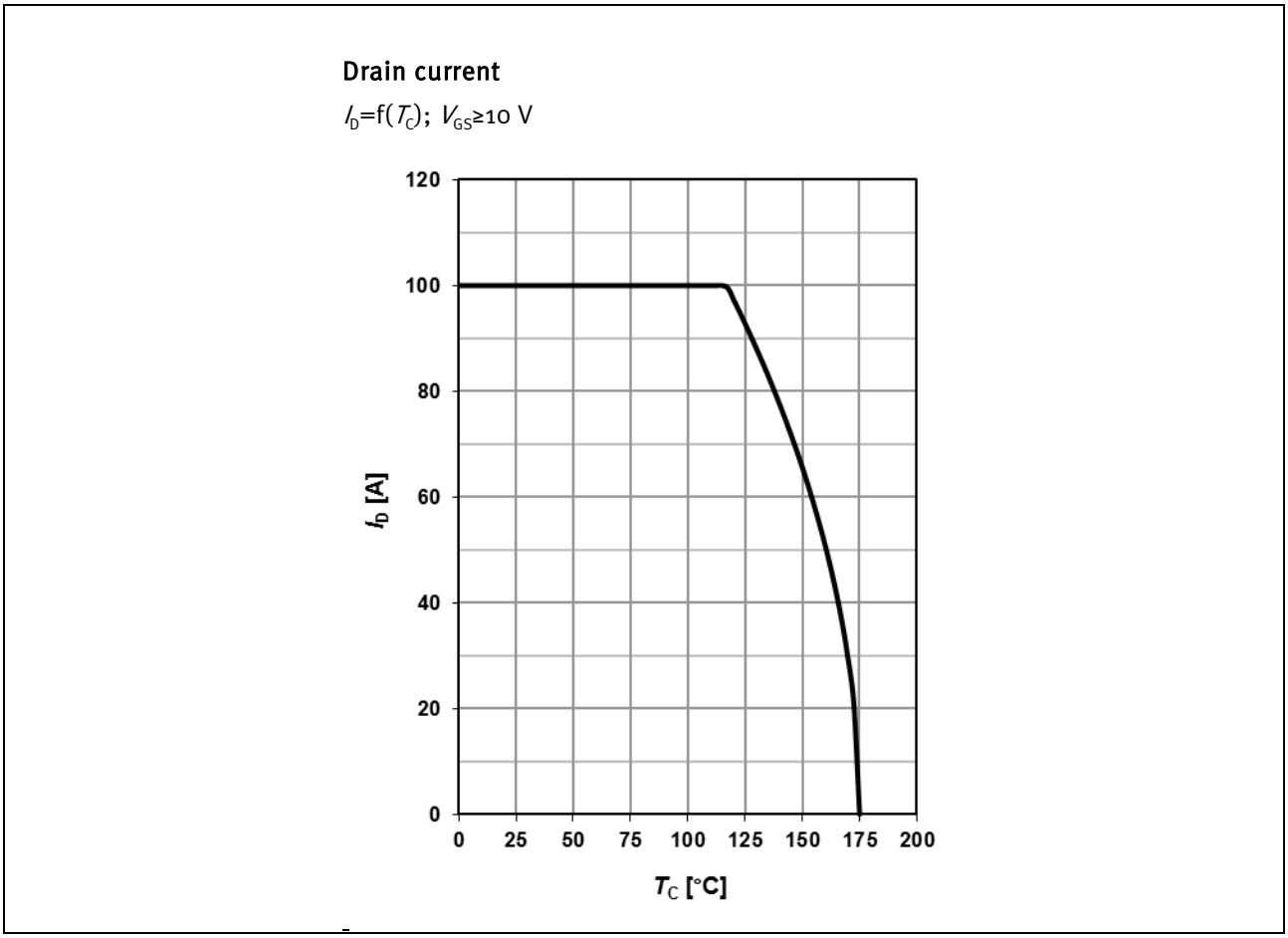


Figure 4 Drain current $I_D = f(T_C)$

2.3 Safe operating area

Figure 5 shows the drain current (I_D) as a function of the drain-source voltage (V_{DS}) with different pulse lengths. This is one of the most complicated but important figure that should not be ignored in the datasheet. This section briefly describes each region of operation and its boundary limits. In complementary to this short section, Infineon also provides a comprehensive application note regarding this topic - Linear Mode Operation and Safe Operating Diagram of Power MOSFETs, where details regarding the linear mode operation and the SOA diagram are discussed.

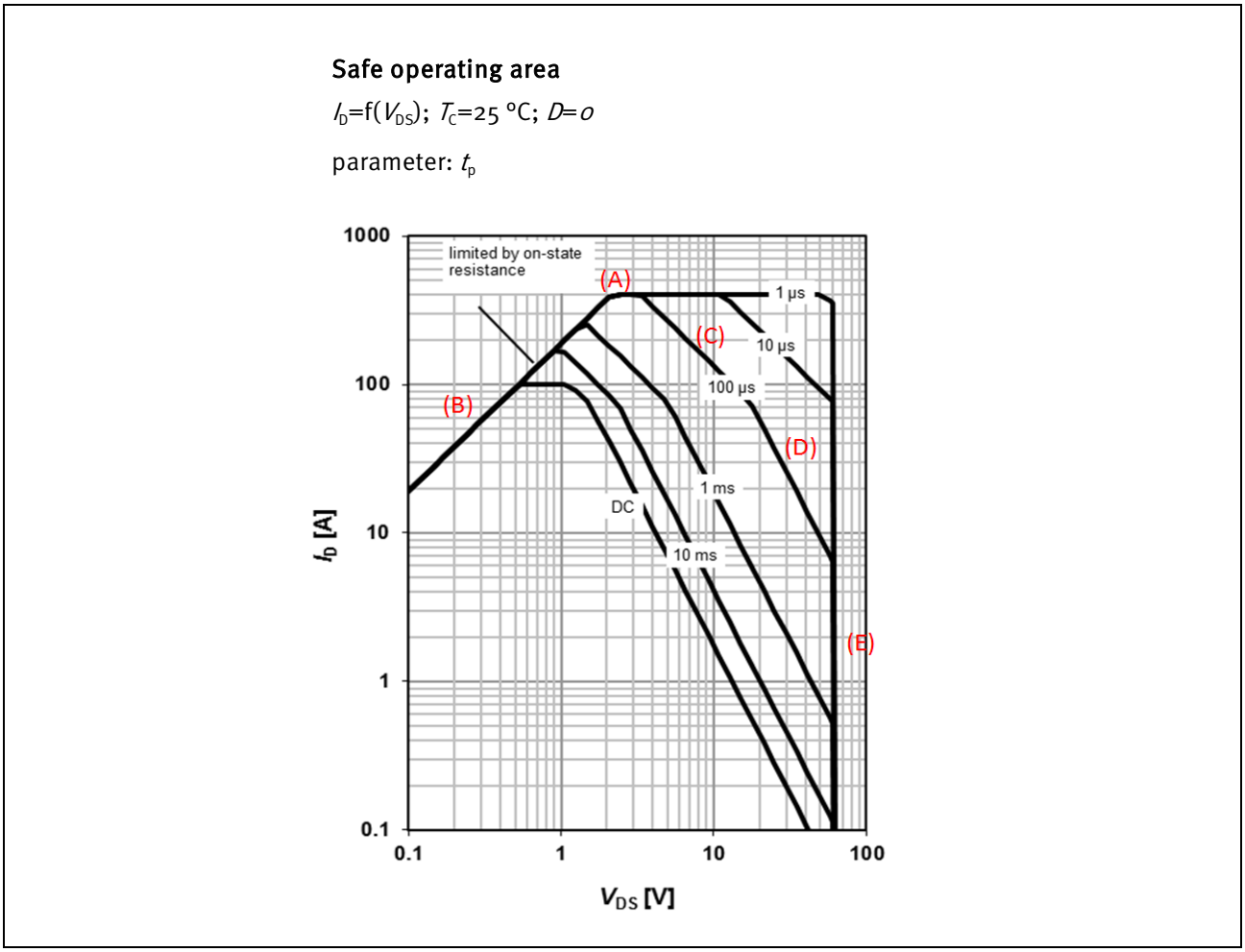


Figure 5 Safe operating area I_D=f(V_{DS})

Note: The SOA diagram is defined for single pulses. Mathematically, the duty cycle of a single pulse is equivalent to zero (D=0) as the period (T) is infinite.

There are several limitations in this diagram and labels (A) to (E) are used to explain the boundary limits using the 100 µs curve as an example.

A) The top line is a limit of the maximum pulsed drain current.

B) This area is limited by the on-state resistance $R_{DS(on)}$ at maximum junction temperature.

C) At fixed T_C, the device is limited by the constant power line in this area. Depending on the applied power pulse width, the maximum power loss varies according to the thermal impedance variation. Next section (Section 2.4) discusses about maximum transient thermal impedance at a different pulse length.

D) In linear mode operation, there is a risk of getting hot spots at low gate-source voltages due to thermal run away. This effect becomes more important for latest trench technologies with high current densities, where the “zero temperature coefficient” point of the transfer characteristic is shifted to higher drain currents. More information can be found in the application note mentioned above Linear Mode Operation and Safe Operating Diagram of Power MOSFETs

With the hot spot effect for higher V_{DS} and longer pulse times considered, the SOA characteristic has a different slope in this region (eq. (5)).

$$I_D(V_{DS}) = \frac{T_j - T_C}{V_{DS} * Z_{thJC}} \quad (5)$$

E) The maximum breakdown voltage ($V_{(BR)DSS}$), which is determined by the technology, limits the SOA curve on the right hand side.

2.4 Maximum transient thermal impedance Z_{thJC}

Thermal impedance (Z_{th}) consists of two components – thermal resistance (R_{th}) and thermal capacitance (C_{th}).

R_{thJC} is the thermal resistance from the junction of the die to the case. The heat through this path is generated by the power loss in the device itself. This parameter is directly linked to the temperature that the chip reaches relative to the case.

Transient thermal impedance (Z_{thJC}) takes also the heat capacity (C_{thJC}) of the device into account. It is used to estimate the temperature resulted from transient power loss.

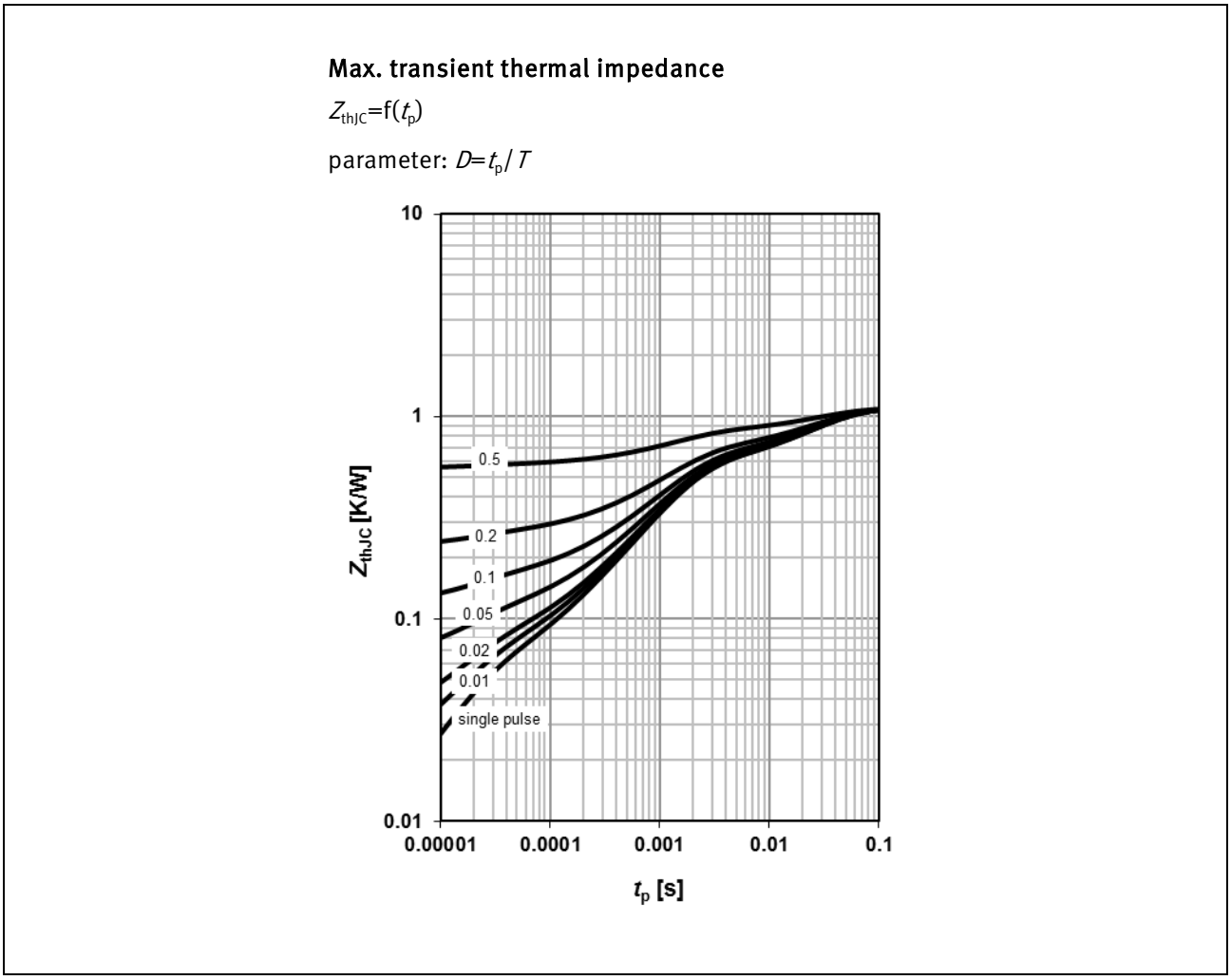


Figure 6 Maximum transient thermal impedance $Z_{thJC}=f(t_p)$

Figure 6 shows that for each specified duty cycle ($D=t_p/T$), the variation of the thermal resistance (Z_{thJC}) as a function of the loading time t_p (pulse width).

To dissipate the heat out of the device, it has to pass several different layers of its characteristic thermal resistances and capacitances. As a result, depending on the pulse width, either the thermal resistance or the thermal capacitance dominates the behavior of the device. The increase of the junction temperature can be calculated as shown in eq. (6). Before power pulse is applied, $T_{j,start}$ is equal to T_C at thermal equilibrium.

$$T_j = T_{j,start} + \Delta T_j = T_{j,start} + Z_{thJC}(t_P, D) * P_{tot} \quad (6)$$

The maximum of R_{thJC} is also listed in the table section of the datasheet as in Figure 7.

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	-	1.1	K/W

Figure 7 Thermal characteristics

2.5 Typical output characteristics

Typical output characteristics graph, Figure 8, illustrates the drain current I_D as a function of the drain-source voltage V_{DS} at given gate-source voltages V_{GS} and chip temperature T_j of 25 °C.

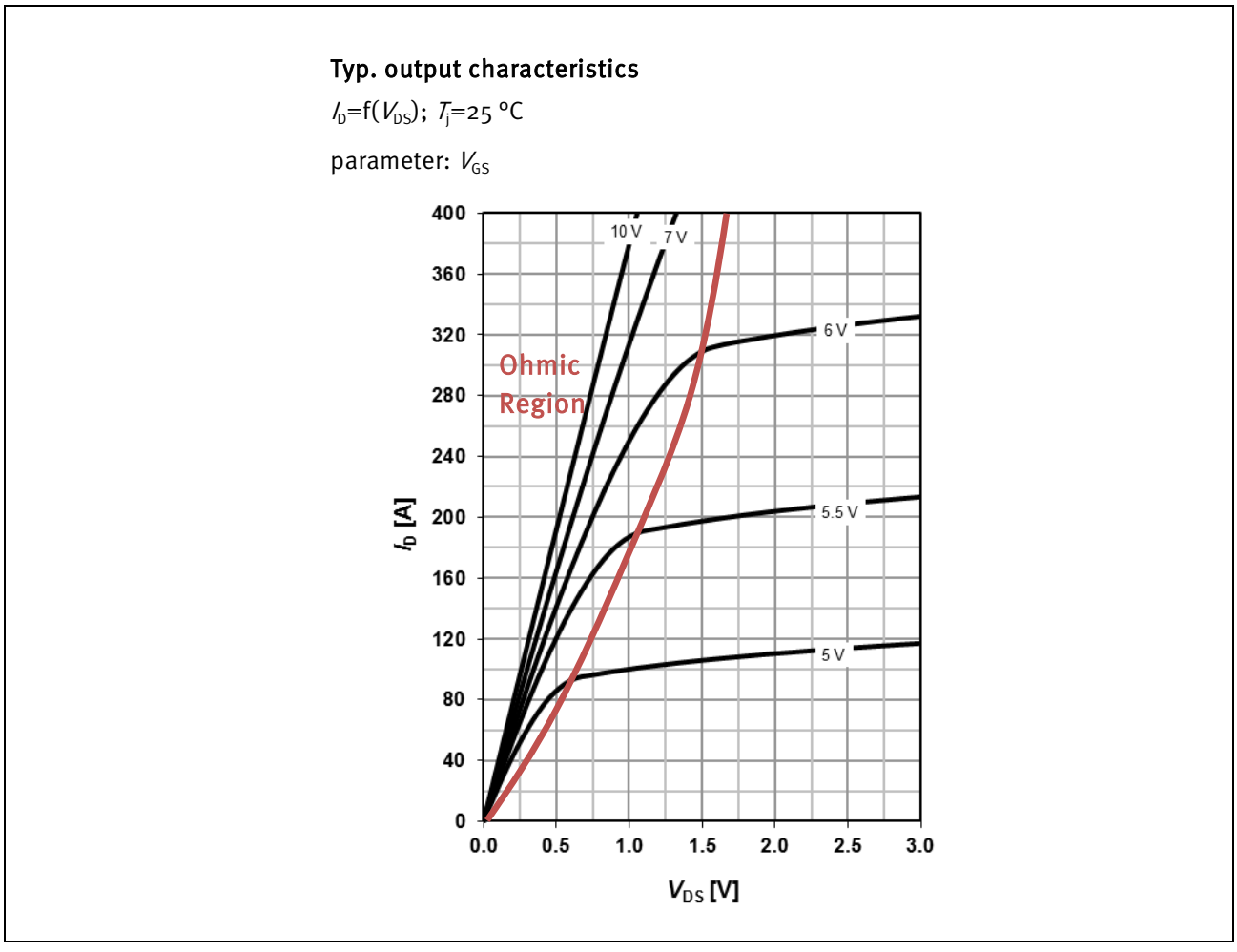


Figure 8 Typical output characteristics $I_D=f(V_{DS})$

For optimal efficiency, the MOSFET should be operated in the “ohmic” region, which is shown in Figure 8 (Note that this diagram includes current range up to the maximum pulsed current limit). This boundary line between ohmic and saturation region is defined by $V_{DS} = V_{GS} – V_{GS(th)}$. At any given gate-source voltage, the drain current of the MOSFET saturates beyond the ohmic region. As the operating point goes into the saturation region, any further increase in drain current leads to a significant rise in drain-source voltage (linear operation mode) and as a result conduction loss increases. In this case, if the power dissipation is not limited, the device may fail.

Gate-source voltage (V_{GS}) is deterministic to the MOSFET’s output characteristics as shown in the diagram. The allowable range of V_{GS} is specified in the table section of the datasheet as shown in Figure 9. The effects of gate-source voltage on drain-source on-state resistance will be discussed in the Section 2.6.

Gate source voltage	V_{GS}		±20	V

Figure 9 Gate source voltage limit

2.6 Drain-source on-state resistance as a function of Drain current

In Figure 10, for each gate-source voltage, the drain source on-state resistances over drain current curve is directly calculated from the typical output characteristic diagram (Figure 8a) using Ohms Law, eq. (7).

$$R_{DS(on)}(I_D) = \frac{V_{DS}}{I_D} \quad (7)$$

Notice that V_{GS} plays an important role in this diagram. The on-resistance curves change tremendously while a different level of V_{GS} is applied. To fully turn on a device, a V_{GS} of 10V is required. For normal level devices, 10V is recommended for efficiency-optimized low drain-source on-state resistance. For logic level devices, shifted $R_{DS(on)}$ curves (Figure 8b) make a lower-than-10V V_{GS} acceptable for fast switching applications, whereas the conduction loss due to higher $R_{DS(on)}$ is less critical. An example application could be synchronous rectification at low load.

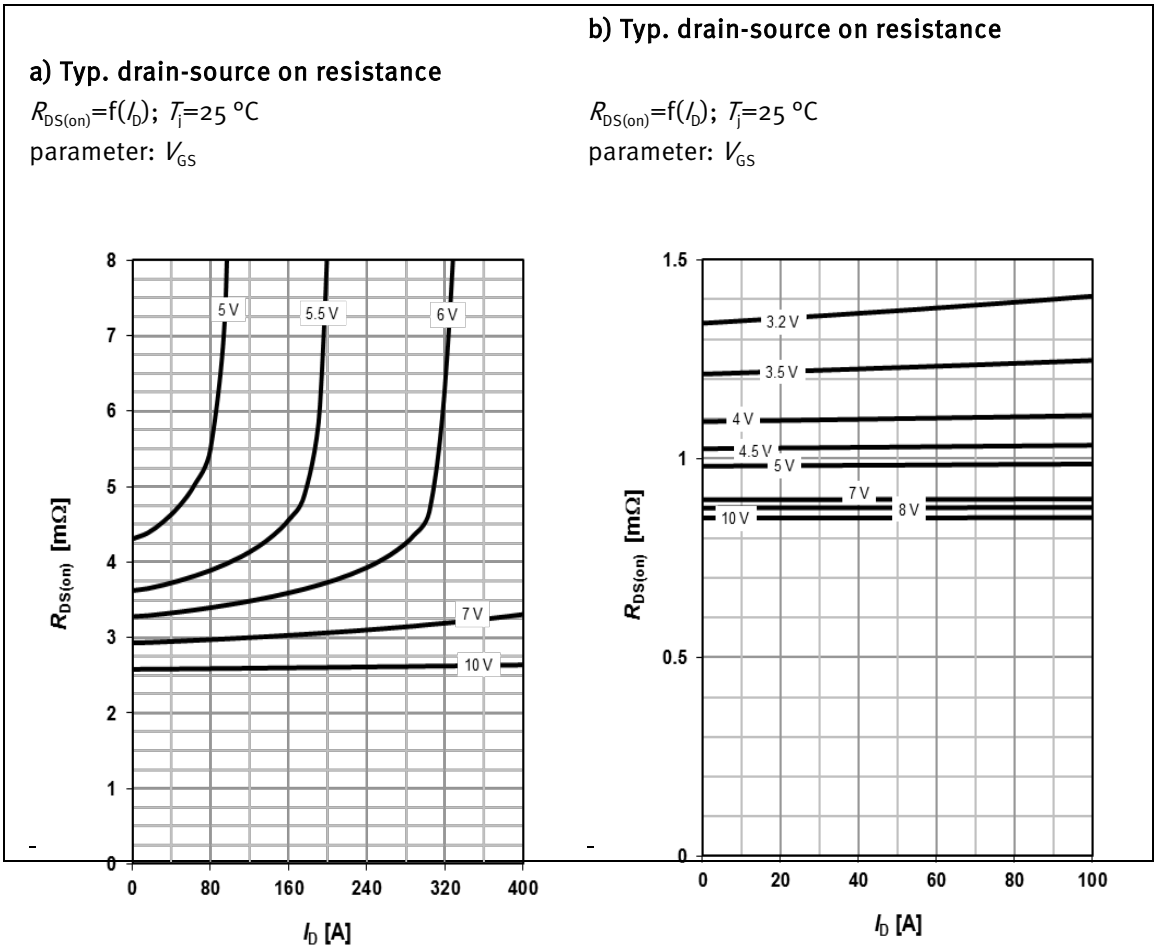


Figure 10 Typical drain-source on-state resistance $R_{DS(on)}$=f(I_D) for a) normal level device and b) logic level device (BSC010N04LS)

2.7 Transfer characteristics

This diagram shows the typical drain current as a function of the applied gate-source voltage. Normally the graphs at different junction temperatures are given. For example, Figure 11 has one curve at 25°C and the other at 175°C. All the graphs should intersect at one point, the so-called temperature stable operating point.

When the gate-source voltage applied to the MOSFET is below this point (in the example V_{GS} < 5.2V), the MOSFET operates with a positive temperature coefficient, meaning with increasing junction temperature the drain current will also increase. Operating at this condition with constant V_{GS} should be avoided due to the possibility of thermal runaway.

Beyond the temperature stable operating point the temperature coefficient is negative, meaning that with increasing junction temperature the drain current decreases. The MOSFET self-limits its current handling capability at high temperatures. Operating in this region is generally safe as long as the junction temperature stays within specification.

Note: For current level higher than the specified maximum continuous conduction current, only pulsed currents are allowed.

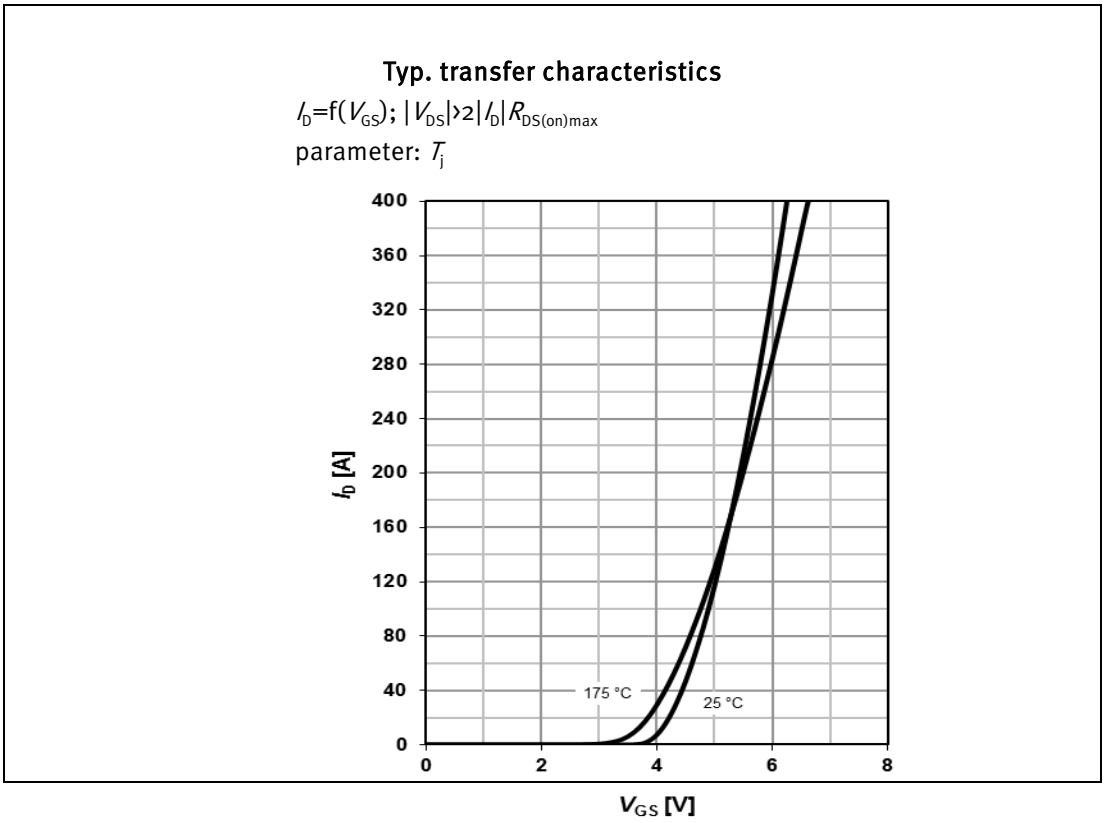


Figure 11 Typical transfer characteristics I_D=f(V_{GS})

To approximate the maximum or minimum rating of this characteristic the curves can be moved in parallel according to the min-max ratings of the threshold voltage (+/- 1V for normal level devices).

2.8 Forward transconductance

Transconductance (g_{fs}) is a measure of sensitivity of the drain current to the variation of the gate-source voltage. Figure 12 shows the typical forward transconductance as a function of drain current at junction temperature of 25°C.

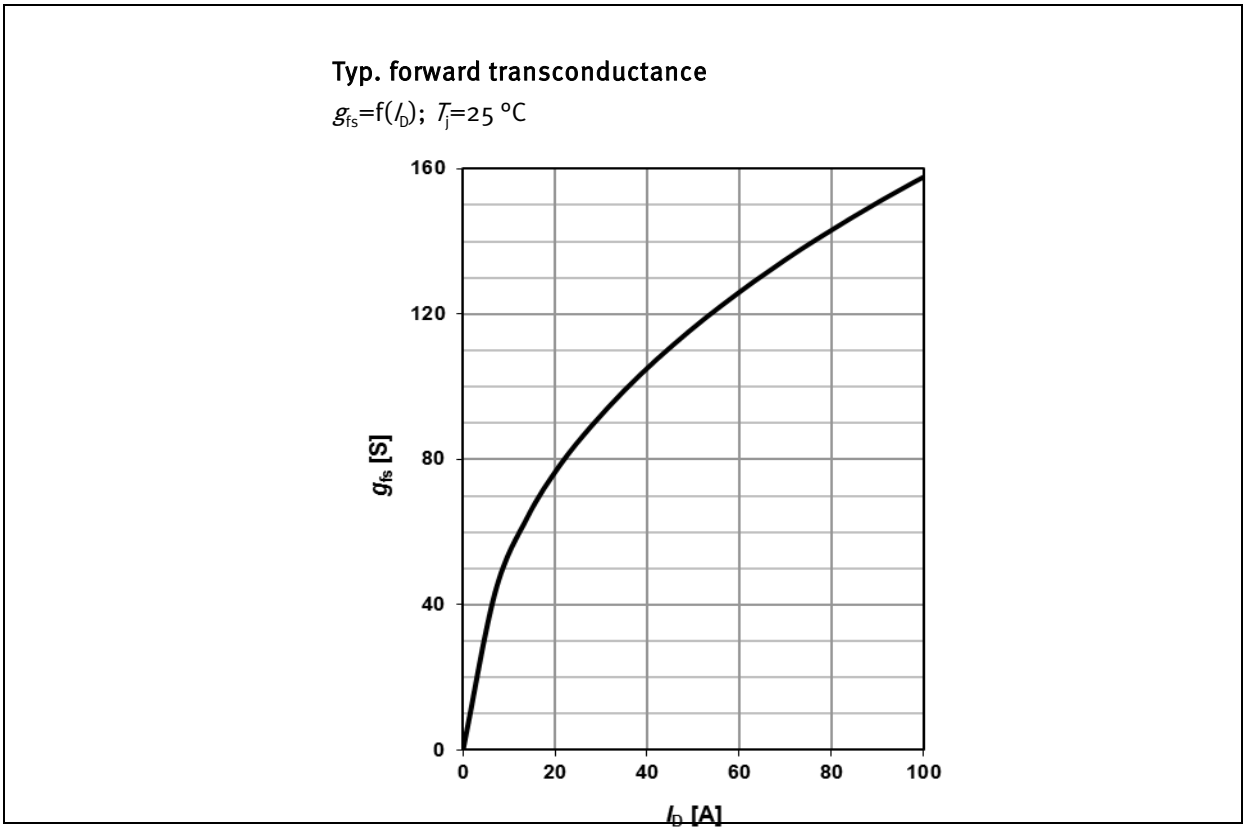


Figure 12 Typical forward transconductance $g_{fs}=f(I_D)$

The forward transconductance (g_{fs}) can be calculated from the typical transfer characteristics diagram from Figure 11 using eq. (8).

$$g_{fs}(I_D) = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}} \quad (8)$$

The minimum and typical values of g_{fs} at the test current are listed in Figure 13.

Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A	80	160	-	S

Figure 13 Transconductance in Static Characteristics section

2.9 Drain-source on-state resistance

The drain-source on-state resistance is one of the key parameters of a MOSFET. In the datasheet there are two sections dealing with this parameter. In the table section, the typical and maximum ratings at room temperature are listed as in Figure 14. These values are determined during production testing at the specified conditions.

For a surface-mount device (SMD), the resistance is measured between the source pin and the backside drain contact of the device. For a through-hole package, the $R_{DS(on)}$ is specified between the drain and source pins at a defined soldering point (approx. 4.5 mm lead lengths for TO-220), which results in an additional 0.3 mΩ of parasitic resistance.

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=100 A	-	2.7	2.9	mΩ
		V_{GS}=6 V, I_D=25 A	-	5.4	-	

Figure 14 Drain to Source on-state resistance

In addition to the table, the datasheet contains a diagram of the on-state resistance as a function of the junction temperature (Figure 15). The higher the junction temperature, the higher the $R_{DS(on)}$ will be. Due to this positive temperature coefficient, it is possible to use multiple devices in parallel. Note that typical and maximum $R_{DS(on)}$ values are shown in the diagram.

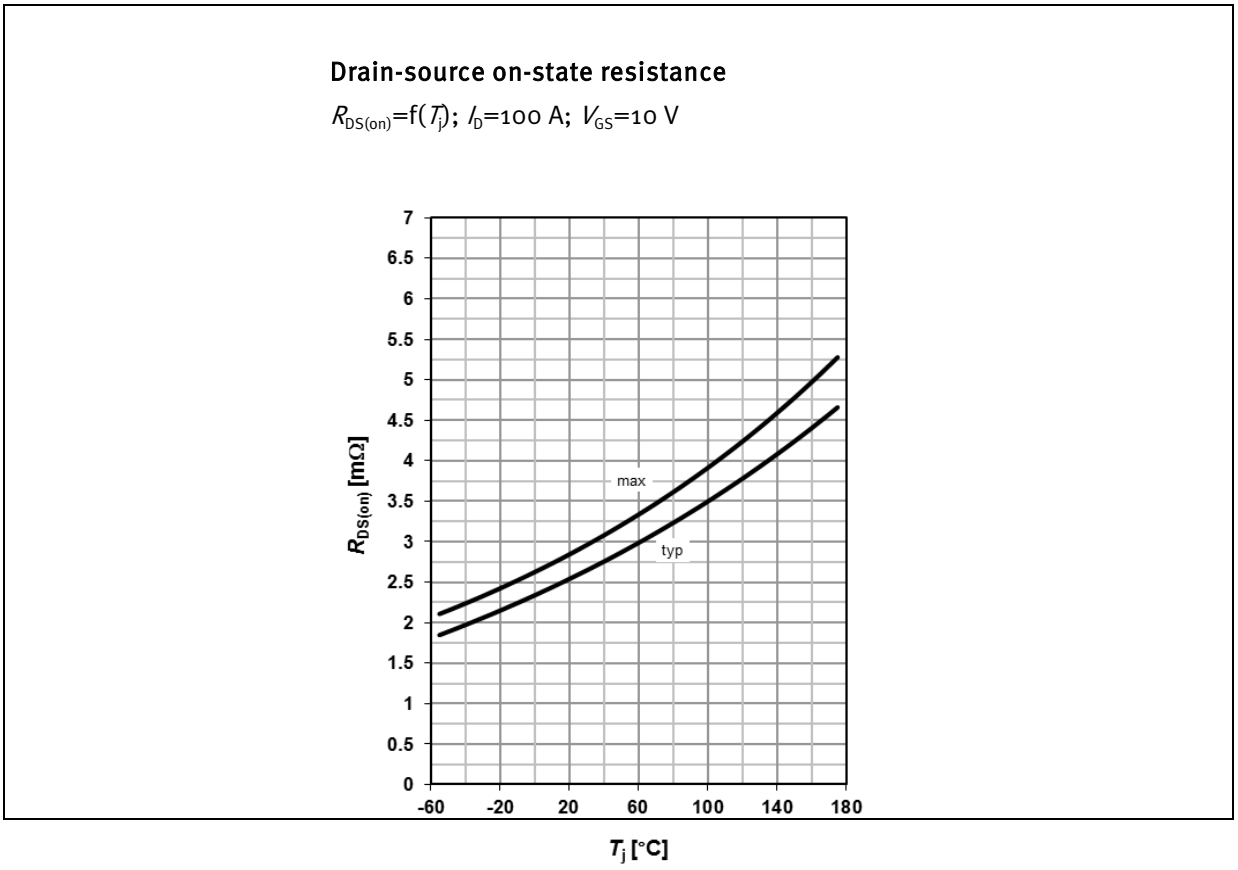


Figure 15 Typical drain-source on-state resistance $R_{DS(on)}$=f(T_j)

To calculate the dependency of the junction temperature, the following formula is used:

$$R_{DS(on)}(T_j) = R_{DS(on),25°C} \cdot (1 + \frac{\alpha}{100})^{T_j - 25°C} \quad (9)$$

α is a technology dependent constant. For OptiMOS™ Power MOSFET, α value of 0.4 can be used for $R_{DS(on)}$ approximation.

2.10 Gate threshold voltage

The gate threshold voltage defines the required gate-source voltage at a specified drain current. During the production, the threshold voltage is measured at room temperature with V_{DS} = V_{GS} and test drain currents in the µA range. The minimum, typical, and maximum ratings are specified in the table as shown in Figure 16.

Gate threshold voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=75 µA	2.0	2.8	3.6	V

Figure 16 Threshold voltage

The threshold voltage decreases with increasing junction temperature. This dependency at typical condition as specified in the table section is illustrated in the Figure 17.

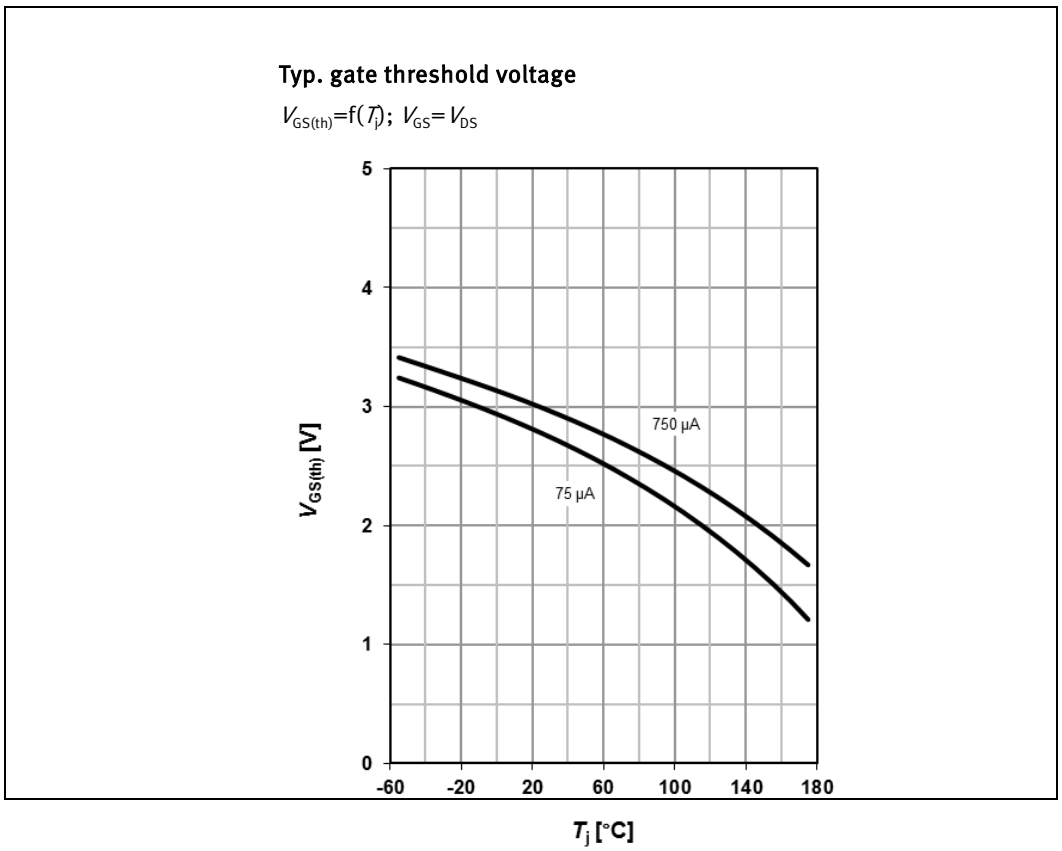


Figure 17 Typical gate threshold voltage $V_{GS(th)}$=f(T_j)

2.11 Capacitances

The capacitances of the MOSFETs are defined both in the table and the diagram sections of the data sheet. The table specifies the ranges for the capacitances (Figure 18), and the diagram shows the dependencies of the drain-source voltage on the capacitances (Figure 19).

The gate-source, gate-drain, and drain-source capacitances cannot be measured directly; however, they can be calculated from the measurable input, output, and reverse transfer capacitances. The three equations (10) below describe the relationships among them.

$$C_{iss} = C_{GS} + C_{GD}$$
$$C_{oss} = C_{DS} + C_{GD} \quad (10)$$
$$C_{rss} = C_{GD}$$

Dynamic characteristics

Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	-	4100	-	pF
Output capacitance	C_{oss}		-	980	-	
Reverse transfer capacitance	C_{rss}		-	39	-	

Figure 18 Dynamic characteristics: capacitances

In the diagram section of the datasheet, the typical capacitances as a function of the drain-source voltage are defined. Clear dependencies of the voltages are shown for reverse (C_{rss}) and output (C_{oss}) capacitances. This is due to the change in the space charge region during the switching transition of the MOSFET

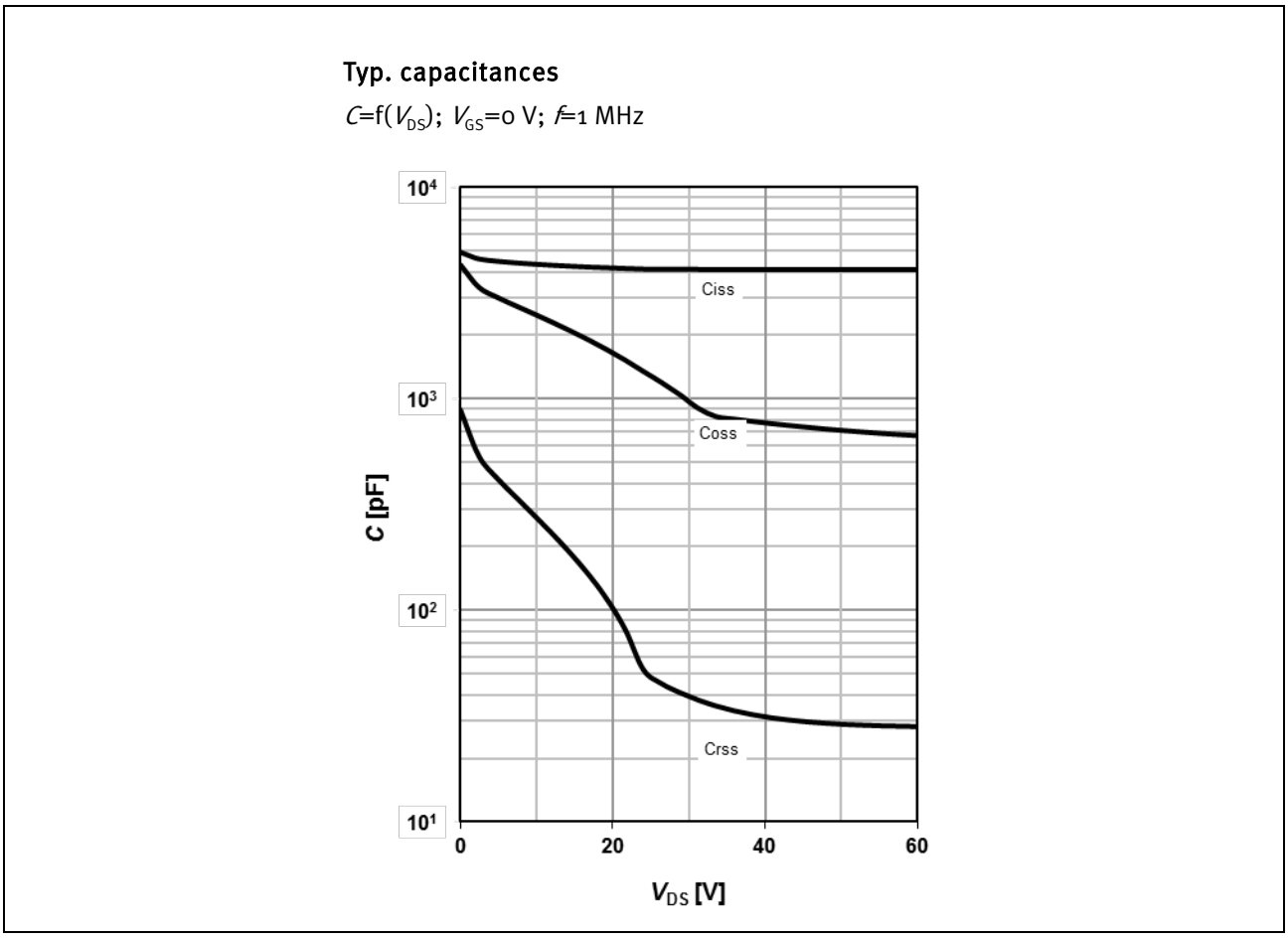


Figure 19 Capacitance C=f(V_{DS})

2.12 Reverse diode characteristics

The characteristics of the MOSFET's body diode are given both in the table and the diagram sections.

In the table section, as in Figure 20, the minimum, typical and the maximum values of the diode parameters are given.

Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	120	A
Diode pulse current	$I_{S,pulse}$		-	-	480	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=100 A, di_F/dt=100 A/µs	-	37	-	ns
Reverse recovery charge	Q_{rr}		-	44	-	nC

Figure 20 Diode characteristics

- Diode continuous forward current: The maximum permissible DC forward current of the body diode at the specified case temperature T_C =25°C, which is normally equal to the MOSFET's continuous current limit.
- Diode pulse current: The maximum permissible pulsed forward current of the inverse diode at the specified case temperature T_C =25°C, which is normally equal to the MOSFET's pulse current limit.
- Diode forward voltage: The source-to-drain voltage during diode's on-state (MOSFET off-state) at test diode forward current (I_F), zero gate-source voltage (V_{GS}) and junction temperature (T_j) of 25°C.
- Reverse recovery time: The time needed for the reverse recovery charge to be removed. The graphical explanation of t_{rr} is given in Figure 21.
- Reverse recovery charge: The charge stored in the diode during its on-state. This charge needs to be completely removed immediately following the diode conduction period before the diode's blocking capability resumes as shown in Figure 21. The higher the switching rate of the current (di/dt on the order of 100A/µs or more), the higher the reverse recovery charge. The graphical explanation of Q_{rr} is also given in Figure 21.

Figure 21 demonstrates that during device turn-on, the diode forward current (I_F) drops from the on-state drain current ($I_{D(on)}$) to beneath zero. I_F then recovers back to zero before the drain-source voltage (V_{DS}) starts to decrease (discharging of C_{oss}). Reverse recovery occurs during the time I_F is below zero, and the charge (Q_{rr}) can be approximated using the area between I_F negative and the zero current line.

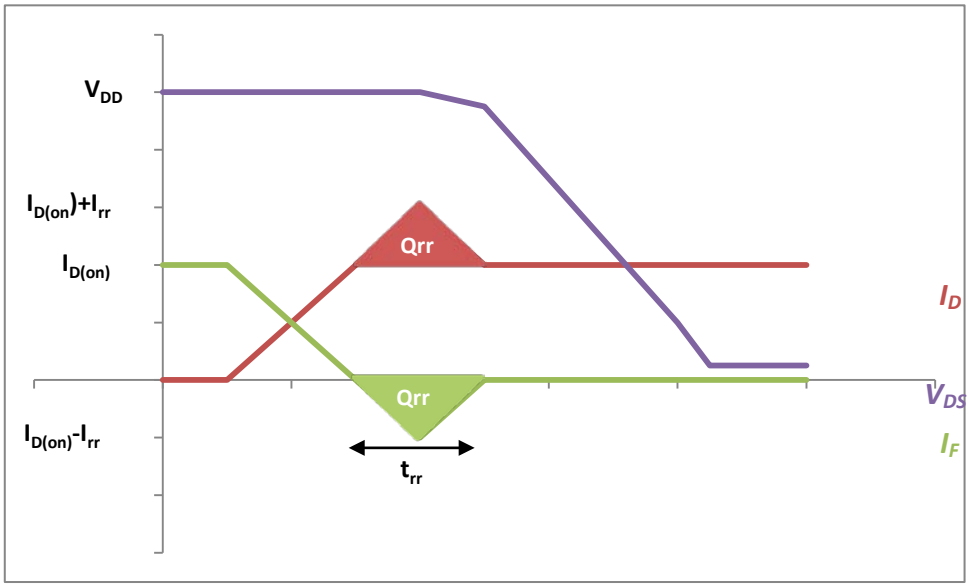


Figure 21 Explanation of Q_{rr} and t_{rr}

Figure 22 illustrates the typical diode forward currents, I_F, of the functions of source-drain voltages, V_{SD}, at junction temperatures, T_j, of 25°C and 175°C.

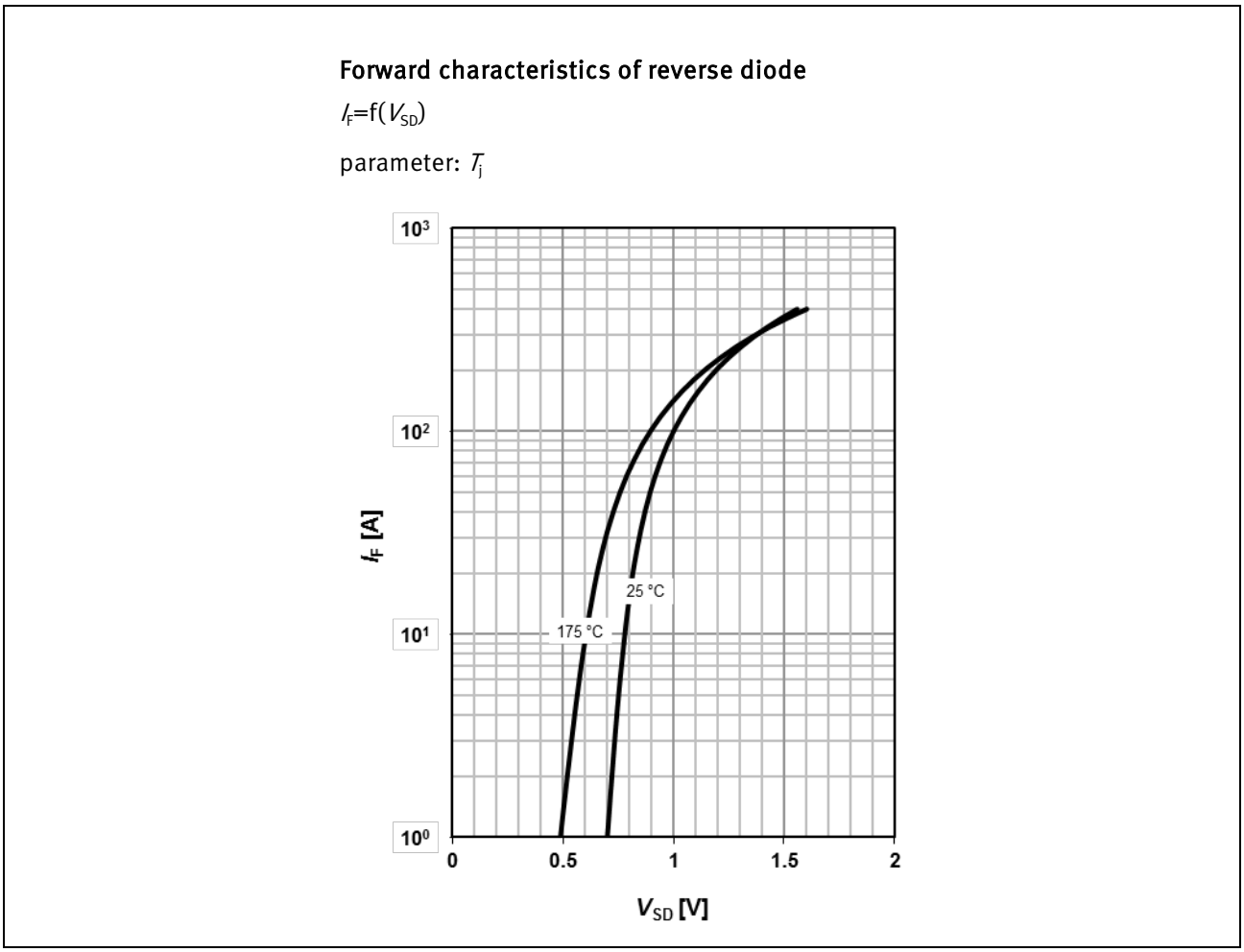


Figure 22 Typical forward diode characteristics I_F=f(V_{SD})

2.13 Avalanche characteristics

The dependence of the pulsed avalanche current I_{AV} on the time in avalanche t_{AV} is presented in Figure 23. Operating MOSFET under the conditions below the curve is allowed with consideration of the maximum junction temperature. This characteristic is bounded by the total avalanche energy of a pulse. The longer the avalanche pulse, the lower the maximum allowed avalanche current.

This figure also includes multiple curves for different junction temperatures at the start of the avalanche event. It shows that with higher temperature, the avalanche capability decreases.

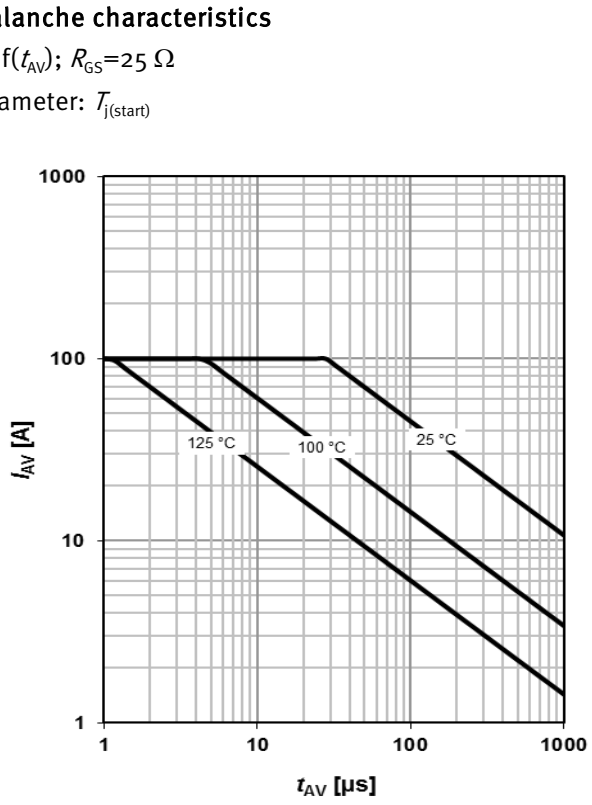


Figure 23 Avalanche characteristics I_{AS}=f(t_{AV})

The table section of the datasheet provides the maximum single-pulse avalanche energy at a given avalanche current and the maximum allowable single-pulse current in avalanche.

Avalanche energy, single pulse	E_{AS}	I_D=100 A, R_{GS}=25 Ω	110	mJ

Figure 24 Avalanche energy and current

2.14 Drain-source breakdown voltage

The diagram in Figure 25 shows the linear temperature dependence of the typical minimum value of the drain-to-source breakdown voltage over the complete allowable temperature range (-55°C…+175°C). The table as shown in Figure 26 gives the minimum value of the breakdown voltage at 25°C.

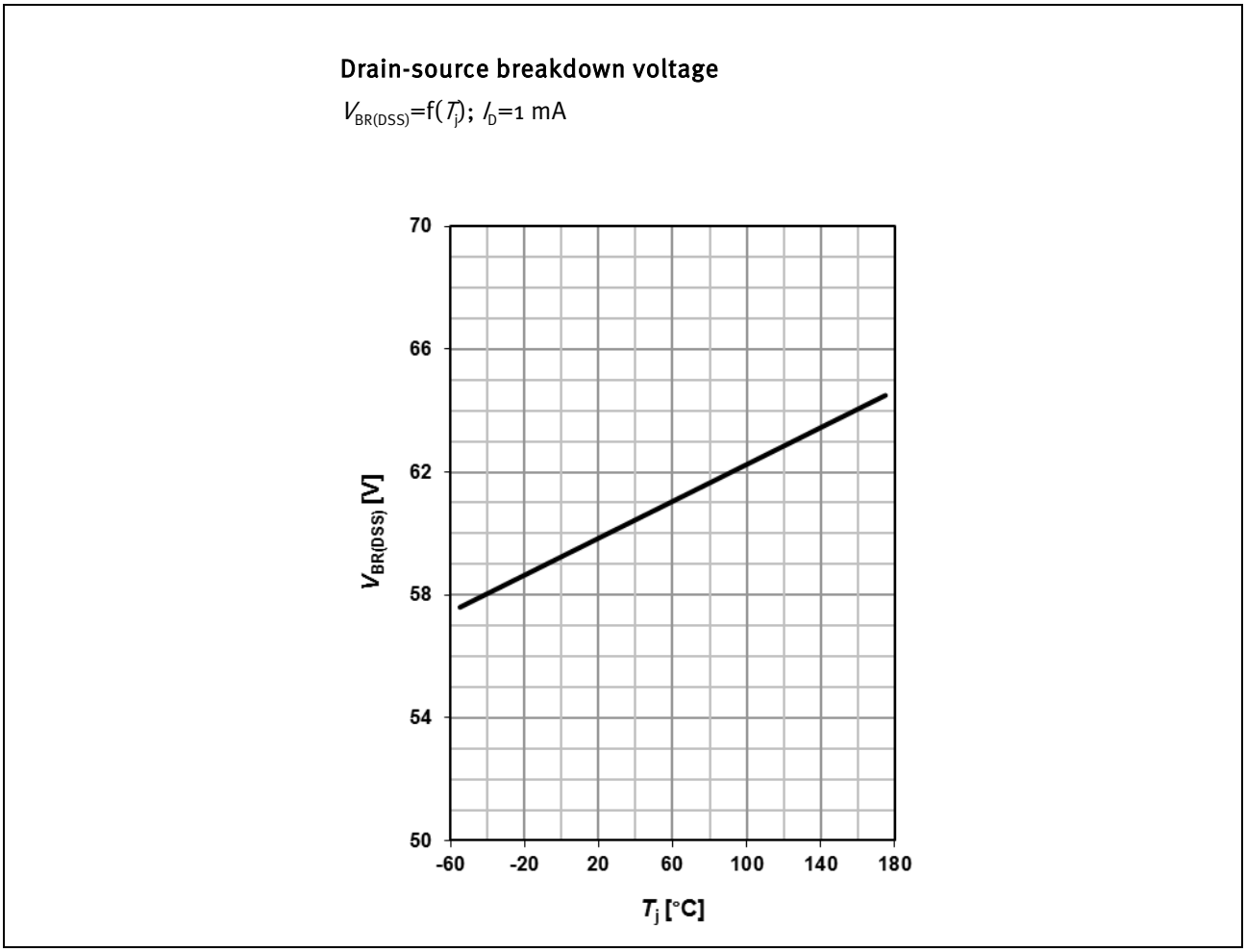


Figure 25 Drain-source breakdown voltage $V_{BR(DSS)}$=f(T_j)

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	-	-	V

Figure 26 Drain-source breakdown voltage $V_{BR(DSS)}$=f(T_j)

2.15 Typical gate charge

Figure 27 includes two diagrams: 1) typical gate charge diagram and 2) gate charge waveform.

The typical gate charge diagram shows the typical variation of the requisite gate charge to switch on a MOSFET at given gate-source voltages and drain-source supply voltages (V_{dd}). The on-state current is given as a parameter.

As indicated in gate charge waveform, the gate charge (Q_g) comprises the gate-source charge (Q_{gs}), the gate-drain charge (Q_{gd}), and the charge required to increase V_{GS} from the plateau to the desired V_{GS} level. Q_{gs} is the charge required for charging the gate-source capacitance (C_{GS}) to the plateau level. During this period, the drain current (I_D) rises up to the load value after the gate threshold voltage ($V_{gs(th)}$) has been reached. The drain-source voltage (V_{DS}) behaves differently based on different loads. For resistive loads, the drain-source voltage falls simultaneously with the rise of the drain current. For inductive loads, V_{DS} starts falling after the drain current reaches the load level. Before the voltage V_{DS} falls to its on-state value (V_{DS} = $R_{DS(on)}$ *I_D), the gate-to-drain capacitance (C_{GD}), the Miller capacitance, has to be discharged. This component is defined as the gate-to-drain charge (Q_{gd}).

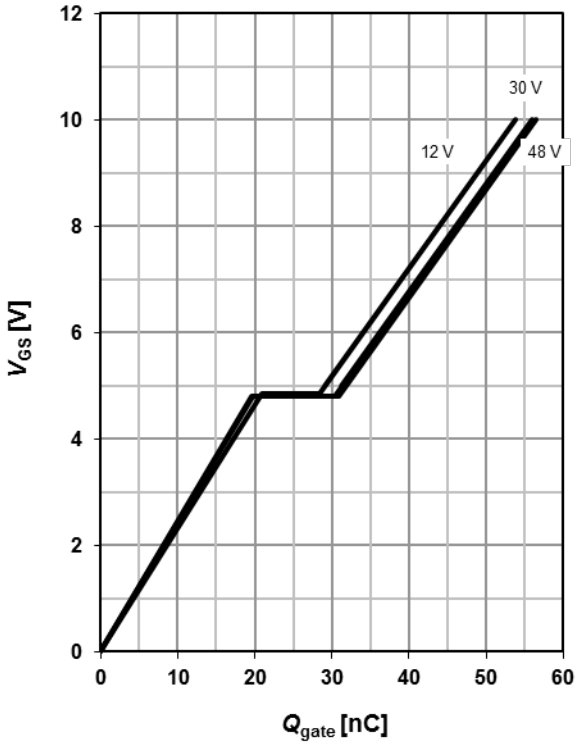
Q_{gs} and Q_{gs} are not sufficient to fully switch on the transistor, because the drain-source on-state resistance is not yet minimized. Only with a charge corresponding to a full gate-source voltage (typically V_{GS} = 10 V for both normal level and logic level MOSFETs), the full turn-on resistance is reached, and thus static loss is optimized. The complete gate-charge waveform changes with the drain-source voltage level (or the supply voltage level). The parameters relevant to gate charge are also listed in the table section as shown in Figure 28.

Note: The plateau level is not fixed. It varies with load conditions.

Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=100 A pulsed

parameter: V_{DD}



Gate charge waveforms

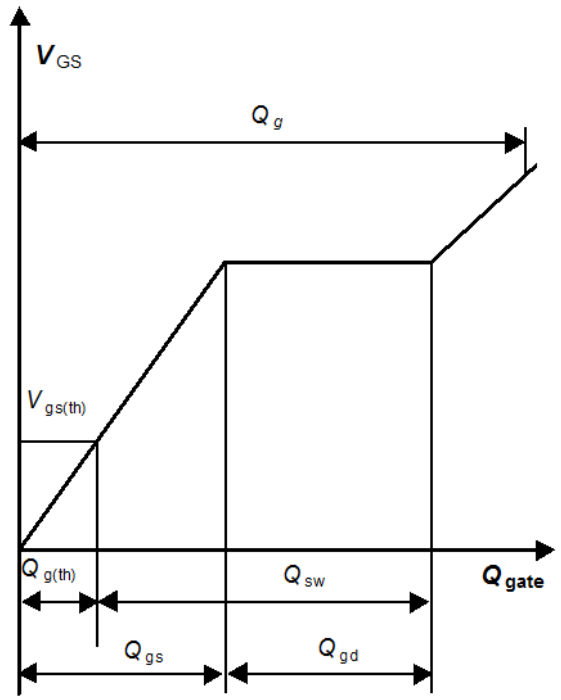


Figure 27 Typical gate charge V_{GS}=f(Q_{gate}) and gate charge waveforms

Gate Charge Characteristics[5]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V	-	20	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	11	-	
Gate to drain charge	Q_{gd}		-	11	-	
Switching charge	Q_{sw}		-	19	-	
Gate charge total	Q_g		-	56	-	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 10 V	-	49	-	nC
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V	-	65	-	

Figure 28 Gate charge and plateau voltage

2.16 Leakage Currents

There are two types of leakage currents specified for a MOSFET (Figure 29):

1) I_{DSS} is the drain-source leakage current at a specified drain-source voltage (typically the minimum drain-source breakdown voltage) and at V_{GS} = 0V.
2) I_{GSS} is the gate-source leakage current at a specified gate-source voltage (typically the maximum gate-source voltage) and at V_{DS} = 0V.

Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	-	0.5	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA

Figure 29 Leakage Currents

2.17 Other important parameters

2.17.1 Switching Times

Figure 30 shows the switching time parameters listed in the table section of the datasheet.

Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=100 A, R_G=3 Ω	-	17	-	ns
Rise time	t_r		-	15	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	8	-	

Figure 30 Switching Times

The turn-on time (t_{on}) of a MOSFET is the sum of the turn-on delay time ($t_{d(on)}$) and the rise time (t_r). $t_{d(on)}$ is measured between the 10% value of the gate-source voltage and the 90% value of the drain-source voltage. t_r is measured between the 90% value and the 10% value of the drain-source voltage.

The turn-off time (t_{off}) of a MOSFET is the sum of the turn-off delay time ($t_{d(off)}$) and the fall time (t_f). $t_{d(off)}$ is measured between the 90% value of the gate-source voltage and the 10% value of the drain-source voltage. t_f is measured between the 10% value and the 90% value of the drain-source voltage.

Figure 31 graphically defines the above mentioned parameters.

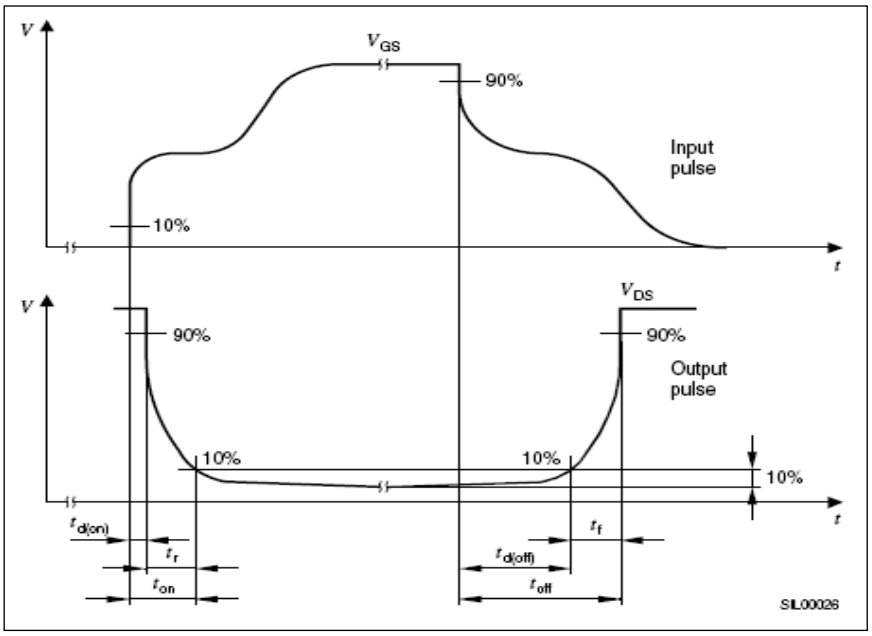


Figure 31 Definition of switching times

Note: this diagram is used for definition only and the real-life waveforms do not necessary look alike due to different application conditions. For a better representation of the switching waveform, please refer to gate charge waveform in Figure 27.

2.17.2 Gate resistance

Internal gate resistance is also listed in the datasheet as in Figure 32.

Gate resistance	R_G		-	1.3	-	Ω

Figure 32 Gate resistance

2.17.3 Additional maximum ratings

The maximum ratings section of the datasheet also lists operating and storage temperature and the IEC climate category as in Figure 33.

Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Figure 33 Additional maximum ratings