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Infineon Technologies Bipolar
GmbH & Co. KG

Technical Information

Bipolar Semiconductors

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Products and Innovations

The goal of highest reliability and efficiency in a core technology is always a moving target; therefore we understand that continuous improvement is essential. On this basis we have established comprehensive standards with our technologies and our products, in the power classes ranging from around 10kW to over 30MW per component. These include for example:

- PowerBLOCK modules in press-pack technology with currents up to 1100 Ampere
- Diodes and thyristors with a silicon diameter up to six inches and blocking voltages up to 9500 Volts
- Light-triggered thyristors with integrated protection functions
- Freewheeling diodes for the highest requirements in fast switching applications such as with IGBTs or IGCTs

Contents

Preface

Power semiconductors are the central components in converters technology.
Due to constant advancement these components find further use in ever new and more complex applications.

Based on the suggestions and questions we have been approached with we compiled this Technical Information (TI) as a reference document.

This Technical Information describes all essential technical terms for bipolar power semiconductors (diodes and thyristors) and thus provides assistance in working and designing as well as a reference document for the development and projection of inverter circuitry with bipolar components.
It is aimed at the relevant specialists in industry, research, development and training.

General information regarding converters, their circuits and specialties can be found in the pertinent literature.

At this point we refer to the appropriate standards which always need to be regarded in their latest version.

The current technical data of Infineon power semiconductors can be down-loaded from www.Infineon.com.

This Technical Information is meant to assist in better understanding the terms and the application of data sheet specifications of bipolar power semiconductors.
Definitions and abbreviations used are mainly in accordance with DIN / IEC / EN.
Please note that no guaranty can be given that circuits, appliances and processes described here are free of patent rights.

1. Introduction

This TI is to give detailed definitions to specifications used in the data sheets. Further, the user is to be assisted to transfer the data sheet specifications correctly in his application.
The following information is generally valid for all Infineon pressure contact components (disc cells and PowerBLOCK-Modules). Exceptions are individually marked.
Information given here is valid in accordance with the currently valid norms and standards.

1.1 Diode

A diode is a component with one P and one N conducting semiconductor zone.
The PN-junction is responsible for the elementary features of this semiconductor (see Figure 1).

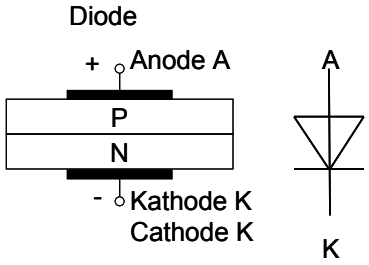


Figure 1: Schematic construction of a diode

The characteristic of a diode is depicted in Figure 2. It consists of two sections: the blocking characteristic and on-state characteristic.

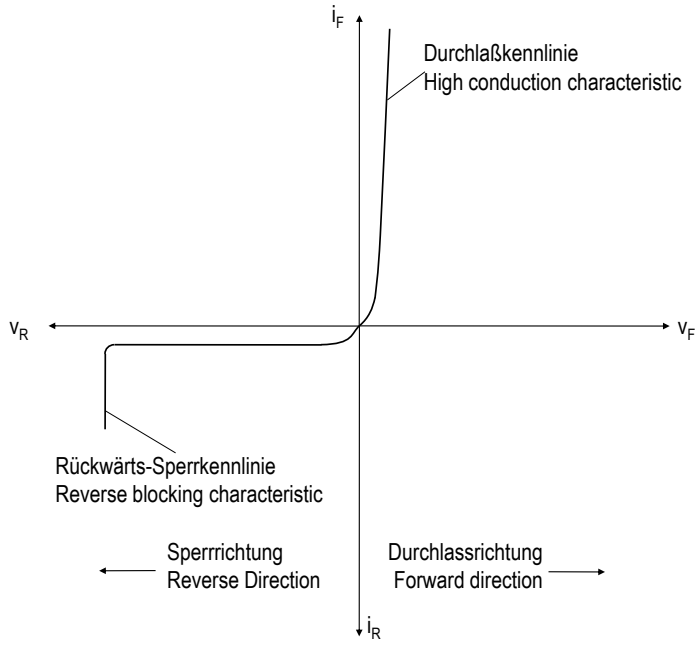


Figure 2 Characteristics of a diode

When a voltage up to several kV is applied in reverse direction, reverse currents in the range of mA will flow via the main terminals anode and cathode.
When a voltage is applied in forward direction, currents up to several kA will flow via the main terminals anode and cathode.

1.2 Thyristor

A thyristor is a component with a total of four alternating P and N conducting semiconductor zones. These will thus form three PN-junctions (see Figure 3).

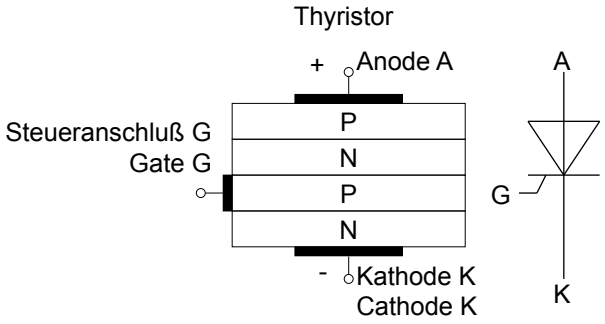


Figure 3: Schematic construction of a thyristor

The characteristics of a conventional (reverse blocking) thyristor are depicted in Figure 4. They consist of three sections: The blocking and the on-state characteristic in forward direction and the blocking characteristic in reverse direction.

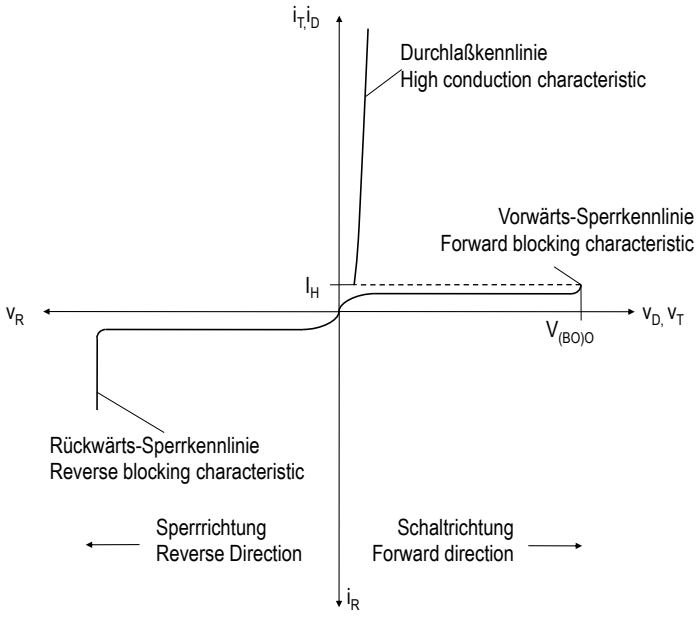


Figure 4 Characteristics of a thyristor

As can be seen from the characteristics, the thyristor is initially blocked in forward and reverse directions. Generally the blocking capability is approximately the same in both directions.
When voltages up to several kV are applied in forward or reverse direction, only small blocking currents will flow via the main terminals anode and cathode. An additional control current I_G between control terminal (gate) and cathode

will trigger the thyristor when a forward voltage v_D is present, i.e. it turns on to the on-state characteristic. However, it may not be turned off via the control terminal. Only when the forward current by changes in the load circuit drops below the holding current I_H, the thyristor will once again block.

Fast thyristors are available in 2 basic versions:

- Symmetrically blocking thyristors
  (SCR ⇢ **S**ilicon **C**ontrolled **R**ectifier)

These thyristors show approximately equal blocking capability in both directions. Individual types are differentiated by their blocking capability, their current carrying capability, their turn-off time and the gate-cathode structure.

- Asymmetrically blocking thyristors
  (ASCR ⇢ **A**symmetric **S**ilicon **C**ontrolled **R**ectifier)

These thyristors provide full blocking capability in forward direction and little blocking capability in reverse. Here the reverse blocking PN-junction is replaced by a stop layer which allows a significant reduction of the silicon height.
The advantages compared to symmetrically blocking thyristor are a shorter turn-off time for the same on-state voltage or a lower on-state voltage for the same turn-off time.

2. Type and polarity designation

2.1 Designation of the terminals

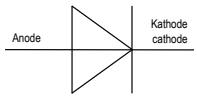
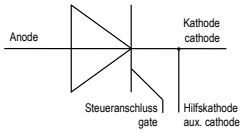
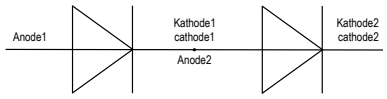
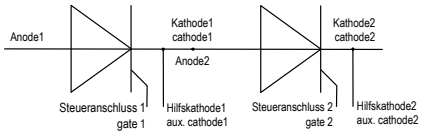
Diode as disc cell, ND or DZ-PowerBLOCK-Module	Thyristor as disc cell or TZ-PowerBLOCK-Module
	
Diodes as DD-PowerBLOCK-Module	**Thyristors as TT-PowerBLOCK-Module**
	

Figure 5 Designation of the terminals

2.2 Constructions

2.2.1 General

The semiconductor element (pellet) is built into a case and thus protected from adverse influences of the external environment.
All semiconductors described here are constructed in pressure contact technology.
The pressure contact technology is known for:

- very high load cycling capability
- very good over-load capability

2.2.2 Disc cells

When mounting disc cells the pressure for the components has to be applied from the exterior. Double sided cooling allows the heat generated through the losses to be dissipated in the best possible way from the disc cells. They are thus used for applications with highest power requirements.

2.2.3 PowerBLOCK-Module

The PowerBLOCK-Module is a case concept which in itself provides sufficient pressure to the semiconductor element. In addition, defined isolation against the base plate is provided. This simplifies the application of the modules significantly, as a complete rectifier for example may be constructed on a common heatsink. Due to the single sided cooling and the limits of the isolation voltage, possibilities of its application in the high power area are limited.

Figure 6 Construction concepts of pressure contact components

2.2.4 Stud type and flat case constructions

In stud (screw) type and flat case constructions the semiconductor element is already pressed correctly. These case types are now out-dated and mostly replaced by the more powerful PowerBLOCK-Module.

3. Electrical properties

The electrical properties of diodes and thyristors are temperature dependent and therefore valid only in conjunction with a temperature specification.
All values mentioned in the data sheets are applicable to mains frequency 40 to 60Hz if not otherwise specified.

Maximum values are those values given by the manufacture as the absolute limits which generally even for short times may not be exceeded as this may lead to a functional deterioration or destruction of the components. Characteristic values are ranges of data distribution at defined conditions and may form the basis of incoming inspection.

3.1 Forward direction

For diodes

the forward direction is the direction between the main terminals in which the diode has reached conduction mode even at a low voltage of just a few volts (see Figure 1, direction anode-cathode).

For thyristors
the forward direction is the direction between the main terminals in which the thyristor may operate in two stable modes – the on- and the off-state - (see Figure 3, direction anode-cathode).

Addition of the words “positive” or “forward” is used to expressly distinguish currents and voltages in forward direction from those in reverse direction.
The forward characteristic of the thyristor consists of an off-state and an on-state region (see Figure 4).

The forward off-state characteristic is that part of the forward characteristic of a thyristor which illustrates the instantaneous values of the forward off-state current and the forward off-state voltage.

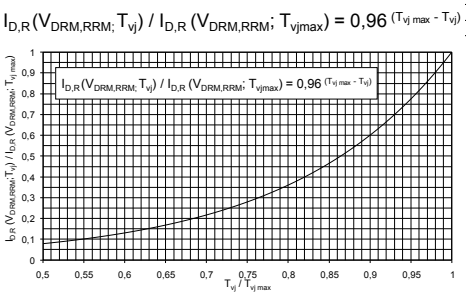


Figure 7 Typical dependence of the off-state current $i_{D,R}(V_{DRM,RRM})$ referenced to $I_{D,R}(V_{DRM,RRM}; T_{vj\,max})$ on the junction temperature T_{vj} referenced to $T_{vj\,max}$

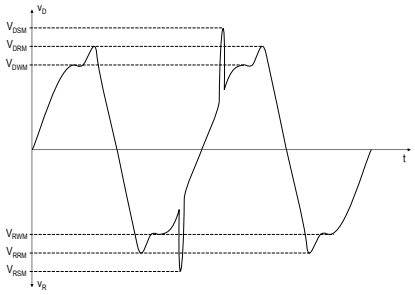


Figure 8 Definition of the off-state voltage occurrences

3.1.1 Forward off-state current i_D

i_D is the current which flows in forward direction through the main terminals in the off-state condition of the thyristor. In the data sheet it is specified for the voltage V_{DRM} and the maximum junction temperature $T_{vj\,max}$.
This current depends on the junction temperature T_{vj} (see Figure 7).

3.1.2 Forward off-state voltage v_D

v_D is the voltage which is applied across the main terminals in forward direction during the off-state condition of the thyristor.

3.1.2.1 Repetitive peak forward off-state voltage V_{DRM}

V_{DRM} is the maximum value of repetitive voltages in the forward off-state direction including all repetitive peak voltages.
In DC applications a reduction to $V_{D\,(DC)}$ is necessary. See also section 3.1.2.3.
In view of transient voltages occurring in operation, thyristors are usually operated at supply voltages of which the peak value is equal to the maximum rated repetitive peak off-state voltage divided by a safety factor of between 1.5 and 2.5.

$$\hat{V}_{line} = V_{DWM,RWM} \quad \frac{V_{DRM}\ \text{bzw.}\ V_{RRM}}{1,5\ldots2,5}$$

A low safety factor is used where the transient voltages mostly known. These are generally self commutated converters with large energy storage. For converters supplied from mains with unknown transient levels a safety voltage margin of 2.0 to 2.5 is preferable.

If transient voltages are likely to occur in operation, which exceed the maximum permissible repetitive peak off-state voltage, a suitable transient voltage protection network has to be provided (see 7.1).

3.1.2.2 Non-repetitive peak forward off-state voltage V_{DSM}

V_{DSM} is the maximum rated non-repetitive peak value of a voltage in forward direction on the thyristor which must not be exceeded.

3.1.2.3 Forward direct off-state voltage $V_{D\ (DC)}$

$V_{D\ (DC)}$ is the permanently allowable direct voltage in forward direction in off-state mode. For the semiconductors described here the value is rated at approximately half repetitive peak off-state voltage. This is valid for a failure probability of approximately 100 fit (failure in time; 1fit = $1*10^{-9}$ failures per hour, i.e. one failure in 10^9 operating hours of the device). Probabilities of failure to be expected for varying DC-voltages are available on request.

3.1.3 Forward breakover voltage $V_{(BO)}$

$V_{(BO)}$ is the value of the off-state voltage in forward direction at which for a given gate current the thyristor switches from the off-state to the on-state.
Exception: For light triggered thyristors (LTT's) with integrated breakover diode (BOD) $V_{(BO)}$ is the minimum voltage at which protective triggering of the thyristor occurs

3.1.4 Open gate forward breakover voltage $V_{(BO)0}$

$V_{(BO)0}$ is the breakover voltage at zero gate current. Triggering the thyristor by exceeding the $V_{(BO)0}$ may cause destruction of the device.
Exception: Light triggered thyristors are protected by an integrated breakover diode (BOD).

3.1.5 Holding current I_H

I_H is the minimum value of on-state current required to maintain the thyristor in on-state. I_H drops with raising junction temperature (see Figure 9).
Light triggered thyristors show a significantly lower holding current than comparable electrically triggered thyristors.

3.1.6 Latching current I_L

I_L is the on-state current required to maintain the thyristor in the on-state once the gate current has decayed. It depends on the rate of change, peak and duration of the gate current as well as on the junction temperature (see Figure 9).
Exception: Light triggered thyristors show a significantly lower latching current than comparable electrically triggered thyristors.

3.1.7 On-state current i_T, I_{TAV}, I_{TRMS} i_F, I_{FAV}, I_{FRMS}

The on-state current is the current which flows via the main terminals in the on-state of the thyristor (i_T, I_{TAV}, I_{TRMS}) or the diode (i_F, I_{FAV}, I_{FRMS}). It is differentiated in:
i_T, i_F = instantaneous value
$I_{TAV,}$ I_{FAV} = average value
I_{TRMS}, I_{FRMS} = RMS (route mean square)

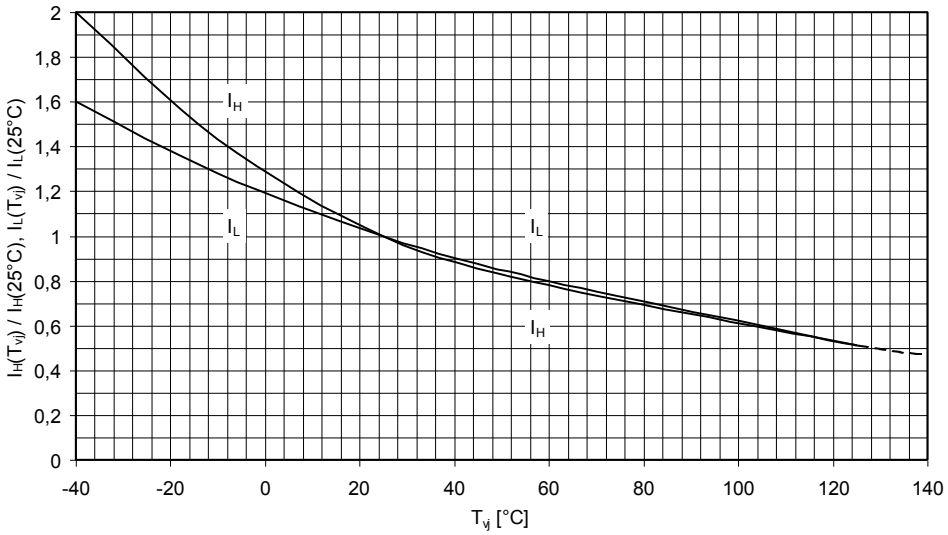


Figure 9 Typical dependence of the latching current I_L and holding current I_H normalized to T_{vj}=25°C of the junction temperature T_{vj}

3.1.8 On-state voltage v_T, v_F

v_T, v_F is the voltage across the main terminals at the defined on-state current. It depends on the junction temperature. Values given in the data sheet are valid for the completely turned on thyristor (v_T) or for the diode (v_F).

3.1.9 On-state characteristic

The on-state characteristic is the relation of the instantaneous values of on-state current and on-state voltage for the diode or for the completely turned on thyristor at a defined junction temperature.

3.1.10 Equivalent line approximation with $V_{T(TO)}$, $V_{F(TO)}$ and r_T

The equivalent line is an approximation to the on-state characteristic of a thyristor ($V_{T(TO)}$, r_T) or of a diode ($V_{F(TO)}$, r_T) to calculate the on-state power dissipation.
Given are:
$V_{T(TO)}$, $V_{F(TO)}$ = threshold voltage
r_T = differential resistance or slope resistance
The value of $V_{T(TO)}$, $V_{F(TO)}$ results from the intersection of the equivalent line approximation and the voltage axis, the value of r_T is calculated from the rate of raise of the equivalent line. Depending on the cooling it may be necessary to adapt the equivalent lines shown in the data sheet to the application. In some data sheets there may hence be an additional low level value for $V_{T(TO)}$, $V_{F(TO)}$and r_T.
For components with high blocking voltages (T…1N, T…3N, D…1N) equivalent lines are shown in addition as an approximation to a typical on-state characteristic which describes approx. the 50% value in the statistical distribution. In applications in which many equal components are used the conduction losses of the entire installation can be calculated using the typical equivalent line approximation.

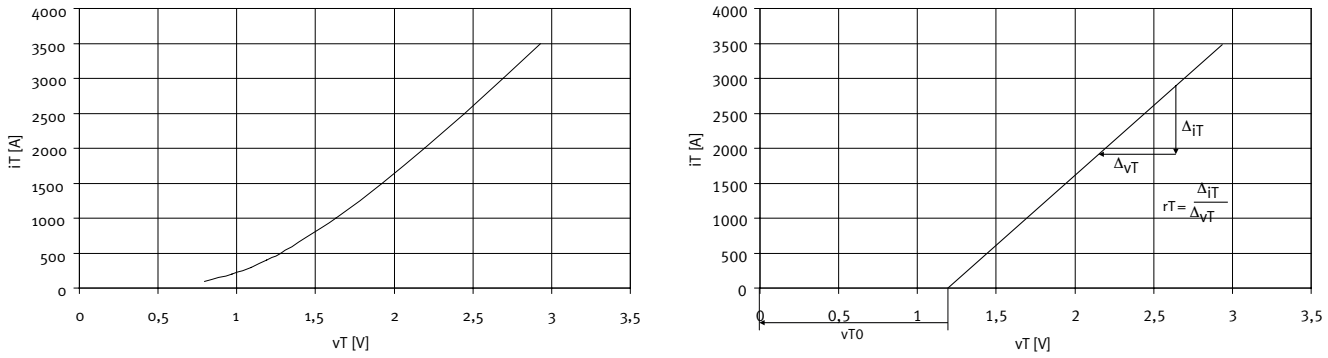


Figure10 Example of an on-state characteristic and the matching equivalent line approximation

3.1.11 Maximum average on-state current I_{TAVM}, I_{FAVM}

I_{TAVM}, I_{FAVM} is the maximum permissible continuous average value of the on-state current in a single phase half-wave resistive load circuit according to DIN VDE 0558, part 1 rated at a defined case temperature T_C and a frequency of 40 to 60Hz.

A diagram is given in the data sheets of the thyristors or diodes with low blocking voltages which shows the maximum average on-state current versus the maximum allowable case temperature T_C for various current conduction angles.

This diagram takes only the conduction losses into account. For components with high blocking voltages (›2200V) additional turn-off losses and to some degree blocking and turn-on losses need to be considered.

For components with very high blocking voltages (›4kV) this diagram is, therefore, omitted in the data sheet.

3.1.12 Maximum RMS on-state current I_{TRMSM}, I_{FRMSM}

I_{TRMSM}, I_{FRMSM} is the maximum value of RMS on-state current permissible considering electrical and thermal stresses of all assembly parts of the device. This current must not be exceeded for flat base and stud type cases and modules even under the best cooling conditions of the thyristor (I_{TRMSM}) or the diode (I_{FRMSM}).

3.1.13 Overload on-state current $I_{T(OV)}$, $I_{F(OV)}$

$I_{T(OV)}$, $I_{F(OV)}$ is the maximum allowable value of on-state current that the thyristor ($I_{T(OV)}$) or the diode ($I_{F(OV)}$) may conduct in short time operation without losing its control property. In the diagram for overload on-state current it is given as the peak value at 50Hz sinusoidal half-waves for different preloads versus time t.

This illustration does not take into account increased blocking or turn-off losses as they occur for devices with high blocking voltages. For components with very high blocking voltages (›4kV) this diagram is, therefore, omitted in the data sheet.

3.1.14 Maximum overload on-state current $I_{T(OV)M}$, $I_{F(OV)M}$

$I_{T(OV)M}$, $I_{F(OV)M}$ is the value of on-state current at which the device must be turned off in order not to destroyed the thyristor ($I_{T(OV)M}$) or the diode ($I_{F(OV)M}$). These values are intended for the design of the protection networks. The thyristor may temporarily lose its forward blocking capability when the current flowing through it reaches this value and may temporarily lose its control properties.

The maximum overload on-state current characteristic shows this value as the peak value of a 50Hz sinusoidal half-wave versus time t. Two conditions are differentiated: no load operation preceding and operation with maximum average on-state currents preceding.

The maximum overload on-state current characteristics given in the individual data sheet applies to a reverse blocking voltage of 80% of the repetitive peak reverse voltage. In cases where the actual reverse voltage is lower, a higher maximum overload on-state current is allowable which is shown in Figure 11 and Figure 12 for a preceding continuous maximum overload on-state current I_{TAVM}. The conditions for a device without preceding load can not be determined from this.
This illustration does not take into account increased blocking or turn-off losses as they occur for devices with high blocking voltages. For components with very high blocking voltages (>4kV) this diagram is, therefore, omitted in the data sheet. The protection concepts for these devices are described in chapter 7.2.

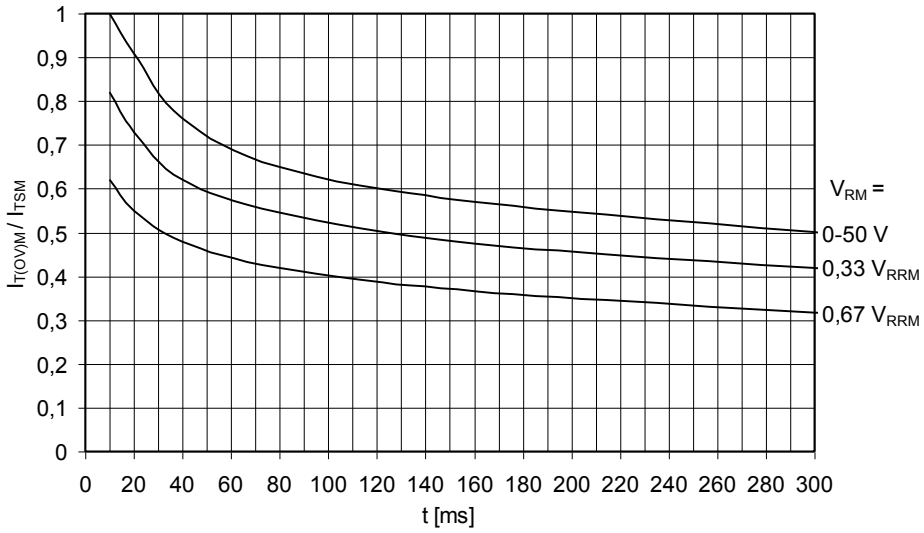


Figure 11 Typical dependence of the maximum overload on-state current $I_{T(OV)M}$, $I_{F(OV)M}$ (in relation to the surge current I_{TSM} or I_{FSM} for 10ms and $T_{vj\ max}$) on the number of half-sinewaves at 50Hz.
Parameter: reverse blocking voltage V_{RM}

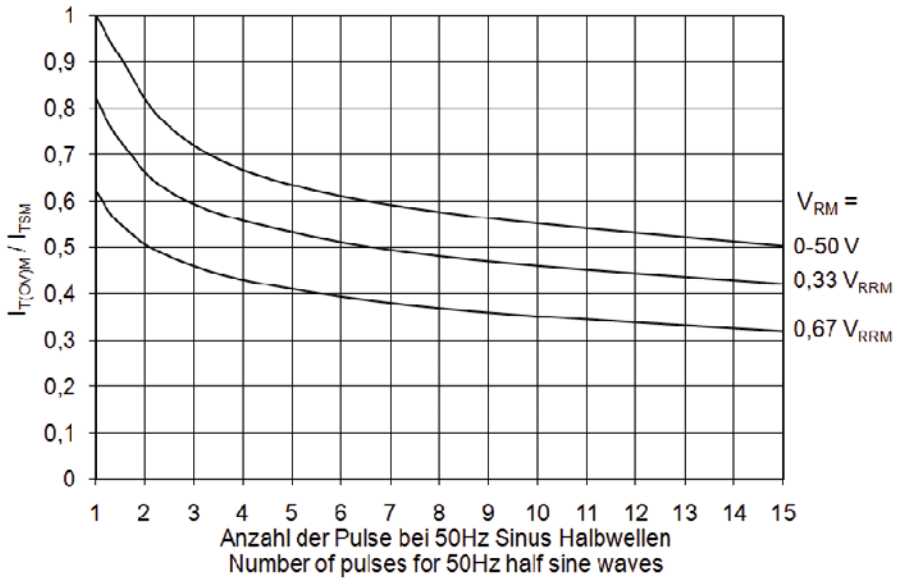


Figure 12 Typical dependence of the maximum overload on-state current $I_{T(OV)M}$, $I_{F(OV)M}$ (in relation to the surge current I_{TSM} or I_{FSM} for 10ms and $T_{vj\ max}$) on the time t for a number of half-sinewaves at 50Hz. Parameter: reverse blocking voltage V_{RM}

3.1.15 Surge on-state current I_{TSM}, I_{FSM}

I_{TSM}, I_{FSM} is the maximum permissible peak value of a single half sine-wave 50Hz current pulse. It is specified at 25°C (equates to a short circuit from no load condition) or at
turn-on at maximum permissible junction temperature (equates short circuit after
permanent load with maximum permissible current). When stressing a semiconductor with the surge on-state current, the device loses its blocking capability. Therefore, no negative voltage shall subsequently be applied. This stress may be repeated during fault conditions in a non-periodic way provided the junction temperature has dropped to
values within the permissible operating temperature area.
When exceeding the maximum permissible value destruction of the device is risked (for details please see chapter 7.2 over current protection).

3.1.16 Maximum rated value ∫i²dt

∫i²dt is the square of the surge on-state current integrated over time.
The maximum rated ∫i²dt-value serves to determine the short-circuit protection (see 7.2).
For half-sinewaves with periods shorter than 10ms the maximum rated ∫i²dt-value is shown in Figure 13. Regarding voltage stress and repetition the same applies as for the surge on-state current. When exceeding the maximum permissible value, destruction of the device is risked. In addition, in particular for large diameter thyristors, it has to be observed that the permissible critical turn-on current rate of change $(di/dt)_{cr}$ may not be exceeded.

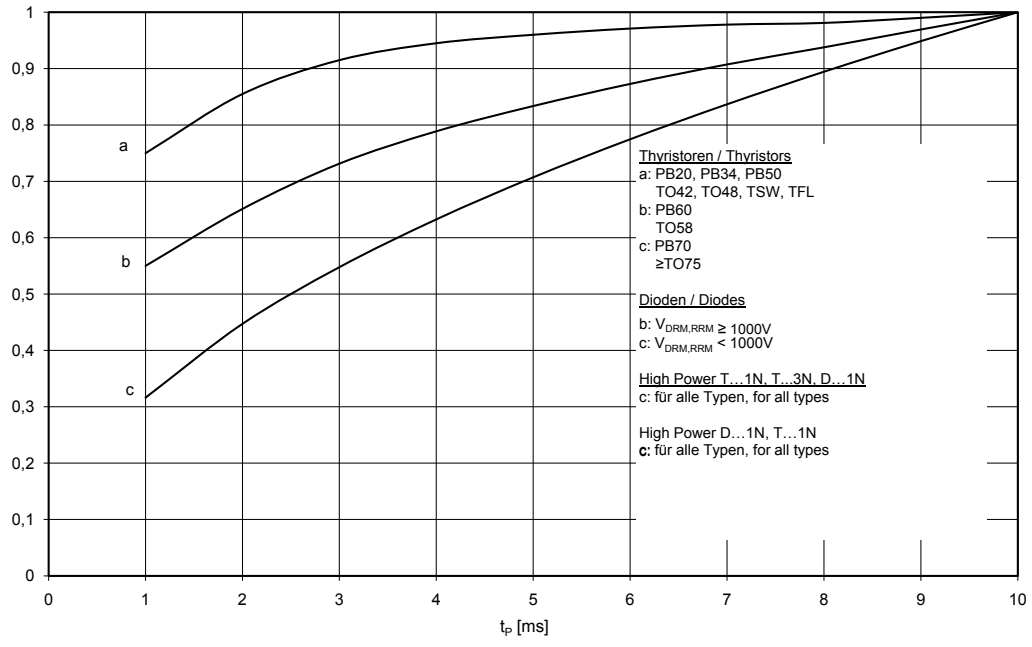


Figure 13 Typical dependence of the ∫i² dt normalized to the value ∫i² dt (10ms) on the half-sinewave duration t_P

3.2 Reverse direction

The reverse direction is the direction from one main terminal to the other in which the thyristor and diode is in a stable high resistance state of operation (direction cathode-anode).
If values (voltages and currents) and data in reverse direction are to be distinguished from those in forward direction, then the term “reverse” or “negative” is used.
The reverse blocking characteristic of a thyristor or a diode represents the instantaneous values of reverse current and reverse voltage.

3.2.1 Reverse current i_R

i_R is the current flowing in reverse direction through the main terminal of the thyristor or diode. The reverse current depends on the reverse voltage and the junction temperature T_{vj} (Figure 7)

3.2.2 Reverse voltage v_R

V_R is the voltage applied across the main terminals of the thyristor or diode in reverse direction.

3.2.2.1 Repetitive peak reverse voltage V_{RRM}

V_{RRM} is the maximum permissible instantaneous value of repetitive voltages in reverse direction including all repetitive peak voltages.
In DC applications a reduction to $V_{R\,(DC)}$ is necessary.
See also section 3.2.2.3.
For supply voltage see section 3.1.2.1.

3.2.2.2 Non-repetitive peak reverse voltage V_{RSM}

V_{RSM} is the maximum allowable non-repetitive peak value of a transient voltage in reverse direction which must not be exceeded even for the shortest duration. The value resulting is:
For blocking voltages ‹ 800V:
$V_{RSM} = V_{RRM} + 50V$ (at $T_{vj} = 25°C \ldots T_{vj\,max}$)

For blocking voltages ≥ 800V:
$V_{RSM} = V_{RRM} + 100V$ (at $T_{vj} = 25°C \ldots T_{vj\,max}$)

3.2.2.3 Direct reverse voltage $V_{R(DC)}$

V_R (DC) is the permanently allowable direct voltage in reverse direction, analogous to forward direct off-state voltage 3.1.2.3.

3.3 Control properties of thyristors

3.3.1 Positive gate control

3.3.1.1 Gate current i_G

i_G is the current flowing through the control path (terminals G – HK).
Thyristors shall only be pulse triggered during the forward off-state phase.
Positive trigger pulses during the reverse off-state phase will lead to significantly increased off-state losses due to the transistor effects caused. These losses adversely affect the functionality and may lead to destruction.
Exception: For light triggered thyristors control pulses during the reverse off-state phase are permissible.

3.3.1.2 Gate voltage V_G

V_G is the positive voltage across the gate terminal (G) and the cathode (K) or auxiliary cathode (HK).

3.3.1.3 Gate trigger current I_{GT}

I_{GT} is the minimum value of gate current which causes the thyristor to trigger. It depends on the voltage across the main terminals and the junction temperature. At the given value of the gate trigger current all thyristors of a given type will trigger. The gate trigger current increases with lower junction temperature and is thus specified at 25°C.

The trigger pulse generator has to safely exceed the data sheet value I_{GTmax} (see also 3.3.1.8).

Exception: For light triggered thyristors the minimum light power P_L is specified which causes all thyristors of a given type to trigger.

3.3.1.4 Gate trigger voltage V_{GT}

V_{GT} is the voltage which occurs across gate terminal and cathode when the gate trigger current I_{GT} flows. It depends on the voltage across the main terminals and the junction temperature. At the given value of the gate trigger voltage all thyristors of a given type will trigger. The gate trigger voltage drops with increasing junction temperature and is thus specified at 25°C. V_{GT} is measured when a specified load current flows.

3.3.1.5 Gate non-trigger current I_{GD}

I_{GD} is the value of the gate current which does just not cause the thyristor to trigger. It depends on the voltage across the main terminals and the junction temperature. At the given maximum value no thyristor of a given type triggers. The gate non-trigger current decreases with increasing junction temperature and is thus specified at $T_{vj\,max}$.

3.3.1.6 Gate non-trigger voltage V_{GD}

V_{GD} is the value of the gate voltage which does just not cause the thyristor to trigger.
It depends on the voltage across the main terminals and the junction temperature. At the given maximum value no thyristor of a given type triggers. The gate non-trigger voltage decreases with increasing junction temperature and is thus specified at $T_{vj\,max}$.

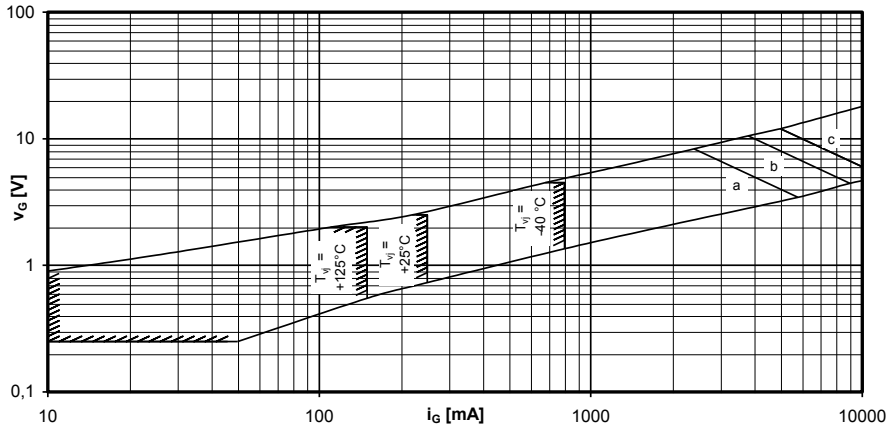


Figure 14 Example for control characteristic $v_G = f(i_G)$ with trigger area for $V_D = 12$ V

3.3.1.7 Control characteristic

It shows the limits of statistical distribution of the input characteristics of a thyristor type. Within the distribution of the input characteristics the temperature dependent trigger areas are detailed as well as the curves of the maximum permissible gate power dissipation P_{GM} (a – 20W / 10ms, b – 40W / 1ms, c – 60W / 0.5ms).

3.3.1.8 Control circuit

In a normal application the design of the control circuit should be done in accordance with the control data which are detailed in connection with the critical rise time of the on-state current, the gate control delay time and the latching current (see Figure 15). The minimum control data given in 3.3.1.3 and 3.3.1.4 are valid only for applications with low requirements with regard to critical current rise time and gate control delay time. In reality overdriving I_{GT} specified in the data sheet 4- to 5-fold assures safe operation even with high requirements for current rise time and gate control delay time.
Terms used in this context are:

di_G/dt = gate current slew rate
i_{GM} = peak gate current
t_G = duration of the trigger pulse
V_L = open circuit voltage of the control circuit
With increasing slew rate of the on-state current di_T/dt as well as repetitive turn-on current $I_{T(RC)M}$ from the snubber an effect from the load circuit to the gate current i_G is notable (see 3.4.1.2 and Figure 21).

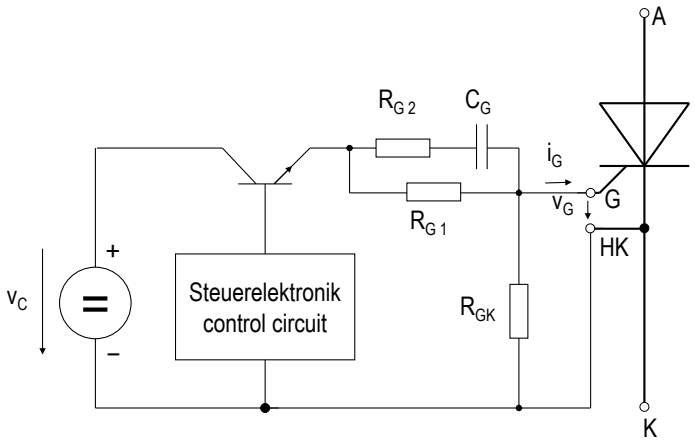


Figure 15 Concept of a trigger circuit for thyristors

Initially there is only a small area around the gate area on the pellet conductive during turn-on of the thyristor which leads to high current density and increased voltage. Due to internal coupling this voltage also appears at the control terminals and, therefore, leads to an intermediate drop of the gate trigger current. In order to avoid the possible destruction of the thyristor, i_G should not drop below the value of the gate trigger current I_{GT}. To prevent the gate pulse from dropping too low, a compensation by means of a higher open circuit voltage V_C of the trigger circuit may be necessary. For parallel or series connection of thyristors high, steep rising and synchronous trigger pulses are necessary in order to achieve equalised turn-on. See also distribution of gate control delay time values (3.4.1.2.1).
Exception: To control light triggered thyristors, laser diodes emitting light in the region of 900 to 1000nm are required. Minimum values for light power P_L are given which in conjunction with the given turn-on voltage will assure safe triggering of the thyristors. The light power is specified at the output of the fibre optic cable. With regard to even turn-on here too overdriving is recommended in particular for parallel and series connection with high di/dt requirements.
Infineon recommends the application of the laser diodes SPL PL90 aligned in the appropriate fitting (see Figure 16) and offers these together with suitable fibre optic cables as ancillary equipment.

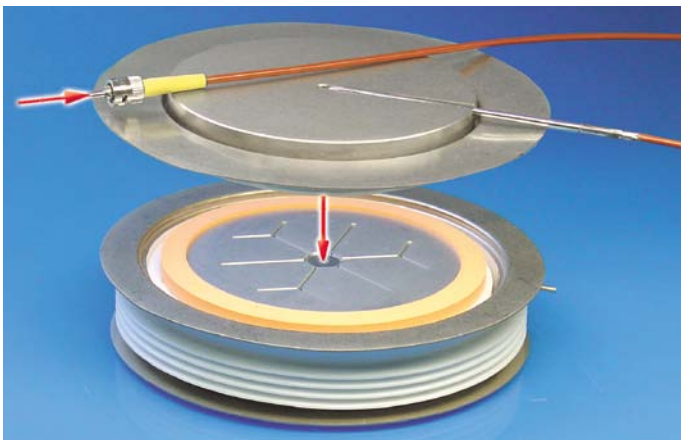


Figure 16 LTT with fibre optic cable

The laser diodes SPL PL 90 comply with the following laser classes: If the laser diode is correctly terminated with the fibre optic cable the control system complies with laser class 1. No operational hazard.
With open operation of the laser diode or in case of a broken fibre optic cable, the system equates to the laser class 3b according to IEC 60825–1. In this case hazard of operation exists due to invisible radiation. Direct or indirect exposure to the eyes or skin is to be avoided.

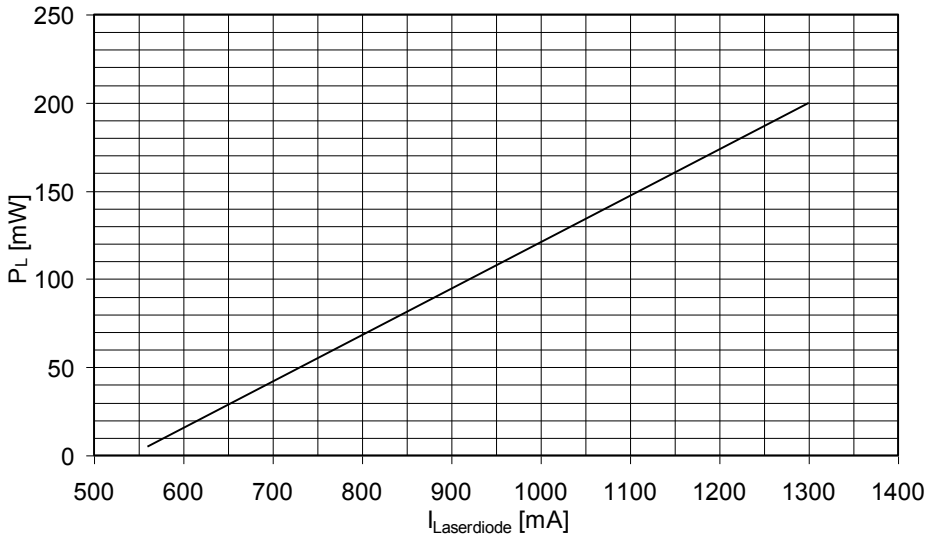


Figure 17 Laser diode SPL PL 90 typical dependence of the light power on the control current

To control light-triggered thyristors, we recommend a current pulse for the laser diode SPL PL90 as in Figure 18. As the laser diode SPL PL90 is not suitable for long-term control, we recommend controlling the laser diode with a frequency of approximately 6kHz, while using the pulse in Figure 18.

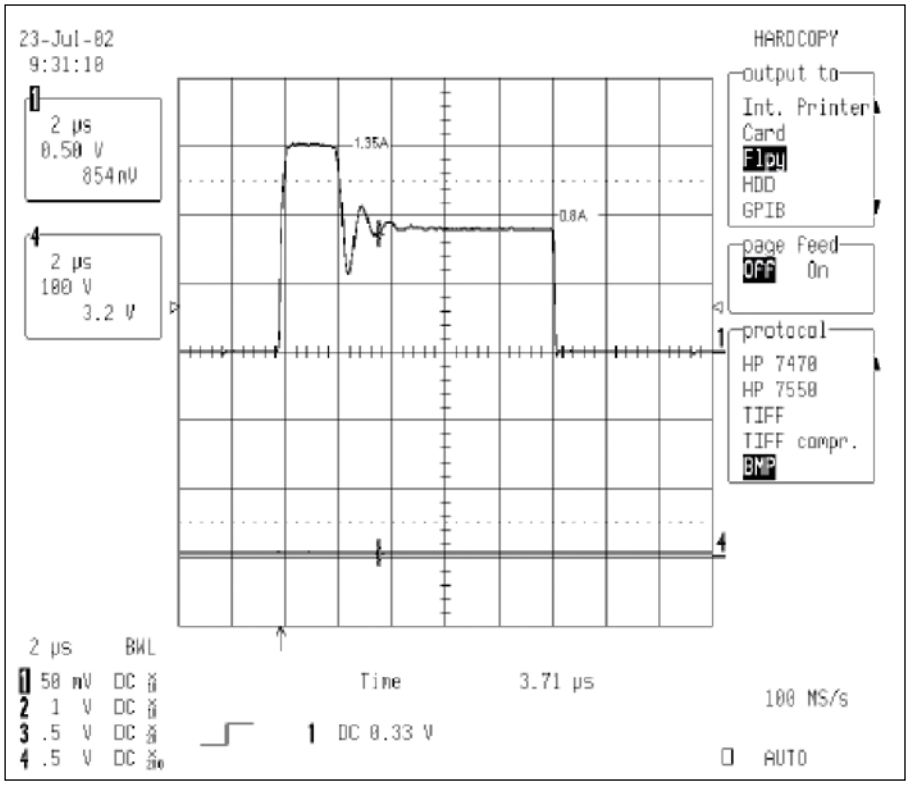


Figure 18 Recommended current pulse for laserdiode SPL PL 90

3.3.1.9 Minimum duration of the trigger pulse t_{gmin}

The trigger pulse has to be applied at least until the latching current of the thyristor (3.1.6) has been exceeded, as otherwise the thyristor will return to its off-state. The gate trigger current of the thyristor must remain at least at its rated value until the end of the trigger pulse.
In applications with very low current rise times or low load currents often a trigger profile with multiple pulses is used (e.g. with a frequency of repetition of 6kHz).
For light triggered thyristors make sure that when using multiple pulses the laser diode does not heat up inadmissibly. The light power of a current controlled laser diode drops with increasing temperature.

3.3.1.10 Maximum permissible peak trigger current

In applications with a high rate of rise of current i_{GT} may be overdriven even harder than described in 3.3.1.8. For this the gate current should be increased for a time $t_{GM} \approx$ 10-20µs to the 8- to 10-fold value of I_{GT} and than continue for a sufficient time t_G with a reduced amplitude. The open circuit voltage of the trigger circuit should at least apply 30V in order to assure a high reactionless gate current.

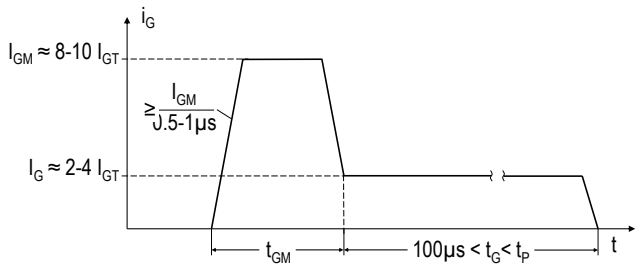


Figure 19 Safe overdrive of the gate trigger current

3.4 Carrier storage effect and switching characteristics

When the state of operation changes in power semiconductors, the stationary values of current and voltage do not change immediately due to the carrier storage effect. Additionally, in thyristors only small areas around the gate structure become conductive when triggered. The switching losses resulting from this have to be dissipated as heat from the semiconductor.

3.4.1 Turn-on

3.4.1.1 Diode

When passing from a non-conducting or blocked state to a conducting state, voltage peaks occur at the diode due to the carrier storage effect (see Figure 20).

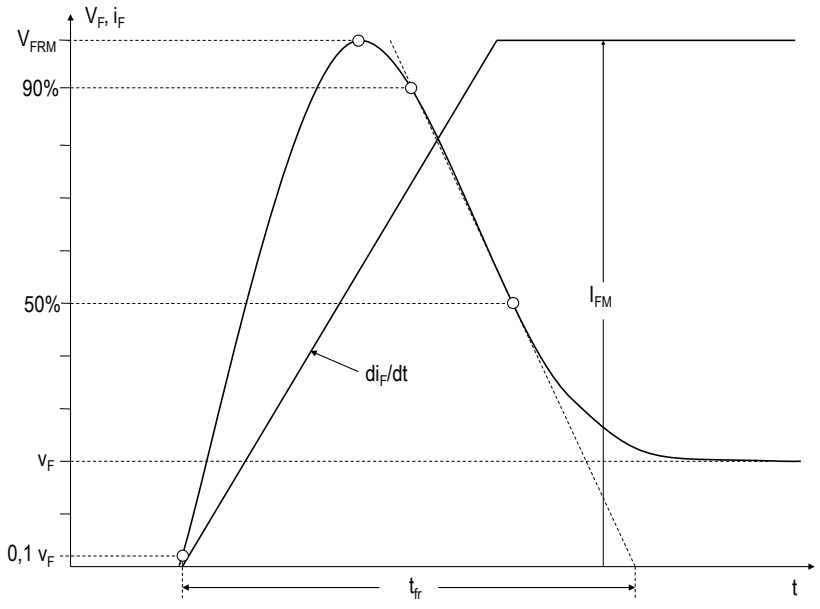


Figure 20 Schematic representation of a diode turn-on process

3.4.1.1.1 Peak value of the forward recovery voltage V_{FRM}

V_{FRM} is the highest voltage value occurring during the forward recovery time (see Figure 20). It increases with rising junction temperature and current slew rate.
In mains operation (50 / 60Hz) with its moderate current slew rates V_{FRM} is negligible. In self-commutated converters with fast switches di/dt››1000A/us (IGBT's, GTO's and IGCT's), however, it may reach values up to several hundred volts. Although the forward recovery voltage exists for just a few microseconds and thus does not contribute to the sum of losses of the diodes in a significant way, its effect on the switching semiconductor has to be considered when designing the converter.
In diagrams for diodes optimized for these applications data is included which details the forward recovery voltage as a function of the current slew rate.

3.4.1.1.2 On-state recovery time t_{fr}

According to DIN IEC 60747-2 t_{fr} is the time the diode needs to become fully conducting and a static on-state voltage v_F appears, when suddenly switched from zero to a defined on-state (see Figure 20).

3.4.1.2 Thyristor

The turn-on process is initiated at forward off-state voltage v_D by a gate current with a slew rate di_G/dt and a magnitude i_{GM}. For light triggered thyristors this applies to an equally specified trigger pulse on the laser diode.
During the gate controlled delay time t_{gd} the blocking voltage across the thyristor drops to 90% (see Figure 21).
As initially only a small area around the gate structure becomes conductive, the initial current density and thus the critical rate of rise of on-state current $(di/dt)_{cr}$ is a gauge for the robustness of the thyristor during turn-on.

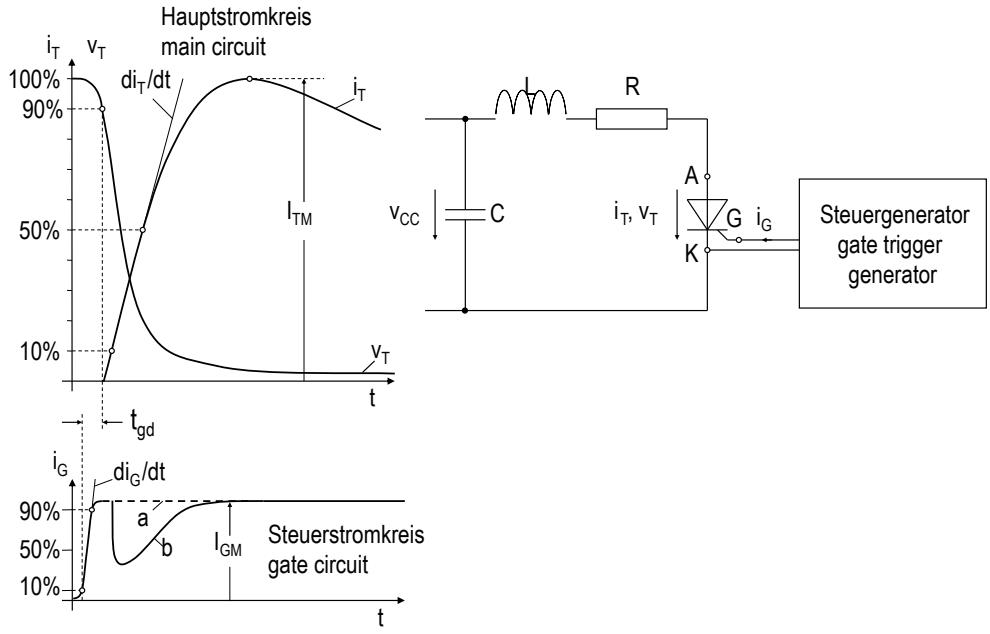


Figure 21 Schematic representation of a thyristor turn-on process
a - gate current with turned off load circuit
b - gate current with steeply rising on-state current (see also 3.3.1.8)

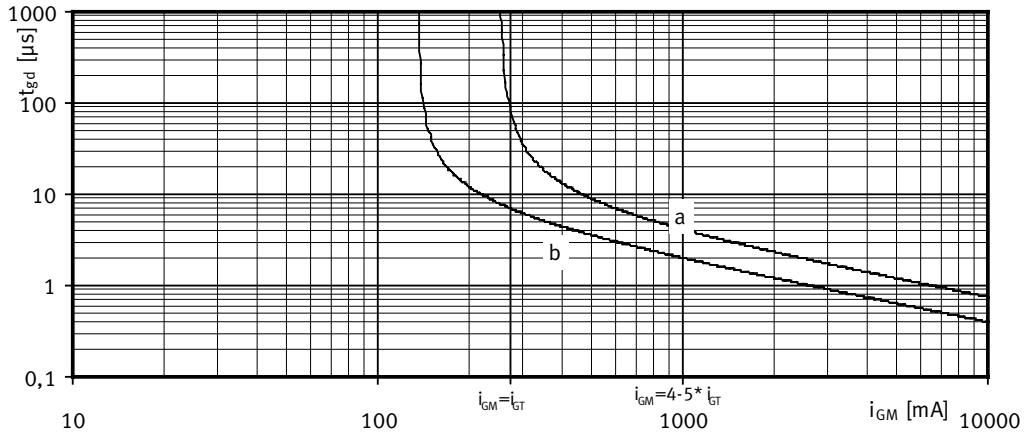


Figure 22 Typical dependence of the gate controlled delay time t_{gd} and the maximum gate current i_{GM}
a) maximum value
b) typical value

3.4.1.2.1 Gate controlled delay time t_{gd}

t_{gd} is the period between the gate current reaching 10% of its maximum value I_{GM} and the time when the anode-cathode voltage drops below 90% of the applied forward off-state voltage v_D (see Figure 21).
It reduces significantly with increasing gate current (light power for LTTs) (see Figure 22).
In high power thyristors the t_{gd} depends also on v_D.

The value given in the data sheet is defined according to DIN IEC 60747 – 6 and is valid for T_{vj} = 25°C and specified trigger pulse.

3.4.1.2.2 Critical rate of rise of the on-state current $(di/dt)_{cr}$

Once the voltage has collapsed due to the thyristor triggering a small area of the cathode around the gate structure begins to conduct on-state current. This current conducting area then spreads out depending on the current density with a speed of typically 0.1mm/µs. The current carrying capability of the system is therefore limited in the beginning. Damage or destruction of the thyristor is impossible, however, when the value given in the data sheet for the critical current slew rate is not exceeded. For S-thyristors and thyristors with large square sections the gate is distributed (finger structure). Therefore, these types show a higher $(di/dt)_{cr}$.

According to DIN IEC 60747 – 6 the critical current rise time $(di/dt)_{cr}$ refers to loading with on-state current over the period of a dampened half sine-wave. It is defined as the angle of a straight line through the 10% and 50% points of the rising on-state current (see Figure 21, Figure 47) whilst the following conditions apply:
Junction temperature $T_{vj} = T_{vj\ max}$
Forward off-state voltage $v_D = 0.67\ V_{DRM}$,
Peak current value $i_{TM} = 2\ I_{TAVM}$
Frequency of repetition f_0 = 50 Hz

The trigger pulse is defined in the individual data sheets (see also 3.3.1.8).
Exception: Light triggered thyristors are tested with a forward off-state voltage of $v_D = V_{DRM}$.

3.4.1.2.3 Repetitive turn-on current $I_{T(RC)M}$

$I_{T(RC)M}$ is the maximum permissible peak value of the on-state current immediately after turn-on with undefined rate of rise. In general this turn-on current is caused by the discharge of the RC-snubber network. The maximum permissible repetitive turn-on current also applies to the following steep current rise up to the critical rate of rise of the on-state current $(di/dt)_{cr}$.
For Infineon components the following values apply
$I_{T(RC)M} = 100A$

Exception: Component with the type designation T...1N or T...3N
$I_{T(RC)M} = 150A$

For applications above 60Hz the values for both the critical current rise time $(di/dt)_{cr}$ as well as the repetitive turn-on current $I_{T(RC)M}$ have to be reduced. Further details for particular conditions on request.

3.4.1.2.4 Critical rate of rise of off-state voltage (dv/dt)cr

$(dv/dt)_{cr}$ is the maximum value for the rate of rise of a voltage applied in forward direction running almost linearly from 0% to 67% of V_{DRM} at which a thyristor will not switch to the on-state.
For an exponential rate of voltage rise it is a line which crosses the exponential function starting from 0% to 63% of the maximum value.
It applies for open trigger circuit and maximum permissible junction temperature. Exceeding $(dv/dt)_{cr}$ may cause destruction.

Exception: Aside from the over-voltage protection (BOD) light triggered thyristors have an integrated dv/dt protection. This causes the thyristors to trigger safely over the entire gate structure when the dv/dt gets to high.

3.4.2 Turn-off

Turning off is usually started by application of a reverse voltage. The load current of the thyristor or the diode does not cease at the zero crossing but continues to flow briefly in reverse direction as reverse recovery current until the carriers have left the junction region.
The softness factor F_{RRS} describes the relation of the rates of rise of the currents during the turn-off process.

3.4.2.1 Recovery charge Q_r

Q_r is the total amount of charge flowing out of the semiconductor after switching from on-state to reverse off-state. It increases with rising junction temperature as well as magnitude and fall time of the on-state current. If not otherwise specified, the given values are valid for $v_R = 0.5V_{RRM}$ and $v_{RM} = 0.8V_{RRM}$ and are not exceeded by 95% of the individual types of thyristors or diodes. For this an appropriately designed RC-snubber network is specified.
For components with the type designation T...1N, T...3N and D...1N the given values in the data sheet are maximum values which are 100% tested in production.
The recovery charge Q_r is mainly dependent on the junction temperature T_{vj} and on the rate of fall of the decaying current (see Figure 24 and Figure 25).

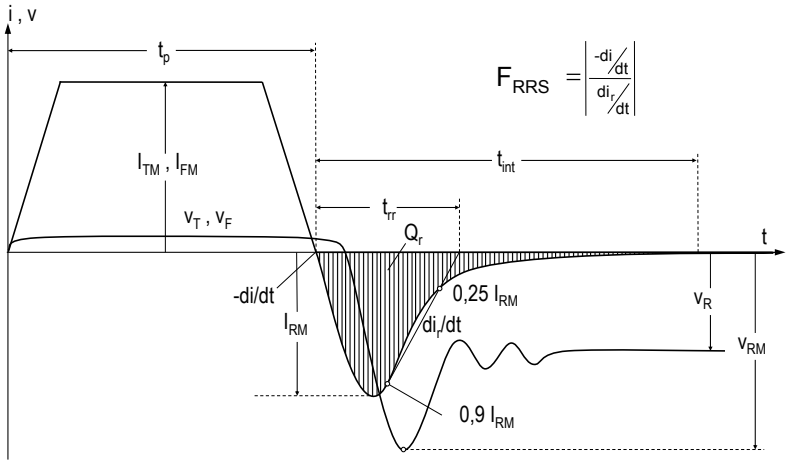


Figure 23 Schematic representation of the thyristor and diode turn-off process

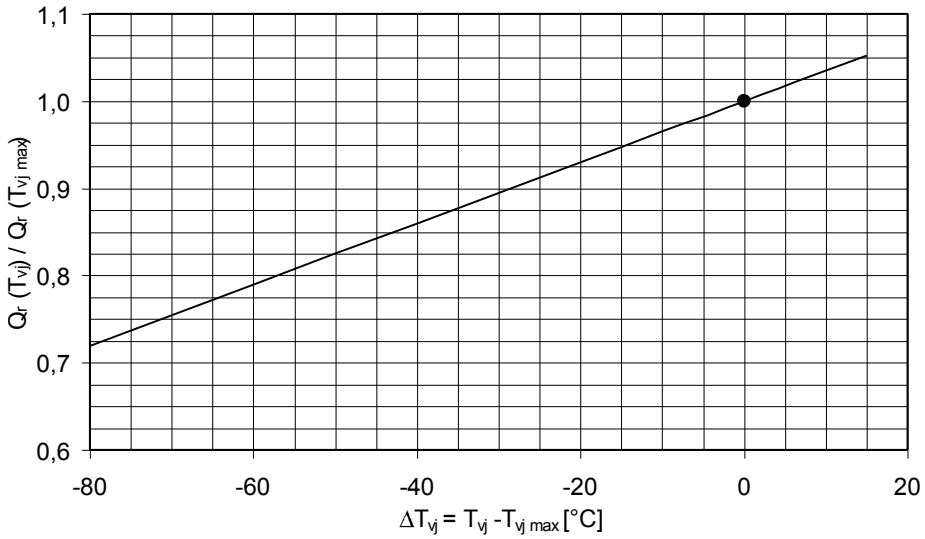


Figure 24 Typical T_{vj}-dependence of the recovery charge Q_r normalized to $Q_r(T_{vj\ max})$

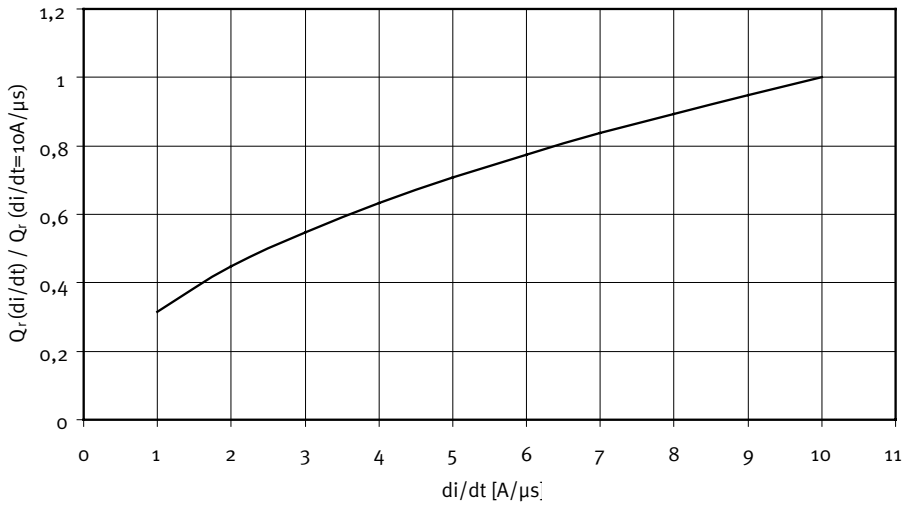


Figure 25 Typical di/dt-dependence of the recovery charge Q_r normalized to $Q_r(di/dt=10A/\mu s)$

3.4.2.2 Peak reverse recovery current I_{RM}

I_{RM} is the maximum value of the reverse recovery current. The dependences and operating conditions given for Q_r also apply. If I_{RM} is not shown in the diagrams, its value may be approximately determined as follows:

$$I_{RM} \approx \sqrt{\frac{|-di/dt| \cdot Q_r}{1...1,3}}$$

For components with the type designation T...1N, T...3N and D...1N the given values in the data sheet are maximum values which are 100% tested in production.
The peak reverse recovery current I_{RM} is mainly dependent on the junction temperature T_{vj} and on the rate of fall of the decaying current (see Figure 26 and Figure 27).

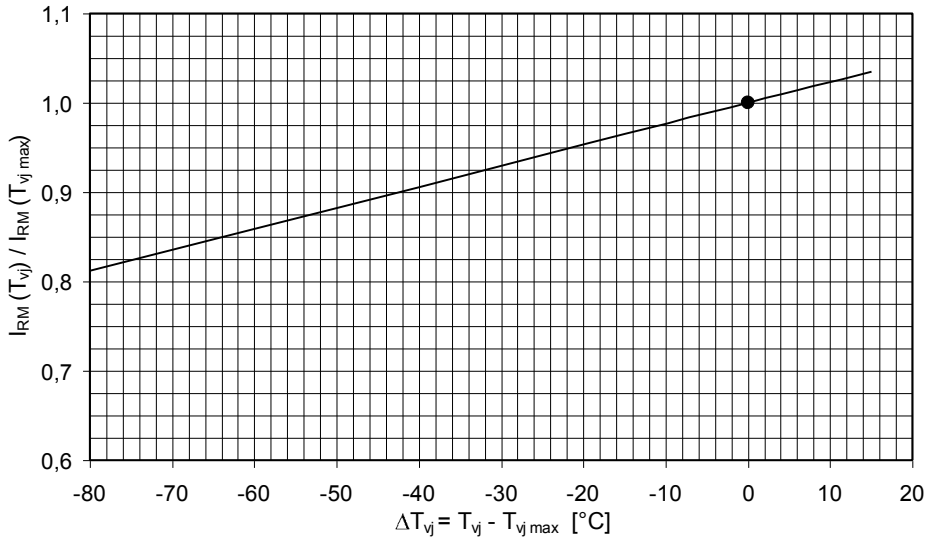


Figure 26 Typical T_{vj}-dependence of the peak reverse recovery current I_{RM} normalized to I_{RM} ($T_{vj\ max}$)

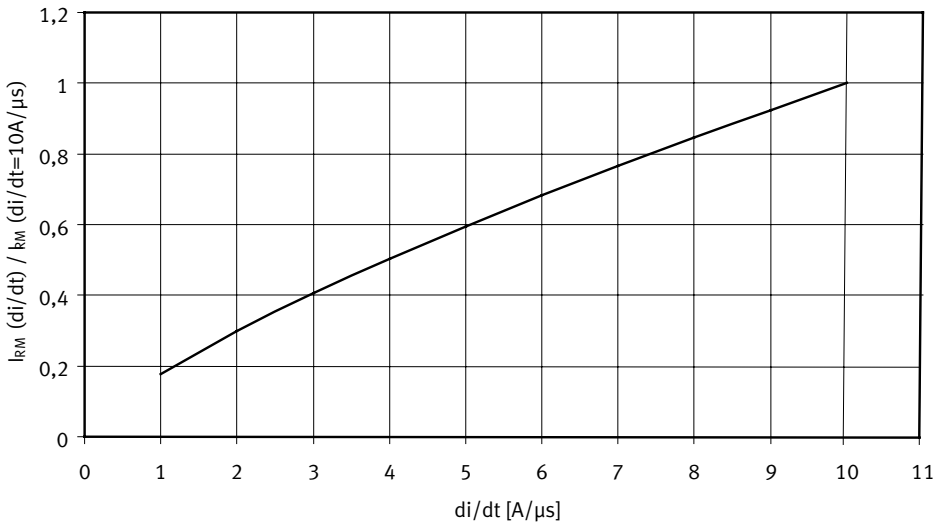


Figure 27 Typical di/dt-dependence of the peak reverse recovery current I_{RM} normalized to I_{RM} (di/dt=10/µs)

3.4.2.3 Reverse recovery time t_{rr}

t_{rr} is the time interval between the zero crossing of the current and the time at which a straight line through the 90% and 25% points of the decaying reverse recovery current crosses the zero line (see Figure 23). Should t_{rr} not be specified, its value may be approximately calculated with the following formula:

$$t_{rr} \approx \frac{2 \cdot Q_r}{I_{RM}}$$

3.4.2.4 Turn-off time t_q

t_q is the time interval between the zero crossing of the current commutated in reverse direction and the reapplication of forward off-state voltage at which a thyristor does not turn-on without a control pulse.
The actual pause time realised in the application before the forward off-state voltage reoccurs is called hold-off time. This time must always be greater than the turn-off time. The turn-off time mainly depends on the fall time of the on-state current, the rate of rise of the forward off-state voltage and the junction temperature (see Figure 29 - Figure 31). To determine t_q the duration t_P of the forward current has to be chosen long enough so that the thyristor at the point of commutation is completely turned on (see Figure 28). The values given in the data sheets are valid for following conditions:

Junction temperature	$T_{vj} = T_{vj\ max}$
Magnitude of on-state current	$i_{TM} \geq I_{TAVM}$
Fall rate of the on-state current	$-di_T/dt = 10\ A/\mu s$
Reverse voltage	$V_{RM} = 100V$
Rate of rise of the forward off-state voltage	$dv_D/dt = 20V/\mu s$
Forward off-state voltage	$V_{DM} = 0.67V_{DRM}$

Exception: Fast thyristors were commutated off with a current rate of fall of –di/dt=20A/µs. The dv_D/dt may vary here and is specified by the 5th letter in the type designation (see section 2.3).

For phase controlled thyristors usually typical values for the turn-off time are given as they are mainly employed in line commutated converters. In these applications the hold-off time is generally much longer than the turn-off time of the thyristor.
If the hold-off time is shorter than the turn-off time, the thyristor will once again turn-on with rising forward off-state voltage without application of a trigger pulse and destruction may be caused (t_q-limit values on request if necessary).

If the thyristor is operated together with an inverse diode (for example free wheeling diode), much longer turn-off times have to be taken into consideration due to the low commutation voltage (typically 30% longer). Additionally, in such applications the inductance of the free wheeling circuit should be minimised as otherwise the turn-off time may increase to significantly higher values.

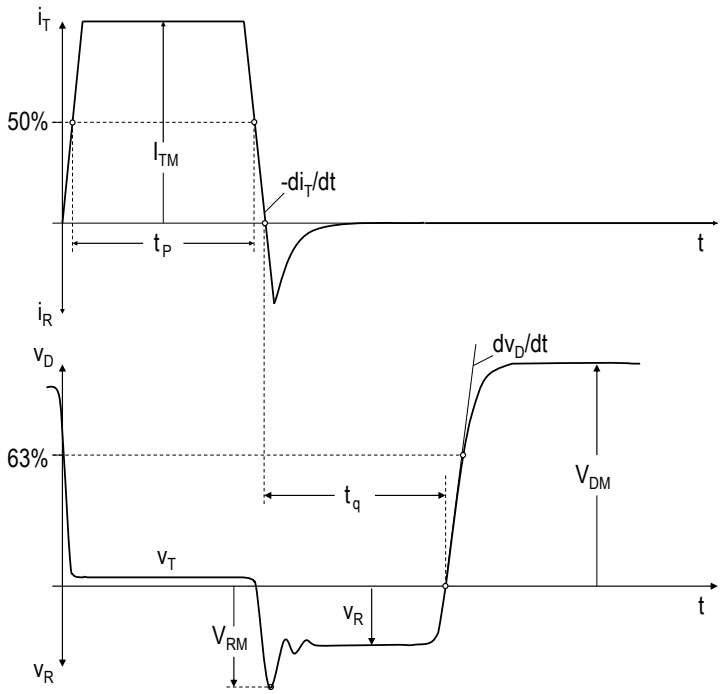


Figure 28 Schematic representation of the turn-off behaviour of a thyristor

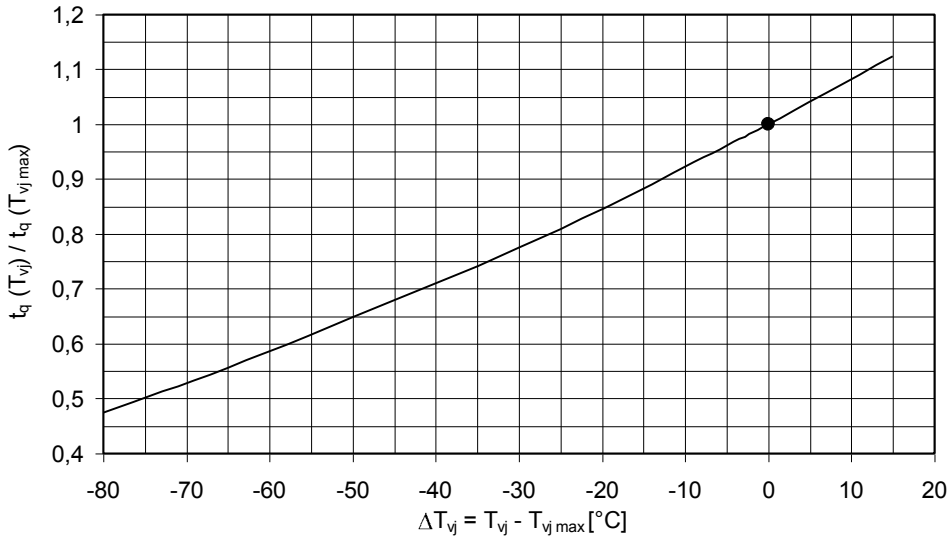


Figure 29 Typical dependence of the turn-off time t_q normalized to $T_{vj\,max}$ on the junction temperature T_{vj}

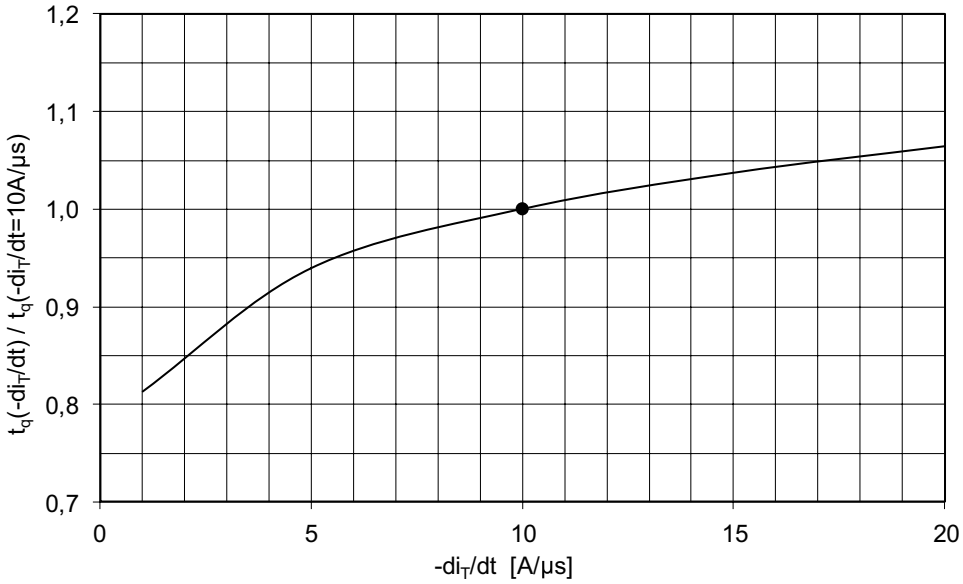


Figure 30 Typical dependence of the turn-off time t_q normalized to the $-di_T/dt_{norm}$ on the off-commutating rate of fall $-di_T/dt$

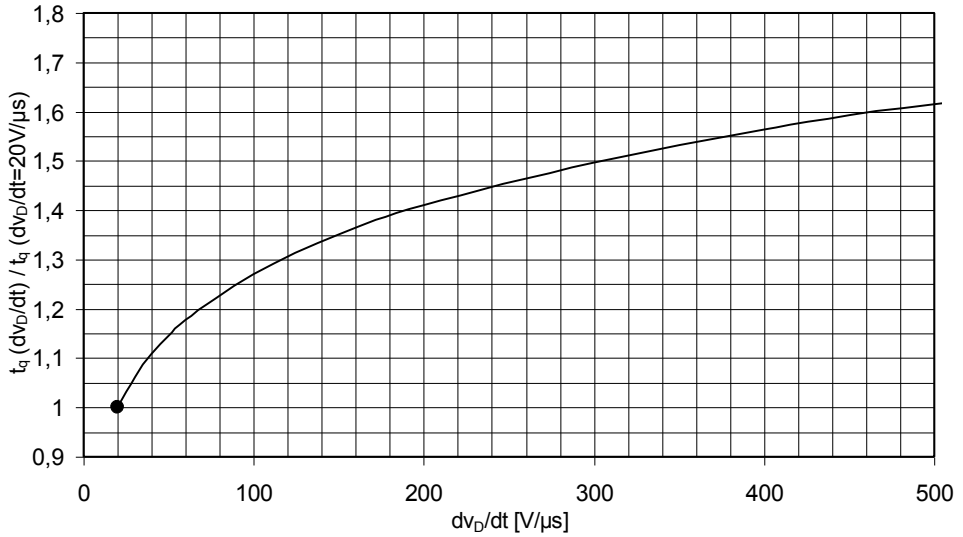


Figure 31 Typical dependence of the turn-off time t_q normalized to the dv_D/dt = 20V/µs on the rate of rise of off-state voltage dv_D/dt

3.5 Power dissipation (losses)

For thyristor and diode the dissipation (or losses) are classified as off-state, on-state, turn-on and turn-off losses. The thyristor also shows control losses. Under given cooling conditions their sum determines the current loading capability.
For mains operation up to 60Hz with its moderate dynamic requirements the dimensioning can be exclusively done based on the on-state losses, as the sum of the others is comparatively negligible.
For semiconductors with high blocking voltages (› 2200V) or large square sections with a pellet Ø ≥ 80mm even for mains operation the turn-off losses should be regarded in the calculation.

3.5.1 Total power dissipation P_{tot}

P_{tot} is the average value of the sum of the individual losses.

3.5.2 Off-state losses P_D, P_R

P_D, P_R are the losses caused by off-state current and off-state voltage in forward direction (P_D) and in reverse direction (P_R).

3.5.3 On-state losses P_T, P_F

P_T, P_F is the electric power converted to heat when only the conducting state in forward direction is considered. The average value of the on-state loss P_{TAV} or P_{FAV} is calculated with the values of the equivalent straight line according to the following formula:

$$P_{TAV} = V_{T(TO)} \bullet I_{TAV} + r_T \bullet I^2_{TRMS} = V_{T(TO)} \bullet I_{TAV} + r_T \bullet I^2_{TAV} \bullet F^2 \text{ (for thyristors)}$$
$$P_{FAV} = V_{F(TO)} \bullet I_{FAV} + r_T \bullet I^2_{FRMS} = V_{F(TO)} \bullet I_{FAV} + r_T \bullet I^2_{FAV} \bullet F^2 \text{ (for diodes)}$$

For formfactors F refer to Table 1

The diagrams in the data sheets show the relation of the average value of on-state dissipation power and on-state current for various shapes of current.

Instead of calculating the on-state losses with v_{T0}, v_{F0} and r_T, alternatively the on-state voltage can be calculated with a more precise approximation with the following relation:

$$v_T = A + B \cdot i_T + C \cdot \mathrm{Ln}(i_T + 1) + D \cdot \sqrt{i_T}$$

The factors A, B, C and D are listed in the datasheets.

Exception: PowerBLOCK-Modules are not listed with the ABCD coefficients.

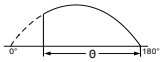
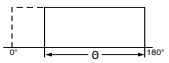
Stromform Current waveform	Scheitelfaktor peak factor $S = \frac{\hat{i}}{I_{RMS}}$	Mittelfaktor average factor $M = \frac{\hat{i}}{I_{AV}}$	Formfaktor form factor $F = \frac{I_{RMS}}{I_{AV}}$	Formfaktor² form factor² F^2
 sinus 180° el	2	π = 3,14	π / 2 = 1,57	2,47
sinus 120° el	2,23	4,18	1,875	3,52
sinus 90° el	2,83	6,29	2,22	4,93
sinus 60° el	3,88	10,9	2,77	7,66
sinus 30° el	5,88	23,42	3,98	15,8
DC	1	1	1	1
 rect 180° el	$\sqrt{2} = 1{,}41$	2	$\sqrt{2} = 1{,}41$	2
rect 120° el	$\sqrt{3} = 1{,}73$	3	$\sqrt{3} = 1{,}73$	3
rect 90° el	$\sqrt{4} = 2$	4	$\sqrt{4} = 2$	4
rect 60° el	$\sqrt{6} = 2{,}45$	6	$\sqrt{6} = 2{,}45$	6
rect 30° el	$\sqrt{12} = 3{,}46$	12	$\sqrt{12} = 3{,}46$	12

Table 1 Form factors for phase angle control conditions

3.5.4 Switching losses P_{TT}, $P_{FT}+P_{RQ}$

P_{TT}, $P_{FT}+P_{RQ}$ are the portions of electric power converted to heat when turning on (P_{TT} for thyristors, P_{FT} for diodes) and turning off (P_{RQ}). The average switching losses increase with increasing rates of rise and fall of the on-state current at turn-on and turn-off as well as with the frequency of repetition. Up to medium size thyristors and diodes with blocking voltages up to 2200V and applications at mains frequencies of up to 60Hz the switching losses are mostly negligible compared to the on-state losses.
For semiconductors with high blocking voltages › 2200V or large square sections with a pellet Ø ≥ 80mm even for mains operation the turn-off losses should be regarded in the calculation (on request if necessary).
The turn-off losses of diodes, however, are generally still negligible.

3.5.4.1 Turn-on losses P_{TT}, P_{FT}

P_{TT}, P_{FT} is that dissipative portion which exceeds the on-state loss P_T (for thyristors) or P_F (for diodes) during turn-on. It is caused on the one hand by the carrier storage effect and on the other hand by the delayed propagation of the current carrying area.
To be able to turn on with the greatest possible square section many thyristors are equipped with trigger amplification. This consist of one or several amplifying gates (= auxiliary thyristors). In thyristors with large square sections the amplifying gate is branched (finger structure). This causes a wider area to become conductive at the time of triggering and thus reduces the turn-on losses.

The sum of turn-on and on-state losses P_{TT}, $P_{FT} + P_T$, P_F important for the dissipation calculation may be drawn from the progression of the on-state current and the on-state voltage during and after turning on.

$$P_{TT} + P_T = \frac{1}{t_T} \int_o^{t_T} i_T(t) \cdot v_T(t)\, dt \qquad \text{(for thyristors)}$$

$$P_{FT} + P_F = \frac{1}{t_T} \int_o^{t_T} i_F(t) \cdot v_F(t)\, dt \qquad \text{(for diodes)}$$

In practice the turn-on losses are generally neglected.

3.5.4.2 Turn-off losses P_{RQ}

Turn-off losses occur due to the carrier storage effect. They depend on the progression of the reverse delay current as well as on the magnitude and rate of rise of the reverse off-state voltage and may therefore be influenced by the snubber (see Figure 23).

$$P_{RQ} = \frac{1}{t_{int}} \int_o^{t_{int}} i_R(t) \cdot v_R(t)\, dt$$

For the time period t_{int} to be determined by integration the turn-off losses are calculated as follows:
An approximation of the turn-off losses may be calculated as follows:

$P_{RQ} = E_{RQ} * f \approx Q_r * v_R * 0.4 * f$ for the on-state limit characteristic
$P_{RQ} = E_{RQ} * f \approx Q_r * v_R * 0.5 * f$ for the typical on-state characteristic

E_{RQ} = turn-off loss energy
f = frequency
Q_r = maximum recovery charge
v_R = (reverse voltage) driving voltage after commutation

3.5.5 Gate dissipation P_G

P_G is the electrical power converted into heat due the gate current flowing between gate terminal and cathode. This is distinguished into peak gate dissipation P_{GM} (product of the peak values of gate current and gate voltage) and average gate dissipation P_{GAV} (average value of gate dissipation referenced to the cycle duration).

3.6 Insulation test voltage V_{ISOL}

The insulation test voltage V_{ISOL} is the RMS-value of a sinewave voltage between the base plate and the terminal of thyristor or diode modules. For DC-requirements $V_{ISOL\,DC}$ is equal to the peak value of the specified RMS-value (i.e. 1.41* V_{ISOL}). During the test all terminals are connected with each other and V_{ISOL} is applied versus the base plate.

4. Thermal properties

In order to maintain the thermal equilibrium the electric power loss converted to heat in the semiconductors has to be dissipated. For this purpose heatsinks with defined cooling properties are available. To describe this function thermal equivalent circuits, by analogy to electrical ciruits, according to Figure 32 are used.

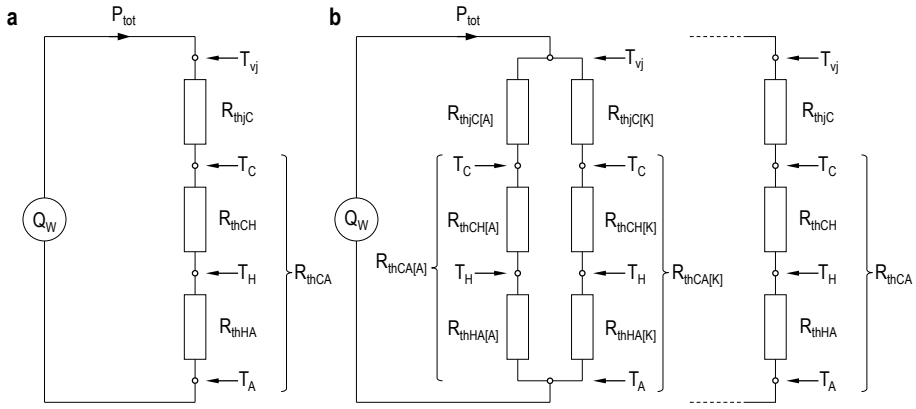


Figure 32 Thermal equivalent circuits for diodes and thyristors

$R_{th\ JC}$= steady state thermal resistance junction - case
$R_{th\ CH}$= steady state transfer thermal resistance case - heatsink
$R_{th\ HA}$= steady state thermal resistance heatsink

a - single sided cooling
b - double sided cooling

4.1 Temperatures

4.1.1 Junction temperature T_{vj}, $T_{vj\ max}$

The junction temperature is the most important reference for all fundamental electrical properties. It represents a mean spatial temperature within the semiconductor systems and is, therefore, known more precisely as the equivalent junction temperature or virtual junction temperature.
To observe the maximum permissible junction temperature $T_{vj\ max}$ is important for the function and reliability of the device. To exceed this maximum value may change the properties of the semiconductor irreversibly and destroy it.

4.1.2 Case temperature T_C

T_C is the maximum temperature at the contact area of the thyristor or diode case of a disc cell or the base plate of a PowerBLOCK-module.

4.1.3 Heatsink temperature T_H

T_H is the temperature of the heatsink resulting from the semiconductor through the contact area of the heatsink and its surrounding cooling media.
The heatsinks offered by Infineon have been tested and specified with components mounted. The heatsink data given, therefore, include the thermal transfer resistance R_{thCH} between device and heatsink. This value can, therefore, be disregarded in the calculation.

4.1.4 Cooling medium temperature T_A

T_A is the temperature of the cooling medium prior to entering the heatsink. For air cooling this is defined at the inlet side of the heatsink. For fluid cooling it is defined at the inlet of the heatsink.

4.1.5 Junction operating temperature range T_{cop}

T_{cop} is the case temperature range in which the power semiconductor may be operated.

4.1.6 Storage temperature range T_{stg}

T_{stg} is the temperature range in which the power semiconductor may be stored without the application of electricity. Independently of the maximum permissible junction temperature unlimited in time, the maximum permissible storage temperature for epoxy disc cells and for PowerBLOCK-modules is T_{stg} = 150°C with a time limit to 672h according to DIN IEC 60747-1.

4.2 Thermal resistances

4.2.1 Internal thermal resistance R_{thJC}

R_{thJC} is the ratio of the difference between the junction temperature T_{vj} and the case temperature T_C to the total power dissipation P_{tot}:

$$R_{thJC} = \frac{T_{vj} - T_C}{P_{tot}}$$

It depends on the internal design as well as the shape and frequency of the on-state current.
The thermal resistance for double sided cooling compared to single sided cooling is lower due to paralleling of the individual thermal resistances (see Figure 32).
The thermal resistance depends on the type and shape of the semiconductor. It is therefore not 100% measured, but established instead during the initial type approval qualification tests.

4.2.2 Thermal transfer resistance R_{thCH}

R_{thCH} is the ratio of the difference between the temperature of the contact areas of the device and the heatsink $T_C - T_H$ to the total power dissipation P_{tot}:

$$R_{thCH} = \frac{T_C - T_H}{P_{tot}}$$

The values given are valid only when mounted correctly (see section 8).

4.2.3 Heatsink thermal resistance R_{thCA}

R_{thCA} is the ratio of the difference between the case temperature T_C and the coolant temperature T_A to the total power dissipation P_{tot}:

$$R_{thCA} = \frac{T_C - T_A}{P_{tot}}$$

4.2.4 Total thermal resistance R_{thJA}

R_{thJA} is the ratio of the difference between the equivalent junction temperature T_{vj} and the coolant temperature T_A to the total power dissipation P_{tot}:

$$R_{thJA} = \frac{T_{vj} - T_A}{P_{tot}} = R_{thJC} + R_{thCA}$$

4.2.5 Transient internal thermal resistance Z_{thJC}

Z_{thJC} describes the progression of the component's thermal resistance over time. In the data sheets Z_{thJC} is given for constant DC-current and partly also for pulse currents. Additionally, the partial thermal resistances R_{thn} and time constants t_n are compiled in a table as an analytical function.

$$Z_{(th)JC} = \sum_{n=1}^{n_{max}} R_{thn}\left(1 - e^{-t/t_n}\right)$$

4.2.6 Transient heatsink thermal resistance Z_{thCA}

Z_{thCA} describes the progression of the heatsink thermal resistance over time. Z_{thCA} is defined in individual data sheets. Additionally, the values R_{thCAn} and t_n of the analytical function are compiled in a table. There is no generally defined transient thermal resistance for heatsinks. On the one hand, it depends on the contact region between power semiconductor and heatsink. On the other hand, the cooling method (natural/ forced) and the flow of the cooling medium have a strong influence.
In case of natural cooling and oil cooling, the flow of the cooling medium is caused by the convection of the air or oil. As the power dissipation defines the convection, the actual power dissipation is specified for natural cooling and oil cooling. The correct direction and position of the heatsink has to be observed.
In case of forced cooling and water cooling, the flow of the cooling medium is specified.

Short-term temperature variations due to pulse currents are widely independent of these parameters. They are equalised through the large thermal capacity of the heatsink.

The heatsinks offered by Infineon have been tested and specified with components mounted. These given heatsink data include the transfer thermal resistance R_{thCH} between device and heatsink. This value is, therefore, to be disregarded.

4.2.7 Total transient thermal resistance Z_{thJA}

Z_{thJA} describes the progression of the total thermal resistance over time. The calculation of the junction temperature for short-term loads is to be based on the total transient thermal resistance. Z_{thJA} is the sum of:

$$Z_{thJA} = Z_{thJC} + Z_{thCA}$$

4.3 Cooling

4.3.1 Natural air cooling

In natural air cooling (air convection cooling) the power losses are dissipated due to natural convection of the air. Generally the current loading capability of power semiconductors is defined at an ambient temperature $T_A = 45°C$.

4.3.2 Forced air cooling

In forced air cooling the cooling air is forced through the fins of the heatsink by means of a fan. Generally the current carrying capability of power semiconductors is defined at an ambient temperature $T_A = 35°C$.

4.3.3 Water cooling

In water cooling the power losses are dissipated by means of water. Generally, the current loading capability of power semiconductors is defined at an inlet water temperature $T_A = 25°C$.

4.3.4 Oil cooling

In oil cooling the power losses are dissipated by means of oil. Generally, the current loading capability of power semiconductors is defined at an inlet oil temperature $T_A = 70°C$.

5. 5. Mechanical properties

5.1 Tightening torque

When mounting PowerBLOCK modules and studs, Infineon recommends keeping the tightening torques as given in the data sheet, as otherwise the correct function within the specifications cannot be guaranteed (see also 8.2).

5.2 Clamping force

The clamping force given in the data sheet is necessary for perfect electrical and thermal contact of devices with flat base or disc housing. It must be largely homogeneous across the contact surfaces (see also 8).
The limits of the clamping force for devices in disc housings are given in the relevant data sheets. These have to be precisely observed. Deviations may alter the data and require special agreement. The clamping force recommended should approximately be in the middle between the given limits.

5.3 Creepage distance

The creepage distance between anode and cathode or anode and gate is defined according to DIN VDE 0110.

5.4 Humidity classification

The values given comply with DIN IEC 60721-3 (3K3).

5.5 Vibration

The values given follow DIN IEC 60068, part 2-6.
It is given in the data sheet as a multiple of the gravitational constant ($1g = 9.81 m/s^2$).

5.6 UL-registration

PowerBLOCK modules normally comply with the standard for electrically insulated semiconductor components of the Underwriters Laboratories Inc.
The appropriate file number is listed in the individual data sheets in the section Mechanical Properties.

6. Notes for applications

6.1 Case non-rupture current

The case non-rupture current is the peak value of a current pulse in reverse direction which causes neither a mechanical destruction of the case nor the escape of combustive plasma.
The non-repetitive surge currents I_{TSM}, I_{FSM} and $\int i^2dt$ values given in the data sheets define the limit of electrical stress in forward direction. They are used to design the short circuit protection. By definition thyristors and diodes will not be destructed by this stress. In any case thyristors have to be triggered by sufficient gate current.
If the short circuit current in forward direction is higher than the given maximum values, at first electrical destruction occurs. The mechanical destruction of the device housing occurs only at substantially higher stress as the total active region of the semiconductor partakes in carrying the current.
If a thyristor or a diode becomes defective in reverse direction, a short circuit current flows in reverse direction. The cathode region not destroyed at that stage does not partake in the current flow. A small edge around the destroyed spot melts and an arc develops inside the case. The melted material vaporizes to hot plasma which depending on its intensity may lead to the destruction of the case. Often a hole in the case results through which hot plasma escapes. In high power installations with strong magnetic fields it may lead to the short circuit and destruction of the equipment.
Destructive tests carried out on thyristors and diodes in reverse direction show great variance in the distribution of the case non-rupture current depending on the location of the destroyed spot on the silicon pellet. Infineon always places the destruction spot at the edge as thereby the most critical case non-rupture currents occur. The rate of rise of the short circuit current which depends on the inductances of the short circuited section of the installation is also of influence. Infineon specifies the case non-rupture current for a 50Hz half-sinewave.
For diodes and thyristors the case non-rupture current may be lower than the non-repetitive surge on-state current I_{TSM} or I_{FSM}. In these instances the case non-rupture current is given as the peak value of a half-sinewave of 50Hz additionally in the data sheets for disc cells. The I^2t-value resulting from this can be recalculated to the peak value of a half-sinewave of 60Hz.
Recalculations of this case non-rupture current to other current wave forms, as for example occur when a short circuit is turned off due to a fuse failure, are not or only partly correct even when they are based on an appropriate current-time-integral.
To avoid damage the user has to provide appropriate protection measures in particular in high power installations.

6.2 Thermal load cycling

Thermal load cycling in semiconductor systems results in mechanical stresses or sliding action due to the different coefficients of expansion of the materials. The load cycle capability of components, therefore, depends on the magnitude as well as the progression of the temperature shifts in the device and on the number of cycles. Rapid temperature changes of low magnitude as they often occur in permanent operation with a frequency of repetition $f_0 \geq 40Hz$ bear no influence on the load cycle capability. Only in operation with heavy load changes or low frequency of repetition, the magnitude of the rapid temperature changes in the device ΔT_{vj} are to be observed with regard to sufficient lifetime for thermal load cycling.

6.3 Parallel connection

When connecting thyristors or diodes in parallel, equal distribution of the load current in the branches should be aimed for. Reasons for deviations from current sharing are:

- Different slope resistances in parallel branches. These are caused by the variance in distribution of the on-state characteristics of the devices and through the construction in the paralleled circuits (see Figure 34).

Dynamic influences, such as:

- variance of the gate controlled delay time
- differences in the dynamic turn-on behaviour
- additionally induced voltages caused by the mechanical construction

In addition, it should be taken into consideration that all RC-snubbers of the paralleled branches will discharge across the thyristor which triggers first.

Equal current sharing in the paralleled branches can be achieved by the following measures:

- Application of thyristors or diodes with approximately the same on-state voltages. On request the supply of such components in groups with the same vT- or vF-class is possible.
- Identification of the vT- or vF-class respectively is provided on the ceramic disc cell, by means of a “V” followed by a 4-digit number printed on it. “V” is an abbreviation standing for the on-state voltage. The 4-digit number indicates the maximum on-state voltage of the corresponding vT-/vF-class and the class width (see Figure 33)

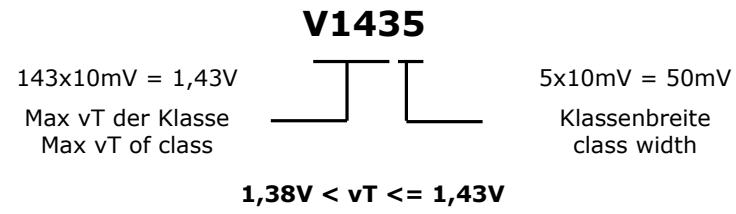


Figure 33 Example of v_T/v_F class definition

- Equal slope resistances as far as possible. Additional series resistances in the individual branches of the paralleled thyristors or diodes e.g. fuses will improve the symmetry.
- Application of series inductances to equalise current sharing of the thyristors.

- Minimal deviation in gate controlled delay time values. To minimise this, triggering of the thyristors with synchronous, steep and high current pulses is required.

  $i_{GM} \geq 4...10\ I_{GT}$
  $d_G/dt \geq i_{GM}/(0.5\text{-}1\mu s)$

  The anode-cathode voltage across the paralleled devices drops to the on-state voltage of the first thyristor which triggers. Consequently, the voltage dependent trigger delay of the thyristors turning on later and the start of turn-on of these thyristors is retarded accordingly.

  This has to be considered in particular for light triggered thyristors as these require a higher anode-cathode voltage to safely turn-on.
  For high power thyristors (T...1N) the data sheet recommends a trigger pulse with gate controlled delay time. With this, the deviation of the gate controlled delay times t_{gd} may be reduced to values $\Delta t_{gd} < 0.5\mu s$ under the listed conditions. In conjunction with the snubber this is generally sufficient for safe triggering of the thyristors which makes additional selection needless.
  To parallel light triggered thyristors (T...3N) Infineon recommends the use of laser diodes SPL PL90 with the appropriate fibre optic cable and a control pulse for the laser diode of 1.3A for 2µs followed by 0.8A for 8µs (see Figure 18).

- The gate pulses described above also assure that the differences in the dynamic on-state characteristics are minimised.

- In particular for large thyristors and those with high blocking voltages the risk exists that some of these will return to the forward off-state after triggering due to a too low on-state current density. Overloading of the current carrying thyristors after renewed load current increase can be avoided by repetitive triggering.

In general, a current sharing imbalance of less than 10% is aimed for.

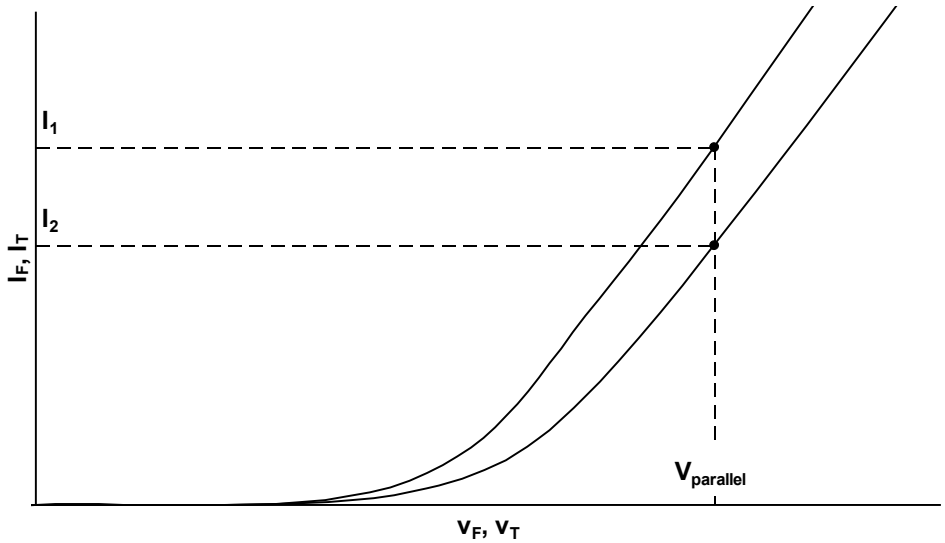


Figure 34 Current sharing imbalance due to different on-state voltages in parallel connection

6.4 Series connection

When connecting thyristors or diodes in series, equal distribution of the off-state voltage should be aimed for. Reasons for deviations from the ideal voltage sharing are:

- Different leakage currents
  Without additional external components, an unfavourable voltage sharing may occur during the steady off-state condition in both directions as the voltage across the individual thyristors or diodes results out of the uniform reverse current in the series circuit (see Figure 35).

- Variance of the gate controlled delay time
  During turn-on the thyristors triggered last are exposed by higher off-state voltage.

- Variance of the reverse recovery charge
  Differences of the reverse recovery charge Q_r cause different reverse recovery times t_{rr} and peak reverse recovery currents I_{RM} which means that the thyristors or diodes take up off-state voltage at different times (see Figure 36). The variance of the reverse recovery charge ΔQ_r of two thyristors or diodes connected in series effects a voltage deviation $\Delta V \approx \Delta Q_r / C$ where C is the capacitor of the parallel snubber circuits (see section 7.1).

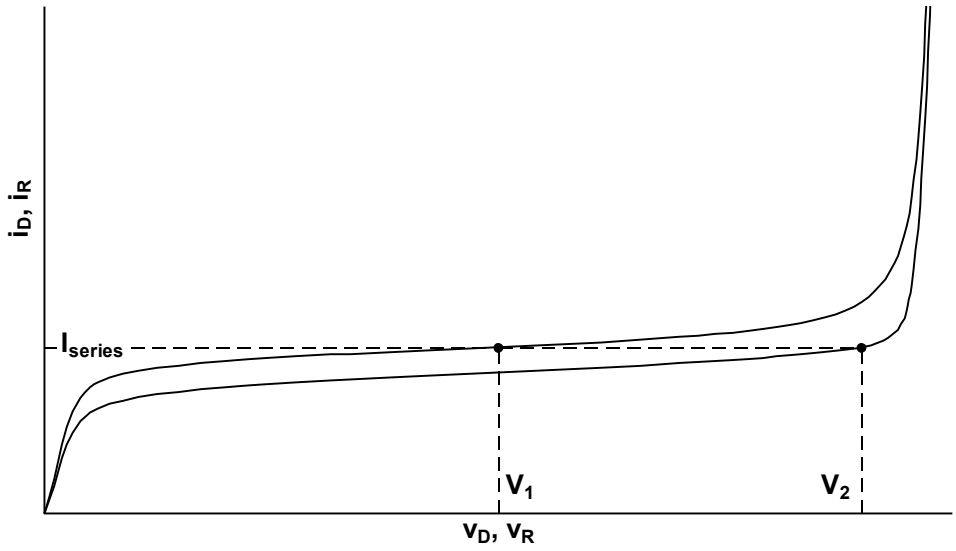


Figure 35 Voltage sharing imbalance due to different leakage currents in series connection

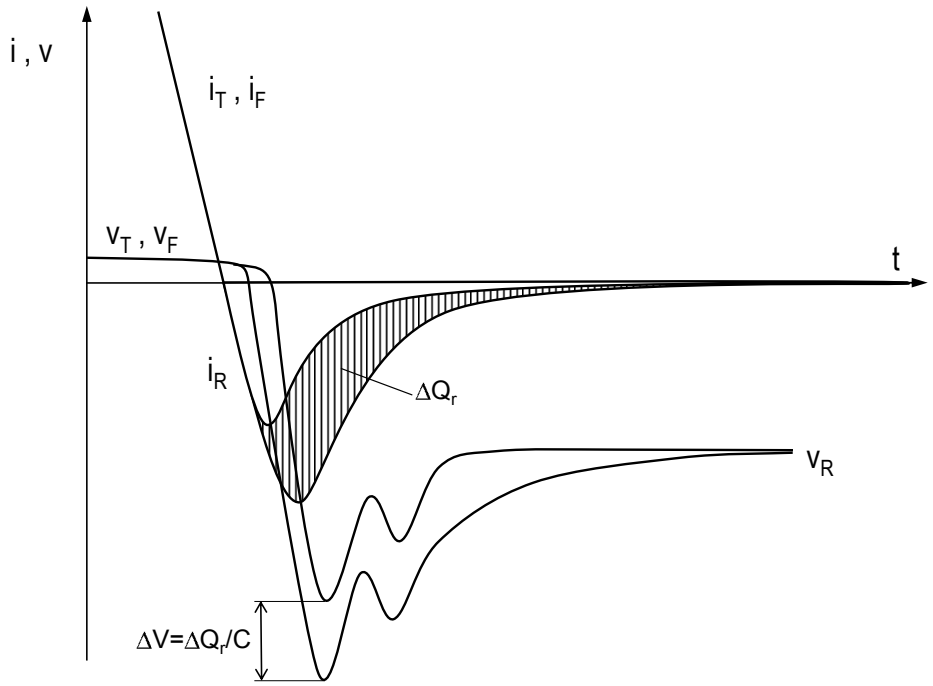


Figure 36 Voltage sharing imbalance due to different turn-off properties

Equal off-state voltage for thyristors and diodes connected in series may be achieved by the following meaures:

- Steady state voltage sharing during the off-state phase
  For this the RC-snubber is often sufficient. In case the DC off-state voltage is applied for longer periods, an additional voltage sharing resistor paralleled to each thyristor or diodes is necessary. It should carry about two to five times the leakage current of the applied power semiconductor at operating temperature in order to externally force a steady state voltage symmetry. If the operating temperature is less then the maximum allowable junction temperature for continuous operation, the leakage current drops per 10°C to approx. 66% of the initial value.
  For example for thyristors with a maximum allowable junction temperature the following applies
  $T_{vj\,max}$ = 125°C:
  0.66 I_D o$_R$ 0.66 I_R at T_{vj} = 115°C
  0.44 I_D o$_R$ 0.44 I_R at T_{vj} = 105°C etc.

- Dynamic voltage sharing at turn-on
  To reduce the variance of the gate controlled delay times, triggering of electrically triggered thyristors is necessary with synchronous, steep and high trigger pulses.

  $i_{GM} \geq 4...10\ I_{GT}$
  $di_G/dt \geq i_{GM}/(0.5\text{-}1\mu s)$

  Such strong trigger pulses reduces the spread of the gate controlled delay time to values $\Delta t_{gd} < 1\mu s$. It has to be ensured that the reverse blocking voltage of the thyristor which is last to turn on (in a series connection)

increases only slowly. Often the RC-snubber is sufficient for this. In case the inductance of this circuit working jointly with the RC networks are not sufficient to reduce the reverse voltage increase additional saturable inductances are to be implemented.

For high power thyristors (T...1N) a trigger pulse for a gate controlled delay time is recommended in the data sheet. With this or better pulses the variance of the gate control delay times may be reduced to values $\Delta t_{gd} < 0.5\mu s$ under the given conditions. For series connection of light triggered thyristors (T...3N) which are exposed to high current rise times Infineon recommends the use of laser diodes SPL PL90 with the appropriate fibre optic cable and a control pulse of 1.3A for 2µs followed by 0.8A for 8µs.

- Dynamic voltage sharing at turn-off
  During turn-off it is possible to improve the imbalance of off-state voltage sharing both by sufficient dimensioning of the paralleled snubbers as well as by a small variance of the recovery charge ΔQ_r of the thyristors in series. The supply of thyristors and diodes in groups with the same Q_r-class is possible on request.

6.5 Pulsed Power

Pulsed power applications are generally applications with very low duty cycle.

To dimension semiconductors for pulsed power applications generally the following has to be observed:

6.5.1 Applications with DC

Often the power semiconductors in pulsed power applications are exposed to high DC-voltages. For this the limitations regarding reduced voltage stress are to be observed (see 3.1.2.3 and 3.2.2.3).

6.5.2 Current rise time at turn-on

Due to the finite propagation in the triggered area (~ 0.1mm/µs) when the thyristor is turned on, the load current is initially concentrated to a small area. If the current density exceeds the critical value, destruction of the device is likely. Therefore the peak current amplitude in short pulse durations drops significantly (see Figure 37).

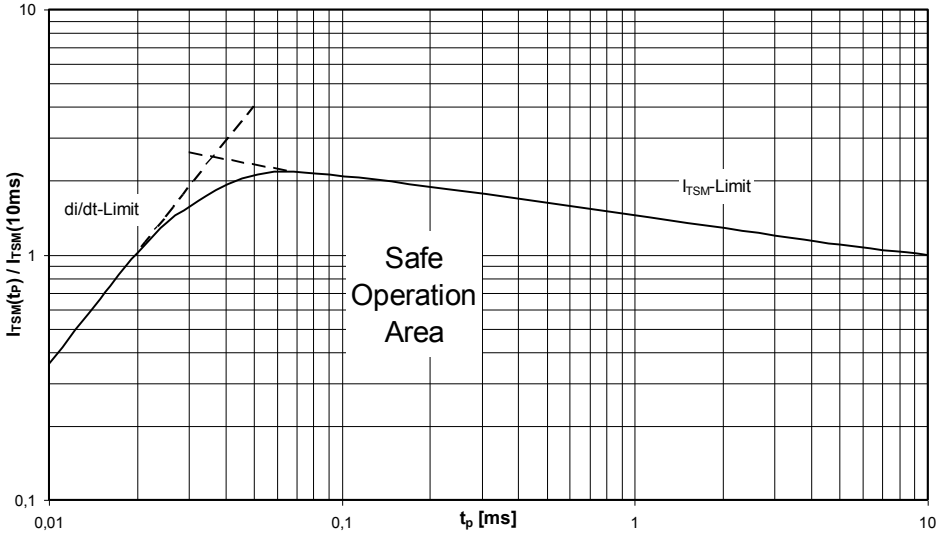


Figure 37 Schematic representation of the Safe Operation Area (SOA) of a thyristor optimised for pulsed power with single sine wave current pulses

6.5.3 Zero crossing of current and voltage during turn-on

With positive voltage applied to a thyristor may be turned on by a trigger pulse. After the gate controlled delay time of up to several µs the voltage collapses sharply, the load current rises and the propagation in the conduction zone starts. If during this process a reversal of voltage and current to negative values occurs, a constriction of the conductive zone results. The energy is concentrated to a small section and can destroy the semiconductor, regardless of whether it is light triggered or electrically triggered.
Such operating conditions are to be avoided by the use of appropriate free-wheeling circuits.

6.5.4 Turn-off with a high di/dt versus a negative voltage

These operating conditions are to be avoided if possible as they require very extensive snubbering if controllable at all. The voltage peaks result from the snap-off of the reverse recovery current and the inductances in the circuit and have to be limited to values permissible for the semiconductor.
Figure 38 and Figure 39 depict circuits suitable for pulsed power applications and the stresses to which the semiconductors are exposed. With the circuit shown in Figure 39 the thyristors are stressed more (see Figure 40 – Var.2). By using circuit shown in Figure 38 the turn-off versus voltage is avoided, however (see Figure 40–Var.1).

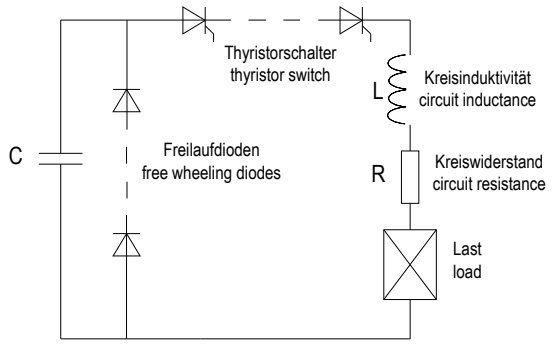


Figure 38 Thyristor switch with free-wheeling circuit at the capacitor side

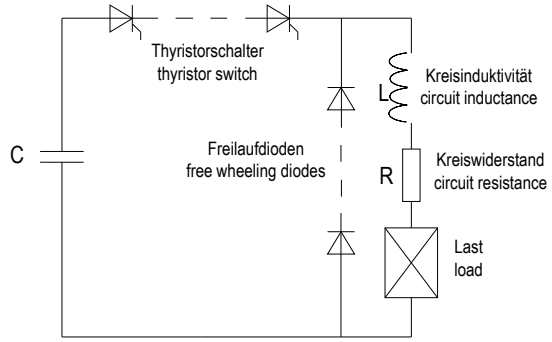
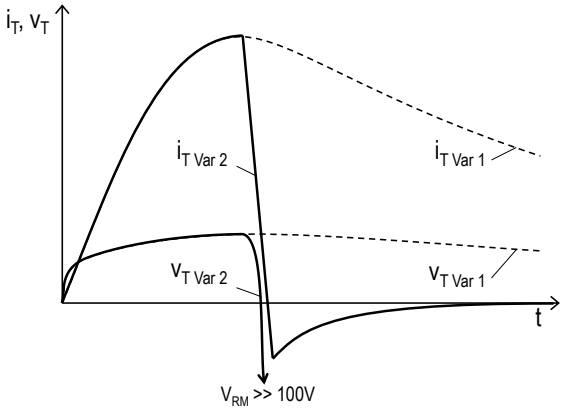


Figure 39 Thyristor switch with free-wheeling circuit at the load side



Var 1: Freilaufdiode am Kondensator
free wheeling diode at capacitor

Var 2: Freilaufdiode an Last
free wheeling diode at load

Figure 40 Current and voltage waveforms at the thyristor

7. Protection

Thyristors and diodes have to be reliably protected versus too high currents and voltages as well as interference pulses in the control circuit.

7.1 Overvoltage protection

On the whole, overvoltages in an installation have the following causes:

- **Internal overvoltages** Due to the carrier storage effect of the power semiconductors

- **External overvoltages** Due to switching processes on the line and atmospherical influences such as
  - switching of transformers without load
  - switching of inductive loads
  - blowing of fuses
  - lightening strikes

As thyristors and diodes may be destructed by overvoltages in the micro second region, their overvoltage protection requires particular attention. When designing appropriate snubbering the blocking capability (V_{DRM}, V_{RRM}) as well as the critical rate of voltage rise $(dv/dt)_{cr}$ has to be considered.

7.1.1 Individual snubbering (RC-snubber)

During turn-off the load current of the thyristor or the diode does not stop to flow at the zero crossing but continues briefly in reverse direction as reverse recovery current due to the carrier storage effect (Figure 23). Once the peak reverse recovery current is reached, the more or less steeply falling reverse delay current causes a voltage peak at the inductances of the load circuit which is superimposed onto the driving voltage and may thus put the semiconductor at risk.
This overvoltage may be effectively reduced by the individual snubbering of the semiconductor with an RC-snubber. To dimension this snubber it is necessary to know the most important factors of influence such as the magnitude of i_{TM} or i_{FM} and rate of fall of $-di_T/dt$ or $-di_F/dt$ of the on-state current, peak reverse recovery current I_{RM}, reverse off-state voltage v_{RM}, repetitive reverse peak off-state voltage V_{RRM} of the semiconductor as well as the critical rate of voltage rise $(dv/dt)_{cr}$ for thyristors. In mains commutated converters RC-snubbers for thyristors and diodes can be used under normal operating conditions according to Table 2 under the following conditions:

- Short-circuit voltage of the converter supply transformer $u_K \geq 4\%$. When connected directly to the mains the protection choke has to be dimensioned accordingly.

- Safety margin between the repetitive peak off-state voltage and the peak value of the supply voltage ≥ 2.2.

			Durchlassstrom I_{TAV}, I_{FAV} on-state current I_{TAV}, I_{FAV}					
			≤ 50 A	≤ 100 A	≤ 200 A	≤ 500 A	≤ 1000 A	≤ 2000 A
Anschlusspannung V_N nominal voltage V_N	≤230V	C [µF]	0,22	0,33	0,68	1,5	3,3	6,8
		R [Ω]	47	33	22	12	6,8	6,8
		P[W]	≥ 5	≥ 10	≥ 15	≥ 30	≥ 70	≥ 150
	≤400V	C [µF]	0,12	0,22	0,47	1,0	2,2	4,7
		R [Ω]	82	56	33	22	15	12
		P[W]	≥ 7	≥ 15	≥ 30	≥ 70	≥ 125	≥ 300
	≤500V	C [µF]	0,10	0,18	0,39	0,82	1,8	3,3
		R [Ω]	120	68	39	27	18	15
		P[W]	≥ 10	≥ 25	≥ 50	≥ 100	≥ 200	≥ 400
	≤690V	C [µF]			0,27	0,56	1,0	1,8
		R [Ω]			47	33	22	22
		P[W]			≥ 70	≥ 125	≥ 250	≥ 500

Table 2 RC-snubbers for individual snubbering in mains applications

Especially in cases of steep rate of fall of the on-state current or low safety margin of the blocking capability the RC-snubbers recommended above should be checked for suitability. In these cases often capacitors with greater capacity as well as appropriately re-dimensioned resistors are required. The best equivalent resistance for the most favourable non-periodic dampened overvoltage progression is calculated as follows:

$$C' = \frac{Qr}{V_R * \sqrt{2}} \qquad R' = (1,5...2) \cdot \sqrt{\frac{L'}{C'}}$$

Where R' and C' are equivalent values of the RC-series snubber and L' is the equivalent value of the converter inductance.

Schaltung	R'	C'	L'
M1	R	C	L_S+L_G
M2	R	C	2 L_S
B2	$^1/_2$ R	C	L_S
M6	$^1/_2$ R	2 C	2 L_S
B6	$^3/_5$ R	$^5/_3$ C	2 L_S

Table 3 Equivalent values for converter circuits

R, C = values of the RC-snubber
L_S = stray inductance of the converter transformer (one phase)
L_G = inductance of the smoothing choke

For thyristors it also has to be observed that the resistor of the RC-snubber has to have the value of

$$R' \geq \frac{V_{DWM}}{I_{T(RC)M}}$$

in order for the thyristor not to be stressed with too high a discharge current from the snubber during turn-on (see also 3.4.1.2.3).

The dissipation power of the resistor is calculated according to the following formula

$P_R=k*V_R^2*C*f$	$k = 2*10^{-6}$	for uncontrolled rectifiers
	$k = 4*10^{-6}$	for controlled single and two pulse circuits and in AC-controllers
	$k = 6*10^{-6}$	for controlled three and six pulse circuits and in three-phase controllers

It should be ensured here that the values with the following units are used in the formula

P_R [W]
V_R [V]
C [µF]
f [Hz]

If required, the snubbers according to Figure 41 may be modified so that the reduction of the over-voltage and thus less stress for the thyristor during turn-on is achieved.

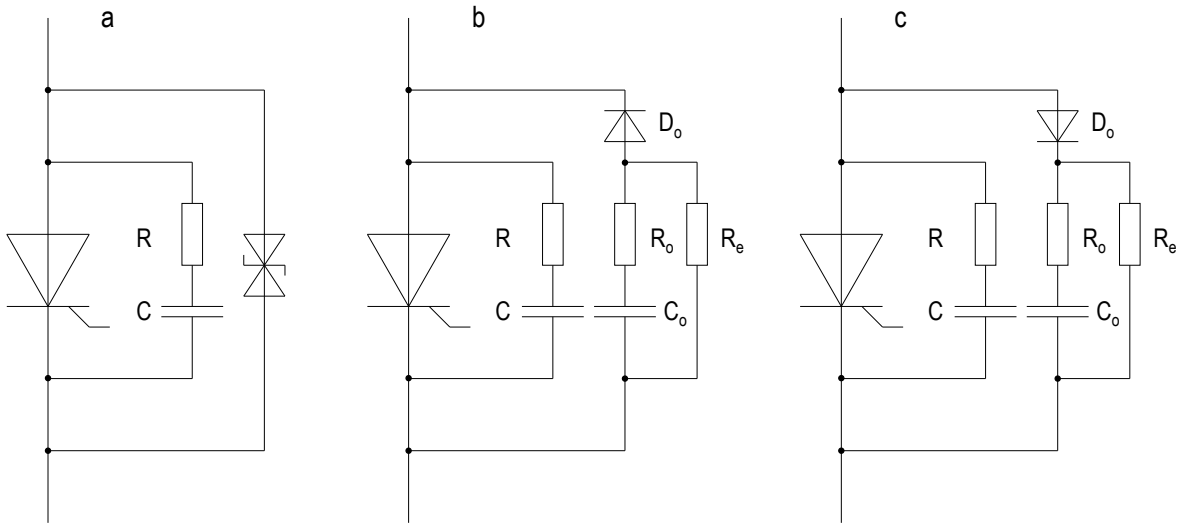


Figure 41 Examples for extending RC-snubbers for thyristors

a – with bipolar voltage surge suppressor
b – with RCD combination to dampen the turn-on current
c – with RCD combination to dampen the dv/dt and forward off-state voltage
Note: D_o = fast diode particularly regarding turn-on

The RC-snubber may usually be omitted for rectifier operation when transformer snubbering exists (see 7.1.3), provided thyristors with a critical rate of voltage rise $(dv/dt)_{cr} \geq 500$ V/µs are used.

7.1.2 Input snubbering for AC-controllers

In AC- and three phase controllers thyristors are used in anti-parallel configuration both for phase control as well as full wave operation for example in soft starters. Figure 42

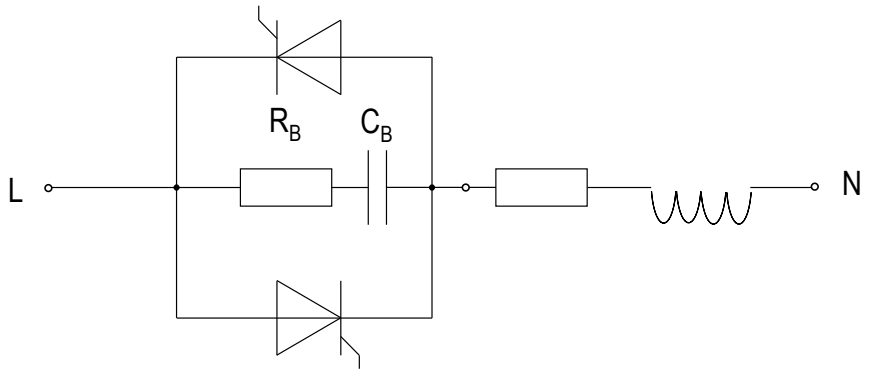


Figure 42 Snubber circuit for AC-controllers

shows the snubber circuit.
The values for RC-series snubbers recommended in Table 2 apply for the snubbering of thyristors under normal operating conditions as well as the following circumstances:

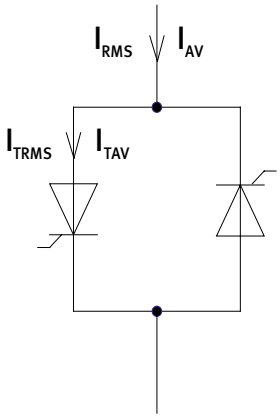
- Inductive phase angle between supply voltage and current ≤ 30°el (cos φ ≥ 0.866). This assures that possible oscillation caused by the series connection of snubber capacitors and inductances is suppressed.

- Safety margin between the repetitive peak off-state voltage of the thyristors and the peak value of the supply voltage ≥ 2.2 (see 3.1.2.1).

- Critical rate of voltage rise of the thyristors $(dv/dt)_{cr} \geq 500$V/µs.

Note: The on-state current I_{TAV} given in Table 2 is to be seen with sufficient accuracy as the average value of a thyristor in one-way configuration. To determine the load current the RMS-value I_{TRMS} of the individual thyristor in anti-parallel configuration and the RMS-value I_{RMS} of the total circuit may be derived from the following formulae:

For high power semiconductors and light triggered thyristors implemented in large



$$I_{TRMS} = \frac{I_{TAV} \cdot \pi}{2} \qquad I_{RMS} = \frac{I_{TAV} \cdot \pi}{\sqrt{2}}$$

Figure 43 Calculation of the current for an AC-controller

installations, it is common to optimise the snubbering according to the circuit parameters and the semiconductor type used. In this, the rate of voltage rise can be disregarded as the critical rate of voltage rise of these thyristors is plainly better than the criteria mentioned above.
Generic recommendations for snubber designs therefore do not make much sense.

7.1.3 Supply snubbers for line commutated converters

Energy intensive overvoltages from the mains or caused by the switching of converter transformers or chokes are preferably dampened by combined snubber circuits. For converters with thyristors or diodes they are placed on the AC-side and consist of auxiliary rectifiers with diodes and protection capacitors with discharge resistors. These discharge resistors are necessary because the diode bridge prevents the discharge of the snubber capacity. Therefore, they have to be designed in a way that this capacitance is discharged within one period (see Figure 44 and Table 4).

Additional individual snubbering of all thyristors and diodes in the converter as well as the auxiliary rectifier is

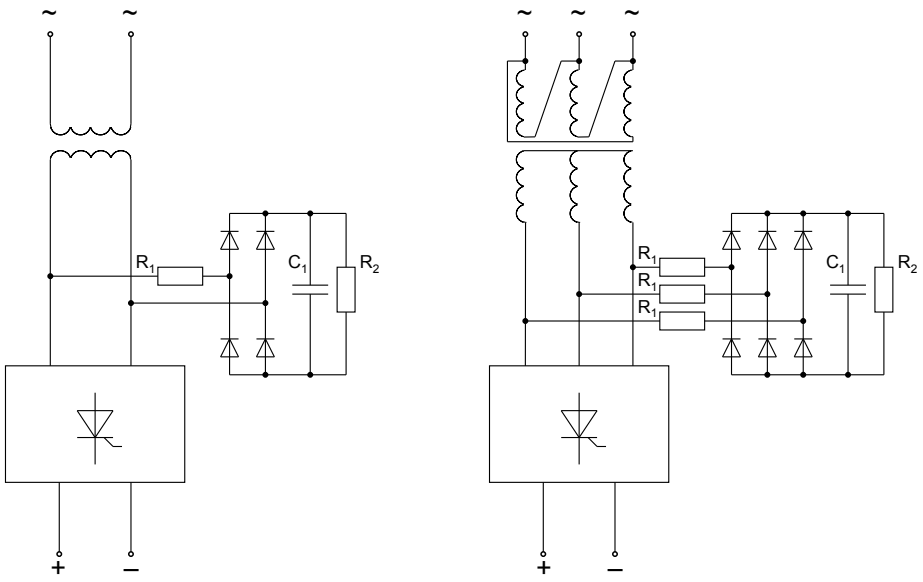


Figure 44 Combined snubber on the AC-side of a the controlled rectifier

Schaltung B6C circuit B6C				Satzausgangsstrom I_{DC} stack output current I_{DC}			
				= 200A	= 1000A	= 2500A	= 5000A
Anschluss-spannung V_N	supply voltage V_N	= 500V	R_1 [Ω]	6,8	3,9	1,8	1
			C_1 [µF]	6,8	10	22	33
			R_2 [Ω]	15	12	4,7	3,3
			P_2 [W]	32	40	104	150

Schaltung B6C circuit B6C				Satzausgangsstrom I_{DC} stack current I_{DC}				
				= 200A	= 750A	= 1500A	= 3000A	= 4000A
Anschluss-spannung V_N	supply voltage V_N	= 690V	R_1 [Ω]	22	8,2	3,9	2,7	1,8
			C_1 [µF]	2,2	4,7	10	15	22
			R_2 [Ω]	47	22	12	6,8	4,7
			P_2 [W]	20	43	78	140	201

Schaltung B6C circuit B6C				Satzausgangsstrom I_{DC} stack current I_{DC}			
				= 500A	= 1000A	= 2000A	= 3000A
Anschluss-spannung V_N	supply voltage V_N	= 1000V	R_1 [Ω]	18	8,2	5,6	3,9
			C_1 [µF]	2,2	4,7	6,8	10
			R_2 [Ω]	47	22	15	12
			P_2 [W]	42	90	133	166

Table 4 Components for a combined snubber on the AC-side of controlled three phase bridge

generally not necessary as the combined snubber acts also as an RC-network. Exempt from this are some double converter circuits such as two three-phase anti-parallel bridges. For the design of the combined snubber the following has to be observed:

- Series resistor R_1
  is there to prevent possible oscillations when the converter transformer is switched. At the same time it limits the discharge peak originating from the protection capacitor through the diodes of the auxiliary rectifier during turn-on and overvoltage stressing.
- Protection capacitor C_1
  has to absorb the energy building up when the converter transformer or a choke is switched off, so that the voltage will not exceed the maximum permissible repetitive peak off-state voltage of the thyristors or diodes to be protected; not included are the arcing losses of the switch.

- Discharge resistor R_2
  is sufficiently dimensioned - according to practical experience - when the discharge time constant t of successive overvoltage energy equals $R_2 \cdot C_1 = 80ms$.
- Auxiliary rectifier diodes
  To be considered for their selection apart from the required blocking capability is also the permissible surge current in dependence of the charge surge current of the protection capacitor. As overvoltages only occur for short periods and far apart, utilisation of the diodes is infrequent and, therefore, their power dissipation is low. As a consequence heatsinks are generally not necessary.

7.1.4 Additional options for protection versus energy intensive overvoltages

RLC – filters
consist of the stray inductivity of the converter transformer or the inductivity of the commutating chokes and the RC-networks grounded at the star point. They are suitable to dampen transient overvoltages of short duration and low energy because, with regard to the discharge current of the capacitors, the resistors may not be chosen too low. Apart from that, due to the occurring losses, the size of the capacitances is limited (see Figure 45).

Spark-gap arrestor
can be used when energy intensive overvoltages are expected from the line. Due to their delayed turn-on after their trigger voltage is reached, usually additional protection measures versus overvoltages are necessary (see Figure 45).

DC-snubbering
Overvoltages originating from the load side may be dampened with DC-snubbers (see Figure 45).
Instead of RC-networks voltage dependent resistors such as metal oxide varistors may be used. On the one hand, it is to be kept in mind that varistors are generally not suitable to limit repetitive overvoltages as they otherwise become thermally instable and are subject to severe ageing. On the other hand, it should be noted that protection for energy intensive overvoltages (usually spark-gap arrestors) must not be thwarted by incorrectly dimensioned varistors.

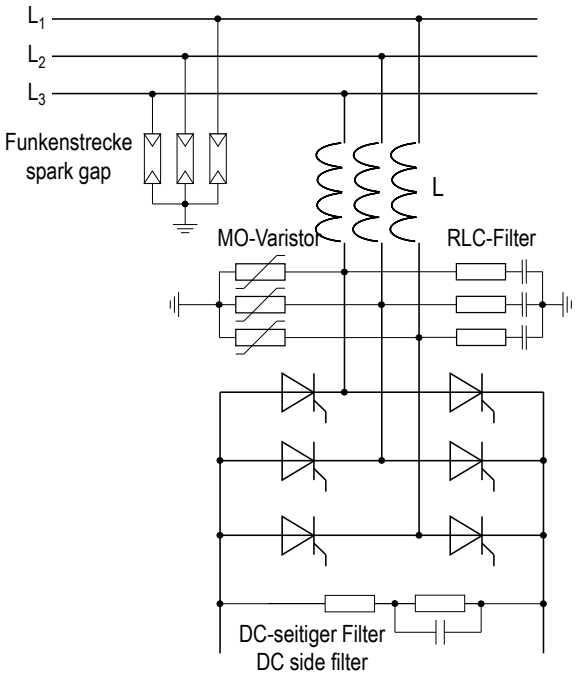


Figure 45 Additional options for protection versus energy intensive overvoltages

7.2 Overcurrent protection

Thyristors and diodes can be loaded with high operating currents but can be destroyed by overcurrents and thus require suitable protection meaures. The selection of appropriate protection depends on the type of overcurrent. In general, it is differentiated between short-term and long-term protection.

7.2.1 Short-term protection with superfast semiconductor fuses

The short-term protection limits the overcurrent originating from a short circuit to a value which does not put the thyristors or diodes at risk in at time span up to a half-sinewave and is achieved by the use of special semiconductor fuses with superfast open-circuiting characteristic. In worst case when turning off they make use of the $\int i^2dt$-value given in the data sheet for the individual type.
The semiconductors loose their off-state and blocking capability entirely or partially when stressed with the $\int i^2dt$-value until the junction temperature has dropped back to the permissible value for permanent operation. This stressing may, therefore, only be repeated after a few seconds and should only rarely occur with a limited number of pulses over the entire period of operation of the converter (see also 3.1.16).

7.2.1.1 Selection of fuses

The fuses may optionally be placed in the phase or in the branch (arm). The branch fuse enables the most secure short-term protection and permits maximum current loading of the thyristors or diodes. A construction with phase fuses reduces the complexity.

However, for possible feedback from a load with back e.m.f. an additional fuse on the output of the converter has to be implemented as a short circuit current from the load fed back into the DC-bus is not registered by the phase fuses.

For some thyristors or diodes with high current loading capability paralleling of two fuses is necessary.
When selecting a fuse the following has to be taken into account:

- Fuse voltage rating
  It has to be higher than the voltage which drives the short-circuit current.

- Voltage which drives the short-circuit current:
  It is generally the same as the supply voltage; only for AC-converter operation will it be up to the 1.8-fold value of the supply voltage.

- Reoccurring voltage V_{RMS}
  This results from the voltage V_{KRMS} driving the short-circuit current divided by the number N of the series fuses placed in the short circuit path multiplied with the safety factor $F_s = 1.3$. The following formula applies:

$$V_{RMS} = \frac{V_{KRMS}}{N} * F_s$$

  for example in B2 and B6-circuits $V_{RMS} = ½ * 1.3 * V_{KRMS} = 0.65 * V_{KRMS}$

- Fuse arcing voltage
  During the quenching process the fuse produces an arcing voltage which depends on the construction of the fuse and the reoccurring voltage. These voltage peaks may not exceed the surge peak voltage of the semiconductors in order not to harm any reversed biased components in the circuit.

- Nominal fuse current rating:
  This usually refers to sine wave AC-current and will be above or below the rated value for deviating current wave forms. The nominal current of the fuse should be somewhat higher than the phase or branch current to be expected.

- $\int i^2t$ turn-off value
  This is the sum of melting and arc integral and has, therefore, to be lower than the $\int i^2dt$-value of the thyristor.

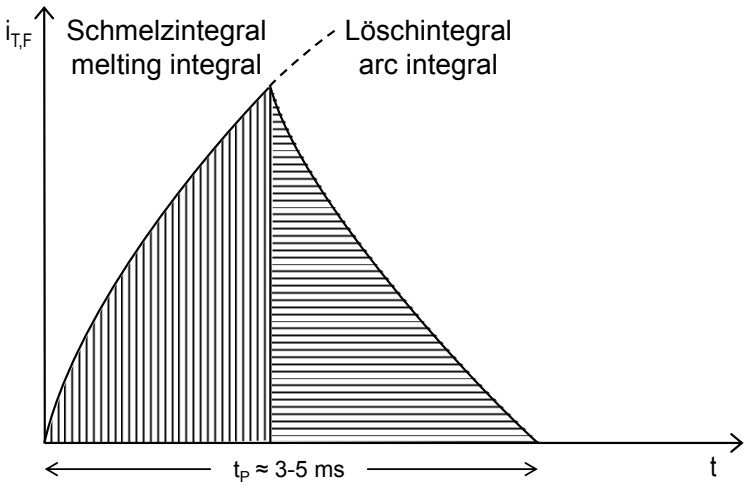
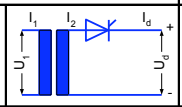
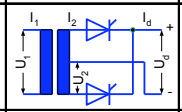
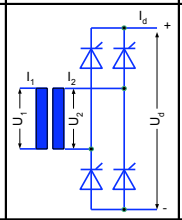
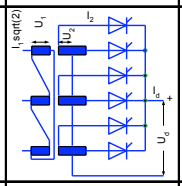
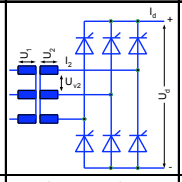
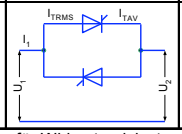


Figure 46 Turn-off characteristic of superfast fuses

Schaltung circuit		Zweigstrom arm current RMS	Strangstrom phase current RMS
M1		$\frac{\pi}{2} I_{d(AV)} = 1{,}57\ I_{d(AV)}$	
M2		$\frac{\pi}{4} I_{d(AV)} = 0{,}79\ I_{d(AV)}$	
B2		$\frac{\pi}{4} I_{d(AV)} = 0{,}79\ I_{d(AV)}$	$\frac{\pi}{2\sqrt{2}} I_{d(AV)} = 1{,}11\ I_{d(AV)}$
M6		$\frac{1}{\sqrt{3}} I_{d(AV)} = 0{,}58\ I_{d(AV)}$	
B6		$\frac{1}{\sqrt{3}} I_{d(AV)} = 0{,}58\ I_{d(AV)}$	$\sqrt{\frac{2}{3}} I_{d(AV)} = 0{,}82\ I_{d(AV)}$
W1C, W3C		$\frac{1}{\sqrt{2}} I_{d(AV)} = 0{,}71\ I_{Phase\,(RMS)}$	

idealisierte Betrachtung für Widerstandslast und Vollaussteuerung
ideal view for resistive load and full conduction

Table 5 Calculation of branch (arm) and phase currents

During the increase of the short-circuit current the fuse-link melts first. The arc resulting hereby is then quenched by the covering filler – usually quartz sand. These fuses open within 3 to 5ms (see Figure 46)

The RMS-value of branch or phase current may be derived the output current of the various converter circuits using the formulas in Table 5.
These factors apply for resistive load and zero-delay output

7.2.2 Further protection concepts: short-term protection of high power semiconductors

7.2.2.1 High speed DC-circuit breakers

electro-dynamic triggering within a few milliseconds in a short circuit situation. They are rarely used due to the high costs.

7.2.2.2 Crowbar (electronic short circuit)

are mostly used in voltage source inverters with turn-off components (IGBT, GTO, IGCT). Once the DC-bus voltage exceeds a defined protection level, the crowbar is triggered and discharges the DC-bus capacitors. When the pulse current reverses polarity, it is fed via a special diode or via the free wheeling diodes in the inverter circuit.

7.2.2.3 Line side circuit breaker

The semiconductors have to carry the short-circuit current until the circuit breaker disconnects the mains. In large installations this happens after three to five half-waves.

7.2.2.4 Blocking of trigger pulses

When exceeding a defined level the trigger pulses for the thyristors are suppressed. The thyristors are then stressed with a current half-wave followed by negative and positive off-state voltage. This requires sufficient blocking capability of the semiconductors.

7.2.3 Long-term protection

This can be achieved by suitable thermal and magnetic overcurrent protection schemes or fuses. The turn-off characteristics of these protection units should be lower than the overcurrent in short-term operation. The blocking capability of the thyristors or diodes will therefore remain. The long-term protection for thyristors may therefore also be achieved by blocking of the trigger pulses. If the maximum blocking capability is not required, the interrupt characteristics can be set on the maximum overload on-state current characteristics according to section 3.1.14.

7.2.4 Fully rated protection

This consists of long and short-term protection and in practice is only achieved by a combination of several protection meauseres.

7.3 Dynamic current limiting with inductors in the load circuit

If the inductance in the load circuit is low, too high rates of rise for the current may occur when a thyristor
turns-on. To avoid destruction insertion of additional inductors L_Z is necessary which causes a reduction in the rate of rise of the turn-on current (see Figure 47). This measure also reduces the turn-on losses.
In case of linear inductances the current density in the propagating triggered silicon area is reduced during the current rise.
In saturation chokes the high rate of rise for the current will only occur after the step time t_{St} (see Figure 47) when already a larger proportion of the silicon pellet is conductive. The step current i_{TSt} (see Figure 47) should, at the beginning of the step time, equate approximately the repetitive turn-on current $I_{T(RC)M}$ (see 3.4.1.2.3).
In case the step current is lower, it can be increased by a resistor R_p in parallel to the choke. If at the time instant 0 a voltage V_0 is applied, the current i_{RSt} resulting is as follows:

$$i_{RSt} = \frac{V_o}{R_p}$$

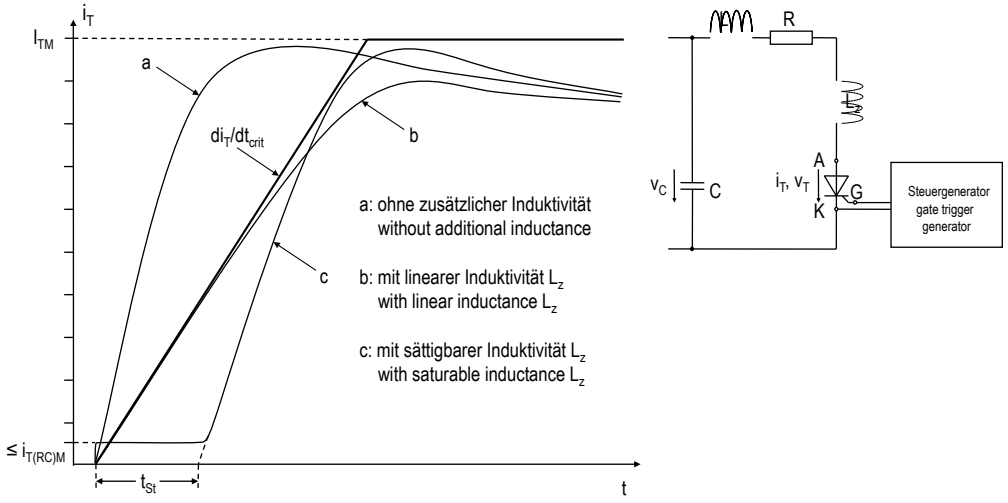


Figure 47 Schematic progression of the turn-on current of thyristors with various series inductances

a: maximum permissible region
b: non-permissible operation without limiting of the rate of rise of current
c: permissible operation with linear series inductance in the load circuit
d: permissible operation with series saturation choke in the load circuit

7.4 Reduction of interference pulses in the gate circuit

Converters produce steep current and voltage changes in the load circuit. This bears the risk of interference pulses appearing at the gate terminal of thyristors as a consequence of inductive or capacitive coupling onto the gate leads and trigger electronics. The thyristors can therefore be triggered inadvertently and cause an operation fault in the installation.

The usual measures to reduce coupling and to avoid interference pulses are twisting and possibly shortening of the gate leads as well as improved shielding even of trigger transformers and possibly trigger electronics. In addition the gate circuit can be protected (see Figure 48).

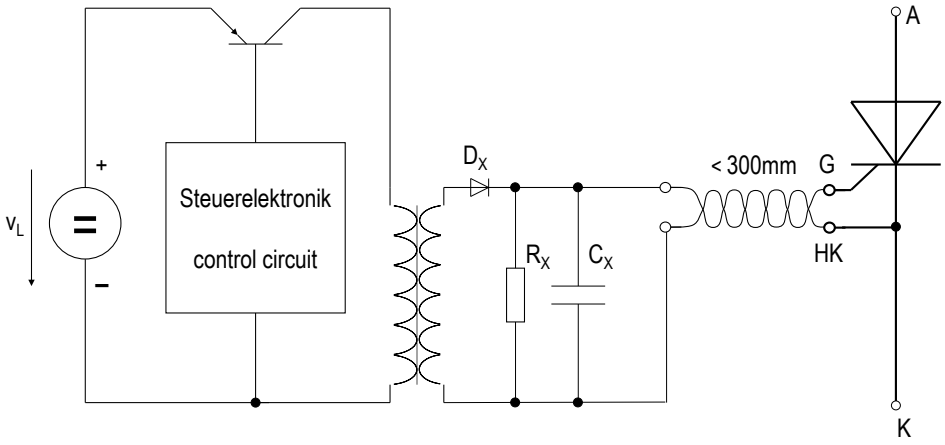


Figure 48 Example of gate protection of thyristors

For standard phase controlled thyristors the following is recommended:

- C_x = 10...47nF
- R_x according to $t_X = R_x C_x$ = 10...20µs
- D_x fast diode

The discharge resistor R_x may not be omitted as otherwise some thyristor data such as the critical rate of voltage rise $(dv/dt)_{cr}$ could detiriorate. If the snubber influences the control current adversely, this has to be taken into account when dimensioning the trigger circuit (see also 3.3.1.8).

8. Mounting

The proper and careful mounting of semiconductors is mandatory for reliable and undisturbed operation as this achieves both thermal and electrical contact.

8.1 Disc cases

8.1.1 Mounting of disc cells

Infineon offers a multitude of heatsinks and stacks. These are designed in conjunction with Infineon semiconductor components. For many of these heatsinks detailed thermal data is available on request.
As some of the disc cell heatsinks are complex to clamp, it is recommended in these cases to purchase both the components and the heatsinks as a complete stack from Infineon.

When mounting the components onto the heatsinks or busbar connecting with clamping plates both thermal and electrical contact is achieved.

For this reason the procedures listed in the following must be closely adhered to:

- The contact surfaces of disc cells and heatsinks as well as the insulation must not be damaged and have to be free of deposits.

- The contact area of disc cells and heatsinks must not exceed the values for flatness and surface roughness Rz 10µm for the heatsink.

- Prior to mounting the contact surfaces should be coated with approx. 50µm – 100µm of suitable electrically conductive heat transfer compound (e.g. Klüber Wolfracoat C), depending on condition of the heatsink contact surface. If a terminal busbar is placed between disc cell and heatsink, than this should also be treated accordingly.

Typical mounting arrangements are outlines in Figure 49 and Figure 50.

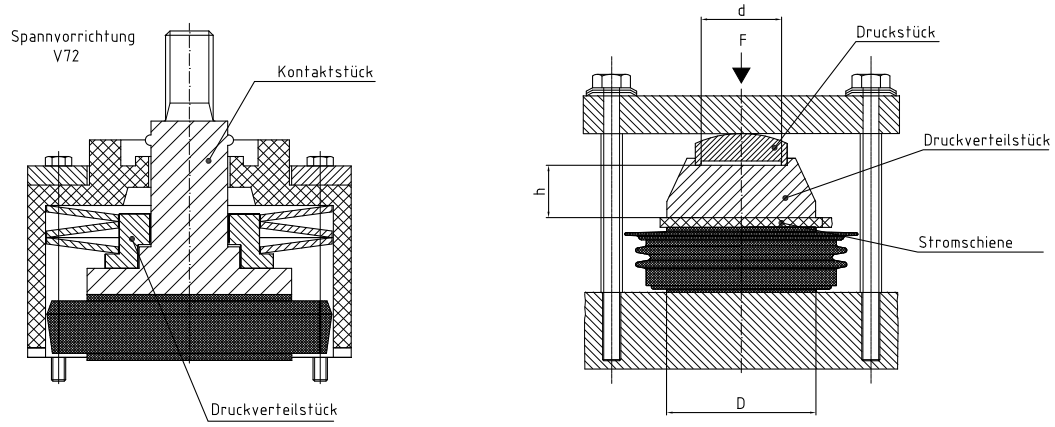


Figure 49 Typical clamping arrangement for disc cells

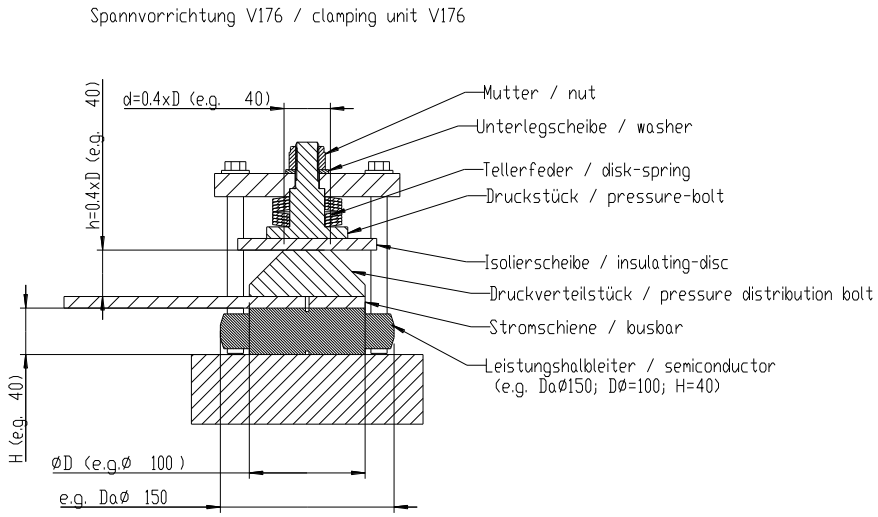


Figure 50 Typical clamping arrangement V176 for disc cells

- Sufficient stiffness of the parts to be clamped has to be assured so that the required clamping forces will not deform the heatsink contact surfaces and that a homogeneous pressure distribution is achieved (see Figure 49 and Figure 50). The deflection must not exceed the value of 0.3µm per mm of contact surface diameter D in fully clamped condition. (Example: contact surface diameter 80 x 0.3µm/mm = 24µm maximum delection)

- A maximum of 0.5% of the surface of any contact area may show pitting greater than the specified roughness. However, the nickel layer must not be damaged.

- Recommendation for dimensioning (see right side of Figure 50): The height of the pressure distribution bolt is to be dimensioned with h = 0.4D. The application of pressure force is to be performed with Ø d =0.4D.
  We recommend the use of steel (e.g. X20Cr13 conforming to EN 10099).

- If centering is not achieved otherwise, when mounting the components it has to be assured that centre holes and pins in the heatsink half shells are present.
  Also it has to be observed that the contact surface of the semiconductor is completely contacted. That means that the contact surface of the heatsink or busbar is at least as wide as the contact diameter of the semiconductor.

- When selecting the centering pins, the correct diameter and in particular the correct length has to be assured. Because the contacts of the semiconductors are made of very soft (easily deformable) copper, too long centering pins can push through to the pellet and damage the semiconductor.

- During assembly or disassembly the bolts must be tightened or loosened crosswise and alternately at a small angle to avoid damaging the disc cell.

- For single sided cooling of disc cells stacking has to be carried out with suitable clamping arrangements such as the types V50, V61 and V72. It now has to be assured that the mounting bolts are tightened in several steps and crosswise. For the types listed above the required clamping force has automatically been reached when the free ends of the clamping arrangement touch the contact surface.

- When using clamping arrangements with load current conducting centre bolts such as V50M, V61M and V72M, the maximum torques for their threads have to be observed.

Figure 51 shows the typical dependence of the thermal resistance R_{thJC} of disc cells on the clamping force.

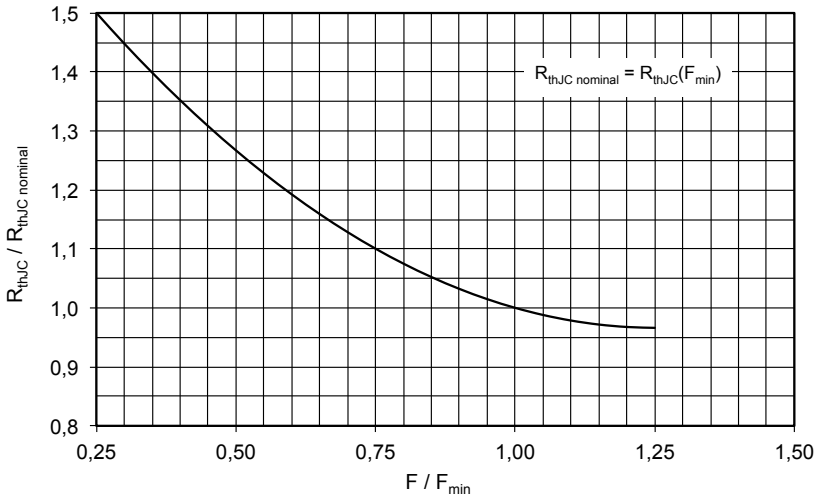


Figure 51 Typical dependence of R_{thJC} on the clamping force F

- As depicted above too low a clamping force results in an increase of the thermal resistance which leads to a reduction of the semiconductor's current loading capability. Also the on-state voltage increases and the surge current behaviour may change adversely.
  A severe reduction in clamping force may also let the thermal cycling capability deteriorate.

- Too high a clamping force may lead to ageing and damage of the disc cells internal contacts (metallisation) which once again can severely reduce the thermal load cycling capability.
  If it is intended to mount the disc cells with a clamping force significantly above the upper limit given in the data sheet, it is recommended to forward an inquiry to Infineon.

- The clamping force selected should thus be in the top third of the specified force range. This should ensure that even in the case of minimum expansion and compression processes with the materials employed, the level of force does not fall below the minimum requirement.

- For testing purposes disc cells have to be clamped with at least 10% of the minimum nominal clamping force or 1kN (which ever value is lower will suffice) in order to assure safe contact between element and contact surfaces of the pellet.

- For tests with load currents at least the minimal clamping force has to be applied, as the data sheet values are only valid for the specified clamping force window.

- Correct measurements in an unclamped condition are not possible.

- In the case of the Medium Power ceramic housings with multi use gate, we recommend the use of the flat connector for the gate connection

8.1.2 Positioning the heatsinks

Mounting disc cells in heatsinks for forced air cooling (F) and water cooling (W) can be done in any position as long as the coolant quantities are adhered to.
For natural air cooling (S) the heatsinks are to be positioned such that the fins take a vertical position and the cooling air can pass uninhibited.
The heatsinks are to be mounted with sufficient distance from the ground and other equipment.
If several heatsinks are mounted on top of each other, a sufficiently large gap has to be left in particular for natural air cooling to avoid mutual heating effects. If necessary, a higher coolant temperature has to be taken into account for the upper heatsinks.

If several devices are combined in a stack, the following points are to be noted.

- In series connection of several devices a multiple of the blocking voltage of each individual device may be achieved. This need to be taken into consideration when designing the insulation of the clamping arrangements.

- In parallel connection of several devices side by side, clamping of the devices between two continuous heatsink half-shells is not permitted. The height tolerances of the devices prevent homogenous application of the pressure force. Instead, the heatsink half-shells should be mechanically separated in order for the two clamp systems to work mechanically independent.

- If individual busbar connections are connected in a stack, it must be prevented that unacceptable forces are applied to the stack especially during assembly.

- If disc cells on heatsinks are heated up by other equipment or components such as fuses or transformers, their load must be reduced accordingly.

- The heatsinks carry potential and are thus to be mounted isolated.

8.1.3 Connection of busbars

It needs to be noted that:

- no additional pull or push forces are applied to the disc cells,

- mechanical oscillations which occur will not cause a ground or short circuit,

- additional heating up of the disc cells by load current carrying components, in particular directly connected fuses is avoided by design.

8.1.4 Connection of the control leads

The following has to be noted:

- Bending or pre-fracturing of the control terminals by improper assembly must be avoided.
- A safe contact of the pin connection is to be assured.
- The gate leads need to be positioned EMC-compatibly and gate protection circuits are positioned in close proximity to the semiconductors.
- The insulation between control and load circuit needs to be coordinated correctly. This is particularly important for the galvanic separation of the trigger circuit with trigger transformers.

8.2 Stud cases

8.2.1 Mounting stud cases

Devices with stud case have to be fastened with a torque wrench which is to be positioned radially to the case in order not to damage the ceramic insulation body. The torque values detailed in the individual datasheets is to be adhered to with a tolerance of +10%/-20%.
Damaged threads or insufficient hole depth may let the torque be reached without the contact areas touching. The heat transfer occurs only via the thread in that case which may lead to a thermal overload of the device.
The following notes must definitely be taken into account:

- The contact areas of stud cases and the heatsinks as well as the insulation body must not be damaged and must be free of deposits.
- In the contact areas of stud cases and heatsinks the deviation in flatness should be within 10µm and the surface roughness Rz of the heatsink must not exceed 10µm for stud mounting.
- Prior to assembly the contact areas should be coated with a suitable electrically conductive heat transfer compound (e.g. Klüber Wolfracoat C), with a thickness of approx. 50-100µm. If a terminal busbar is placed between stud and heatsink, this should also be coated.

8.2.2 Positioning the heatsinks

Mounting stud cases in heatsinks for forced air cooling (F) can be done in any position as long as the required coolant quantities are adhered to.
For natural air cooling (S) the heatsinks are to be positioned such that the fins take a vertical position and the cooling air can pass uninhibited.

The heatsinks are to be mounted with sufficient distance from the ground and other equipment.
If several heatsinks are mounted on top of each other, a sufficiently large gap has to be left in particular for natural air cooling to avoid mutual heating effects. If necessary, a higher coolant temperature has to be taken into account for the upper heatsinks.

If components on heatsinks are heated up by other equipment or components such as transformers, their load must be reduced accordingly.

The heatsinks carry potential and are thus to be mounted isolated.

8.2.3 Connection of busbars

It needs to be noted that:

- no additional pull or push forces are applied to the components,
- mechanical oscillations which occur will not cause a ground or short circuit,
- additional heating up of the semiconductors by load current carrying components, in particular directly connected fuses is avoided by design.
- the minimum bending radius of the flexible leads must be observed.

8.2.4 Connection of the control leads

See section 8.1.4

8.3 Flat base cases

8.3.1 Mounting flat base devices

The required clamping force is applied by the clamping plate supplied. When heatsinks made of copper or aluminium are used then the length of the four bolts is to be such that it reaches into the threaded section at least 50% further than the bolt diameter. The required clamping force has been reached when the mounting bolts have been tightened in several steps and crosswise in such a way that the clamping plate is in parallel position to the contact surface.
The following notes should definitely be taken into account:

- The contact areas of flat base devices and the heatsinks as well as the insulation body must not be damaged and must be free of deposits.
- In the contact areas of flat base devices and heatsinks the deviation in flatness should be within 10µm and the surface roughness Rz of the heatsink must not exceed 10µm for flat base mounting.

- Prior to assembly the contact areas should be coated with a suitable electrically conductive heat transfer compound (e.g. Klüber Wolfracoat C), with a thickness of approx. 50-100µm. If a terminal busbar is placed between flat base and heatsink, this should also be coated.

8.3.2 Positioning the heatsinks

See also section 8.2.2.

8.3.3 Connection of busbars

See also section 8.2.3.

8.3.4 Connection of the control leads

See section 8.1.4

8.4 PowerBLOCK-Modules

8.4.1 Mounting PowerBLOCK-modules

The contact surfaces of the modules and the heatsink have to be free of damage and deposits. The contact surface of the heatsink may not exceed the value of 10µm for flatness and roughness R_z. Prior to mounting the contact surfaces should be coated with a layer of approximately 50µm – 100µm of suitable heat transfer compound (e.g. DOW CORNING DC340), depending on condition of the heatsink contact surface.
A maximum of 0.5% of the surface of any contact area may show pitting greater than the specified roughness. However, the nickel layer of the module base plate must not be damaged.
All mounting bolts are to be tightened evenly with the specified torque.

8.4.2 Positioning the heatsinks

Mounting PowerBLOCK-modules in heatsinks for forced air cooling (F) and water cooling (W) can be done in any position as long as the coolant quantities are adhered to.

For natural air cooling (S) the heatsinks are to be positioned such that the fins take a vertical position and the cooling air can pass uninhibited.
The heatsinks are to be mounted with sufficient distance from the ground and other equipment.
If several heatsinks are mounted on top of each other, a sufficiently large gap has to be left in particular for natural air cooling to avoid mutual heating effects. If necessary, a higher coolant temperature has to be taken into account for the upper heatsinks.

If several modules are connected in series on the same heatsink, the specified isolation voltage is generally no longer sufficient. Infineon does not recommend this form of construction.

If modules on heatsinks are heated up by other equipment or components such as transformers, their load must be reduced accordingly.

The number of modules per heatsink is to be chosen so that cross talking between them is avoided or considered in the calculation.

8.4.3 Connection of busbars

It needs to be noted that:

- no additional pull or push forces are applied to the modules,
- mechanical oscillations which occur will not cause a ground or short circuit,
- additional heating up of the modules by load current carrying components, in particular directly connected fuses is avoided by design.

8.4.4 Connection of the control leads

See section 8.1.4

9. Maintenance

Thyristors and diodes as solid state components are virtually maintenance free. Their isolation paths, however, are not protected against splashing or dropping water as well as contamination. In order not to affect the insulation capability and the heat transfer, the components and in particular their isolation paths as well as the heatsinks are to be cleaned regularly.

10. Storage

After receipt of the shipment, the disc cells and PowerBLOCK-modules may be stored in their original packaging for a period of at least 2 years, subject to suitable conditions prevailing. For this, climatic conditions should conform to IEC 60721-3-1 Class 1K2.

11. Type designation

Disc cell

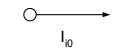
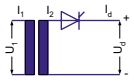
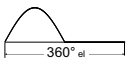
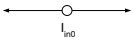
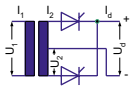
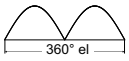
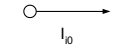
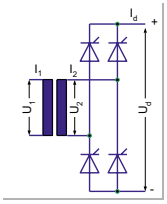
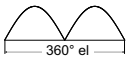
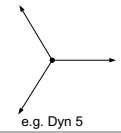
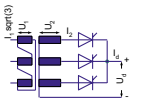
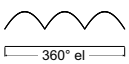
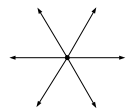
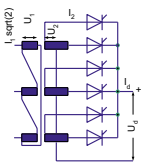
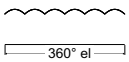
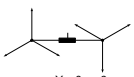
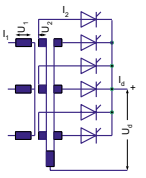
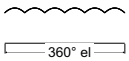
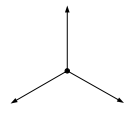
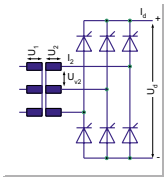
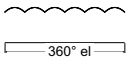
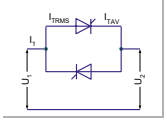
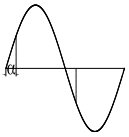
T	930	N	36	T	O	F	
T							Symmetrically blocking thyristor
D							Diode
	930						Maximum average on-state current (A)
	0						Medium power ceramic disc
	1						High power ceramic disc
	3						Light triggered thyristor in ceramic housing (LTT ⇢ Light Triggered Thyristor)
							Application:
		N					Phase control diode, phase control thyristor
		NH					Pulsed Power Diode with Soft Recovery, LTT with high turn-on-di/dt
		K					Phase control diode with cathode on case (stud and flat base housings)
		S					Fast diode
		SH					Fast diodes soft recovery - GCT, IGCT and IGBT free wheeling diodes
		U					Fast diode with cathode on case (only stud and flat base housings)
		A					Avalanche diode
		B					Avalanche diode with cathode on the case (only stud and flat base housings)
							Blocking voltage:
			36				repetitive forward off-state and reverse peak voltage in 100V 36 = 3600V
							Design:
				B			Stud base metric thread with cable
				C			Stud base metric thread with solder terminal
				E			Flat base housing with cable
				T			Disc cell
							Turn-off time:
					O		no guaranteed turn-off time (see data sheet)
							Critical rate of rise of off-state voltage:
						C	500 V/µs
						F	1000 V/µs
						G	1500 V/µs
						H	2000 V/µs
							Special type:
					Bo1…n		Construction variant
					So1…n		special electric selection

PowerBLOCK Module

TT	162	N	16	K	O	F	-K	
TT								PowerBLOCK-module with 2 thyristors
DD								PowerBLOCK-module with 2 diodes
ND, DZ, TZ								PowerBLOCK-module with 1 thyristor or 1 diode
TD, DT								PowerBLOCK-module with 1 thyristor and 1 diode
	162							Maximum average on-state current (A)
								Application:
		N						Phase control diode, phase control thyristor
		S						Fast diode
								Blocking voltage:
			16					Repetitive forward off-state and reverse peak voltage in 100V 16 = 1600V
								Design:
				A				Power block module with Advanced Medium Power Technology
				K				Power block module
								Turn-off time:
					O			no guaranteed turn-off time (see data sheet)
								Critical rate of rise of off-state voltage:
						C		500 V/µs
						F		1000 V/µs
						G		1500 V/µs
								Connection type:
							-K	construction with common cathode
							-A	construction with common anode
								Special type:
							Bo1…n	Construction variant
							So1…n	special electric selection

12. Circuit topologies

ideal with inductive filtering

Circuit topology according to DIN 41761	Vector diagram of the component side AC-voltage connection of converter transformer according to VDE 0558	Effective circuit	Voltage diagram	AC-content of the DC-voltage WU %	Frequency of the superimposed AC-voltage Hz	rms voltage per arm U_{2RMS}	rms current per arm I_{2RMS}
Single pulse connection **M1** **M1C**				121	50	2.22 * U_{di}	1.57 * I_d
Two-pulse centre-tap connection **M2** **M2C**				48	100	1.11 * U_{di}	0.707 * I_d
Two-pulse bridge connection **B2** **B2C**				48	100	1.11 * U_{di}	I_d
Three-pulse star connection **M3** **M3C**				18	150	0.855 * U_{di}	0.58 * I_d
Six-pulse star connection **M6** **M6C**				4.2	300	0.74 * U_{di}	0.408 * I_d
Double three-pulse star connection **M3.2** **M3.2C**				4.2	300	0.855 * U_{di}	0.289 * I_d
Six-pulse bridge connection **B6** **B6C**				4.2	300	0.427 * U_{di}	0.82 * I_d
Anti-parallel connection **W1C** **W3C**							

	Phase current I_{1RMS}	Transformer nominal power $P_{TR}=\frac{P1+P2}{2}$ P_2 P_1 P_{TR}	Branch current RMS I_{pRMS}	average I_{par}	Peak blocking voltage U_{im}	Current conduction angle ϴ	Nominal DC-voltage (VDE 0588 / IEC60146-1-1) U_d
M1	$1.21*\frac{U2}{U1}*Id$	$3.49*P_{di}$ $2.69*P_{di}$ $3.1*P_{di}$	$1.57*I_d$	I_d	$U_{2RMS}*\sqrt{2}$	180°el	$\frac{\sqrt{2}}{\pi}*U_{2RMS}$ $0.45*U_{2RMS}$
M2	$\frac{U2}{U1}*Id$	$1.57*P_{di}$ $1.11*P_{di}$ $1.34*P_{di}$	$0.707*I_d$	$0.5*I_d$	$2*U_{2RMS}*\sqrt{2}$	180°el	$\frac{2\sqrt{2}}{\pi}*U_{2RMS}$ $0\ 9*U_{2RMS}$.
B2	$\frac{U2}{U1}*Id$	$1.11*P_{di}$ $1.11*P_{di}$ $1.11*P_{di}$	$0.707*I_d$	$0.5*I_d$	$U_{2eff}*\sqrt{2}$	180°el	$\frac{2\sqrt{2}}{\pi}*U_{2RMS}$ $0.9*U_{2RMS}$
M3	$0.47*\frac{U2}{U1}*Id$	$1.48*P_{di}$ $1.21*P_{di}$ $1.35*P_{di}$	$0.58*I_d$	$0.33*I_d$	$1.73*U_{2RMS}*\sqrt{2}$	120°el	$\frac{3\sqrt{3}}{\sqrt{2}*\pi}*U_{2RMS}$ $1.17*U_{2RMS}$
M6	$0.577*\frac{U2}{U1}*Id$	$1.81*P_{di}$ $1.28*P_{di}$ $1.55*P_{di}$	$0.408*I_d$	$0.17*I_d$	$2*U_{2RMS}*\sqrt{2}$	60°el	$\frac{3\sqrt{2}}{\pi}*U_{2RMS}$ $1.35*U_{2RMS}$
M3.2	$0.408*\frac{U2}{U1}*Id$	$1.48*P_{di}$ $1.05*P_{di}$ $1.26*P_{di}$	$0.289*I_d$	$0.17*I_d$	$2*U_{2RMS}*\sqrt{2}$	120°el	$\frac{3\sqrt{3}}{\sqrt{2}*\pi}*U_{2RMS}$ $1.17*U_{2RMS}$
B6	$0.82*\frac{U2}{U1}*Id$	$1.05*P_{di}$ $1.05*P_{di}$ $1.05*P_{di}$	$0.58*I_d$	$0.33*I_d$	$1.73*U_{2RMS}*\sqrt{2}$	120°el	$\frac{3\sqrt{2}}{\pi}*U_{v2RMS}$ $1.35*Uv_{2RMS}$
W1C W3C			I_{1RMS} $*0.707$	I_{1RMS} $*0.45$	$U_{1RMS}*\sqrt{2}$	180°el	

A1. Abbreviations

C	Kapazität	capacitance
C_{null}	Nullkapazität	zero capacitance
E	Verlustenergie	energy
E_{tot}	Gesamtverlust-Energie	total energy
f	Frequenz	frequency
f_o	Wiederholungsfrequenz	repetition frequency
F	Anpresskraft	clamping force
G	Gewicht	weight
i_D	Vorwärts-Sperrstrom	forward off-state current
i_G	Steuerstrom	gate current
I_A	Ausgangsstrom	RMS on-state current
I_{GD}	nicht zündender Steuerstrom	gate non-trigger current
i_{GM}	Spitzensteuerstrom	peak gate current
I_{GT}	Zündstrom	gate trigger current
I_H	Haltestrom	holding current
I_L	Einraststrom	latching current
i_R	Rückwärts-Sperrstrom	reverse current
I_{RM}	Rückstromspitze	peak reverse recovery current
I_{RMS}	Strom-Effektivwert	RMS current
$I_{RMS(case)}$	Gehäusegrenzstrom	peak case non-rupture current
i_T/i_F	Durchlassstrom Thyristor/ Diode (Augenblickswert)	on-state current thyristor/diode (instantaneous value)
I_{TAV}/I_{FAV}	Durchlassstrom Thyristor/ Diode (Mittelwert)	on-state current thyristor/diode (average value)
I_{TAVM}/I_{FAVM}	Dauergrenzstrom Thyristor/ Diode (Mittelwert)	maximum average on-state current thyristor/diode
I_{TINT}/I_{FINT}	Höchstzulässiger Durchlassstrom bei Aussetzbetrieb	maximum permissible on-state current in intermittent duty
I_{TM}/I_{FM}	Durchlassstrom Thyristor/ Diode (Spitzenwert)	on-state current thyristor/diode (peak value)
$I_{T(OV)}/I_{F(oV)}$	höchstzulässiger Überstrom bei Kurzzeitbetrieb	maximum permissible on-state current in short-time duty
$I_{T(OV)M}/I_{F(OV)M}$	Grenzstrom	maximum permissible overload on-state current
$I_{T(RC)M}$	höchstzulässiger periodischer Einschaltstrom (aus RC)	maximum permissible turn-on current (from snubber)
I_{TRM}/I_{FRM}	höchstzulässiger periodischer Spitzenstrom	maximum permissible repetitive peak on-state current
I_{TRMSM}/I_{FRMSM}	höchstzulässiger effektiver Durchlassstrom	maximum permissible RMS on-state current
I_{TSM}/I_{FSM}	Stoßstrom-Grenzwert	maximum rated on-state surge current
$\int i^2dt$	Grenzlastintegral	maximum rated value $\int i^2dt$
di_G/dt	Steilheit des Steuerstroms	rate of rise of gate current
di_T/dt	Steilheit des Durchlassstroms	rate of rise of on-state current
$(di_T/dt)_{cr}$	kritische Stromsteilheit	critical rate of rise of on-state current
L	Induktivität	inductance
M	Anzugsdrehmoment	tightening torque
P	Verlustleistung	power losses
P_D	Sperrverlustleistung (Vorwärtsrichtung)	forward off-state power losses
P_G	Steuerverlustleistung	gate power losses
P_R	Sperrverlustleistung (Rückwärtsrichtung)	reverse power losses
P_{RQ}	Ausschaltverlustleistung	turn-off power losses
P_{RSM}	Stoßsperrverlustleistung	surge non-repetitive reverse power losses
P_T/P_F	Durchlassverlustleistung Thyristor/ Diode	on-state power losses thyristor/diode
P_{TAV}/P_{FAV}	Durchlassverlustleistung Thyristor/ Diode (Mittelwert)	on-state power losses thyristor/diode (average value)
P_{TT}/P_{FT}	Einschaltverlustleistung Thyristor/ Diode	turn-on power losses thyristor/diode
P_{RQ}	Ausschaltverlustleistung	turn-off power losses
P_{tot}	Gesamtverlustleistung	total power losses
Q_r	Sperrverzögerungsladung	recovered charge
R	Widerstand	resistance
r_T	Ersatzwiderstand	slope resistance
R_{thCA}	Wärmewiderstand Gehäuse-Kühlmittel	thermal resistance, case to coolant
R_{thCH}	Wärmewiderstand Gehäuse-Kühlkörper	thermal resistance, case to heat sink
R_{thJA}	Gesamtwärmewiderstand	thermal resistance, junction to coolant
R_{thJC}	innerer Wärmewiderstand	thermal resistance, junction to case
t	Zeit	time

T	Periodendauer	period
T_A	Kühlmitteltemperatur	coolant temperature
T_C	Gehäusetemperatur	case temperature
t_G	Steuerimpulsdauer	trigger pulse duration
t_{gd}	Zündverzug	gate controlled delay time
t_{fr}	Durchlassverzögerungszeit	forward recovery time
T_H	Kühlkörpertemperatur	heatsink temperature
t_p	Strompulsdauer (Sinusform)	current pulse duration (sinusoidal)
t_q	Freiwerdezeit	circuit commutated turn-off time
t_{rr}	Sperrverzugszeit	reverse recovery time
T_{stg}	Lagertemperatur	storage temperature
T_{vj}	Sperrschichttemperatur	junction temperature
$t_{vj\ max}$	höchstzulässige Sperrschichttemperatur	maximum permissible junction temperature
T_{op}	Betriebstemperatur	operating temperature
t_W	Stromflusszeit (Trapezform)	current pulse duration (trapezoidal)
V_A	Ausgangsspannung	output voltage
$V_{(Bo)}$	Kippspannung	forward breakover voltage
$V_{(Bo)o}$	Nullkippspannung	forward breakover voltage, gate open
V_D	Vorwärts-Sperrspannung (Augenblickswert)	forward off-state voltage (instantaneous value)
V_{DM}	Vorwärts-Sperrspannung (Spitzenwert)	forward off-state voltage (peak value)
$V_{D\ (DC)}$	Vorwärts-Gleichsperrspannung	forward DC off-state voltage
V_{DRM}	höchstzulässige periodische Vorwärts-Spitzensperrspannung	maximum permissible repetitive peak forward off-state voltage
V_{DSM}	höchstzulässige Vorwärts-Stoßspitzensperrspannung	maximum permissible non-repetitive peak forward off-state voltage
V_G	Steuerspannung	gate voltage
V_{GD}	nicht zündende Steuerspannung	gate non trigger voltage
V_{GT}	Zündspannung	gate trigger voltage
V_{FRM}	Durchlassverzögerungsspannung	forward recovery voltage
V_{ISOL}	Isolations-Prüfspannung	insulation test voltage
V_L	Steuergenerator-Leerlaufspannung	no-load voltage of trigger pulse generator
V_R	Rückwärts-Sperrspannung (Augenblickswert)	reverse voltage (instantaneous value)
V_{RM}	Rückwärts-Sperrspannung (Spitzenwert)	reverse voltage (peak value)
$V_{R\ (DC)}$	Rückwärts-Gleichsperrspannung	reverse DC voltage
V_{RM}	Rückwärts-Sperrspannung (Spitzenwert)	reverse voltage (peak value)
V_{RRM}	Höchstzulässige periodische Rückwärts-Sperrspannung	maximum permissible repetitive peak reverse voltage
V_{RSM}	höchstzulässige Rückwärts-Stoßspitzensperrspannung	maximum permissible non-repetitive peak reverse voltage
V_T/V_F	Durchlassspannung Thyristor/Diode (Augenblickswert)	on-state voltage thyristor/diode (instantaneous value)
$V_{(To)}$	Schleusenspannung	threshold voltage
dv_D/dt	Steilheit der Vorwärts-Spannung	rate of rise of forward off-state voltage
$(dv/dt)_{cr}$	kritische Spannungssteilheit	critical rate of rise of off-state voltage
V_L	Luftmenge	air quantity
V_W	Wassermenge	water quantity
W	Verlust-Energie	energy
W_{tot}	Gesamtenergie	total energy
$Z_{(th)CA}$	Transienter äußerer Wärmewiderstand	transient thermal impedance, case to coolant
$Z_{(th)JA}$	Transienter Gesamtwärmewiderstand	transient thermal impedance, junction to coolant
$Z_{(th)JC}$	Transienter innerer Wärmewiderstand	transient thermal impedance, junction to case
θ	Stromflusswinkel	current conduction angle

A2. List of Figures

A3. List of tables

A4. Conditions of use

The data contained in this Technical Information is exclusively intended for technically trained staff. You or your technical departments will have to evaluate the suitability of the products for the intended application and the completeness of the product data provided with respect to such application.

No guarantee of any kind will be given for the product or its properties.

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If, and to the extent necessary, please forward equivalent notices to your customers.

Changes to this Technical Information are reserved.

Notes

600A/9.5 kV Thyristor Technology for Soft Starter and Power-Supplies

The 9.5 kV thyristor disc is developed and designed for the special requirements in medium voltage soft starter as well as for medium voltage power supply applications. For these kinds of applications it is necessary to use several thyristors in series connection. They are optimized to achieve an excellent voltage sharing under all operating conditions.

The device is designed for a high surge current capability. To ensure a narrow spread of dynamic parameters which enables best cost designs with less devices in series high technology production processes are used for this type.

Of course the thyristor is suitable for general purpose line voltage rectifier applications, e.g. for power supplies or standard electrical drives.

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Where you need it. When you need it.

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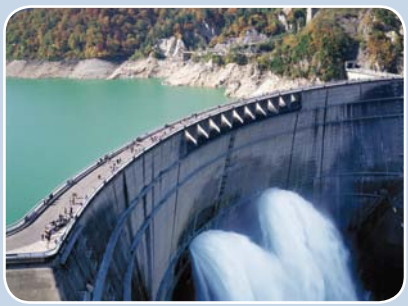

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