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Predicting Distortion in PIN-Diode Switches

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Never stop thinking

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All	Document layout change

1 Predicting Distortion in PIN-Diode Switches

This application note describes the orgin of distortion in PIN-diode switches. Distrotion is related to physical parameters of the diode and operating conditions and thus can be minimized by an appropriate diode selection. A simple relation to calculate the intercept point IP_3 from parameters given in the data sheet is provided and limits for prediction of intermodulation power from the intercept point are shown.

1.1 Intercept Point IP_3

Generally the orgin of distortion in electronic circuits is the nonlinear transfer characterictics of v_{in} to v_{out}. This response can be discribed by the power series:

$$v_{out} = A_1 v_{in} + A_2 v_{in}^2 + A_3 v_{in}^3 + \ldots \quad (1)$$

AN058_formula_1.vsd

Figure 1 Formula (1)

If two signals of equal amplitude v_0 and similar frequencies (f_1 and $f_1 \approx f_2$) are applied, parasitic frequency components occur in the output signal. Of these components, the third-order term in (1) is typically the troublesome one, since it gives components

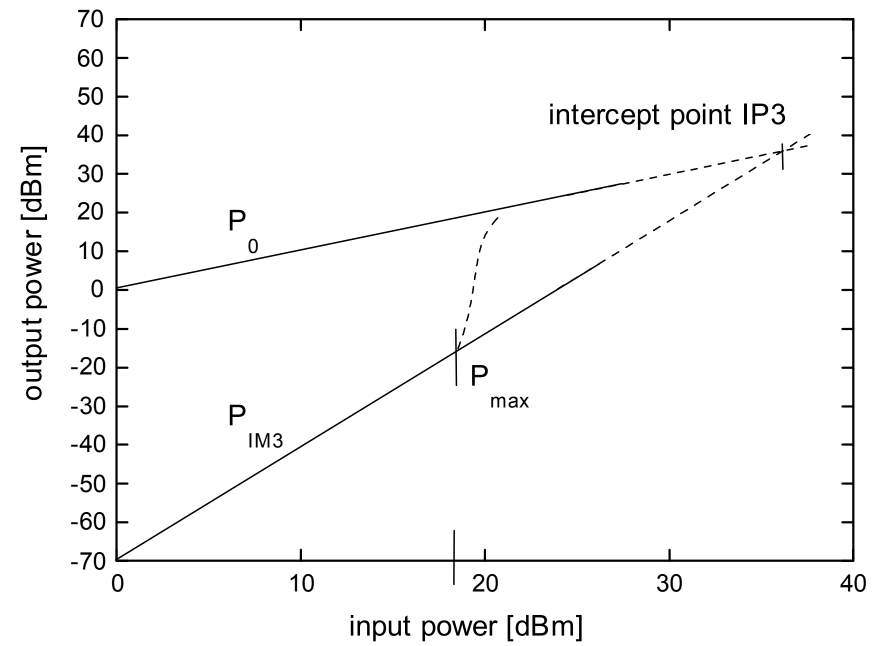
$$A_3 v_{in}^3 = \frac{3}{4} A_3 v_0^3 [\cos[2\pi(2f_1 - f_2)t] + \cos[2\pi(2f_2 - f_1)t] \ldots] \quad (2)$$

AN058_formula_2.vsd

Figure 2 Formula (2)

This third-order products occur at frequencies $2f_1 - f_2$ and $2f_2 - f_1$, which are so close to the desired signal, they typically cannot be filtered out.

Due to their cubic dependence on v_0 (2), third order intermodulation components are strongly dependent on the input power, Thus third-order inter-modulation is commonly characterized by the intercept-point IP_3, a fictitious input power level, where the power of the third-order intermodulation product intercept with the power of the linear transfer component (**Figure 3**)



Theoretical power dependence of fundamental (P_0) and third-order inter modulation product (P_{IM3}). Actually, above a certain input power P_{max}, inter-modulation of a PIN-diode shows a significant increase (dashed) and therefore cannot be calculated from the intercept point IP_3.

AN058_OutputPower_InputPower.vs

Figure 3 Intercept point

From a given intercept point (IP_3) and input power the inter-modulation distortion products can be easily determined (1). A PIN-diode is expected to exhibit the same distortion effects when the input level changes. However, as illustrated in **Figure 3**, above a certain power level the distortion in PIN-diode switches rises much more rapidly than predicted.

In the following we will relate the intermodulation distortion to physical parameters of the PIN-diode and show the limits of the basic IP_3 concept.

1.2 Third-Order Distortion in Forward-Biased PIN-Diodes

Origin of Distortion

If the PIN-diode is forward biased, as for example it is the case in the "on"-state of an antenna switch (**Figure 6**), electrons and holes are injected into the instrinsic region. Under this condition the steady state forward resistance of the instrinsic region is given by

$$r_f(f=0) = \frac{W^2}{(\mu_n + \mu_p)\,\tau\, I} \qquad (3)$$

AN058_formula_3.vsd

Figure 4 Formula (3)

Where W denotes the width of the intrinsic zone, τ the carrier lifetime and μ_n and μ_p appropriate mobilities.

If a high-frequency AC-signal of frequency *f* is superimposed to the DC signal, the carrier concentration at the boundaries of the intrinsic zone is modulated (**Figure 6**). The spatial dependence of this concentration is determined by the AC-diffusion length, given by

$$L_{AC} = \sqrt{\frac{D\tau}{1 + j(2\pi f\tau)}} \qquad (4)$$

AN058_formula_4.vsd

Figure 5 Formula (4)

Where *D* denotes the ambipolar diffusion constant. Assuming no depletion within the instrinsic zone during the half-cycle of the RF-signal.

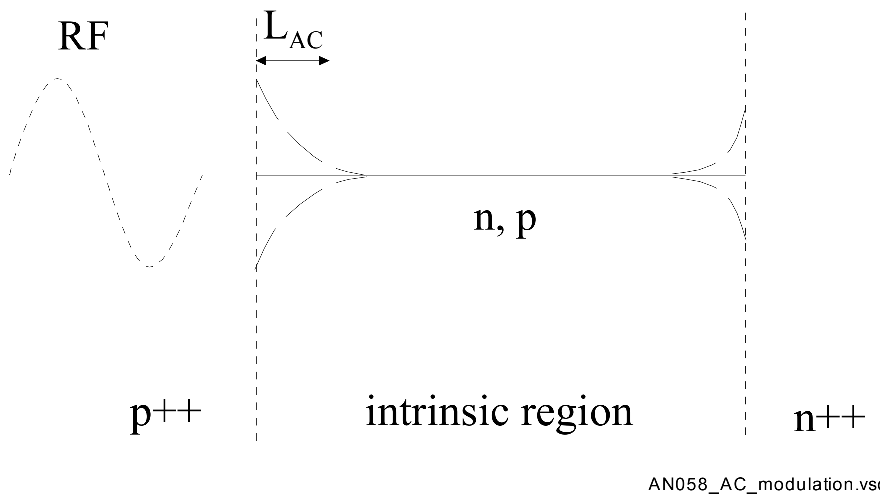


Figure 6 AC-modulation of the carrier concentration in the intrinsic region of the PIN-diode

The high frequency diffusion region shows the current-voltage dependence.

$$i(t) = \sqrt{2\pi f D}\,\frac{\tau\ I}{W}\exp\frac{v(t)}{2v_T} \qquad (5)$$

AN058_formula_5.vsd

Figure 7 Formula (5)

With *i*(t) and *v*(t) the time dependent current and voltage drop across the diffusion region, respectively; v_T = kT / q denotes the thermal voltage. This non-linear i-v-characteristics is the main source of intermodulation distortion in the “on”-state of the PIN-diode.

Considering a simple diode-switch with equivalent circuit shown in **Figure 11** and expanding (5) in a power series, yields for the third-order intermodulation product at frequency $2f_1$ - f_2, dependent on the power P_0 of the fundamental

$$P_{IM3} = \frac{3}{4}\frac{{v_T}^2}{{Z_0}^4}\left[\frac{W}{I\,\tau\sqrt{2\pi f_1 D}}\right]^6 {P_0}^3 \qquad (6)$$

AN058_formula_6.vsd

Figure 8 Formula (6)

Where $r_f << Z_0$ has been assumed. This gives for the intercept-point

$$IP3 = \sqrt{\frac{4}{3}\frac{1}{v_T}{Z_0}^2\left[\frac{2\pi\, I\, D\,\tau\, f}{W^2}\right]^{3/2}} \qquad (7)$$

AN058_formula_7.vsd

Figure 9 Formula (7)

Equations (6) and (7) show that lower third-order distortion with forward biased PIN-diode can be achieved with diodes of short intrinsic region, and higher carrier lifetime. Another important relationship is that the IP_3 can be improved by increasing the diode operating current.

From a given IP_3 level, the intermodulation power at any level of input power can be determined by

$$\log P_{IM3} = 3\log P_0 - 2\log IP3 \qquad (8)$$

AN058_formula_8.vsd

Figure 10 Formula

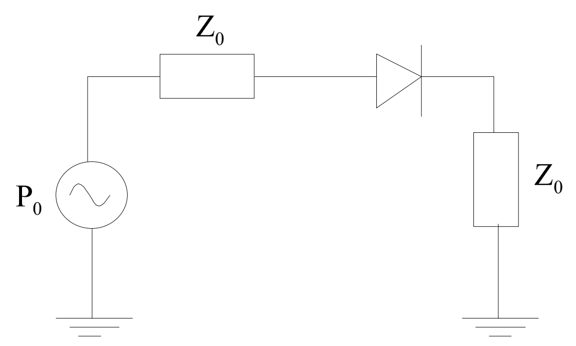


Figure 11 High-frequency equivalent circuit of a PIN-diode switch

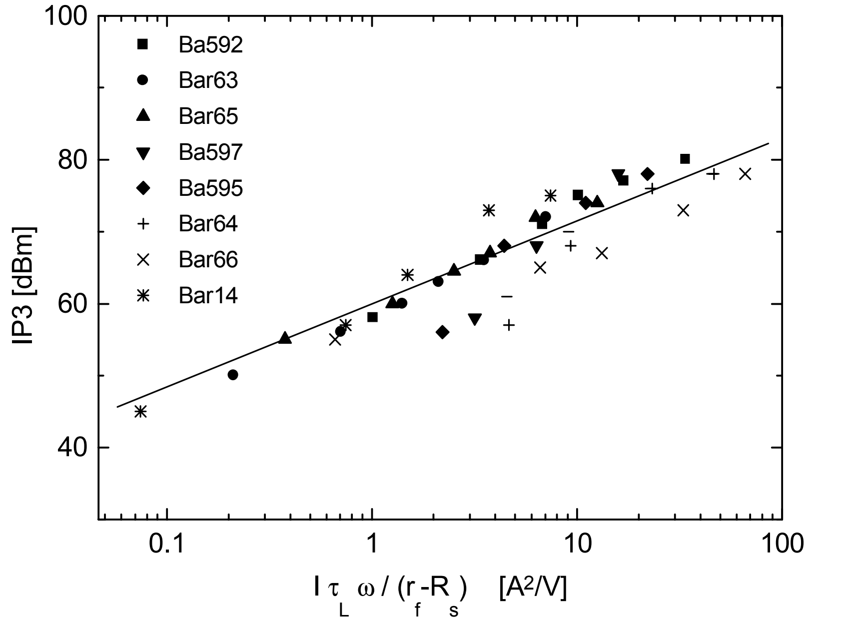


Figure 12 Comparison of IP_3 measurement results with calculation results based on PIN-diode datasheet parameters

However, when P_0 exceeds a certain limit, as specified by

$$P_{\max} = \frac{\pi}{2} Z_0 I^2 \left(\frac{D}{W}\right)^2 f \, \tau^2 \tag{9}$$

AN058_formula_9.vsc

Figure 13 Formula (9)

Third-order distortion increases much more rapidly than described by relation (6) (see **Figure 3**). Above this power, the AC-modulation of the carrier concentration leads to a depletion of the intrinsic zone in the negative half-cycle and thus to an even stronger non-linear i-v-characteristic. In this region, assumptions which led to the derivation of (6) are not valid anymore and thus the IP_3 concept for calculation of the third-order distortion fails. As a consequence, to suppress third-order distortion, the diode should always be operated in regions where $P_0 < P_{\max}$ is fulfilled. For given P_0 and a certain diode this requires at least a minimum operating current.

Calculation of IP_3 and $P_{\max}$ from PIN-Diode Data Sheet Parameters

For most PIN-diodes the current in the region of interest is rather determined by surface recombination and recombination in the $p^{++}$and n^{++} regions than by bulk recombination in the intrinsic region. Thus the electron and hole charge in the intrinsic region is proportional to τ *sqrt (I)*. With (3) for IP_3 and $P_{\max}$ follows:

$$IP3 = \sqrt{2v_T}\, Z_0{}^2 \left[\frac{2\pi\, f\, \tau_L\, I}{r_f - R_s} \right]^{3/2} \qquad (10)$$

AN058_formula_10.vsd

Figure 14 Formula 10

$$P_{max} = \frac{1}{2} Z_0 v_T \left(\frac{2\pi\, f\, \tau_L\, I}{r_f - R_s} \right)^2 \qquad (11)$$

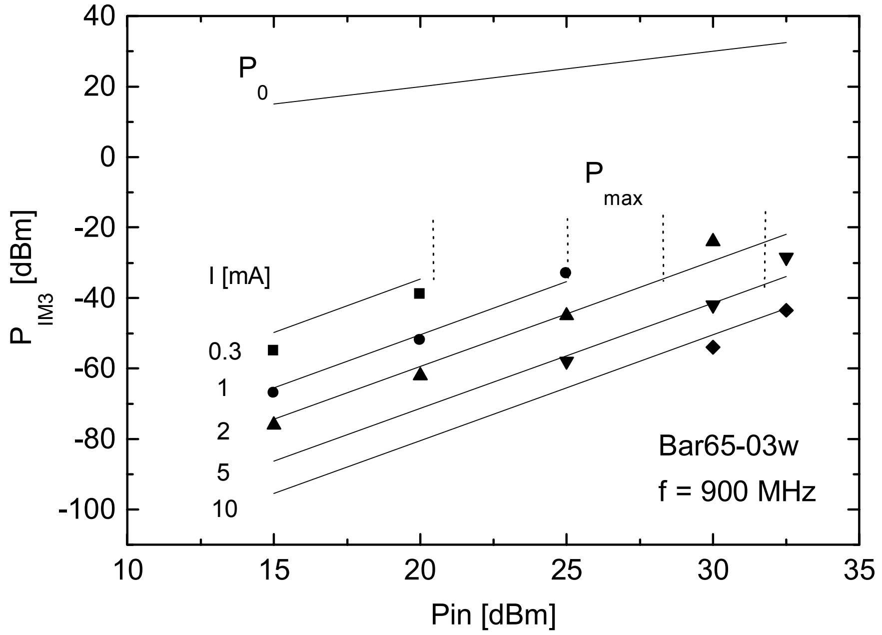
AN058_formula_11.vsd

Figure 15 Formula 11

Here τ_L and r_f denote the effective lifetime and resistance available from the diode data sheet. R_s denotes the series resistance of highly doped p^{++} and n^{++} regions as well as the package resistance. With the typical value of R_s = 0.2 Ω, P_{max} can be estimated from PIN-diode data sheet parameters.

In **Figure 12** measurement results for a variety of PIN-diodes at different operation currents are compared to results of our simple model. The comparison shows that third-order inter-modulation for $P_0 < P_{max}$ can be well predicted with (10) from the diode data sheet parameters.

Figure 16 shows third-order inter-modulation for the PIN-diode BAR65-03W at different bias currents. Our model shows good agreement with measurement results. For an input power higher than P_{max} intermodulation increases more rapidly than predicted with our model.



Third-order inter-modulation for PIN-diode BAR65-03W at differend current levels and RF-input power for a 50 Ω antenna switch compared to calucations of equation (10), (8) (solid). Also shown are the validity limits P_{max} (11) for the IP_3 concept

AN058_IP3_third_order_inter_modulation.vs

Figure 16 Third-order inter-modulation

1.3 Distortion in Reverse-Biased PIN-Diodes

The RF-characteristics of the reverse biased PIN-diode is primarily determined by the (small signal) depletion capacitance C_d. Thie capacitance generally depends only slightly on the reverse-voltage. These variations give rise to another generation of intermodulation products. For a diode switch within this simple model the intercept point for the third-order intermodulation poduct is given by (2)

$$IP3 = \frac{1}{32}\left[\frac{\mathrm{d}^2 C_d}{\mathrm{d}V_R^{\,2}} Z_0^{\,2} (2\pi f)\right]^{-1} \qquad (12)$$

AN058_formula_12.vsd

Figure 17 Formula 12

The voltage-dependence of the capacitance is due to the variation of the depletion region with increasing reverse-bias and therefore mainly determind by the diffusion tails of the highly doped p^{++} and n^{++} contact regions of the PIN-diode. Since this dependence decreases with the width of the intrinsic region, inter-modulation is weaker for thicker PIN-diodes.

If the diode gets forward biased during the half-wave of the RF-signal, carrier injection into the intrinsic region significantly reduces the width of the depletion region. Thus for power-levels higher than [**Formula 13**] diodes with small intrinsic region might show a major increase of inter-modulation.

$$P_{\max,rev.} = \frac{V_R^{\,2}}{2Z_0} \qquad (13)$$

AN058_formula_13.vsd

Figure 18 Formula 13

Also worth mentioning is that intermodulation of the reverse biased PIN-diode increases for higher frequencies. This is in contrast to intermodulation in the on-state of the diode being reduced with increasing frequency.

Table 1 Third-order inter-modulation for a variety of PIN-diodes[1)]

PIN-Diode	IP_3 [dBm] Forward Bias		IP_3 [dBm] Reverse Bias	τ_L [µs]	r_f (10 mA) [Ω]
	I_F = 2 mA	I_F = 10 mA	V_R = 15 V		
BA592	> 67	> 67	44	0.12	0.4
BAR63-03W	61	> 67	50	0.1	1
BAR65-03W	64	> 67	47	0.08	0.56
BA595	67	> 67	> 73	1.6	4.5
BA885	> 67	> 67	> 73	1.6	0.4
BAR14	63	> 67	> 73	1	8
BAR66	67	> 67	58	0.7	1
BAR64	> 67	> 67	73	1.4	2

1) f = 900 MHz / Input Power 20 dBm

1.4 Appropriate Diode Selection

In **Table 1** intercept-points for forward and reverse bias are summarised for a variety of PIN-diodes. The table shows that intermodulation robustness in forward-bias might be contrary to the robustness in reverse bias. This is due to the fact, that IP_3 in forward-bias decreases with increasing epi-thickness, while IP_3 in reverse-bias increases. So dependent on the application and system specifications an appropriate choice of the diode is required.

2 Summary

Reducing inter-modulation distortion in PIN-diode applications requires a careful choice of the appropriate diode and its operating point. In this note a model has been introduced to estimate third-order distortion in the “on”-state of the diode from diode parameters given in the data sheet. For the case of a forward biased as well as a reverse biased diode, maximum power levels are given, which, for reason of moderate inter-modulation, should not be exceeded.

3 References

- R.Caverly and G. Hiller, “Predict Intercept Points in PIN-Diode Switches”, Microwaves & RF, Dec. 1985
- R. H. Caverly and G. Hiller, “Distortion in Microwave and RF Switches by Reverse Biased PIN-Diodes”, Proceedings in the *IEEE MTTS International Microwave Symposium*, Long Beach, Ca, 1989

Nomenclature

V_{out}	Output voltage
V_{in}	Input voltage
A_1, A_2, A_3	Taylor coefficients of device transfer characteristics
f_1, f_2	Input frequencies
r_F	High-frequency resistance of the PIN-diode intrinsic region
μ_n, μ_p	Electron and hole mobility
W	Intrinsic region thickness
τ	Carrier lifetime in the intrinsic region
D	Ambipolar diffusion-coefficient
f	Frequency
L_{AC}	AC difussion-length
V_T	Thermal-voltage
P_{IM3}	Third-order inter-modulation power
IP_3	Intercept point power
P_0	Power of fundamental frequency
Z_0	Characterictic (wave) impedance
$P_{max,IP3}$	Power limit for the validity of the IP3-concept
R_S	PIN-diode series resistance
τ_L	PIN-diode recovery time available from the data sheet
C_d	PIN-diode small signal depletion capacitance
V_R	Reverse voltage
$P_{max,rev.}$	Maximum power in reverse mode for prevention of intermodulation increase