

Repetitive Avalanche of Automotive MOSFETs

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Standard

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Abstract

Table of Content

Table	able of Content	
1	Abstract	5
2	Introduction and motivation	6
3	The MOSFET in avalanche – single pulse	7
4	Failure modes – single pulse	9
5	The MOSFET in repetitive avalanche	10
6	Failure modes – repetitive avalanche	11
7	Applications	13
8	Summary and Conclusion	14
9	References	15



1 Abstract

This paper will focus on one of the most difficult operation modes of automotive MOSFETs, the operation in repetitive avalanche. Whereas single pulse avalanche conditions are typically very well defined and tested, repetitive avalanche operation is always an area of discussion as the number of influencing parameters is considerably higher.

In automotive applications a vast range of requirements for repetitive avalanche exist: Applications from very limited numbers of avalanche cycles at high energy, to billions of events at very low avalanche energies.

In this paper we discuss the requirements of repetitive Avalanche from application point of view, provide information on avalanche modes and test results of single and repetitive avalanche.



2 Introduction and motivation

Today's state of the art power MOSFET have typical resistance rating in the mOhm range and are capable of handling 100A and more. They are used in a wide variety of electric control units (ECUs) in the car. They are used to control electric motors, solenoid valves or basically to turn on or off an electric loads.

Along with nearly all of these loads goes some kind of inductance, either a load inductance in case of solenoids or electric motors or some kind of stray inductance caused by the wire harness or the board layout. The inductance has to be accounted for in the switching performance as it will generate high voltage peaks at each switching transition. It is possible to suppress the voltage spikes and hence the avalanche mode for the MOSFET by placing freewheeling diodes parallel to the load or by using input capacitors or snubber networks.

Some applications, however, like gasoline or diesel injection are designed to operate in avalanche mode with the target of fast demagnetization and fast turn off of the valves.

The key question for this kind of repetitive operation is how the quality and endurance of the MOSFET can be assured over the lifetime of the vehicle. Failure models of repetitive avalanche must be understood and acceleration models must be developed. An extensive repetitive avalanche tests must be performed with a sufficient statistic for model verification considering a vast range of customer requirements.



The MOSFET in avalanche – single pulse

3 The MOSFET in avalanche – single pulse

The avalanche mode occurs when the Drain to Source voltage reaches values where the MOSFET will turn on without supplying a Gate to Source voltage. In that mode, the device operates in breakdown similar to a Zener diode, holding the voltage across the device constant. The avalanche voltage is a factor of 1.3 ... 1.5 above the rated breakdown voltage. For example a 40V device will have an avalanche breakdown voltage of approximately 50V. An avalanche test setup is shown in Figure 1. As the MOSFET is turned on, the current is rising depending on the inductance and energy is stored in the circuit. When the current reaches a preset value, the MOSFET is turned off and the inductance will continue to force a current in the circuit. This will immediately increase the Drain voltage driving the device under test (DUT) into avalanche. The device will stay in avalanche until the entire energy stored in the inductance is dissipated in the device. The current is linearly decreasing during this time.

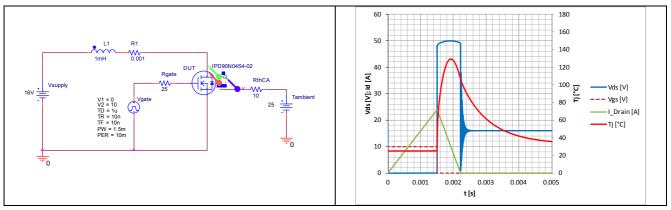


Figure 1 Basic avalanche test circuit

During the avalanche pulse, the junction temperature rises rapidly. For the shown example it is starting from 25°C and reaches 130°C after about 30µs. An interesting side effect is the shape of the Drain to Source voltage wave form. At the beginning of the avalanche event, the voltage goes up (from 48V to 50V) and decreases afterwards. This is due to the positive temperature coefficient of the breakdown voltage. As the temperature of the device increases, the breakdown voltage increases as well! The highest point in the breakdown voltages matches with the peak in the junction temperature.

In MOSFET data sheets the single pulse avalanche conditions are specified with half the nominal current as usual application condition. Tested avalanche parameters are full nominal current 180A and energy of 625 mJ. (Half the energy because twice the given current at datasheet condition.) Attached is an extract out of an Infineon MOSFET data sheet (IPB180N04S4-00¹)

Avalanche energy, single pulse ²⁾	E _{AS}	/ _D =90 A	1250	mJ
Avalanche current, single pulse	I _{AS}	-	180	A
	I			



The MOSFET in avalanche – single pulse

The maximum inductance for these conditions can be calculated as follows:

$$L = \frac{2 \cdot E_{AS}}{I_{AS^2}} \cdot \frac{V_{AS} - V_{dd}}{V_{AS}}$$

$$L = \frac{2 \cdot 625mJ}{(180A)^2} \cdot \frac{50V - 0V}{50V}$$

$$L = 39\mu H$$
(1)

 V_{AS} is the avalanche voltage of the device (1.3 ... 1.5 x V_{Brdss}) and V_{dd} is the supply voltage during the avalanche event. In our special case the supply voltage will be turned off during the avalanche event. In an automotive application it would be typically the battery voltage of the car.

The duration of the avalanche pulse can be calculated as well by using simple equations:

$$t_{av} = \frac{L \cdot I_{AS}}{V_{AS} - V_{dd}}$$

$$t_{av} = \frac{39\mu H \cdot 180A}{50V - 0V}$$

$$t_{av} = 0.14ms$$
(2)

Besides these figures typically two additional diagrams are part of a MOSFET datasheet, one showing the maximum avalanche current over the pulse length for different temperatures and the other showing the avalanche energy over the starting temperature for different current conditions (see Fig. 2).

Two points are important to mention:

Even at a temperature of $T_J = 175^{\circ}$ C, e.g. the maximum specification in the data sheet, the MOSFET is capable of handling some avalanche energy. This means, however, that the device will operate above 175°C for a short period of time as single pulse!

For smaller currents the maximum avalanche capability becomes larger. The reason behind this is the criterion for the energy limitation of the diagram, which is given by the maximum delta T_J . At lower currents, the dissipated power is smaller and the device needs a longer time to reach that delta T_J , thus resulting in a higher avalanche energy. The dependency in that case is linear. Half the current would result in double the energy.

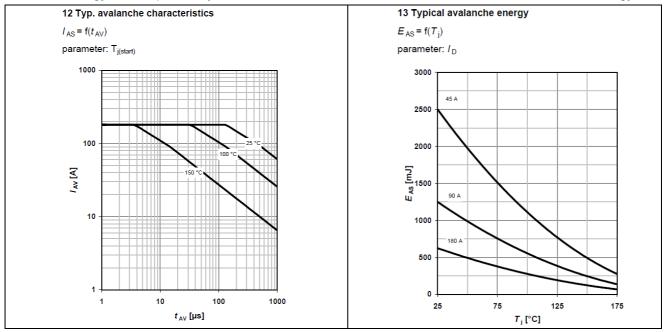


Figure 3 Avalanche diagrams



4 Failure modes – single pulse

During the electrical characterization of the MOSFET, the single pulse avalanche capability is assessed. The test matrix includes a variation of the avalanche current and the starting temperature. The tests are destructive! For single pulse avalanche one generally differentiates two limitations:

- energy limitation and
- current limitation

In the case of current limitation the load current density is so high that it will cause a direct latching of the parasitic bipolar transistor. In modern power devices the required current density, however, is so high, that it is rarely reached in most applications. In case of energy limitation the device is heated up as in Fig. 1. With increasing temperature the leakage current of the parasitic bipolar transistor also increases. If the total leakage current reaches the load current the positive temperature coefficient of the leakage current will cause a filamentation. At this hot spot the device is destroyed. For typical power devices the temperature where filamentation will occur is in the range of 350°C ... 450°C. As the temperature increase is mainly depending on the size of the device, the single pulse avalanche capability is a function of the silicon area of the device. The technology concept, e.g. planar or trench MOSFET, is of minor importance if the same die sizes are considered.



The MOSFET in repetitive avalanche

5 The MOSFET in repetitive avalanche

In case of repetitive avalanche the challenge is not the electrical limit of the device but the occurrence of thousands or even billions of avalanche events over lifetime and the requirement of a zero defect quality for automotive applications in particular. This cannot be covered by a single pulse destructive avalanche test. One needs an extensive test matrix applying repetitive avalanche pulses to the device under test until end of live basically. Conditions of repetitive avalanche can differ significantly in the applications varying from long pulses with rather moderate currents to very short pulses at high currents and any condition in between. Tests to assess the capability of the MOSFET in repetitive avalanche should therefore include different load and current conditions resulting in different maximum junction temperatures during cycling. Additionally the starting temperature and the pulse length must be varied.

The Repetitive Avalanche Test Integrated System (RATIS) by Infineon is designed to support parallel measurement of many devices under all odds of avalanche conditions. The starting temperature can be changed from -40°C till 150°C, the inductance can be varied from 2μ H till 100mH and the current can be driven up to 250A. To avoid damaging of some system components in case of any not foreseen event, a complex protection concept is implemented.



Figure 4 Test bench for repetitive avalanche

In Figure 4 the complete setup is visible on the left hand side. On the right hand side some devices under test within the climate chamber are shown. Parallel operation of many devices is possible, thereby all findings of the tests are showing statistically significant results!



Failure modes – repetitive avalanche

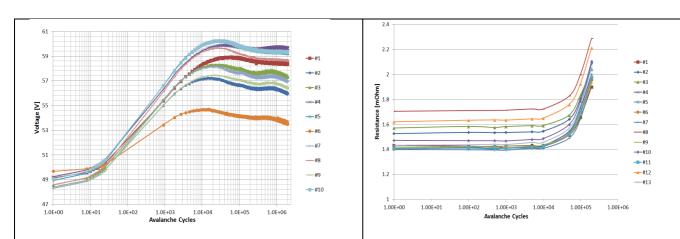
6 Failure modes – repetitive avalanche

Whereas the maximum single pulse avalanche is given by a thermal limit of the device, such a simple correlation cannot be written down for the repetitive case. Nevertheless the failure mechanisms in repetitive avalanche can be categorized in two failure modes:

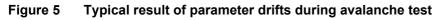
- degradation of materials in particular the top side metallization due to the high number of temperature cycles leading eventually to a drift in device parameters such as the on-state resistance,
- drift of device parameters such as the leakage currents, the drain to source voltage or output capacitance due to high electrical stress during the avalanche event possibly caused by hot carrier injection

Both failure modes can be investigated simultaneously if the test setup allows readouts of the parameters after predefined number of cycles. Electrical parameters which are monitored during the test should be those that are influenced by material interfaces. The most prominent certainly is the oxide interface of the gate oxide, but also the metal/silicon interface in the contact hole might be critical. The following parameters should be recorded in any case:

- On state resistance R_{DSon}
- Breakdown voltage V_{BRDSS}
- Leakage currents Drain to Source and Gate to Source, I_{DSS} and I_{GSS}



- Dynamic parameter like Coss



In Figure 5 two examples of parameter drift under repetitive avalanche are shown. A 20% drift in breakdown voltage can be seen in the left. This large drift did not however lead to destruction. In the right graph the drift on the on-state resistance is shown. Note that the drift in the on-resistance starts after a considerable larger number of pulses. The question which drift is more critical will depend on the application.

From our investigations we have seen that the MOSFET technology has a significant impact on the robustness in repetitive avalanche. One common failure mode in repetitive avalanche is front side metallization fatigue due to temperature cycling.

When selecting a MOSFET for a repetitive avalanche application the first question should be whether the avalanche is a failure mode like Load Dump, short circuit etc., or an application mode like switching an inductive load. In the first case the number of avalanche pulses is typically limited to about a thousand whereas in the second the number of pulses is difficult to specify.



Failure modes - repetitive avalanche

In case repetitive avalanche is an application condition Infineon's OptiMOSTM-(non-T) technology is recommended. Two boundary limits should be considered: the maximum delta T_J must not exceed 60K and the maximum junction temperature must stay below 175°C. Higher delta T_J or T_{J_max} will reduce the life time of the device significantly. Within these temperature limits the starting temperature and time in avalanche t_{av} are only of minor importance.

In case repetitive avalanche is a failure mode more modern MOSFET technologies like Infineon's OptiMOS™-T2 technology can be used.





7 Applications

Achieved results can be used to assess different application cases in automotive surrounding. Two prominent automotive applications using MOSFETs in avalanche mode are "anti-lock brake systems" (ABS) and electric power steering (EPS).

- ABS valves: repetitive avalanche conditions

In ABS the solenoid valves can be controlled by a discrete MOSFET and for fast turn off, the devices are forced into avalanche. This will happen during some braking events leading to high number of cycles (>>1.000.000) over the lifetime of the car.

According to the findings of the repetitive avalanche test setup, an OptiMOS[™]-(non-T) part should be selected to assure safe operation. One typical MOSFET could be the IPG20N06S2L-35².

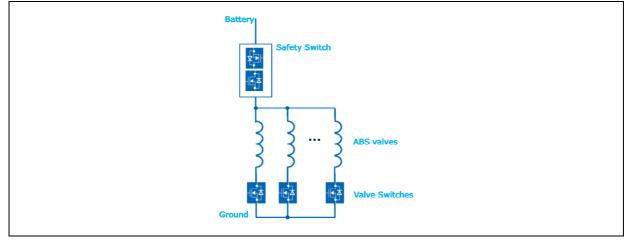


Figure 6 Power MOSFETs of an ABS system – valves only

- Star point relay replacement by MOSFETs

As a second example the EPS system might be considered. Whereas in the past just six MOSFETs were used for the B6-bridge, today up to 11 MOSFETs are considered. There is one safety switch combining the function of reverse polarity protection and an additional device for turn off in case of a mal-function of the bridge. The former topology used a star point relay that today can be replaced by MOSFETs. This device will disconnect the motor windings from the battery in case of bridge malfunction. If this happens, the motor will drive these three devices into avalanche. Since this happens only in case of a failure in the system, the number of cycles is limited (<<1.000 cycles).

According to the findings of the repetitive test, an OptiMOS[™]-T2 40V device can be used for such an application. Typical part could be the IPB180N04S4-00¹.

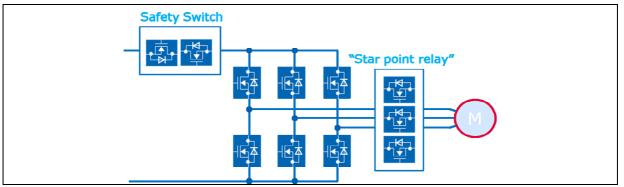


Figure 7 Power MOSFETs of an EPS system



Summary and Conclusion

8 Summary and Conclusion

Avalanche is an operation mode which will be used for power MOSFETs in automotive applications. There is a huge range of conditions which should be considered for the selection of the right MOSFET. Whereas single pulse avalanche is well understood and can be easily characterized, tested and specified, repetitive avalanche operation is still a difficult topic. No standard tests for an investigation of the capability in repetitive avalanche are available today.

With the test setup as presented, several devices can be investigated in parallel. The statistics of the results achieved are therefore significant.

Findings of the tests can be summarized by following statements:

- The MOSFET technology has a significant impact on the robustness in repetitive avalanche.
- For high number of cycles, OptiMOS[™]-(non-T) technology is recommended.
- For very low number of cycles (avalanche occurs in failure mode only) more modern technologies like the OptiMOS™-T2 can be used.
- One common failure mode in repetitive avalanche is front side metallization fatigue due to temperature cycling.
- Key impact on number of cycles in avalanche is delta T and T_{J max}.
- One limit is visible at delta T_J of 60K staying below the maximum junction temperature of 175°C. Higher cycles will reduce the number significantly.
- Minor impact on number of cycles in avalanche is the starting temperature and time in avalanche t_{av}.

The results out of the repetitive avalanche can be used to assess different application cases. In the paper two prominent ones were selected with complete different requirements. In the ABS system where the MOSFETs are used with a high number of avalanche cycles, MOSFETs from Infineon's OptiMOS[™]-(non-T) family should be used. For systems where avalanche occurs in case of a malfunction, the number of cycles is limited. For such applications MOSFETs from Infineon's OptiMOS[™]-T2 technology can be selected.



References

9 References

- [1] Infineon Data Sheet IPB180N04S4-00_DS_1_0 issued 06.04.2010
- [2] Infineon Data Sheet IPG20N06S2L-35_DS_10 issued 07.09.2009

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