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GreenChip TEA1755 integrated PFC and flyback controller

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Document information

Info	Content
Keywords	GreenChip, TEA1755, PFC, flyback, high-efficiency, adaptor, notebook, PC power, low-power Standby power mode
Abstract	The TEA1755 is a member of the new generation of combined PFC and flyback controller ICs, used for efficient switched mode power supplies. Burst mode enhances the overall efficiency of the system at low-output power and improves the audible noise performance. The TEA1755 has a high level of integration allowing cost-effective design of power supplies using the minimum number of external components. The TEA1755 is fabricated in a Silicon-On-Insulator (SOI) process, enabling it to operate at a wide voltage range.

Revision history

Rev	Date	Description
v.1	20121112	first issue

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1. Introduction

The TEA1755 is a combination controller comprising an integrated PFC and flyback controller in an SO16 package. Both controllers operate in Quasi-Resonant (QR) mode and in Discontinuous Conduction Mode (DCM) with valley detection and are independently switched.

The PFC output power is on-time controlled for simplicity. It is not necessary to sense the phase of the mains voltage. The flyback output power is current mode controlled providing good input voltage ripple suppression.

The integrated communication circuitry between the controllers does not require adjustment.

Remark: The voltage and current levels contained in this application note are typical values The specification of the pin level spreading is given in the *TEA1755T* and *TEA1755LT* data sheets.

Remark: In all cases where a parameter value in this application note is different from that in the applicable data sheet, the data sheet is leading.

1.1 Scope

This application note describes the functionality of the TEA1755 and the adjustments needed within the power converter application.

Excluded from this document are the large signal parts of the PFC/flyback power stages and the coil/transformer design and data.

1.2 The TEA1755 GreenChip controller

The GreenChip features allow the design of reliable, cost-effective and efficient Switched Mode Power Supplies (SMPS) using the minimum number of external components.

1.2.1 Key features

- PFC and flyback controller integrated in one SO16 package
- Switching frequencies of PFC and flyback controller are independent of each other
- No external hardware required for the communication between both controllers
- High level of integration, resulting in a low external component count
- Integrated mains voltage enable and brownout protection
- Fast-latch reset function implemented
- Power-down functionality for very low Standby mode power requirements

1.2.2 System features

- Safe restart mode for system fault conditions
- High voltage start-up current source (5 mA)
- Reduction of HV current source (1 mA) in safe restart mode
- Wide V_{CC} range (13.4 V to 38 V)
- MOSFET driver voltage limited
- Easy control of start-up behavior and V_{CC} circuit
- General-purpose input for latched protection
- Internal IC overtemperature protection
- Accurate PFC switch on/switch off control using flyback switching frequency measurement
- One high-voltage spacer between the HV pin and the next active pin
- Open pin protection on the VINSENSE, VOSENSE, PFCAUX, FBCTRL and FBAUX pins

1.2.3 PFC features

- Dual-output voltage boost converter
- QR/DCM operation with valley switching
- Frequency limitation (139 kHz) to reduce switching losses and ElectroMagnetic Interference (EMI)
- t_{on} controlled
- Mains input voltage compensation for control loop for good transient response
- OverCurrent Protection (OCP)
- Soft-start and soft-stop
- Open/short-circuit detection for PFC feedback loop: no external OverVoltage Protection (OVP) circuit necessary
- Adjustable delay for switching off the PFC
- Overriding the PFC switch on/switch off functionality

1.2.4 Flyback features

- Burst/FR/QR/DCM operation with valley switching
- Frequency Reduction (FR) with an adjustable minimum peak current and valley switching to maintain high efficiency at low output power levels
- Burst mode enhances the overall efficiency at low-output power
- Burst mode benefits the reduction of audible noise
- Frequency limitation (130 kHz) to reduce switching losses and EMI
- Current mode controlled
- Overcurrent protection
- Soft-start
- Accurate OVP through auxiliary winding

- Time-out protection for output overloads and open feedback loop, available as safe restart (TEA1755T) or latched (TEA1755LT) protection
- V_{CC} undervoltage prevention during burst mode

1.3 Application schematic

Refer to Figure 1 (part 1) and Figure 2 (part 2) for an overview of a typical application.

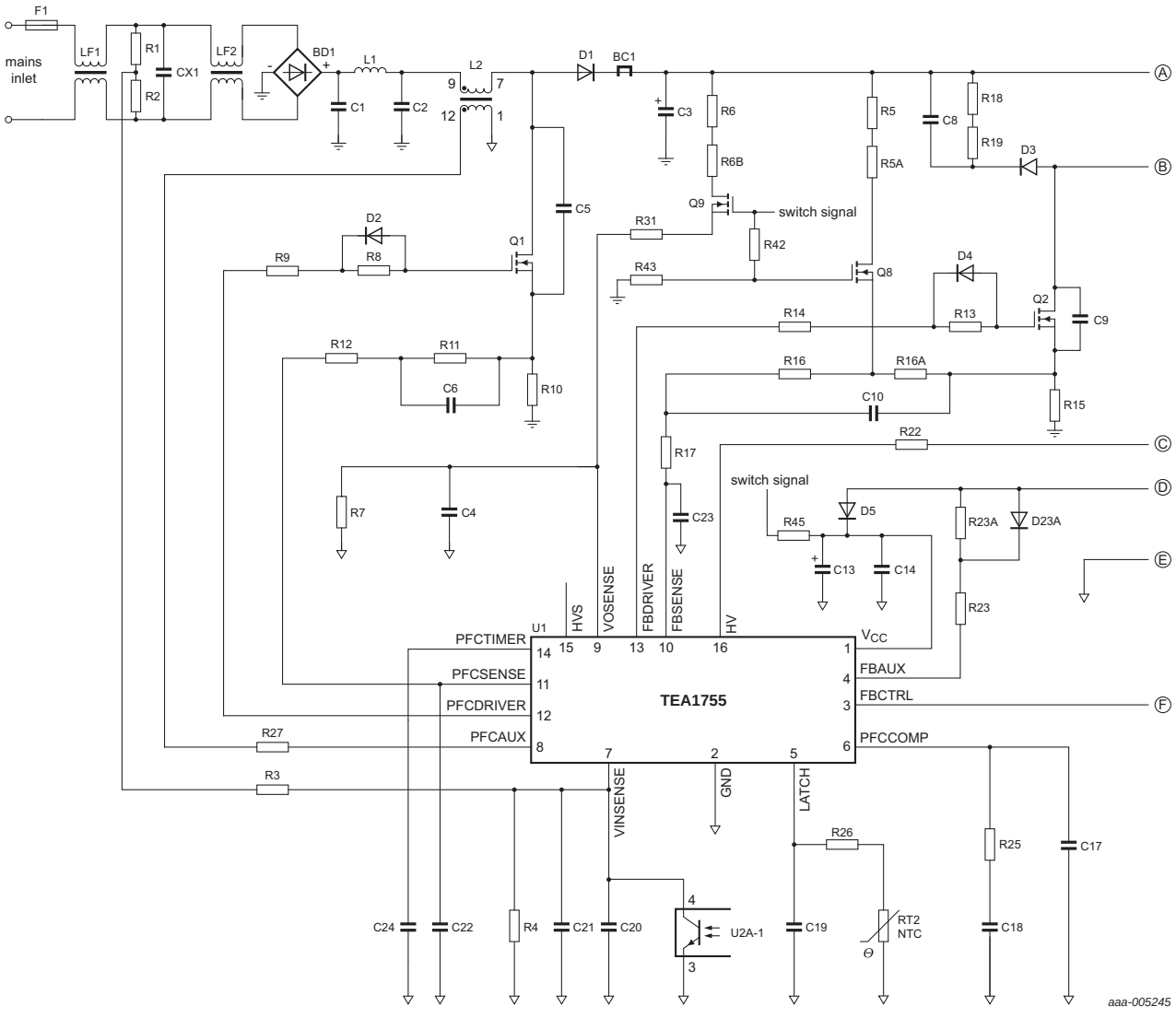


Fig 1. TEA1755 application schematic (part 1)

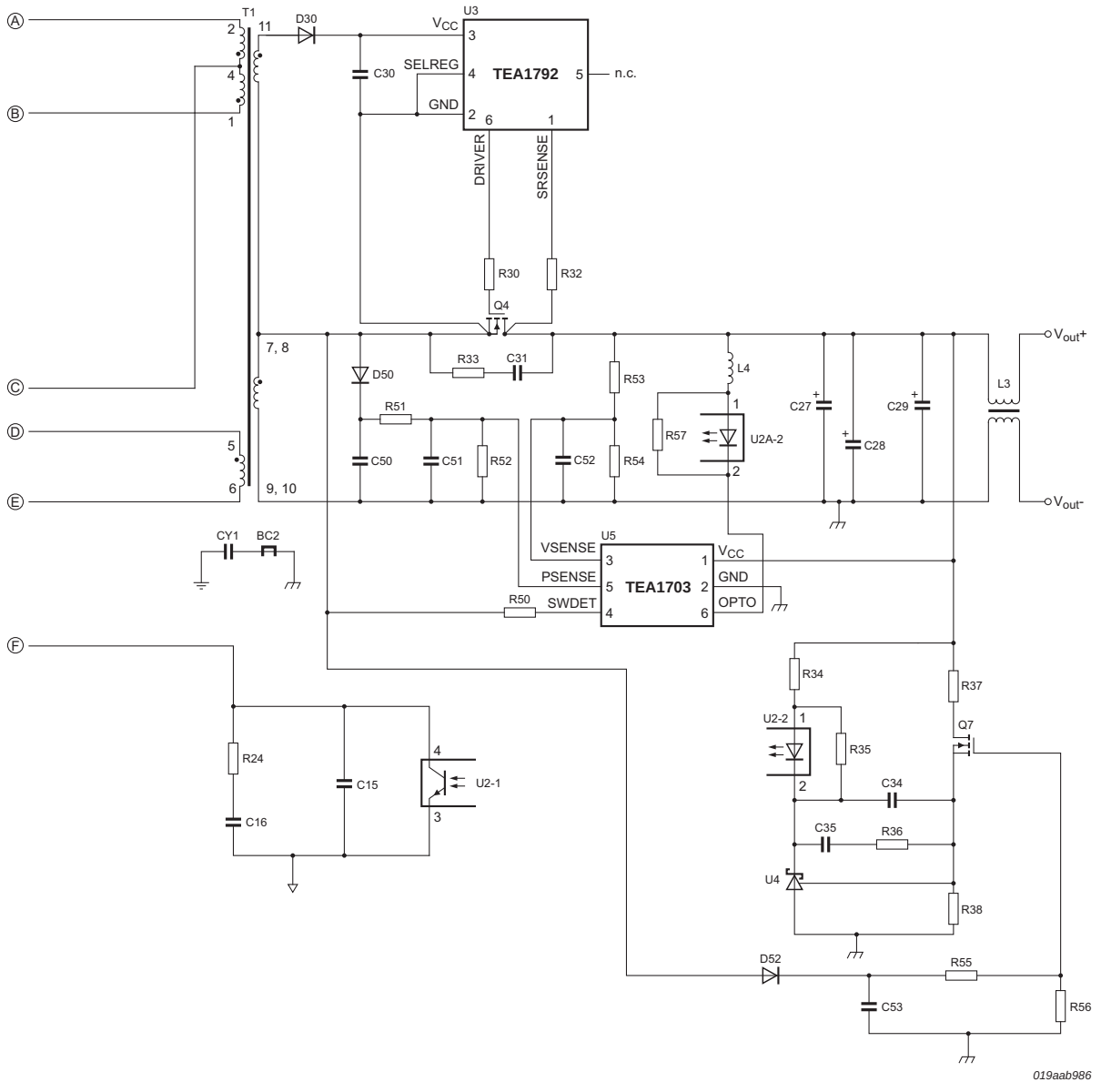


Fig 2. TEA1755 application schematic (part 2)

2. Pin description

Table 1. Pin description

Pin	Name	Functional description
1	V_{CC}	Supply voltage: $V_{startup}$ = 22.3 V, $V_{th(UVLO)}$ = 13.4 V. At mains switch-on, the capacitor connected to this pin is charged to $V_{startup}$ by the internal HV current source. When the V_{CC} is < 0.6 V, the charge current is limited to 1.1 mA. This feature prevents overheating of the IC if the V_{CC} pin is short-circuited. When the pin voltage is between 0.6 V and $V_{th(UVLO)}$, the charge current is 5 mA to enable a fast start-up. When it is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current is limited to 1 mA again to reduce the safe restart duty cycle. This results in a reduction of the input power during fault conditions. When $V_{startup}$ is reached, the HV current source is pinched off and V_{CC} is regulated to $V_{startup}$ until the flyback starts. See Section 3.2 for a complete description of the start-up sequence.
2	GND	Ground connection.
3	FBCTRL	Control input for flyback for direct connection of the optocoupler. At a control voltage of 4.9 V, the flyback delivers maximum power. The flyback enters FR mode at a control voltage of 4 V and burst mode at a control-voltage of approximately 1.2 V. It exits burst mode at 2.8 V. The flyback driver stops switching when FBCTRL is lower than 0.77 V. The built-in logic controls an internal 29 μA current source that is connected to the pin. This current source can be used to implement a time-out function to detect an open control loop or a short circuit of the output voltage. The time-out function is disabled by connecting a resistor of 180 kΩ between this pin and ground.
4	FBAUX	Input from auxiliary winding for transformer demagnetization detection, mains dependent OverPower Protection (OPP) and OverVoltage Protection (OVP) of the flyback. The combination of demagnetization and the valley detection on the HV pin determine the switch-on moment of the flyback controller in the valley. A flyback OVP is detected at a current higher than 300 μA to the FBAUX pin. Internal filtering prevents false detection of an OVP. The flyback OPP starts at a current lower than −100 μA from the FBAUX pin.
5	LATCH	General-purpose latched protection input. When $V_{startup}$ (on the V_{CC} pin) is reached, the LATCH pin is charged to 582 mV before the PFC and flyback controllers can be switched on. The latched protection is triggered when the pin is pulled below 494 mV and the PFC and the flyback are switched off. The logic controls an internal 30.5 μA current source which is connected to the pin. Using this current source, an optional Negative Temperature Coefficient (NTC) resistor can be directly connected to the LATCH pin for temperature protection.
6	PFCCOMP	Frequency compensation pin for the PFC control loop.

Table 1. Pin description *…continued*

Pin	Name	Functional description
7	VINSENSE	Sense input for mains voltage. The VINSENSE pin has six functions: • mains start level: $V_{start(VINSENSE)}$ = 1.16 V; • mains stop level (brownout): $V_{stop(VINSENSE)}$ = 0.89 V; • mains voltage compensation for the PFC control loop gain bandwidth; • fast-latch reset: V_{flr} = 0.75 V; • dual-boost switch-over point: $V_{bst(dual)}$ high = 2.28 V or low = 2.08 V (see Section 4) for more information • Standby mode: $V_{th(pd)}$ = 385 mV • Exit Standby mode: $V_{th(pd)exit}$ = 460 mV The voltage on the VINSENSE pin must be an averaged DC value, representing the AC line voltage. The pin is not used for sensing the phase of the mains voltage.
8	PFCAUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control PFC switching. Connect the auxiliary winding using a 5 kΩ series resistor to prevent damage to the input because of EMI surges.
9	VOSENSE	Sense input for the PFC output voltage. VOSENSE pin, open-loop and short-circuit detection; $V_{th(stop)(VOSENSE)}$ = 1 V; VOSENSE pin, start level $V_{th(start)VOSENSE}$ = 1.1 V; PFC output voltage regulation; $V_{reg(VOSENSE)}$ = 2.5 V; PFC soft OVP (cycle-by-cycle): $V_{ovp(VOSENSE)}$ = 2.62 V; Control output for the output voltage of the PFC; dual-boost current: $I_{bst(dual)}$ = −8.1 μA
10	FBSENSE	Flyback current sense input. On this pin, the sum of three voltages across three resistors is measured. Selecting the proper resistor values: • Prevents or minimizes the risk of saturation of the flyback transformer; • Allows some adjustment for switching on or switching off the PFC controller; • Allows a system that operates line voltage independently. The maximum $V_{sense(fb)max}$ level is 545 mV at dV/dt = 0 mV/μs. The $V_{sense(fb)min}$ level is 232 mV at dV/dt = 0 mV/μs. $V_{sense(fb)min}$ is related to the adjustable peak current through the flyback transformer when flyback is running in burst mode or frequency reduction mode. There are two internal current sources connected to this pin, $I_{start(soft)fb}$ and $I_{adj(FBSENSE)}$. The internal logic controls a 60 μA current source $I_{start(soft)fb}$. The current source is used to implement a soft-start function for the flyback controller. The flyback driver only starts when the internal current source can charge the soft-start capacitor to a voltage of more than 0.55 V. Therefore a minimum soft-start resistor of 15 kΩ is required to guarantee the flyback controller is switched on. The current source $I_{adj(FBSENSE)}$ = 2.1 μA. It is intended to support the adjustment for switch on and switch off the PFC.

Table 1. Pin description *…continued*

Pin	Name	Functional description
11	PFCSENSE	PFC overcurrent protection input. This input is used to limit the maximum peak current in the PFC core. The PFCSENSE is a switching-cycle-by-switching-cycle protection. The PFC MOSFET switches off when the PFCSENSE reaches 495 mV at dV/dt = 0 mV/μs. The logic controls a 60 μA current source which is connected to this pin. This current source is used to implement a soft-start and soft-stop function for the PFC to prevent audible noise. The PFC driver only starts when the internal current source can charge the soft-start capacitor to a voltage of more than 0.5 V. A soft-start resistor of at least 15 kΩ is required to guarantee the PFC starts-up.
12	PFCDRIVER	PFC MOSFET gate-driver output
13	FBDRIVER	Flyback MOSFET gate-driver output
14	PFCTIMER	This pin enables the use of two options: • Option 1: The timer delays the switching off the PFC when the load of the flyback is removed or minimized. The PFC is switched off when two conditions are met: – the filtered flyback operating frequency < 53 kHz (only valid during FR mode) and, – the voltage across the PFCTIMER pin is high (≥ 3 V). • Option 2: When an external voltage supply is connected to this pin, the typical PFC behavior is overridden. The PFC is switched on when the $V_{PFCTIMER}$ is forced ≤ 1.03 V. The PFC is switched off when the voltage ≥ 4.4 V.
15	HVS	High-voltage safety spacer, not connected.
16	HV	High-voltage input for the internal start-up current source (output on the V_{CC} pin) and valley sensing of the flyback. Valley detection input: The combination of demagnetization detection at the FBAUX pin and valley detection at the HV pin determine the switch-on moment of the flyback MOSFET in the valley.

3. System description and calculation

3.1 PFC and flyback start conditions

Figure 3 and Figure 4 show the conditions for switching on the PFC and the flyback during initial start-up. If start-up problems occur, check these conditions to find the cause of the problem. Some of the conditions are dynamic signals (see Figure 5). Check them using an oscilloscope.

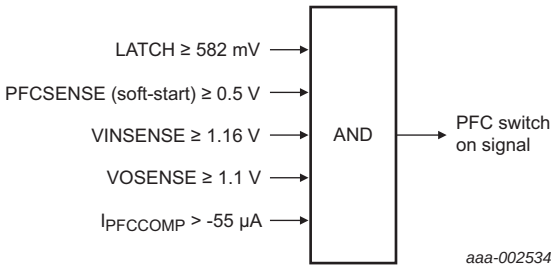


Fig 3. Switching on the PFC during initial start-up

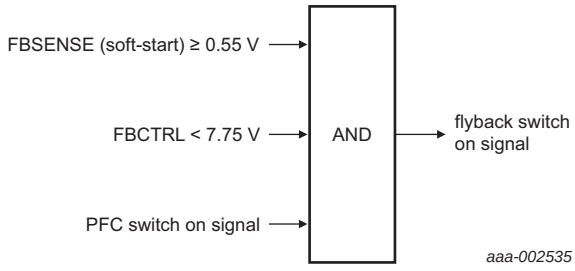


Fig 4. Switching on the flyback during initial start-up

3.2 Initial start-up sequence

At switch-on with a low mains voltage the TEA1755 power supply has the following start-up sequence (see Figure 5):

1. The HV current source is set to 1.1 mA and the electrolytic capacitor C_{VCC} is charged to 0.60 V to enable short-circuit detection on the V_{CC} pin.
2. At V_{CC} = 0.60 V, the HV current source is set to 5 mA and the C_{VCC} is quickly charged to $V_{th(UVLO)}$.
3. At $V_{CC} = V_{th(UVLO)}$, the HV current source is set to 1 mA and the V_{CC} electrolytic capacitor is charged to $V_{startup}$.
4. At $V_{startup}$, the HV current source is switched off. The 30.5 µA LATCH pin current source is switched on to charge the LATCH pin capacitor. The PFCSENSE and FBSENSE soft-start current sources are switched on.
5. When the LATCH pin is charged to 582 mV, the PFC can start switching when the VOSENSE = 1.1 V and VINSENSE = 1.16 V.
6. Two additional conditions for enabling the PFC driver are:
   a. charge the soft-start capacitor on PFCSENSE to 0.5 V.
   b. charge the capacitor connected to the PFCCOMP pin to either 1.92 V or 3.32 V depending on the VINSENSE voltage and wait until $I_{PFCCOMP}$ < 55 µA.
7. Conditions to enable the flyback driver are:
   a. all conditions for enabling the PFC are met.
   b. charge the soft-start capacitor on the FBSENSE pin to 0.55 V.
   c. ensure that the voltage on the FBCTRL pin is lower than 7.75 V. Normally, the voltage on the FBCTRL pin is lower than 7.75 V at the first flyback switching cycle, unless the FBCTRL pin is open. When flyback starts, the FBCTRL time-out current source is switched on.

8. When flyback has reached its nominal output voltage, the auxiliary winding takes over the V_{CC} supply. If the flyback feedback loop signal is missing, the time-out protection on the FBCTRL pin is triggered. Both converters are switched off, V_{CC} drops to the $V_{th(UVLO)}$ level and the IC restarts at step 3 of the start-up cycle. Step 3 is the safe restart cycle for the TEA1755T. The TEA1755LT is latched off and does not return to step 3. Instead, V_{CC} starts cycling between $V_{th(UVLO)}$ and $V_{startup}$ without restarting.

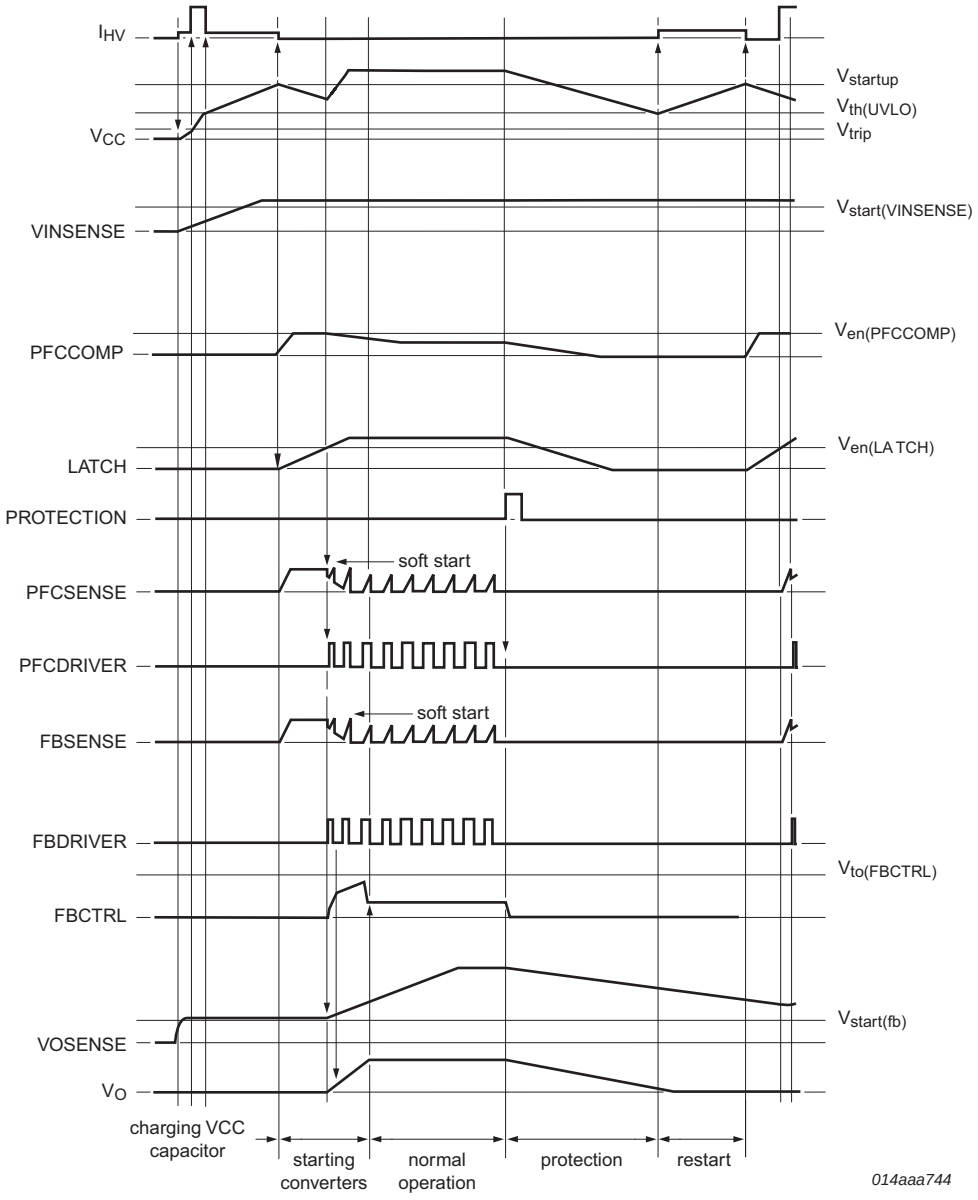


Fig 5. Start-up sequence at low mains voltage

The charge time of the soft-start capacitors can be chosen independently for the PFC and the flyback.

3.3 V_{CC} cycle in safe restart mode

In safe restart mode, the controller goes through the steps 3 to 8 as described in Section 3.2.

3.4 Mains voltage sensing and brownout

The mains input voltage is measured through the VINSENSE pin. When the VINSENSE pin has reached $V_{start(VINSENSE)}$ (1.16 V), the PFC starts switching. However, only if the other start conditions are also met (see Section 3.1).

When the voltage on the VINSENSE pin ≤ $V_{stop(VINSENSE)}$ (0.89 V), the PFC stops switching. However, the flyback driver continues switching until the maximum flyback on-time protection $t_{on(fb)max}$ (38.5 μs) is triggered. When this protection is triggered, the IC stops switching and enters safe restart mode.

The voltage on the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimally using a time constant of approximately 150 ms on the VINSENSE pin.

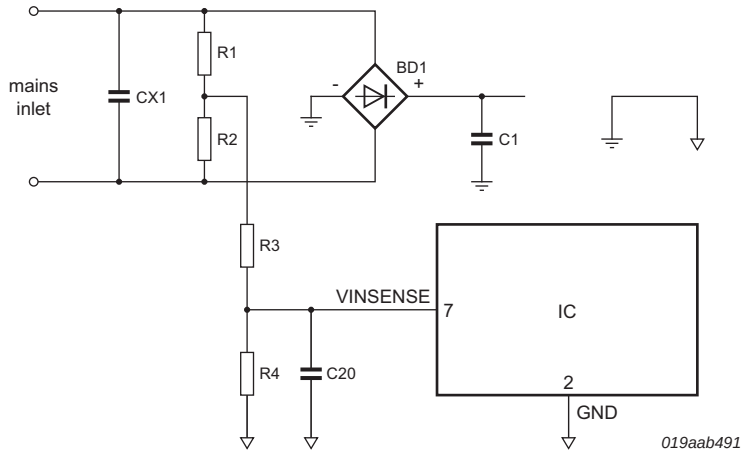


Fig 6. VINSENSE circuitry

3.4.1 Discharging the mains input capacitor

Discharge the X-capacitors in the ElectroMagnetic Compatibility (EMC) input filter using a time constant of τ < 1 s for safety reasons.

Use Equation 1 to determine the replacement resistor value of R_V:

$$R_V = R + \frac{R \times (R3 + R4)}{R + R3 + R4} \quad (1)$$

Where:

- R = R1 = R2

A 90 W adapter often uses a value of 220 nF for CX1. Therefore, the R_V value must be lower than or equal to:

$$R_V \leq \frac{\tau}{CX1} = \frac{1}{220\ nF} = 4.55\ M\Omega \quad (2)$$

3.4.2 Brownout voltage adjustment

The rectified AC input voltage is measured using R1 and R2. Make sure that both resistors have the same value because each resistor alternately senses half the sine wave. Equation 3 shows the calculation for the average rectified line voltage value:

$$V_{avg} = \frac{2 \times \sqrt{2}}{\pi} \cdot V\ (AC)\ RMS \quad (3)$$

The V (AC) brownout RMS level is calculated using Equation 4:

$$V_{bo}\ (AC) = \frac{\pi}{2 \times \sqrt{2}} \times V_{stop(VINSENSE)} \times \frac{(RV + R3 + R4)}{R4} \quad (4)$$

Where: $V_{stop(VINSENSE)}$ = 0.89 V

At a brownout threshold of 68 V (AC) and in compliance to *IEC-60950 chapter 2.1.1.7 discharge of capacitors in equipment* (Ref. 3). Example values are shown in Table 2.

Table 2. VINSENSE component values

CX1	R1	R2	R3	R4
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

A 3.3 μF value for C20 and a 47 kΩ R4, gives the recommended ~150 ms time constant on the VINSENSE pin.

3.4.3 Minimizing the influence of the dark-current of the optocoupler

The TEA1755 enters Standby mode when VINSENSE ≤ $V_{th(pd)}$ (385 mV) and exit Standby mode when VINSENSE ≥ $V_{th(pd)exit}$ (460 mV). The Standby mode functionality is achieved by pulling the VINSENSE voltage down to ground using an optocoupler.

The transistor of an optocoupler is not ideal, it always conducts a leakage current. The optocoupler transistor leakage current is known as dark-current. Dark-current current is temperature and voltage dependent. Figure 7 shows the proposed circuit that can handle dark-current up to 10 μA.

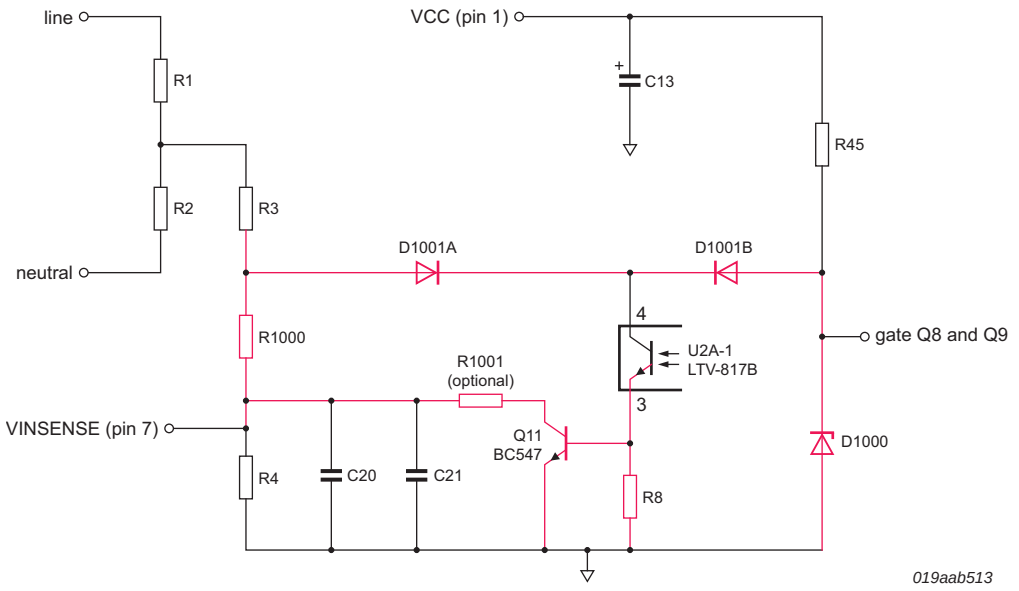


Fig 7. The proposed VSENSE circuit for minimizing the influence of the dark current

The VINSENSE voltage must reach the $V_{th(pd)exit}$ before the internal HV current source is enabled. The V_{CC} supply voltage increases and supports any dark-current needed for the optocoupler. The optocoupler dark-current no longer influences the VINSENSE voltage.

Add the red colored components to the schematic shown in Figure 1. Diode D1001A and D1001B are available in one component. Remove two resistors (R42 and R43) in Figure 1 when Figure 7 is added.

3.5 Internal OverTemperature Protection (OTP)

The IC has an internal temperature protection to protect the IC from overheating. When the junction temperature exceeds the thermal shutdown temperature, the IC stops switching. As long as the OTP is active, the V_{CC} capacitor is not recharged from the HV mains. If the V_{CC} supply voltage is not sufficient, the OTP circuit is supplied from the HV pin. OTP is a latched protection.

3.6 LATCH pin

The LATCH pin is a general-purpose input pin which can be used to latch off both converters. The pin sources a bias current $I_{O(LATCH)}$ of 30.5 μA for the direct connection of a NTC. When the voltage on the LATCH pin is pulled below $V_{prot(LATCH)}$, switching of both converters is stopped immediately. V_{CC} starts cycling between the $V_{th(UVLO)}$ (13.4 V) and $V_{startup}$ (22.3 V) without a restart. Switching off the mains input voltage and then switching it on triggers the fast-latch reset circuit and resets the latch (see Section 3.7).

At start-up, the LATCH pin is charged above $V_{en(LATCH)}$ (582 mV) before both converters are enabled. Charging of the LATCH pin starts when $V_{CC} = V_{startup}$.

A 10 nF capacitor is placed between the LATCH pin and the IC GND pin to prevent false triggering. In addition, when the LATCH pin function is not used add a 10 nF capacitor.

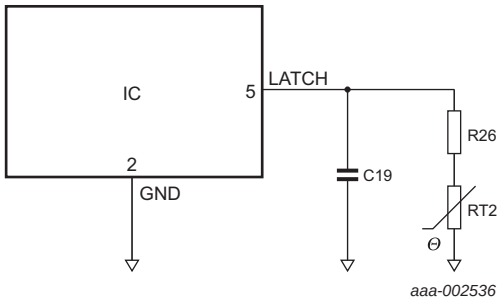


Fig 8. Usage of the LATCH pin protection

Latching on application overtemperature occurs when the total resistance value of the NTC plus the series resistor drops under the following:

$$R_{OTP} = \frac{0.495\ V}{30.5\ \mu A} = 16.13\ k\Omega \quad (5)$$

3.7 Fast-latch reset

Switching off the mains input voltage and then switching on resets the latched protection. After the mains input is switched off, the voltage on the VINSENSE pin drops ≤ V_{flr} (0.75 V). The voltage drop triggers the fast-latch reset circuit but does not reset the latched protection. After the mains input is switched on, the voltage on the VINSENSE pin rises again. The latch is reset when the level has passed V_{flr} + $V_{flr(hys)}$ (0.86 V). The system restarts when the V_{CC} pin is charged to $V_{startup}$ (See step 4 of Section 3.2).

4. PFC description and calculation

The PFC controller operates in either QR mode or DCM mode with valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to $f_{sw(PFC)max}$ (139 kHz) to reduce switching losses. If necessary, one or more valleys are skipped to keep the frequency below 139 kHz.

The PFC is designed as a dual-boost converter with two output voltage levels that are dependent on the mains input voltage range. The advantage is that the overall system efficiency at low mains is improved because of the reduction of the PFC switching losses. In low and medium power adapters (< 120 W), the contribution of PFC switching losses to the total losses is relatively high.

An internal current source of 8.1 µA ($I_{bst(dual)}$) on the VOSENSE pin controls the dual-output voltage. The mains input voltage measured at the VINSENSE pin is used to control the internal current source as shown in Figure 9. This current source, in combination with the resistors connected to the VOSENSE pin, sets the lower PFC output voltage. At high mains, the current source is switched off. The maximum PFC output voltage is unaffected by the current source accuracy. In a typical adapter, with a 385 V (DC) PFC output voltage at high mains, the PFC output voltage is 250 V (DC) at low mains. A voltage of 2.3 V at the VINSENSE pin corresponds with a mains input voltage of approximately 170 V (AC). The small slope at the transfer function ensures a stable switchover of the PFC output voltage without hiccups.

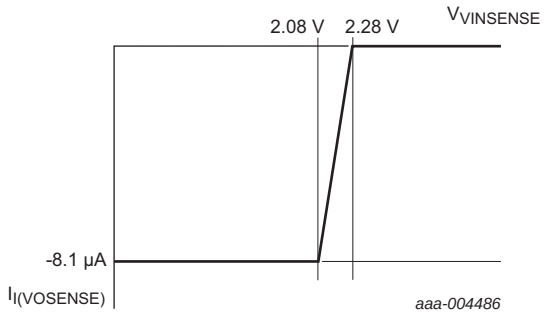


Fig 9. Transfer function of VINSENSE voltage to dual-boost current at VOSENSE

The PFC is switched off to ensure high efficiency during low output currents. After switch off, the electrolytic bulk capacitor voltage V_{Cbulk} drops to $line\ voltage \times \sqrt{2}$.

4.1 PFC output power and voltage control

The PFC of the TEA1755 is on-time controlled, therefore it is not necessary to measure the mains phase angle. The on-time is kept constant during the half sine wave to obtain a good Power Factor (PF) and a class-D Mains Harmonics Reduction (MHR).

The PFC output voltage is controlled using the VOSENSE pin. At the VOSENSE pin, there is a transconductance error amplifier with a reference voltage of 2.5 V ($V_{reg(VOSENSE)}$). The error on the VOSENSE pin is converted with 77 µA/V (g_m) to a current on the PFCCOMP pin. The voltage on the PFCCOMP pin, in combination with the voltage on pin VINSENSE, determines the PFC on-time.

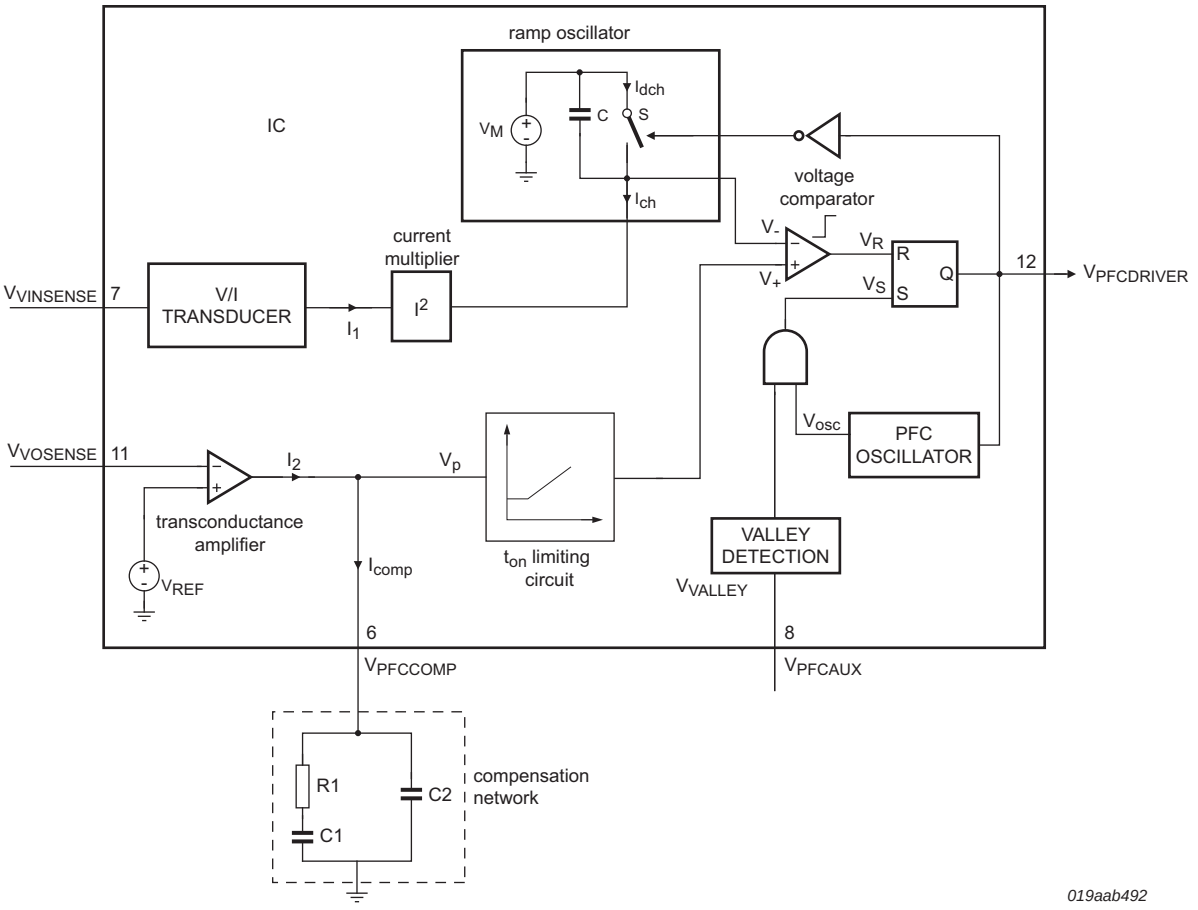


Fig 10. TEA1755 PFC converter on-time control

A network with one resistor and two capacitors at the PFCCOMP pin is used to stabilize the PFC control loop. The equation for a boost converter transfer function contains the square of the mains input voltage. In a typical application, this results in a low regulation bandwidth for low mains input voltages and a high regulation bandwidth for high input voltages. The result can be that at high mains input voltages, it can be difficult to meet the MHR requirements. The TEA1755 uses the mains input voltage measured through the VINSENSE pin to compensate the control loop gain as a function of the mains input voltage. As a result the gain is constant over the entire mains input voltage range.

The voltage on the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimally with a time constant of approximately 150 ms on the VINSENSE pin.

4.1.1 Setting the PFC output voltage

The PFC output voltage is set using a resistor divider between the PFC output voltage and the VOSENSE pin. In normal mode, the PFC output voltage is regulated so that the voltage on the VOSENSE pin is equal to $V_{reg(VOSENSE)}$ (2.5 V).

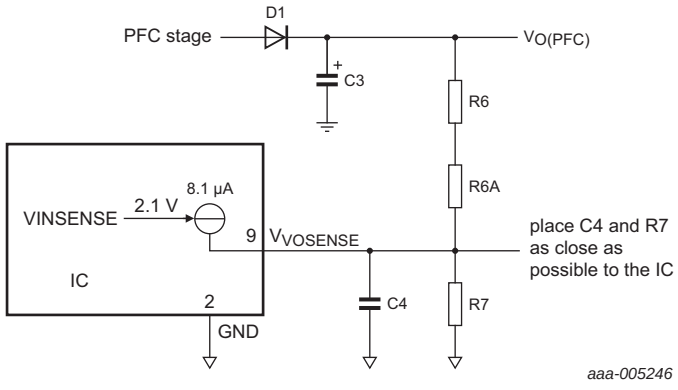


Fig 11. TEA1755 PFC converter output voltage setting

The VOSENSE pin has an integrated protection circuit to detect an open circuit pin (see Section 4.3.2). The open-circuit pin protection operates reliably when $R7 \leq V_{th(stop)VOSENSE(min)} / I_{bst(dual)max}$ = 0.95 V / 9.1 µA = 104.4 kΩ. The first possible resistor value (below the 104.4 kΩ) available in the E96 series is 102 kΩ.

Remark: MAX is the maximum limiting current value. In data sheet, it is a negative number. Normally, we calculate using positive numbers, so it is called in this application note the maximum value.

Selecting a larger value for R7 can override PFC open-loop protection. The maximum bulk electrolytic capacitor voltage ($V_{bulk(PFC)high}$) can be calculated using Equation 6:

$$V_{bulk(PFC)high} = 2.5\ V \times \left(\frac{R6 + R6A + R7}{R7} + 1\right) \quad (6)$$

The PFC converter only operates correctly when $V_{bulk(max)} > V_{mains(max)} \times \sqrt{2}$ + 10 V (voltage margin). In a universal mains adapter, the highest line voltage is typically 264 V.

Therefore, $V_{bulk(max)} = 264 \times \sqrt{2} + 10 \approx 383$ V. Using this information together with Equation 6 the minimum resistor divider value is calculated (see Equation 7):

$$\frac{R6 + R6A + R7}{R7} \geq \frac{V_{bulk(PFC)high} - 2.5}{2.5} \geq \frac{383 - 2.5}{2.5} \geq 153.34 \quad (7)$$

Rewriting Equation 7 results in:

$$\frac{R6 + R6A}{R7} = \frac{R6 + R6A + R7}{R7} - \frac{R7}{R7} = 153.34 - 1 = 152.34 \quad (8)$$

$V_{bulk(PFC)low}$ is calculated using:

$$V_{bulk(PFC)low} = V_{reg(VOSENSE)} + \frac{R6 + R6A}{R7} \times (V_{reg(VOSENSE)} - I_{bst(dual)} \times R7) \quad (9)$$

At low line voltages, the recommended value for $V_{bulk(PFC)low} \geq 250$ V.

Equation 9 looks as follows when rewritten with the values:

$$V_{bulk(PFC)low} = 2.5 + 152.34 \times (2.5 - 8.1 \times 10^{-6} \times 102 \times 10^{3}) \approx 258\ V \quad (10)$$

With R6 + R6A equal to:

$$R6 + R6A = 152.34 \times R7 = 152.34 \times 102 \times 10^{3} = 15539\ k\Omega \quad (11)$$

If R6 = R6A, therefore R6 =15539 / 2 = 7769 kΩ = 7.77 MΩ.

The calculated $V_{bulk(PFC)low}$ value fits with the recommended minimum value of 250 V at low line voltages. Lowering the R7 value results in an increased $V_{bulk(PFC)low}$ and $V_{bulk(PFC)high}$. Table 3 shows some calculation examples using R6 = 7680 kΩ and R6A = 7870 kΩ (R6 + R6A = 15550 kΩ).

Table 3. R6 and R6A calculated using different R7 values

R7 (kΩ)	R6 + R6A / R7	$V_{bulk(PFC)low}$ (V)	$V_{bulk(PFC)high}$ (V)
102	152.45	258	386
100	155.55	265	394
97.6	159.32	275	403

Remark: The selected R7 values in Table 3 are standard values of the E96 series

When R7 ≤ 104.4 kΩ and $V_{bulk(PFC)low} \geq 250$ V meet their requirements, the results are within limits.

Capacitor C4 (see Figure 1) filters noise and prevents protection modes false triggering because of MOSFET switching noise. False triggering of the $V_{ovp(VOSENSE)}$ protection can cause audible noise and disturbance of the AC mains input current.

A time constant between 500 ns and 1 μs at the VOSENSE pin is sufficient, resulting in a 4.7 nF C4 capacitor value.

Place R7 and C4 as close as possible to the IC between the VOSENSE pin and the GND pin.

4.1.2 Calculation of the PFC soft-start and soft-stop components

Soft-start and soft-stop are implemented using the RC network connected to the PFCSENSE pin.

To enable PFC driver start-up, resistor R_{SS1} must be ≥ 15 kΩ minimum value to ensure that the $V_{start(soft)PFC}$ voltage of 0.5 V is reached. See Section 3.2 for a description of start-up.

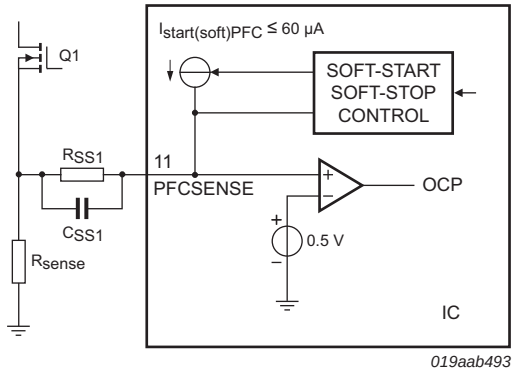


Fig 12. PFC soft-start and soft-stop

The total soft-start or soft-stop time is $t_{soft\text{-}start} = 3 \times R_{SS1} \times C_{SSI}$. Switching off the PFC always ends with a soft-stop. However, there is an exception to this rule. The switched on PFC does not generate a soft-stop when the system enters burst mode even though C_{SS1} charges up to $V_{sense(PFC)max}$ after switching off the PFC. The charged C_{SS1} capacitor allows a fast restart of the PFC when applicable.

Keep the soft-start time of the PFC shorter than the soft-start time of the flyback controller. It is also recommended that the soft-start time is kept within a range of 2 ms to 5 ms.

Using C6 = 100 nF and R11 = 15 kΩ results in a soft-start time of 4.5 ms.

4.2 PFC demagnetizing and valley detection

The PFC MOSFET is switched on after the transformer is demagnetized. The internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next primary stroke is started when the voltage across the PFC MOSFET is at its minimum level. When the voltage is at the minimum level, switching losses and ElectroMagnetic Interference (EMI) (valley switching) are reduced.

To reduce the switching losses, the PFC converter maximum switching frequency is limited to 139 kHz. If necessary, one or more valleys are skipped to keep the frequency under 139 kHz.

When demagnetization is not detected on the PFCAUX pin, the controller generates a Zero-Current Signal (ZCS) 48 µs ($t_{to(demag)PFC}$) after the last PFC gate signal. If a valley signal is not detected on this pin, the controller generates a valley signal 4.2 µs ($t_{to(demag)PFC}$) after demagnetization was detected.

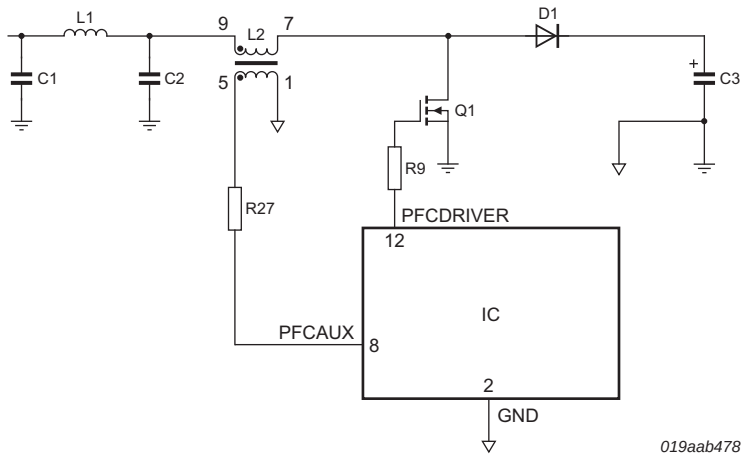


Fig 13. TEA1755 PFCAUX circuitry

4.2.1 Design of the PFCAUX winding and circuit

Set the voltage on pin PFCAUX as high as possible within the absolute maximum voltage rating of ± 25 V. This setting guarantees valley detection at low ringing amplitudes.

The number of turns of the PFCAUX winding is calculated using Equation 12.

$$N_{aux(max)} = \frac{V_{PFCAUX}}{V_{L(max)}} \times N_p = \frac{25\ V}{V_{L(max)}} \times N_p \quad (12)$$

- V_{PFCAUX} is the absolute maximum rating of the PFCAUX pin
- $V_{L(max)}$ is the maximum voltage across the PFC primary winding

The PFC output voltage at the PFC OVP level determines the maximum voltage across the PFC primary winding and is calculated using Equation 13:

$$V_{L(max)} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \times V_{O(PFC)} = \frac{2.62\ V}{2.5\ V} \times V_{O(PFC)} \quad (13)$$

When a PFC coil with a higher number of auxiliary turns is used, place a resistor voltage divider between the auxiliary winding and the PFCAUX pin. The total resistive value of the divider must be ≤10 kΩ to prevent a valley detection delay due to parasitic capacitance.

The polarity of the signal at the PFCAUX pin is reversed compared to the PFC MOSFET drain signal.

Add a 5 kΩ resistor between the PFC auxiliary winding and the PFCAUX pin to protect against electrical overstress during lightning surge events. Place the resistor as close as possible to the IC to prevent incorrect valley switching of the PFC because of external disturbances.

4.3 PFC protection modes

4.3.1 VOSENSE overvoltage protection

Overvoltage can occur across the bulk electrolytic capacitor during the initial start-up and large load changes. The relative slow response of the PFC control loop causes this overvoltage. The PFC control loop response must be relatively slow to guarantee a good power factor and meet the MHR requirements. The OverVoltage Protection (OVP) on the VOSENSE pin limits the overvoltage.

When the $V_{ovp(VOSENSE)}$ level = 2.62 V is detected, the PFC MOSFET is switched off immediately regardless of the on-time setting. The switching of the MOSFET is blocked until the voltage on the VOSENSE pin drops < 2.62 V again. OVP is also triggered when the resistor between the VOSENSE pin and ground is open. The peak voltage during an overshoot across the electrolytic bulk capacitor is calculated using Equation 14.

$$V_{O(PFC)pk} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot V_{O(PFC)nom} = \frac{2.62\ V}{2.5\ V} \cdot V_{O(PFC)nom} \quad (14)$$

4.3.2 VOSENSE open and short pin detection

The VOSENSE pin senses the PFC output voltage. The VOSENSE pin has an integrated protection circuit to detect an open and short circuited pin. The VOSENSE pin also senses that one of the resistors in the voltage divider is open making the VOSENSE pin failsafe.

It is not necessary to add an external OVP circuit for the PFC.

When the pin is open, an internal current source pulls $V_{VOSENSE}$ up and $V_{OVP(VOSENSE)}$ is detected. The PFC stops switching when $V_{OVP(VOSENSE)}$ is detected and an internal voltage clamp limits the maximum VOSENSE voltage. The same condition applies when only resistor R7 is open (see Figure 11). The internal voltage clamp again limits the maximum VOSENSE voltage to acceptable values.

The PFC is not switching when $V_{VOSENSE} \leq V_{Vth(stop)VOSENSE}$, this condition is applicable when VOSENSE is short ciruited to ground. The same condition is applicable if only resistor R6 or R6A (see Figure 11) is open. However under the condition that R7 ≤ 104.4 kΩ (see Section 4.1.1).

4.3.3 VINSENSE open pin detection

The VINSENSE pin senses the mains input voltage, The VINSENSE pin has a protection circuit to detect an open pin. An internal current source pulls down the pin to ≤ $V_{stop(VINSENSE)}$ (0.89 V) when the pin is open.

4.3.4 Overcurrent protection

The overcurrent protection limits the maximum current through the PFC MOSFET and PFC coil. The current is measured via a current sense resistor in series with the MOSFET source. The MOSFET is switched off immediately when the voltage on the PFCSENSE pin exceeds the $V_{sense(PFC)max}$ level of 495 mV at dV/dt = 0 mV/µs. OCP is a cycle-by-cycle protection.

To avoid false triggering of the PFC OCP by the flyback converter switching, use a 100 mV margin. False triggering of the $V_{sense(PFC)max}$ protection can cause interference to the AC mains input current. Place a small capacitor between 100 pF and 220 pF next to the PFCSENSE pin to suppress any external disturbance.

The current sense resistor is calculated using Equation 15:

$$R_{ocp(PFC)} = \frac{V_{sense(PFC)max} - V_{margin}}{I_{pQR(PFC)max}} = \frac{0.495\ V - 0.1\ V}{I_{pQR(PFC)max}} \quad (15)$$

Where: the maximum PFC peak current is $I_{pQR(PFC)max}$ at the high output load and low mains.

The maximum peak current for the PFC operating in Quasi-Resonant (QR) mode is calculated using Equation 16:

$$I_{pQR(PFC)max} = \frac{2\sqrt{2} \cdot P_{i(max)} \cdot 1.1}{V(AC)min} = \frac{2\sqrt{2} \cdot \frac{P_{o(max)}}{\eta} \cdot 1.1}{V(AC)min} \quad (16)$$

Where:

- $P_{o(max)}$ is the maximum output power of the flyback
- Factor 1.1 is used to compensate the dead-time between zero-current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in quasi-resonant mode
- η is the expected efficiency of the total converter at maximum output power
- V(AC)min is minimum mains input voltage.

5. Flyback description and calculation

5.1 Flyback output power control

The TEA1755 flyback system waits until the transformer is demagnetized and at least one valley has appeared before it is magnetized again for the next cycle. The FBAUX pin detects demagnetization via the auxiliary winding. The HV pin detects the bottom of the valley via the drain of the MOSFET or the central tap of the primary winding.

The output power (P_O) of the flyback is calculated using Equation 17:

$$P_O = \frac{1}{2} \cdot L_p \cdot I_{pk}^{2} \cdot f_s \cdot \eta \quad (17)$$

Where:

- L_p is the flyback transformer primary inductance
- I_{pk} is the flyback transformer primary peak current
- f_s is the flyback controller operating frequency
- η is the flyback controller efficiency

L_p is selected at the start of the design. The primary peak current controls the (high) output power in QR and DCM mode. The switching frequency is a result of external application parameters and IC parameters.

External application parameters are the transformer turns ratio, primary inductance, the drain source capacitance, input voltage, output voltage and the feedback signal from the control loop. IC parameters are the oscillator setting, the peak current setting and the demagnetization and valley detection.

The primary current I_{pk} is fixed at medium and low output power. The power is controlled by changing the operating frequency. Output power and operating frequency are linearly related during this type of control. In this application note, it is called operating in frequency reduction mode (See Section 5.1.1.3). The minimum switching frequency in FR mode is 25 kHz. At even lower output powers, the IC enters the burst mode which minimizes audible noise.

The burst mode is a hysteresis controlled system, used during low output-power. The primary peak current I_{pk} and operating frequency of the flyback are both fixed when the system supports power to the output.

Using V_{FBCTRL} as a hysteresis input results in a variable amount of FBDRIVER switching pulses combined with a changing burst mode repetition frequency.

The flyback input voltage is measured using the FBAUX pin and it is used to implement an OverPower Protection (OPP). OPP keeps the maximum output power of the flyback converter constant over the input voltage.

The flyback has an accurate OverVoltage Protection (OVP) circuit. The overvoltage is measured through the FBAUX pin. Both flyback and PFC controllers are switched off in a latched protection when an overvoltage is detected.

5.1.1 Four TEA1755 operation modes

At initial start-up, the flyback always starts at the maximum output power. This means that the system starts up in Quasi-resonant mode. The flyback of the TEA1755 passes through four operation modes (see Figure 14) from maximum to minimum output power:

- Quasi-Resonant (QR) mode
- Discontinuous Conduction Mode (DCM)
- Frequency Reduction (FR) mode
- Burst Mode (BM)

The internal demagnetization detection and valley switching circuitry is active in all four operating modes.

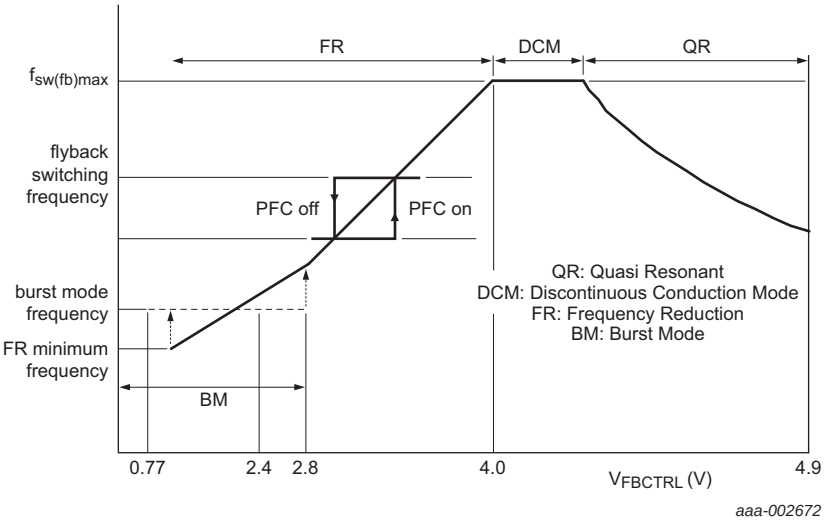


Fig 14. Flyback operation modes

5.1.1.1 Quasi-resonant mode

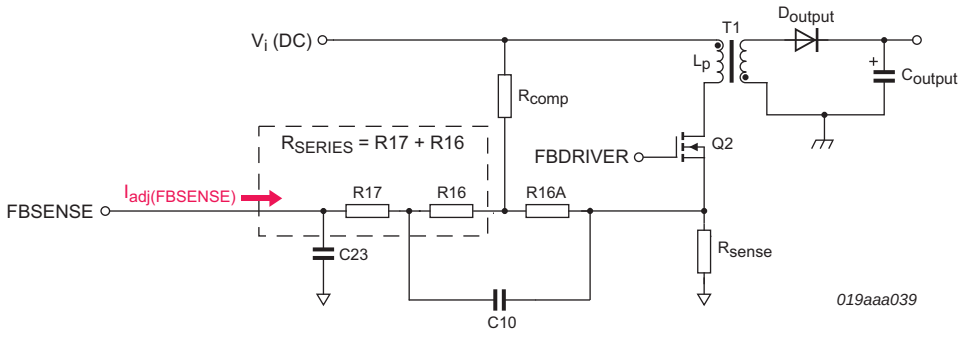
The flyback operates in quasi-resonant mode at high and maximum output power. The peak current controls the output power (see Section 5.1). A lower peak current than the maximum allowed value results in lower output power and a higher operating frequency until the maximum operating frequency is reached. The quasi-resonant mode can easily be recognized. The next primary switching cycle starts when the bottom of the first valley is detected.

The voltage on the FBCTRL pin sets the primary peak current (I_{pk}). Place the 220 pF noise filter capacitor (C15) as close as possible to the FBCTRL pin to avoid flyback controller interference by the PFC MOSFET switching. The voltage on the FBCTRL pin is measured back at the FBSENSE pin and is calculated using Equation 18 (only valid in QR mode or DCM):

$$V_{Rsense(fb)} \cong 0.315 \times V_{FBCTRL} - 1.1591 - I_{adj(FBSENSE)} \times (R16 + R17) \quad (18)$$

Where:

- V_{FBCTRL} is allowed to vary between the 4 V and 4.9 V (only valid in QR mode and DCM mode)
- $I_{adj(FBSENSE)}$ related to a current source inside the IC, connected to the FBSENSE pin
- Resistors R16 and R17 are found in the circuit diagram, see Figure 15.



FBSENSE has two internal reference levels:

(1) $V_{sense(fb)max}$ = 545 mV at dV/dt = 0 mV/µs

(2) $V_{sense(fb)min}$ = 232 mV at dV/dt = 0 mV/µs

Fig 15. Most important components for adjusting the flyback in the application

Equation 19 defines the peak current I_{pk} through the flyback transformer:

$$I_{pk} = \frac{V_{sense(fb)} - I_{adj(FBSENSE)} \times \{R16 + R17\}}{R_{sense}} \quad (19)$$

$V_{sense(fb)max}$ determines the maximum peak current $I_{pk(max)}$. R16A is not mentioned in Equation 18 and Equation 19, but R16A is explained in Section 5.1.5. Decreasing the output power results in the flyback entering discontinuous conduction mode when the maximum switching frequency is reached.

5.1.1.2 Discontinuous conduction mode

Reducing the peak current (I_{pk}) and skipping more valleys decreases the output power. It results in a switching frequency close to but never higher than $f_{sw(PFC)max}$ (139 kHz). The operating mode switches from DCM to FR mode when V_{FBCTRL} = 4 V ($V_{start(red)f}$).

Sometimes DCM is not reached when the selected primary inductance of the inductor is too large. In this case, flyback skips DCM when it is reducing power. It jumps directly from QR mode to FR mode.

5.1.1.3 Frequency reduction mode and PFC switch on/switch off control

The voltage across the FBCTRL pin in Frequency reduction mode does not set the peak current, instead it sets the operating frequency. The minimum primary peak current $I_{pk(min)}$ through the flyback transformer is kept constant during FR mode.

The ratio $I_{pk(min)}$: $I_{pk(max)}$ mainly depends on the sense resistor R_{sense} value assuming that the core is not saturated at $I_{pk(max)}$. Decreasing the output power reduces the operating frequency. As a result of the frequency reduction, more valleys are skipped.

The flyback operating frequency during FR mode determines when the PFC is switched on or switched off.

Decreasing the output-power from maximum to minimum switches off the PFC before it has reached 25 % of the nominal output current. Switching off the PFC improves the overall efficiency at low output power.

Increasing the output-power from minimum to maximum starts the PFC up before it has reached 50 % of the nominal output current. Starting up the PFC improves the power factor of the line current at high output power.

The PFC switch-on/switch-off state depends on the primary inductance value, the output power and the line voltage. It is therefore, important to select the right inductance value to ensure enough hysteresis between the PFC switch-on/switch off state, especially at low line voltages (see Section 5.1.2).

The following three options are used to switch on the PFC:

1. The PFC is using the flyback operating frequency during FR mode ($f \geq f_{sw(fb)swon(PFC)}$).
2. $V_{FBCTRL} \geq V_{en(PFC)FBCTRL}$ (3.75 V), applicable at initial start-up or when the flyback operating frequency cannot reach $f_{sw(fb)swon(PFC)}$.
3. When the duty-cycle of the FBDRIVER ≥ 50 %.

Option 3 is useful during line dips, assuming that some residual line voltage is present that can support power. The flyback can support more power to the output when its input voltage is higher (because of the switched on PFC), it can therefore, hold the nominal output voltage for a longer time.

Table 4. PFC switch on and switch off signals[1]

Options	PFC switch-on signal	PFC switch off signal
1	$f_{sw(fb)} \geq 73$ kHz	$f_{sw(fb)} \leq 53$ kHz
2	$V_{FBCTRL} \geq 3.75$ V	
3	$\delta_{FBDRIVER} \geq 50$ %	

[1] The table does not list the PFC table override function. See Section 5.2.1 and Section 5.2.2.

Remark: VINSENSE ≤ $V_{stop(VINSENSE)}$ switches off the PFC, regardless which PFC switch-on signal is used.

The minimum operating frequency during FR mode is 25 kHz. This frequency is above the audible frequency for humans.

5.1.1.4 Burst mode

Requesting less output power activates the frequency clamp and the flyback controller starts to operate in burst mode. The PFC continues to operate if it was switching. The PFC stops switching when $V_{PFCTIMER} \geq V_{stop(PFCTIMER)}$ (3 V). The internal circuitry of the TEA1755 is partly shut down, resulting in a reduced supply current.

The peak current $I_{pk(min)}$ during burst mode is equal to the value in FR mode.

The burst mode repetition frequency and amount of FBDRIVER pulses depends on the feedback loop and output power.

The maximum burst mode repetition frequency is preferably below the 700 Hz, some adjustment can be made by changing the value of R34. A relatively low burst mode repetition frequency minimizes the risk on audible noise.

The flyback driver operating frequency is fixed at $f_{sw(fb)burst}$ (36.5 kHz) during BM and starts when the FBCTRL > $V_{th(burst)on}$ (2.4 V). Starting the driver results in a fast reduction in the control voltage and the driver continues to operate until FBCTRL < $V_{th(burst)off}$ (0.77 V).$V_{FBDRIVER}$ voltage is constant LOW during the increase of V_{FBCTRL} up to 2.4 V.

The FBCTRL voltages for BM and higher output powers are tuned to each other. This tuning benefits the design allowing standard feedback component values for the feedback loop.

Requesting more output power results in a higher control voltage overshoot (> 2.4 V) when the driver starts. However, the IC remains in BM as long as $V_{FBCTRL} \leq 2.8$ V. Requesting more output power results in $V_{FBCTRL} > V_{th(burst)exit}$ (2.8 V) and the IC switches to FR mode. Figure 16 shows this behavior.

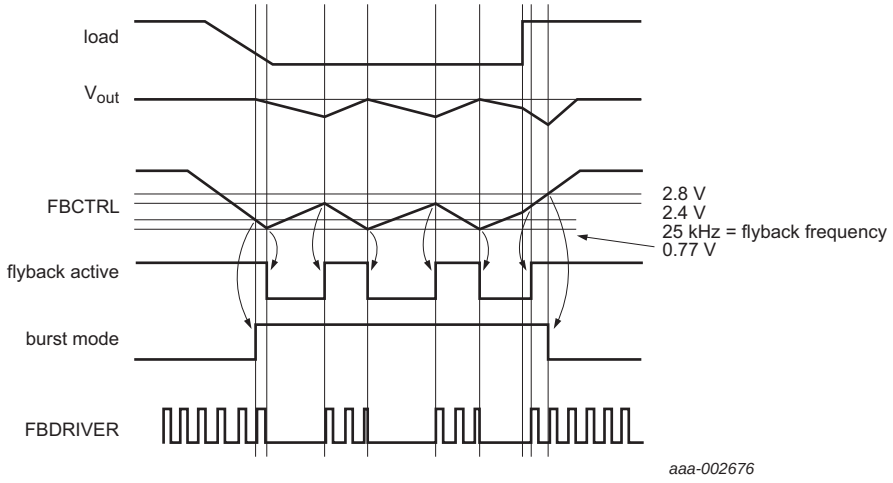


Fig 16. TEA1755 in burst mode

5.1.1.5 V_{CC} undervoltage protection during burst mode

The duty cycle and repetition frequency during BM are both very low when the flyback output power is close to no-load. This low output power results in a very low V_{CC} for the IC.

The IC prevents $V_{CC} < V_{th(UVLO)}$. It allows the FDRIVER to switch for a few cycles until V_{CC} has increased its value with 0.8 V ($V_{prot(UVLO)} = V_{th(UVLO)} + 0.8$ V). These cycles have no impact on the output voltage because all the energy is transferred to the auxiliary winding when V_{CC} is just above $V_{th(UVLO)}$.

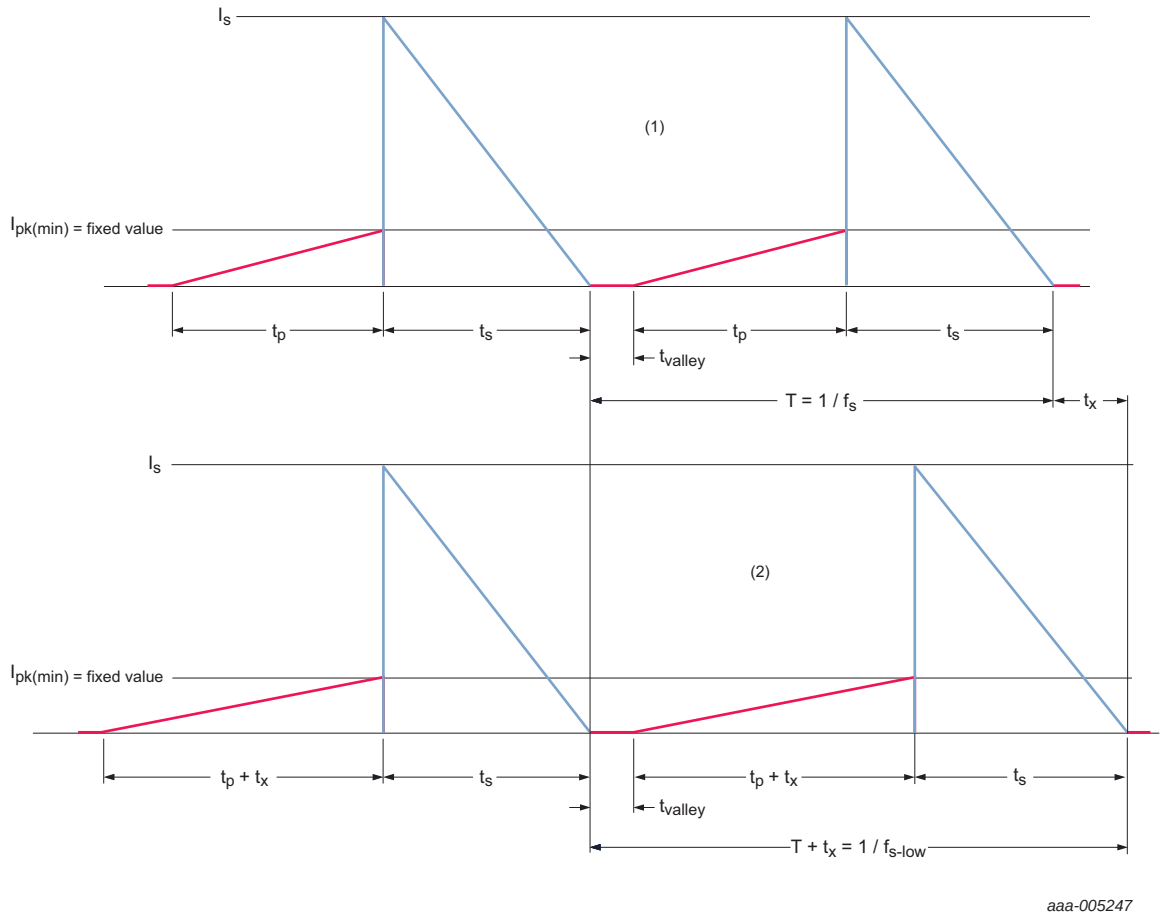
5.1.2 The relationship between inductance value and the PFC hysteresis

The TEA1755 operates at a fixed minimum peak current ($I_{pk(min)}$) to control the output power during the FR mode, see Section 5.1. The value of $I_{pk(min)}$ is calculated using Equation 23.

The MOSFET on-time depends on the selected inductance value and input voltage. The t_{on} is linearly related to the inductance value and inversely proportional to the input voltage. The relationship between the MOSFET t_{on} and t_{off} is fixed based on:

- the transformer turns ratio
- the output voltage excluding the influence of the short valley time

The relatively large inductance results in the flyback running in QR mode at low line voltages although the flyback controller is running in FR mode. This situation is easy to recognize. FBDRIVER is immediately activated at the bottom of the first valley. (Normal operation usually skips valleys during FR mode). Figure 17 shows the operation of a flyback controller at low and lower line voltages.



(1) Flyback controller driven at low line voltages assuming a relatively large primary inductance for the flyback transformer.

(2) Flyback controller driven at very low line voltages assuming a relatively large primary inductance for the flyback transformer.

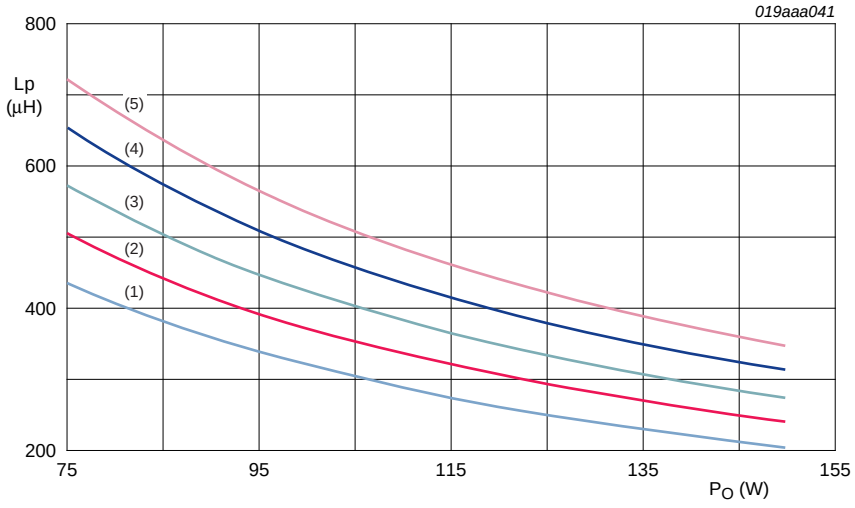
Fig 17. Operating frequency as a function of low line voltages, assuming a relatively large selected primary inductance value for the flyback transformer

Lowering the line voltage results in a lower operating frequency and output power when the selected primary inductance is relatively high.

In practice, the flyback driver supports a limited amount of power at low line voltages. Requesting more power activates the feedback loop and the PFC controller starts up at a lower output power than was originally intended. The hysteresis between PFC switch-on and switch-off becomes smaller therefore at low line voltages. The PFC starts switching when $V_{FBCTRL} \geq V_{en(PFC)FBCTRL}$ = 3.75 V, if the flyback operating frequency cannot reach $f_{sw(fb)swon}$.

Normally, a relatively large primary inductance value is preferred because it minimizes switching losses. However, it must not result in unwanted system behavior at low line voltages because of lost hysteresis. Limiting the maximum inductance value prevents any unwanted system behavior at low line voltages. In addition, a longer valley time makes the hysteresis between PFC switch-on and switch-off even smaller. It is recommended to keep the valley time close to 1.1 μs.

It is helpful to have an indication of the acceptable maximum transformer primary inductance value at the start of the design. Several assumptions are made when calculating these inductance values as shown in Figure 18. Therefore, these values are only for use as indications.



$L_p = f(P_O)$.

Assumptions: Minimum voltage across the buffer capacitor (C3) is approximately 100 V (DC) at 50 % of the nominal output power.

(1) $N \times (V_O + V_f) = 80$ V.

(2) $N \times (V_O + V_f) = 92$ V.

(3) $N \times (V_O + V_f) = 104$ V.

(4) $N \times (V_O + V_f) = 118$ V.

(5) $N \times (V_O + V_f) = 130$ V.

Fig 18. Indication of the maximum primary inductance value, related to output power and $N \times (V_O + V_f)$

Figure 18 shows an indication for the maximum primary flyback inductance value at different output powers and turn ratios.

The following effects are seen for the primary inductance:

- Selecting a higher value results in a reduction of the PFC switch on and switch off hysteresis
- Selecting a lower value results in lower efficiency (related to more overall switching losses)

The inductance values shown in Figure 18 result in the loss of some hysteresis at ≤ 115 V (AC) line voltage. However, the hysteresis is usually still acceptable at 90 V (AC), assuming that the voltage across C3 does not drop under approximately 100 V (DC) at 50 % of the nominal load.

Usually this minimum voltage condition is achieved when C3 in µF is equal to the nominal output power in W as a rule of thumb. The assumption is the minimum line voltage is 90 V RMS / 60 Hz and $P_{PFC(swon)} \leq 0.5 \times P_{nominal}$

The following methods can be used to select the inductance value:

- using Figure 18
- using Equation 20

$$L_p = \left(\frac{N \times (V_O + V_f)}{104.3}\right) \times 43061 \times 10^{-6} \times (I_{O(nom)} \times (V_O + V_f))^{-1.0005} \quad (20)$$

Where:

- $I_{O(nom)}$ stands for the nominal output current according to the type plate of the adapter
- V_O the output voltage
- V_f the forward voltage across the secondary diode
- L_p the flyback transformer primary inductance
- N the turns ratio between the primary and secondary windings (N_p/N_s)

Equation 20 gives some deviation at a low and a high value of the $N \times (V_O + V_f)$ product. It is recommended to keep this value between 80 V and 130 V.

Example:

- $I_{O(nom)}$ = 4.62 A
- V_O = 19.5 V
- V_f = 0.1 V
- $N \times (V_O + V_f)$ = 104.5

$$L_p = \left(\frac{104.5}{104.3}\right) \times 43061 \times 10^{-6} \times (4.62 \times (19.5 + 0.1))^{-1.0005} = 475 \times 10^{-6}\ H \quad (21)$$

The final value used is 450 μH.

5.1.3 Relationship between $I_{pk(min)}$ and the required PFC(swon)/PFC(swoff) level

The PFC is switched on and switched off usually between 50 % and 25 % of the nominal output current of the flyback. The PFC is only switched on or switched off when the flyback controller is running in FR mode. The PFC switches on at a flyback operating frequency of 73 kHz ($f_{sw(fb)swon(PFC)}$) and switches off the PFC at 53 kHz ($f_{sw(fb)swoff(PFC)}$).

The recommended PFC switch off output power is 30.3 % of the typical output-power. The margin between 30.3 % and the 25 % requirement is used for a range of tolerances. Use components with a tolerance values that comply with those given in *in the bill of materials section of UM10514* . Allowing more tolerance for the components requires a larger margin for the recommended output power when a 25 % power requirement is met.Using this information results in Equation 22:

$$0.303 \times I_{O(nom)} \times (V_O + V_f) = \frac{1}{2} \times L_p \times I_{pk(min)}{}^2 \times f_{sw(fb)swoff(PFC)} \times \eta_{fb} \quad (22)$$

or:

$$I_{pk(min)} = \sqrt{\frac{2 \times 0.303 \times I_{O(nom)} \times (V_O + V_f)}{L_p \times f_{sw(fb)swoff(PFC)} \times \eta_{fb}}} \quad (23)$$

Where:

- 0.303 is the recommended multiplying factor related to PFC(swoff)
- V_O is the output voltage
- $I_{O(nom)}$ is the nominal output current according to the type of adapter plate
- V_f is forward voltage across the secondary diode
- L_p is the primary inductances of the flyback transformer
- $f_{sw(fb)swoff(PFC)}$ is 53000
- η_{fb} is the efficiency of the flyback (use relatively high values, such as 0.94 to 0.96)

Example:

- $I_{O(nom)}$ = 4.62 A
- V_O = 19.5 V
- V_f = 0.1 V
- L_p = 450 μH
- η_{fb} = 0.95

$$I_{pk(min)} = \sqrt{\frac{2 \times 0.303 \times 4.62 \times (19.5 + 0.1)}{450 \times 10^{-6} \times 53000 \times 0.95}} = 1.556\ A \quad (24)$$

PFC(swon) is calculated using Equation 25:

$$PFC(swon) = 0.5 \times L_p \times I_{pk(min)}^2 \times f_{sw(fb)swon(PFC)} \times \eta_{fb} \quad (25)$$

Using the data results in:

$$PFC(swon) = 0.5 \times 450 \times 10^{-6} \times 1.556^2 \times 73000 \times 0.95 = 37.8\ W \quad (26)$$

This value can be translated into an output current $I_{out(en)}$, see

$$I_{OUT(en)} = \frac{PFC(swon)}{V_O + V_f} = \frac{37.8}{19.5 + 0.1} = 1.93\ A \quad (27)$$

5.1.4 The influence of R_{sense} and the R16/R17 series resistance

The sense resistor, R_{sense}, together with the series impedance R16 and R17, has four functions:

- prevent or minimize the risk of saturation of the flyback transformer
- allow enough power to the output (assuming the inductance is not going into saturation)
- allow some adjustment for switching on or switching off the PFC at a certain output power level. The value of R_{sense} is more dominant for this adjustment than the value of R16, as its influence is much smaller
- R17 and C23 prevent FBSENSE being charged negative because of disturbances across R_{sense}

The saturation level (I_{sat}) of the transformer and the value of the sense resistor are important design parameters. Section 5.1.4.1 shows the calculation for the transformer saturation level. Next, the maximum peak current ($I_{pk(max)}$) through the transformer is determined. This value is preferably below the transformer saturation level.

5.1.4.1 Calculating the flyback transformer saturation current I_{sat}

The transformer saturation level is calculated using Equation 28.

$$I_{sat} = \frac{N_p \times B_{max} \times A_e}{L_p} \quad (28)$$

Example based on the following assumptions:

- N_p = 32 turns
- B_{max} = 390 mT (PQ3220, material PC44, B_{max} at 100 °C)
- $A_e = 170 \times 10^{-6}$ m^2 (from transformer supplier data sheet)
- $L_p = 450 \times 10^{-6}$

Result: $I_{sat} = \frac{32 \times 0.39 \times 170 \times 10^{-6}}{450 \times 10^{-6}} = 4.715\ A$

Values for A_e and B_{max} are contained in the transformer data sheet. The B_{max} value depends on temperature. It decreases rapidly at high operating temperatures. Therefore, select the B_{max} value at high operating temperatures. Core saturation does not occur when the maximum peak current ($I_{pk(max)}$) is less than the saturation current (I_{sat}). Section 5.1.4.2 shows the calculation of $I_{pk(max)}$. A saturated core deteriorates the overall system performance. It results in more stress, EMI and in the worst case, a possible system failure.

5.1.4.2 Calculation of $I_{pk(max)}$ for flyback operating in Quasi-resonant mode

The flyback peak current in QR mode is calculated using Equation 29:

$$I_{pk(max)} = \frac{-b + \sqrt{(b^2 - 4 \times a \times c)}}{2 \times a} \quad (29)$$

Where:

- $a = N \times V_{i(DC)min} \times L_p$
- $b = -2 \times I_O \times L_p \times \{N \times (V_O + V_f) + V_{i(DC)min}\}$
- $c = -2 \times I_O \times t_{valley} \times N \times V_{i(DC)min} \times (V_O + V_f)$

For a, b and c:

- V_O is the output voltage
- N is the turns ratio between the primary and secondary windings (N_p/N_s)
- V_f is the forward voltage across the secondary diode
- L_p is the inductance value of the primary winding
- t_{valley} is the valley time, sometimes also described as dead-time. This time is usually around the 1.1 μs
- $V_{i(DC)min}$ is the minimum voltage across electrolytic bulk capacitor C3 during a load-step. The customer defines the load step but the maximum value of the load step is limited to the nominal output power. In this example, $V_{i(DC)min}$ = 75 V (DC). The voltage depends on the load step, the value of the C_{bulk} and when the PFC is switched on during the mains cycle. It is recommended that this value is checked in every application.

Examples:

- $a = 5.3333 \times 75 \times 450 \times 10^{-6} = 180 \times 10^{-3}$
- $b = -2 \times 4.62 \times 450 \times 10^{-6} \times \{5.3333 \times (19.5 + 0.1) + 75\} = -746.499 \times 10^{-3}$
- $c = -2 \times 4.62 \times 1.1 \times 10^{-6} \times 5.3333 \times 75 \times (19.5 + 0.1) = -79.6875 \times 10^{-3}$

$$I_{pk(max)}\ (at\ I_O = 4.62\ A) = \frac{746.50 \times 10^{-3} + \sqrt{(-746.50 \times 10^{-3})^2 - 4 \times 180 \times 10^{-3} \times -79.69 \times 10^{-3}}}{2 \times 180 \times 10^{-3}} = 4.25\ A \quad (30)$$

The calculated peak current is under the 4.71 A saturation level (see Section 5.1.4.1). Allow a margin between the calculated value and the saturation level of the core. For example, the system could still run into a problem during a peak load. Check carefully for these instances in the final design.

Assuming the PFC has been switched on for some time, Equation 31 shows the results using a peak output current of 5.7 A and V_{bulk} = 250 V (DC).

- $a_1 = 5.3333 \times 250 \times 450 \times 10^{-6} = 0.6$
- $b_1 = -2 \times 5.70 \times 450 \times 10^{-6} \times \{5.3333 \times (19.5 + 0.1) + 250\} = -1.8188$
- $c_1 = -2 \times 5.70 \times 1.1 \times 10^{-6} \times 5.3333 \times 250 \times (19.5 + 0.1) = -32.77 \times 10^{-3}$

$$I_{pk(max)}\ (at\ I_O = 5.7\ A) = \frac{1.82 + \sqrt{(-1.82)^2 - 4 \times 0.6 \times -32.77 \times 10^{-3}}}{2 \times 0.6} = 3.05\ A \quad (31)$$

Select the highest $I_{pk(max)}$ value (with I_O = 4.62 A and I_O = 5.7 A). Compare the $I_{pk(max)}$ value with the I_{sat} value. The highest $I_{pk(max)}$ value must be lower than the I_{sat} value.

If so, use the I_{sat} value for I_{pmax} to allow a better maximum output power margin.

5.1.4.3 Calculation of the current sense resistor R_{sense}

The next step is calculating the R_{sense} value, see Equation 32:

$$R_{sense} = \frac{V_{sense(fb)max} - V_{sense(fb)min}}{I_{pk(max)} - I_{pk(min)}} = \frac{0.545 - 0.232}{I_{pk(max)} - I_{pk(min)}} = \frac{0.313}{I_{pk(max)} - I_{pk(min)}} \quad (32)$$

Remark: fill in the highest for $I_{pk(max)}$ level (see Section 5.1.4.2).

Using the saturation current I_{sat} for $I_{pk(max)}$ is often preferred (assuming that $I_{sat} > I_{pk(max)}$) because it allows a higher maximum output power.

Using the highest peak current of all (I_{sat} = 4.715 A, see Section 5.1.2) results in a value for R_{sense} as calculated in Equation 33:

$$R_{sense} = \frac{0.313}{4.715 - 1.556} \approx 0.100\ \Omega \quad (33)$$

5.1.4.4 Calculation of the series resistance R16 and R17

Equation 34 calculates the series resistance of R16 and R17:

$$R_{SERIES} = \frac{I_{pk(max)} \times V_{sense(fb)min} - I_{pk(min)} \times V_{sense(fb)max}}{I_{adj(FBSENSE)} \times (I_{pk(max)} - I_{pk(min)})} = \frac{I_{pk(max)} \times 0.232 - I_{pk(min)} \times 0.545}{2.1 \times 10^{-6} \times (I_{pk(max)} - I_{pk(min)})} \quad (34)$$

A typical 90 W adapter example:

$$R_{SERIES} = \frac{4.715 \times 0.232 - 1.556 \times 0.545}{2.1 \times 10^{-6} \times (4.715 - 1.556)} = 37.1\ k\Omega \quad (35)$$

The value of R17 is often roughly between 680 Ω and 1.2 kΩ. Its purpose is to prevent C10 being charged in an unwanted way because of spikes across R_{sense} which can trigger the internal ESD protection. Selecting a value between these two limits allows some freedom for trimming R16 or the delay compensation resistor R16A. When the R17 value is chosen as 1000 Ω then the R16 value = 37100 Ω − 1000 Ω = 36100 Ω.

5.1.5 Calculation of the delay compensation resistors R_{comp} and R16A

R_{comp} and R16A are intended to compensate the sum of the following three delays:

- the internal delay time of the IC
- the switch off time of the MOSFET
- the delay time related to R17 × C23 (filter in front of the FBSENSE pin)

The transformer still conducts current on the primary side during the sum of all these delay times. These delay times are translated into an extra current I_{DELAY} through the transformer (see Figure 19) which results in extra output energy. The amount of extra energy depends on the input voltage.

The current flows through two resistors placed in series, R5 and R5A. The combined resistance of R5 and R5A resistors is called R_{comp}. It is recommended to select $R_{comp} \leq 13.6\ M\Omega$.

R_{comp} is calculated using Equation 36:

$$R_{comp} = R5 + R5A \tag{36}$$

Resistors R_{comp} and R16A compensate for the unwanted current (I_{DELAY}) using a corresponding delay time.

The voltage across R16A is translated to the current I_{PRESET} with the corresponding preset time. When the preset values cancel the delay values, the system is compensated.

The voltage across resistor R16A depends on the current passing through it.

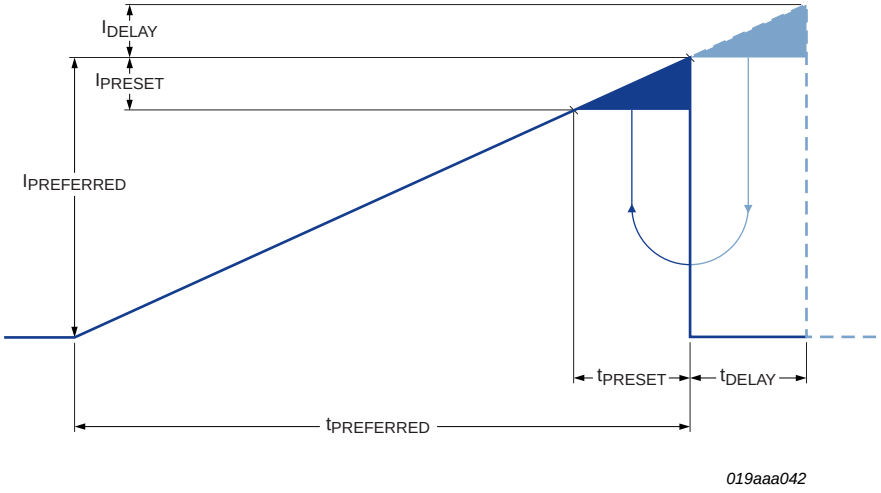


Fig 19. Principle of delay compensation

An example calculation for a typical 90 W adapter: $R_{comp} = 6.8 + 6.8 = 13.6\ M\Omega$

The IC internal delay time, MOSFET switch off response time and the R17 × C23 time constant determine the final delay time. A minimum RC time is required to filter out disturbances on the FBSENSE pin.

An RC time selection that is too large cannot follow the input voltage ramp-up properly. All other delays are subtracted first from the flyback MOSFET conducting time. The remaining time must be at least 5.5 times the minimum RC time required for filtering out interference on the FBSENSE pin.

$t_{d(FBDRIVER)}$ defines the internal delay of the TEA1755 at 80 ns. Switching off the MOSFET usually takes around 60 ns.

Remark: Check the time for switching off the MOSFET ($t_{d(MOSFET)off}$) in the final application because using different MOSFETs and gate resistors can change its duration.

The conduction time of the flyback MOSFET is shortest when the input voltage is at its highest. The highest value is usually 390 V (DC). Equation 37 shows the calculation for R17 × C23:

$$R17 \times C23 \leq \frac{\frac{L_p \times I_{pk(min)}}{390 \times 10^{-9}} - t_{d(FBDRIVER)} - t_{d(MOSFET)off}}{5.5} \quad (37)$$

An example calculation for a typical 90 W adapter:

$$R17 \times C23 \leq \frac{\frac{450 \times 10^{-6} \times 1.556}{390 \times 10^{-9}} - 80 - 60}{5.5} \leq 301\ ns \quad (38)$$

A commonly used RC time for this filter is 220 ns using 1 kΩ for R17 and 220 pF for C23. The RC time value is used in the subsequent equations. The tolerance of capacitor C23 is ≤ 10 %.

Using a maximum tolerance of 10 % for C23 limits the impact on the overall spreading for the PFC(swon) on and PFC(swoff) level.

The output follows the input with a delay of just one RC time after roughly five RC times. The total delay time is calculated using Equation 39:

$$t_d = t_{d(int)} + t_{d(MOSFET)off} + R17 \times C23 \quad (39)$$

An example for a typical 90 W adapter:

$$t_d = 80 \times 10^{-9} + 60 \times 10^{-9} + 1 \times 10^{3} \times 220 \times 10^{-12} = 360\ ns \quad (40)$$

The R16A value is calculated using Equation 41:

$$R16A = \left(\frac{1}{(1 + 8.4 \times 10^{-9} \times R_{comp})}\right) \times \left(\frac{R_{sense} \times R_{COMP} \times t_d}{L_p}\right) \quad (41)$$

An example for a typical 90 W adapter:

$$R16A = \left(\frac{1}{(1 + 8.4 \times 10^{-9} \times R_{comp})}\right) \times \left(\frac{0.100 \times 13.6 \times 10^{6} \times 360 \times 10^{-9}}{450 \times 10^{-6}}\right) = 976\ \Omega \quad (42)$$

5.1.6 Calculation of the flyback soft-start components

Soft-start is implemented using the RC network connected to the FBSENSE pin.

The sum of R16, R16A and R17 must be > 15 kΩ to ensure $V_{start(soft)fb}$ (0.55 V) is reached and flyback start-up is enabled. See the *TEA1755T and TEA1755LT data sheets* (Ref. 1/Ref. 2).

In general, the R16A and R17 values are much smaller than the value of R16. Therefore, the soft-start time is: $\tau_{soft-start} \approx 3 \times R16 \times C10$.

Make $t_{soft\text{-}start}$ for flyback longer than for the PFC. Keep $t_{soft\text{-}start}$ in the range of 5 ms to 10 ms. When C10 = 68 nF and R16 = 36 kΩ, the total $t_{soft\text{-}start}$ is approximately 7 ms.

5.2 Two PFCTIMER pin options

The PFCTIMER pin can be used to extend the PFC operating time when the output power drops below the PFC switch off level. This option prevents the PFC from constantly switching on and off because of fast, large dynamic load changes at the output. Preventing this results in reduced audible noise. This option is further described in Section 5.2.1.

Another option for the PFCTIMER pin is overriding the PFC switch-on (PFC(swon)) and switch off (PFC(swoff)) functionality. Refer to Section 5.2.2 for more information about this subject.

5.2.1 Option 1: adjustable PFC(swoff) time

A capacitor connected to an internal current source determines the adjustable PFC(swoff) time. Capacitor C24 charges from 0 V to 3 V during this adjustable time, the PFC typically switches off using a soft-stop when $V_{PFCTIMER}$ > 3 V. Equation 43 shows how this time is calculated.

$$t_{d(PFC)swoff} = C24 \times \left(\frac{V_{stop(PCFTIMER)}}{I_{source(PFCTIMER)}}\right) = \frac{C24 \times 3\ V}{4.7\ \mu A} \quad (43)$$

Example: a capacitance of 1.5 µF for C24 results in a 0.96 s delay approximately. Typically, after the PFC is switched off, C24 is charged to 3.8 V.

Remark: Always connect a capacitor with a minimum value of 1 nF to the PFCTIMER pin.

Table 5 shows the behavior and conditions of the PFCTIMER pin when it is not overridden by an external source.

Table 5. PFCTIMER adjustable PFC disable time

Typical status without overriding signal[1]	PFC(swon)	PFC(swoff)
Activation signal	$f_{sw(fb)} \geq$ 73 kHz or $V_{FBCTRL} \geq$ 3.75 V	$f_{sw(fb)} \leq$ 53 kHz and $V_{PFCTIMER} \geq$ 3 V
Activation delay	no delay	adjustable
Z_o or $I_{source(PFCTIMER)}$	resistor impedance = 5.3 kΩ	$I_{source(PFCTIMER)}$ = −4.7 µA
Condition	0 < $V_{PFCTIMER}$ < 3 V	3 < $V_{PFCTIMER}$ < 3.8 V

[1] The PFC can only be switched on or switched off when the flyback is running in FR mode.

Capacitor $C_{PFCTIMER}$ discharges when the PFC switches on.

An operating PFC continues switching when P_o drops within the range of $P_{o(PFC)swon}$ (see Figure 20). An output power below the PFC off level for a short time results in charging of capacitor $C_{PFCTIMER}$. However, $C_{PFCTIMER}$ immediately discharges when the output power is back in the $P_{o(PFC)swon}/P_{o(PFC)swoff}$ range if the PFCTIMER voltage was still under 3 V.

The PFCDRIVER signal operates continuously during these load changes at the output (see Figure 20).

Applying less power than $P_{o(PFC)swoff}$ during a time that allows $V_{PFCTIMER}$ to rise above the 3 V causes the PFC to switch off.

The PFC switches on immediately when $P_o > P_{o(PFC)swon}$ and the $C_{PFCTIMER}$ is discharged.

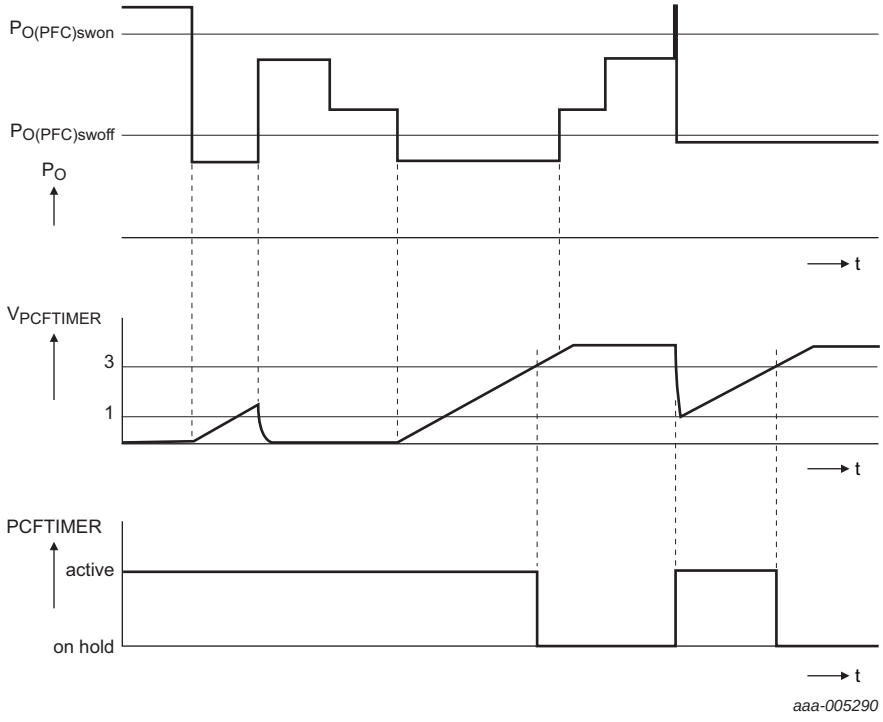


Fig 20. Control of the PFCTIMER pin when PFC is not overridden

5.2.2 Option 2: Overriding the PFC(swon) and PFC(swoff) functions

The PFC in the TEA1755 is typically switched on or switched off using the filtered flyback operating frequency. However, the PFCTIMER allows overriding of this functionality, if necessary (see Table 5). The conditions for overriding the PFC are as follows:

- the disabled PFC is overridden (PFC(swon)) when $V_{PFCTIMER} \leq 1.0$ V but $V_{PFCTIMER} > 1$ V immediately switches off the PFC again.
- the enabled PFC is overridden (PFC(swoff)) when $V_{PFCTIMER} \geq 4.4$ V but $V_{PFCTIMER} < 4.4$ V switches on PFC again.

The TEA1755 does not allow overriding of the PFC during flyback burst mode. All other flyback operation modes enable overriding of the PFC(swon) and PFC(swoff) functionality.

The recommended $C_{PFCTIMER}$ capacitor value is 1 nF. The recommended capacitance value results in the shortest PFCTIMER pin response time to an external signal. Correct timing is important if an external signal is used to override the PFC, especially when switching on the PFC.

Keep $V_{PFCTIMER}$ close to the 4.4 V ($V_{th(off)PFCTIMER}$) when the PFC is switched off. This action minimizes the external driver current required to override the PFC. In addition, together with the small PFCTIMER capacitance, it allows the fastest response on the external PFC switch on signal.

Table 6 shows the behavior and required conditions of the PFCTIMER pin when it is overridden by an external source.

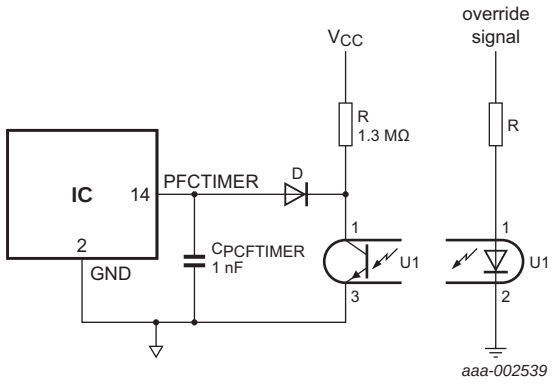
Table 6. PFCTIMER behavior and required conditions when overridden by an external source

Typical status	Override signal state change	$V_{PFCTIMER}$	Time delay ($t_{d(PFCTIMER)}$)	Override trigger ($I_{th(PFCTIMER)}$)	Condition
PFC(swoff)	PFC(swoff)	≥ 4.4 V	none		1 V ≤ $V_{PFCTIMER}$ ≤ 10 V ⇒ PFC state is not changing
	PFC(swon)	≤ 1 V	minimize any delay	$I_{th(PFCTIMER)}$ >> +4.7 μA	0 V ≤ $V_{PFCTIMER}$ ≤ 1 V but $V_{PFCTIMER} > 1$ V ⇒ PFC(swoff); use $V_{PFCTIMER(max)} \approx 4.4$ V[1] and $C_{PFCTIMER} = 1$ nF
PFC(swon)	PFC(swoff)	≥ 4.4 V	possible negligible delay	resistor impedance 5.3 kΩ so $I_{th(PFCTIMER)} = V_{PFCTIMER} / 5.3$ kΩ	4.4 V ≤ $V_{PFCTIMER}$ ≤ 10 V but $V_{PFCTIMER} < 4.4$ V ⇒ PFC(swon); use $V_{PFCTIMER(max)} \approx 4.4$ V[2] and $C_{PFCTIMER} = 1$ nF
	PFC(swon)	≤ 1 V	none		0 V ≤ $V_{PFCTIMER}$ ≤ 3 V ⇒ PFC state is not changing

[1] $V_{PFCTIMER}$ refers to the recommended value before overriding to allow the fast PFC(swon).

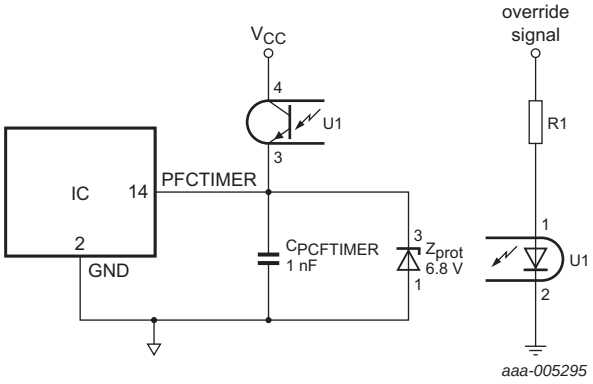
[2] $V_{PFCTIMER}$ refers to the recommended value when overridden to allow the lowest required external sourcing current.

Two circuit solutions for overriding the PFC(swon) and PFC(swoff) functionality are shown in Figure 21 and Figure 22. The optocoupler transistor operates as a current source. The constant current through the optocoupler diode determines the transistor current setting. The figure notes describe the condition the circuit overrides. All solutions can handle optocoupler dark-current up to 10 μA.



Override a switched off PFC by pulling down $V_{PFCTIMER}$.

Fig 21. Switching on the PFC by overriding its switch off mode



Z_{prot} protects the PFCTIMER pin when the PFC is not switched off by the external override signal.

Fig 22. Switching off the PFC by overriding its switch-on mode

5.3 Flyback protection mode

5.3.1 Short-circuit on the FBCTRL pin

If the FBCTRL pin is shorted to ground, switching of the flyback controller is inhibited.

5.3.2 Open FBCTRL pin

As shown in Figure 23, the FBCTRL pin is connected to an internal 7 V voltage source via an internal 13.2 kΩ resistor. When the voltage on the FBCTRL pin exceeds 5.5 V, this connection is disabled. The FBCTRL pin is biased with an internal 29 μA current source. When the voltage on the FBCTRL pin > $V_{to(FBCTRL)}$ (7.7 V), a fault is assumed. Flyback and PFC switching is blocked and the controller:

- TEA1755T: enters the safe restart mode
- TEA1755LT: triggers the latched protection

An internal switch pulls the FBCTRL pin down when the controller is blocked.

5.3.3 Time-out flyback control loop

A time-out function can be created to protect against an output short-circuit at initial start-up or against an open control loop situation. This feature is made when a resistor is mounted in series with a capacitor between the FBCTRL pin and ground. Triggering the time-out protection generates:

- TEA1755T: a safe restart
- TEA1755LT: a latched protection

When the voltage on the FBCTRL pin > 5.5 V (see Figure 23), the switch in series with the 13.2 kΩ resistor is opened. The FBCTRL pin and therefore the RC combination is biased with a 29 μA current source ($I_{to(FBCTRL)}$).

When the voltage on the FBCTRL pin > 7.75 V, flyback and PFC switching is blocked and the controller enters the relevant protection mode. The resistor and capacitor are both used to set the time delay required to reach 7.75 V on the FBCTRL pin. The resistor is also necessary to separate the relatively large time-out capacitor from the control loop response. Use a resistor value ≥ 30 kΩ.

The time-out time t_{to} is calculated using Equation 44:

$$t_{to} = -R \times C \times In\left(\frac{I_{to(FBCTRL)} \times R}{V_{to(FBCTRL)enable}}\right) + C \times \frac{d_{Vto(FBCTRL)}}{I_{to(FBCTRL)}} \quad (44)$$

Remark: $d_{vto(FBCTRL)}$ value 2.25 V in Equation 44 is related to $V_{to(FBCTRL)}$, it is the trip value minus enable value: 7.75 V − 5.5 V = 2.25 V.

An example based on the following assumptions:

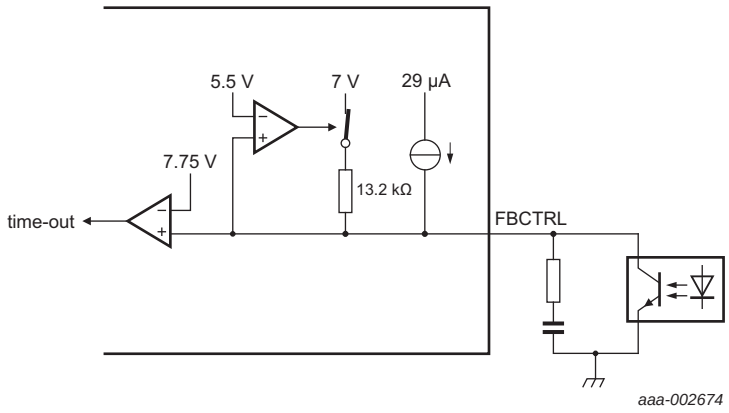
- R24 = 39 kΩ
- C16 = 330 nF

$$t_{to} = -39 \times 10^{3} \times 330 \times 10^{-9} \times In\left(\frac{29 \times 10^{-6} \times 39 \times 10^{3}}{5.5}\right) + 330 \times 10^{-9} \times \frac{2.25}{29 \times 10^{-6}} \quad (45)$$

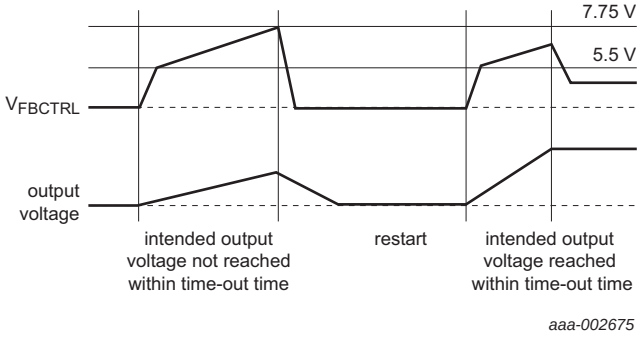
If time-out protection is not required, it is disabled by placing a resistor of 180 kΩ between the FBCTRL pin and ground.

The result of Equation 45 is:

$$t_{to} = 20.4\ ms + 25.6\ ms = 46\ ms \quad (46)$$



a. Circuit diagram



b. Timing diagram

Fig 23. Time-out protection

5.3.4 Overvoltage protection flyback

The IC has an internal latched overvoltage protection circuit which switches off both controllers when an overvoltage is detected at the output of the flyback. The IC detects overvoltage on the flyback transformer secondary winding during the secondary stroke by measuring the voltage on the auxiliary winding.

A series resistor between the auxiliary winding and the FBAUX pin converts this voltage to a current through the FBAUX pin.

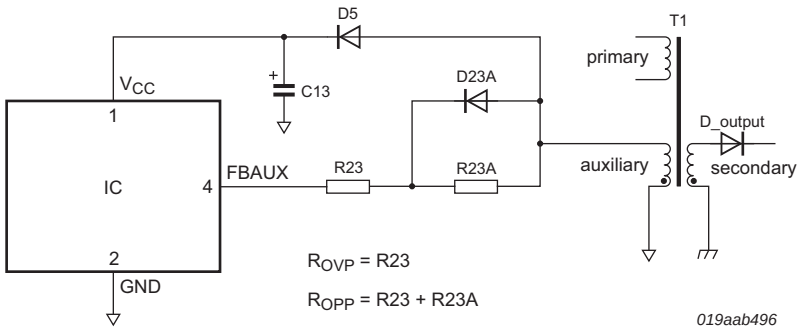


Fig 24. Flyback OVP and OPP circuit

When a 300 μA current $I_{ovp(FBAUX)}$ is applied to the FBAUX pin, the IC detects an overvoltage. An internal integrator filters noise and voltage spikes. The output of the integrator is used as an input for a counter. The counter has been added as an extra filter to prevent false OVP detection which can occur during ESD or lightning events.

If the integrator detects an overvoltage, the counter increases its value by one. If another overvoltage is detected during the next switching cycle, the counter increases its value by one again. If no overvoltage is detected during the next switching cycle, the counter subtracts its value by two. (The minimum value is zero.) If the value reaches six, the IC assumes a true overvoltage and activates the latched protection. Both converters are switched off immediately and V_{CC} starts cycling between $V_{th(UVLO)}$ and $V_{startup}$ without a restart.

Switching off the mains input voltage and then switching on again, triggers the fast-latch reset circuit and resets the latch.

Resistor R_{ovp} sets the OVP level:

$$R_{ovp} = \frac{\left(\frac{N_{aux}}{N_s}\right) \times (V_O + V_f) - V_{clamp(FBAUX)} - V_{f(D23A)}}{I_{ovp(FBAUX)}} = \frac{\left(\frac{N_{aux}}{N_s}\right) \times (V_O + V_f) - 0.92 - V_{f(D23A)}}{300\ \mu A} \quad (47)$$

Where:

- N_s is the number of turns on the secondary winding.
- N_{aux} is the number of turns on the flyback transformer auxiliary winding.
- $V_{clamp(FBAUX)}$ is the FBAUX pin positive clamp voltage.
- $V_{f(D23A)}$ is the forward voltage of D23A at a current of 300 μA.
- V_O is the output voltage
- V_f is the forward voltage across the secondary diode

Take the tolerances on $I_{ovp(FBAUX)}$ into account for the $V_{ovp(VOSENSE)}$ level calculation to avoid OVP triggering during normal operation.

5.3.5 OverPower Protection (OPP)

The maximum power that the flyback can support depends on its input voltage. A higher input voltage allows more output power which can result in more stress during fault conditions. The OPP circuit is implemented to limit the output power to a predefined value at higher input voltages. Triggering the OPP circuit results in activation of the time-out protection (see Section 5.3.3 for more information).

The design of the circuit starts with calculating the required flyback input voltage that matches the predefined OPP level. Equation 48 shows the calculation

$$V_{bulk(opp)min} = \frac{2 \times L_p \times I_{sat} \times \frac{P_{opp}}{\eta_{fb}}}{N \times L_p \times I_{sat}^2 - \frac{2 \times L_p \times I_{sat}}{(V_O + V_f)} \times \frac{P_{opp}}{\eta_{fb}} - 2 \times N \times t_{valley} \times \frac{P_{opp}}{\eta_{fb}}} \quad (48)$$

Where:

- N is the turn ratio between primary turns and secondary windings of the flyback transformer
- L_p is the primary inductances of the flyback transformer
- I_{sat} is the calculated maximum peak current
- V_O is the output voltage of the flyback
- V_f is forward voltage across the secondary diode (or conducting MOSFET)
- P_{opp} is the requested maximum output power of the flyback
- t_{valley} is the measured valley time
- η_{fb} is the efficiency of the flyback. Use relatively high values, such as 0.94 to 0.96

The example is based on the following assumptions:

- N = 5.3333 (see Section 5.1.4.2)
- I_{sat} = 4.715 A (see Section 5.1.4.1)
- V_O = 19.5 V (see Section 5.1.2)
- V_f = 0.1 V (see Section 5.1.2)
- P_{opp} = 131.3 W; the assumed and preferred OPP level of the flyback
- t_{valley} = 1.1 µs (see Section 5.1.4.2)
- η_{fb} = 0.95 (see Section 5.1.3)

Using these values in Equation 46 results in: $V_{bulk(opp)min}$ = 143.4 V (DC).

The preferred OPP output power level is almost independent of the line voltage when $V_{bulk(opp)min} < V_{bulk(PCF)low}$. Refer to Section 4.1.1 for more information about $V_{bulk(PCF)low}$. Keep a margin of 50 V between $V_{bulk(PCF)low}$ and $V_{bulk(opp)min}$. A transformer running very close to saturation has a negative effect on the tolerance of the OPP circuit. Using at least a margin of 50 V minimizes this effect.

During the flyback primary stroke, the input voltage is sensed by measuring the current drawn from the FBAUX pin. A resistor, placed between the flyback transformer auxiliary winding and the FBAUX pin, converts the voltage to the current I_{FBAUX}. The IC uses the current information to reduce the setting of the maximum flyback peak current measured through the FBSENSE pin.

See Figure 24 for the limitation of the maximum $V_{FBSENSE}$ level as a function of I_{FBAUX}.

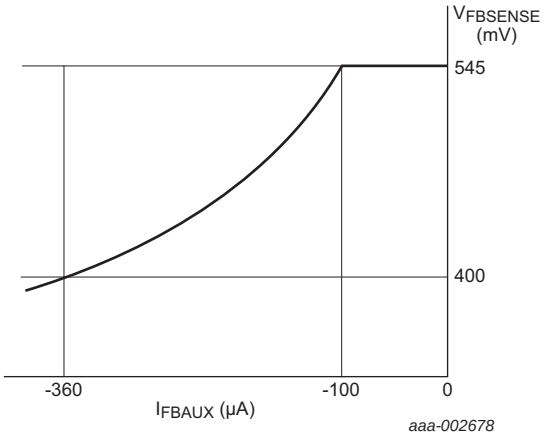


Fig 25. OPP maximum FBSENSE voltage

The total OPP resistance (R23 + R23A) determines the I_{FBAUX} current during the flyback primary stroke (see Figure 25). The OVP resistor R23 has to be calculated before the remaining part of the OPP resistor R23A can be calculated.

The value of R23A is calculated using Equation 49:

$$R23A = \frac{\frac{N_{aux} \cdot V_{bulk(opp)min}}{N_p} - V_{clamp(FBAUX)}}{I_{start(opp)FBAUX}} - R_{ovp} = \frac{\frac{N_{aux} \cdot V_{bulk(opp)min}}{N_p} - 0.7}{100 \times 10^{-6}} - R_{ovp} \quad (49)$$

Calculation example based on the following assumptions:

- N_{aux} = 7 turns
- N_p = 32 turns
- $V_{clamp(FBAUX)}$ is the FBAUX pin negative clamp voltage.
- $V_{bulk(opp)min}$ = 143.4 V(DC)

$$R23A = \frac{\frac{7 \cdot 143.3}{32} - 0.7}{100 \times 10^{-6}} - R_{ovp} = 306 \times 10^{3} - R_{ovp} \quad (50)$$

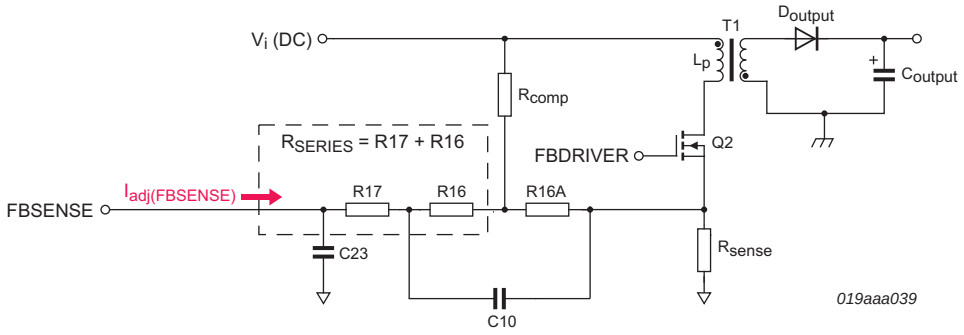
The OPP resistance (R_{opp}) is limited by Equation 51.

$$R_{opp} \leq \frac{V_{th(comp)FBAUX\_MIN}}{I_{prot(FBAUX)\_MAX}} = \frac{60\ mV}{65\ nA} = 923\ k\Omega \quad (51)$$

It is recommended to keep a margin to this maximum resistor value. The recommended maximum value for $R_{opp} \leq 650\ k\Omega$. Larger resistor values can result in a slower output voltage rise during initial start-up which can trigger the time-out protection (See Section 5.3.3).

6. Summary of calculations for flyback adjustment

See Figure 1 application schematic for component reference numbers.

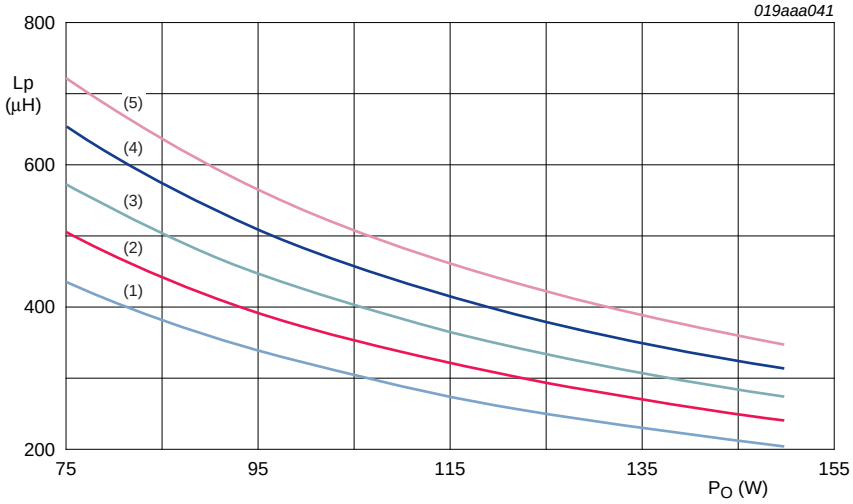


FBSENSE has two internal reference levels:

(1) $V_{start(soft)fb}$ = 545 mV at dV/dt = 0 mV/µs

(2) $V_{sense(fb)min}$ = 232 mV at dV/dt 0 mV/µs

a. Most important components for adjusting the flyback in the application



L_p as a function of P_O

Assumptions: Minimum voltage across C_{bulk} (C3) is approximately 100 V (DC) at 50 % of the nominal output power.

(1) $N \times (V_O + V_f)$ = 80 V

(2) $N \times (V_O + V_f)$ = 92 V

(3) $N \times (V_O + V_f)$ = 104 V

(4) $N \times (V_O + V_f)$ = 118 V

(5) $N \times (V_O + V_f)$ = 130 V

b. Indication of the maximum inductance value, related to output power and $N \times (V_O + V_f)$

Fig 26. Most important components and maximum inductance value for adjusting the flyback in the application

Step 1: Use the graph in Figure 26 to determine an indication for the maximum primary inductance value or use Equation 52:

$$L_p = \left(\frac{N \times (V_O + V_f)}{104.3}\right) \times 43061 \times 10^{-6} \times (I_{O(nom)} \times (V_O + V_f))^{-1.0005} \quad (52)$$

Step 2: Select a transformer and calculate the saturation current:

$$I_{sat} = \frac{N_p \times B_{max} \times A_e}{L_p} \quad (53)$$

Step 3: Calculate the required peak current through the flyback transformer. Calculate this value at nominal output power in combination with the minimum V_{bulk} and when the PFC is operating at maximum peak output power. Calculate using both values for $I_{pk(max)}$ but only use the highest value of these two parameters.

A common rule is that $I_{sat} > I_{pk(max)}$. Selecting the higher I_{sat} value for $I_{pk(max)}$ prevents transformer saturation and allows a power margin. In general, the calculation is carried out using $I_{pk(max)} = I_{sat}$.

$$I_{pk(max)} = \frac{-b + \sqrt{(b^2 - 4 \times a \times c)}}{2 \times a} \quad (54)$$

Where:

- $a = N \times V_{i(DC)min} \times L_p$
- $b = -2 \times I_O \times L_p \times \{N \times (V_O + V_f) + V_{i(DC)min}\}$
- $c = -2 \times I_O \times t_{valley} \times N \times V_{i(DC)min} \times (V_O + V_f)$

Step 4: Calculate $I_{pk(min)}$ (related to switching off the PFC):

$$I_{pk(min)} = \sqrt{\frac{2 \times 0.303 \times I_{O(nom)} \times (V_O + V_f)}{L_p \times 53000 \times \eta_{fb}}} \quad (55)$$

η_{fb} is the flyback efficiency. Use a relatively high value, for example, approximately 0.94 to 0.96.

Step 5: Calculate the value of R_{sense}:

$$R_{sense} = \frac{V_{sense(fb)max} - V_{sense(fb)min}}{I_{pk(max)} - I_{pk(min)}} = \frac{0.545 - 0.232}{I_{pk(max)} - I_{pk(min)}} = \frac{0.313}{I_{pk(max)} - I_{pk(min)}} \quad (56)$$

Step 6: Calculate the value of R_{SERIES}:

$$R_{SERIES} = \frac{I_{pk(max)} \times V_{sense(fb)min} - I_{pk(min)} \times V_{sense(fb)max}}{I_{adj(FBSENSE)} \times (I_{pk(max)} - I_{pk(min)})} = \frac{I_{pk(max)} \times 0.232 - I_{pk(min)} \times 0.545}{2.1 \times 10^{-6} \times (I_{pk(max)} - I_{pk(min)})} \quad (57)$$

The R_{SERIES} resistance comprises two components, R16 and R17. The common value for R17 is between 820 Ω and 1.2 kΩ. A typical value that is used often is 1 kΩ.

Step 7: Checking/calculating the R17 × C23 time constant:

$$R17 \times C23\ (ns) \leq \frac{\frac{L_p \times I_{pk(min)}}{390 \times 10^{-9}} - t_{d(int)} - t_{d(MOSFET)off}}{5.5} \quad (58)$$

Where:

- $t_{d(FBDRIVER)}$ = 80 ns
- $t_{d(MOSFET)off} \cong$ 60 ns (The value can be different in other applications. Check on the application board.)

In general, the calculation often shows that R17 × C23 ≥ 220 ns. If so, 220 ns is sufficient for the constant R17 × C23. A smaller value can be acceptable but is not preferred.

Step 8: Calculate the delay time:

$$t_d = t_{d(int)} + t_{d(MOSFET)off} + R17 \times C23 \quad (59)$$

Remark: The commonly used value for R17 × C23 is 220 ns (see step 7).

Step 9: Calculate the compensating resistor R_{comp}:

$$R_{comp} = R5 + R5A \quad (60)$$

Calculate the value of R16A:

$$R16A = \left(\frac{1}{1 + 8.4 \times 10^{-9} \times R_{comp}}\right) \times \left(\frac{R_{sense} \times R_{comp} \times t_d}{L_p}\right) \quad (61)$$

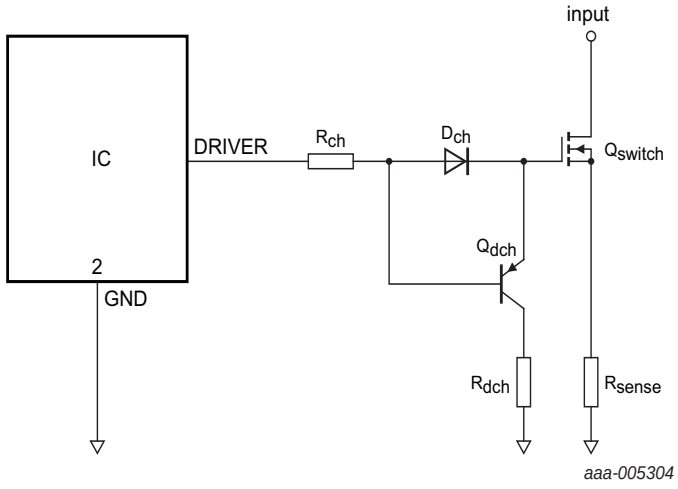
7. PCB layout considerations

A good layout is an important part of the final design. It minimizes many kinds of disturbances and makes the overall performance more robust with less risk of EMI. Guidelines for the improvement of the layout of the PCB are as follows:

- Separate large signal grounds from small signal grounds (see Figure 28). A triangular symbol indicates small signal grounds. All other ground symbols are related to large signal grounds
- Make the print area within the indicated large signal loops (see Figure 28) as small as possible. Each indicated large signal loop has its own color. Make the copper tracks as short and wide as possible
- The connection between both MOSFETs (PFC and flyback) and the IC driver outputs must be as short as possible (green line in Figure 28). Use wide tracks. Increase the distance between the copper tracks and/or preferably using a separate guided ground track for both connections minimizes the coupling between the PFCDRIVER and FBDRIVER. A circuit diagram according to Figure 27 can be added in case it is impossible to locate the MOSFET and IC close to each other.
- The power ground and small signal ground are only connected with one short copper track (make this track as short and as wide as possible). Preferably it should become one spot (connection between ground 4a and ground 6a, shown as a green line in Figure 28)
- Use a ground shield underneath the IC, connect this ground shield to the GND pin of the IC
- Connect all series connected resistors that are fixed to an IC pin as close as possible to that pin
- Connect heatsinks which are connected to the component nearest corresponding ground signal. Make this connection as short as possible. Connect the heatsink of diode bridge BD1 to ground 1, Q1 to 4 and Q2 to 4b. In typical applications, all three components are often mounted on a single heatsink. If so, make one wide copper track that connects all three grounds to each other. Also combine in this copper track ground 2
- Connect the grounds of 6b to each other
- Make a local "star ground" from ground 6a, 6b, 6c, and 7. Ground 6a is the middle of the star and is connected to the GND pin (the ground of the IC)
- Grounds marked 7 do not have to be a star ground
- Place the Y-capacitor across grounds 1 and 8. Use one copper track, separated from all others for this connection. Alternatively in a typical application setup, use the heatsinks connection copper track for this purpose.
- Place C4, C15, C23 and C22 (in order of priority) as close as possible to the IC. Reduce coupling between the PFC switching signals (PFC driver and PFCAUX) and the flyback sense signals (FBSENSE and FBCTRL) as much as possible. The coupling reduction minimizes the risk of electromagnetic interference and audible noise
- Figure 28 shows an overview of the hierarchy of the different grounds at the bottom

- Connect the anode of the TL431 (ground 8) to ground 9 using one special separate connecting copper track. Minimize all other currents in this special track. Make the connection as close as possible to the output
- Place the TEA1792 close to the power MOSFET Q4
- Connect the ground of the TEA1792 directly to a wide and short copper track to the source of Q4
- Connect the series resistor R32 directly between the drain of Q4 and the V_{CC} pin of the IC. Use a separate copper track for this purpose
- Make the connection between MOSFET Q4 and the TEA1792 driver pin as short as possible (green line in Figure 28). Use a guided ground track
- Make the connection between R50 and SWDET of the TEA1703 as short as possible and place the resistor close to the IC

Remark: It is recommended to use the circuit shown in Figure 27 when the distance between the IC drive output and corresponding MOSFET are relatively large.



Transistor is mounted close to the MOSFET with wide and short tracks.

See Section 7for the layout rules.

Fig 27. Switching off the MOSFET when the distance between IC and MOSFET is large

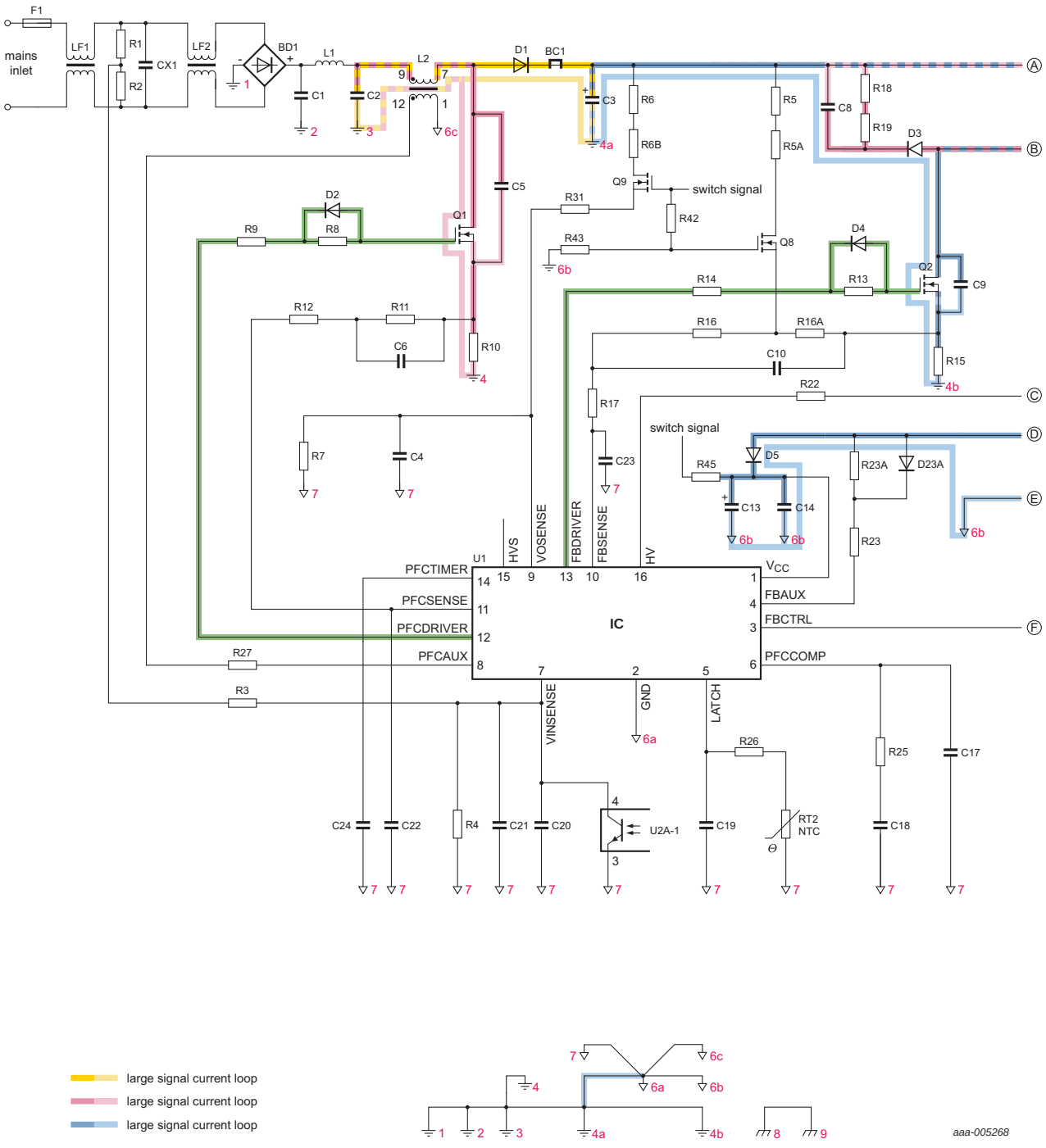


Fig 28. PCB layout considerations (part 1)

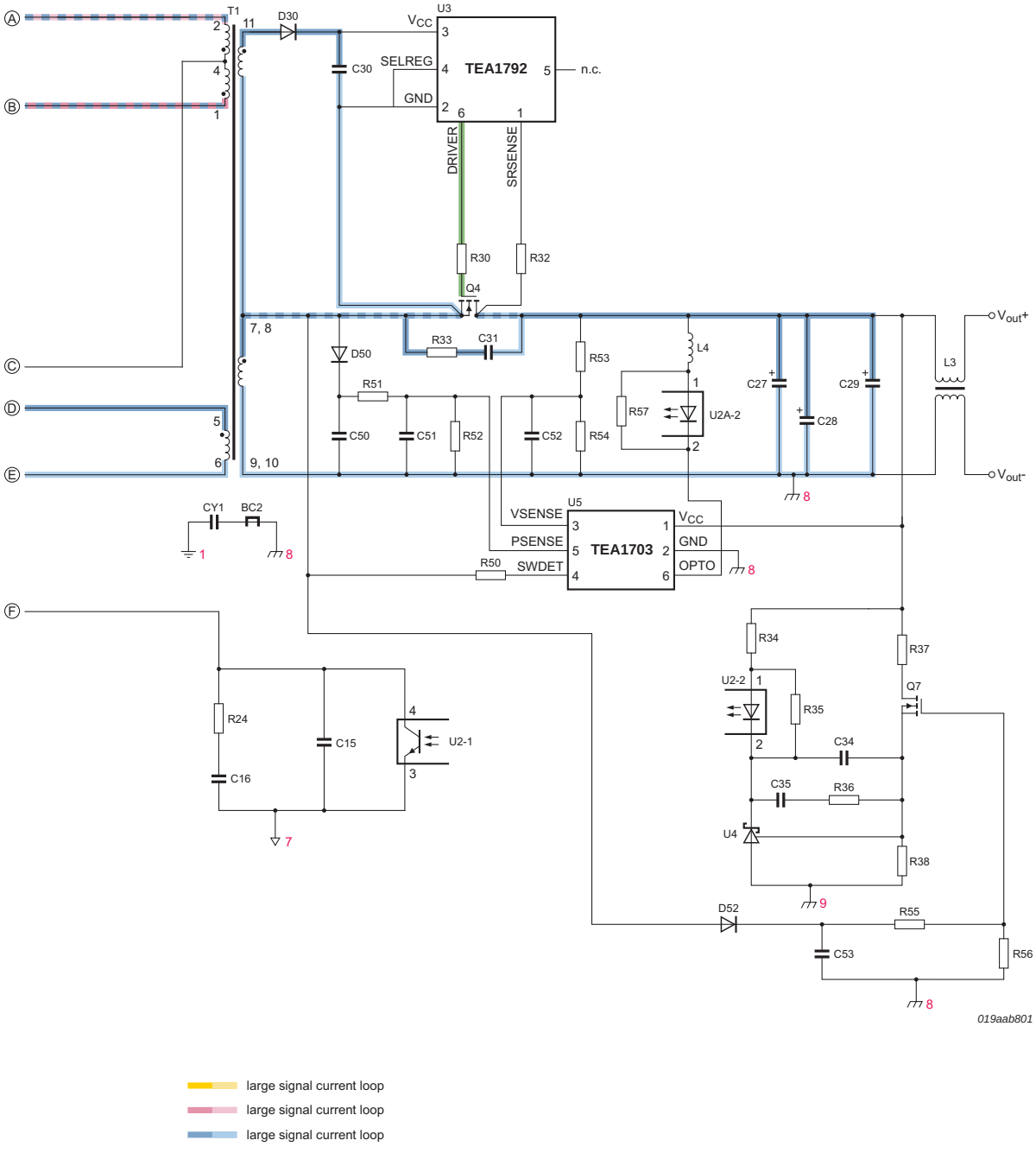


Fig 29. PCB layout considerations (part 2)

8. Abbreviations

Table 7. Abbreviations

Acronym	Description
BM	Burst Mode
DCM	Discontinuous Conduction Mode
EMI	ElectroMagnetic Interference
FR	Frequency Reduction
HV	High Voltage
MHR	Mains Harmonics Reduction
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PFC	Power Factor Converter/Controller/Correction
QR	Quasi-Resonant
SMPS	Switched Mode Power Supply

9. References

[1] **TEA1755T —** HV start-up DCM/QR flyback controller with integrated DCM/QR PFC controller

[2] **TEA1755LT —** HV start-up DCM/QR flyback controller with integrated DCM/QR PFC controller

[3] **UM10514 —** Notebook adaptor using the TEA1755

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11. Contents

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