



TWR-K64F120M Tower Module

User's Guide

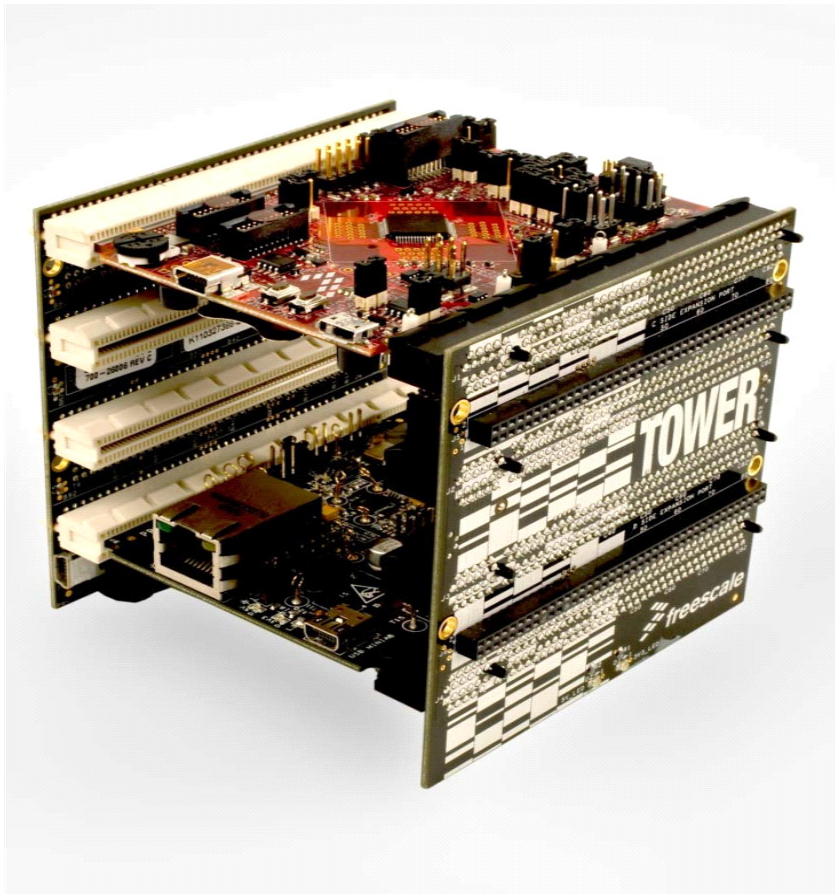
by *Freescale Semiconductor, Inc.*

1 TWR-K64F120M

The TWR-K64F120M microcontroller module is designed to work in either a standalone mode or as part of the Freescale Tower System, a modular development platform that enables rapid prototyping and tool reuse through reconfigurable hardware. Take your design to the next level and begin constructing your Tower System today by visiting www.freescale.com/tower for additional Tower System microcontroller modules and compatible peripherals. For TWR-K64F120M-specific information and updates visit www.freescale.com/TWR-K64F120M.

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2 Contents

The TWR-K64F120M includes:

- TWR-K64F120M for board assembly
- Quick Start Guide
- USB A to mini-B cable for debug interface and power
- CR2032 coin cell battery for VBAT power supply
- USB A to micro-B cable for MK64FN1M0VMD12 USB interface

3 TWR-K64F120M Features

- Tower-compatible microcontroller module
- MK64FN1M0VMD12 MCU (120 MHz, 1024 KB Flash, 256 KB RAM, low power, 144 MAPBGA package)
- Dual-role USB interface with Micro-AB USB connector
- General purpose Tower Plugin (TWRPI) socket

- On-board debug circuit: MK20DX128VM5 open (OpenSDA) with virtual serial port
- Three axis accelerometer (MMA8451Q)
- Four user controllable LEDs
- Two user pushbutton switches for GPIO interrupts
- One user pushbutton switch for MK64FN1M0VMD12 or MK20DX128VFM5 reset
- One Potentiometer
- Independent, battery-operated power supply for Real Time Clock (RTC) and tamper detection modules
- SD card slot

4 Get to know the TWR-K64F120M

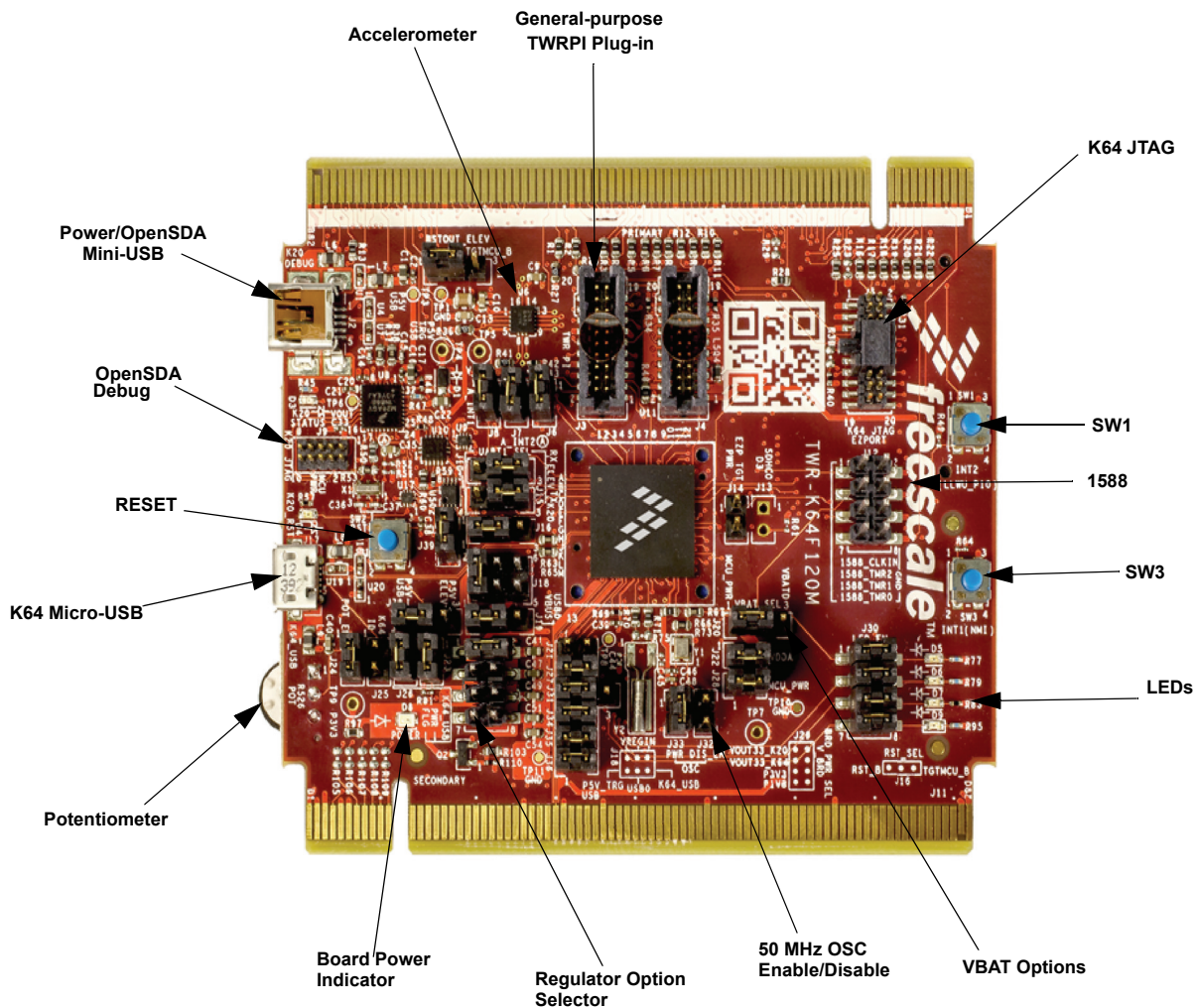


Figure 1. Front side of TWR-K64F120M module (TWRPI devices not shown)

TWR-K64F120M Tower Module, Rev. B

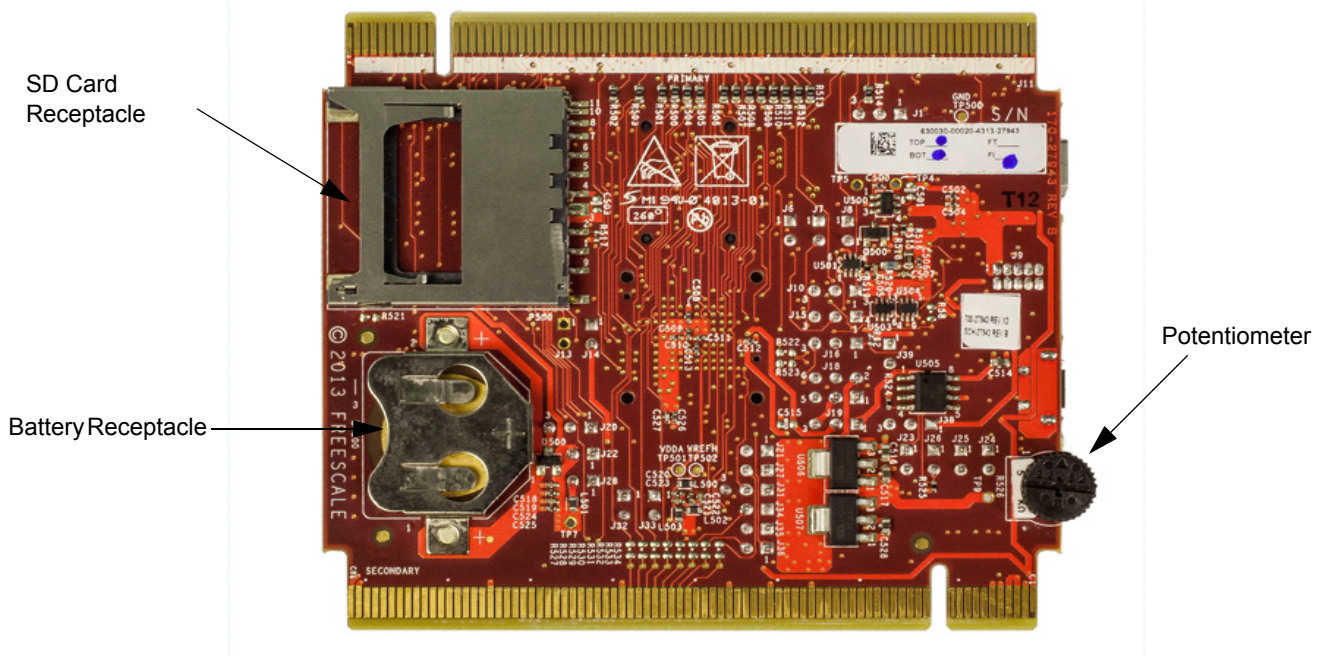


Figure 2. Back side of TWR-K64F120M

5 Reference Documents

The documents listed below should be referenced for more information on the Kinetis family, Tower System, and MCU Modules. These can be found in the documentation section of <http://www.freescale.com/kinetis>

- TWR-K64F120M-SCH: Schematics
- TWR-K64F120M-PWA: Design Package
- K64P144M120SF5RM: Reference Manual
- Tower Configuration Tool
- Tower Mechanical Drawing

6 Hardware description

The TWR-K64F120M is a Tower MCU Module featuring the MK64FN1M0VMD12—a Kinetis microcontroller in a 144 MAPBGA featuring a USB 2.0 full speed on-the-go (OTG) controller, a 10/100 Ethernet MAC with IEEE1588, hardware encryption, and tamper detection coupled with a secure real-time clock on an independent battery supply. It is intended for use in the Freescale Tower System but can also operate alone. The on-board OpenSDA debug circuit provides a Serial Debug interface and a power supply input through a single mini-USB connector.

6.1 Block Diagram

The block diagram of the TWR-K64F120M board is presented in Figure 3:

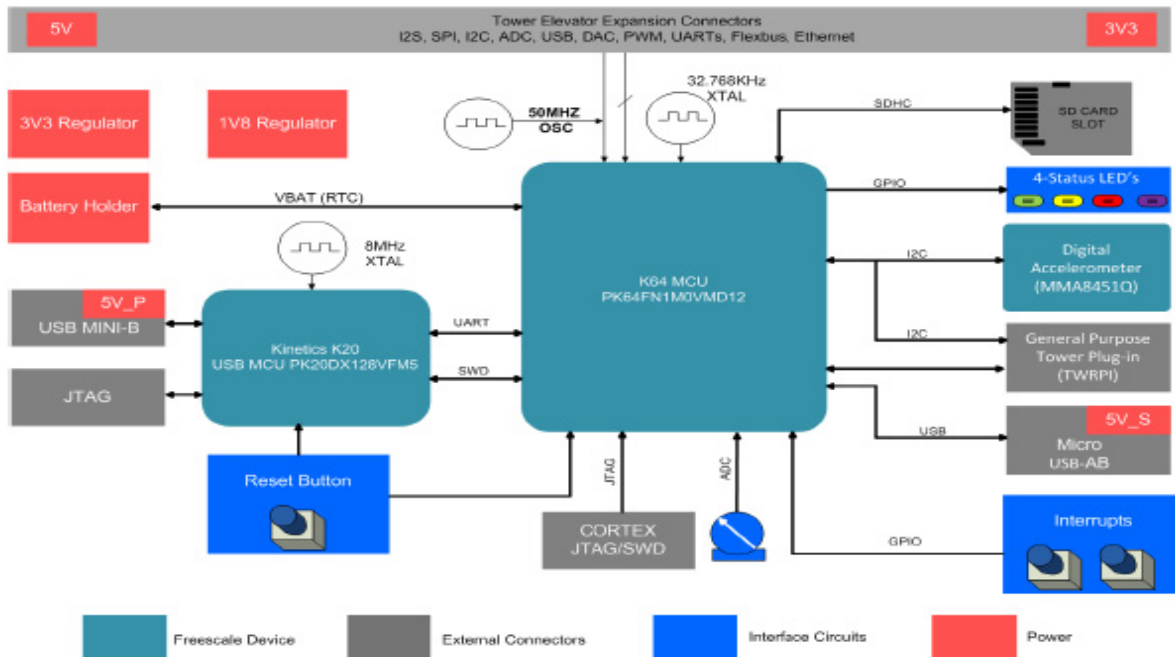


Figure 3. Block diagram

6.2 Microcontroller

The TWR-K64F120M features the MK64FN1M0VMD12 MCU. This 120 MHz microcontroller is part of the Kinetis K6x family and is implemented in a 144 MAPBGA package. The following table notes some of the features of the MK64FN1M0VMD12 MCU.

Table 1. Features of MK64FN1M0VMD12

Feature	Description
Ultra low power	<ul style="list-style-type: none"> – 11 low-power modes with power and clock gating for optimal peripheral activity and recovery times. – Full memory and analog operation down to 1.71 V for extended battery life – Low-leakage wake-up unit with up to six internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes – Low-power timer for continual system operation in reduced power states
Flash and SRAM	<ul style="list-style-type: none"> – 1024KB flash featuring fast access times, high reliability, and four levels of security protection – 256 KB of SRAM – No user or system intervention to complete programming and erase functions and full operation down to 1.71 V

Table 1. Features of MK64FN1M0VMD12

Mixed signal capability	<ul style="list-style-type: none"> – High-speed 16-bit ADC with configurable resolution – Single or differential output modes for improved noise rejection – 500-ns conversion time achievable with programmable delay block triggering – Three high-speed comparators providing fast and accurate motor overcurrent protection by driving PWMs to a safe state – Optional analog voltage reference provides an accurate reference to analog blocks – Two 12-bit DACs
Performance	<ul style="list-style-type: none"> – 120MHz ARM CortexM4 core with DSP instruction set, single cycle MAC, and single instruction multiple data (SIMD) extensions – Up to four channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput – Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth – Independent flash banks allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines
Timing and Control	<ul style="list-style-type: none"> – Four FlexTimers with a total of 12 channels – Hardware dead-time insertion and quadrature decoding for motor control – Carrier modulator timer for infrared waveform generation in remote control applications – Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block – One low power timer – One independent real time clock
Connectivity and Communications	<ul style="list-style-type: none"> – Full-Speed USB Device/Host/On-The-Go with device charge detect capability – Optimized charging current/time for portable USB devices, enabling longer battery life – USB low-voltage regulator supplies up to 120 mA off chip at 3.3 volts to power external components from 5volt input – Six UARTs: One UART supports RS232 with flow control, RS485, and ISO7816 Five UARTs support RS232 with flow control and RS485 – One Inter-IC Sound (I2S) serial interface for audio system interfacing – Three DSPI modules and two I2C modules – One Ethernet module with 1588 – A multi-function external bus interface (FlexBUS) controller capable of interfacing to slave-only devices. – A secured digital host controller (SDHC) – One FlexCAN module
Reliability, Safety and Security	<ul style="list-style-type: none"> – Hardware Encryption co-processor for secure data transfer and storage. Faster than software implementations and with minimal CPU loading. Supports a wide variety of algorithms - DES, 3DES, AES, MD5, SHA-1, SHA-256 – System security and tamper detection with secure real-time clock (RTC) and independent battery supply. Secure key storage with internal/external tamper detection for unsecured flash, temperature, clock, and supply voltage variations and physical attack detection – Memory protection unit provides memory protection for all masters on the cross bar switch, increasing software reliability – Cyclic redundancy check (CRC) engine validates memory contents and communication data, increasing system reliability – Independently-clocked COP guards against clock skew or code runaway for fail-safe applications such as the IEC 60730 safety standard for household appliances – External watchdog monitor drives output pin to safe state for external components in the event that a watchdog timeout occurs – Included in Freescale's product longevity

6.3 Clocking

The Kinetis MCUs start up from an internal digitally-controlled oscillator (DCO). Software can enable the main external oscillator (EXTAL0/XTAL0) if desired. The external oscillator/resonator can range from 32.768 KHz up to a 50 MHz. A 50 MHz Oscillator is the default external source for the MCG oscillator inputs (XTAL/EXTAL).

A 32.768 KHz crystal is connected to the RTC oscillator inputs by default.

By populating isolation resistors, other external clock sources for the MK64FN1M0VMD12 can be used, including the CLKIN0 signal that can be provided by either pin B24 on primary TWR-ELEV or pin 20 of TWRPI connector J3.

6.4 System Power

When installed into a Tower System, the TWR-K64F120M can be powered from either an on-board source or from another source in the assembled Tower System.

In standalone operation, the main power source (5.0 V) for the TWR-K64F120M module is derived from either the OpenSDA USB mini-B connector (J2) or the MK64FN1M0VMD12 USB micro-AB connector (J17). Two low dropout regulators provide 3.3 V and 1.8 V supplies from the 5.0 V input voltage.

Additionally, the 3.3 V regulator built into the MK64FN1M0VMD12 MCU can be selected to power the 3.3 V bus. All the user selectable options can be configured using two headers, J18, J19, and J29. Refer to sheet 4 and 5 of the TWR-K64F120M schematics for more details.

6.5 DryIce and RTC VBAT

The DryIce tamper detection module and the Real Time Clock (RTC) module on the MK64FN1M0VMD12 have two modes of operation: system powerup and system powerdown. During system powerdown, the tamper detection module and the RTC are powered from the backup power supply (VBAT) and electrically isolated from the rest of the MCU. The TWR-K64F120M provides a battery receptacle for a coin cell battery that can be used as the VBAT supply. The receptacle can accept common 20mm diameter 3 V lithium coin cell batteries.

6.6 Debug Interface

There are two debug interface options available: the on-board OpenSDA circuit and an external ARM JTAG connector. The ARM JTAG connector (J5) is a standard 2x10pin connector, with one pin keyed, to allow an external debugger access to the JTAG interface of the MK64FN1M0VMD12. Alternatively, the on-board OpenSDA debug interface can be used to access the debug interface of the MK64FN1M0VMD12.

6.7 OpenSDA

An on-board MK20DX128VFM5 based Open-Standard serial and debug adapter (OpenSDA) circuit provides a JTAG debug interface to the MK64FN1M0VMD12. A standard USB A male to mini-B male cable (provided) can be used for debugging via the USB connector (J2). The OpenSDA interface also provides a USB to serial bridge. Drivers for the OpenSDA interface are provided in the P&E Micro

OpenSDA Tower Toolkit. These drivers and more utilities can be found online at <http://www.pemicro.com/opensda>.

6.8 Cortex Debug Connector

The Cortex Debug connector is a 20pin (0.05") connector providing access to the SWD, JTAG, EzPort signals available on the K64 device. The pinout and K64 pin connections to the debug connector (J5) are shown in the following table.

Table 2. Cortex Debug Connector

Pin	Function	TWR-K64F120M Connection
1	VTref	3.3 V MCU supply (MCU_PWR)
2	TMS / SWDIO	PTA3/JTAG_TMS/SWD_DIO/UART0_RTS/FTM0_CH0
3	GND	Ground
4	TCK / SWCLK	PTA0/JTAG_TCLK/SWD_CLK/EZP_CLK/UART0_CTS/UART0_COL/FTM0_CH5
5	GND	Ground
6	TDO / SWO	PTA2/JTAG_TDO/TRACE_SWO/EZP_DO/UART0_TX/FTM0_CH7
7	Key	—
8	TDI	PTA1/JTAG_TDI/EZP_DI/UART0_RX/FTM0_CH6
9	GND Detect	PTA4/LLWU_P3/NMI/EZP_CS/FTM0_CH1
10	nRESET	RESET_b
11	Target Power	5 V supply (via J14)
12	TRACECLK	PTA6/FTM0_CH3/CLKOUTB/TRACE_CLKOUT
13	Target Power	5 V supply (via J14)
14	TRACEDATA[0]	PTA10/FTM2_CH0/MII0_RXD2/FTM2_QD_PHA/TRACE_D0
15	GND	Ground
16	TRACEDATA[1]	PTA9/FTM1_CH1/MII0_RXD3/FTM1_QD_PHB/TRACE_D1
17	GND	Ground
18	TRACEDATA[2]	PTA8/ADC0_SE11/FTM1_CH0/FTM1_QD_PHA/TRACE_D2
19	GND	Ground
20	TRACEDATA[3]	PTA7/ADC0_SE10/FTM0_CH4/TRACE_D3

6.9 Accelerometer

An MMA8451Q digital accelerometer is connected to the MK64FN1M0VMD12 MCU through an I2C interface (I2C1) and GPIO/IRQ signals (PTA6 and PTA8).

6.10 Potentiometer, Pushbuttons, LEDs

The TWR-K64F120M also features:

- A potentiometer connected to an ADC input signal (ADC1_SE18).
- Two pushbutton switches (SW1 and SW3 connected to PTC6 and PTA4, respectively)
- Four user controllable LEDs connected to GPIO signals (optionally isolated using jumpers):
 - Yellow/Green LED (D5) to PTE6
 - Yellow LED (D6) to PTE7
 - Orange LED (D7) to PTE8
 - Blue LED (D9) to PTE9

6.11 General Purpose Tower Plug-in (TWRPI) Socket

The TWR-K64F120M features a socket (J3 and J4) that can accept a variety of different Tower Plugin modules featuring sensors, RF transceivers, and other peripherals. The General Purpose TWRPI socket provides access to I2C, SPI, IRQs, GPIOs, timers, analog conversion signals, TWRPI ID signals, reset, and voltage supplies. The pinout for the TWRPI Socket is defined in [Table 3](#).

Table 3. General Purpose TWRPI Socket Pinout

J4		J3	
Pin	Description	Pin	Description
1	5 V VCC	1	GND
2	3.3 V VCC	2	GND
3	GND	3	I2C: SCL
4	3.3 V VDDA	4	I2C: SDA
5	VSS (Analog GND)	5	GND
6	VSS (Analog GND)	6	GND
7	VSS (Analog GND)	7	GND
8	ADC: Analog 0	8	GND
9	ADC: Analog 1	9	SPI: MISO
10	VSS (Analog GND)	10	SPI: MOSI
11	VSS (Analog GND)	11	SPI: SS
12	ADC: Analog 2	12	SPI: CLK
13	VSS (Analog GND)	13	GND
14	VSS (Analog GND)	14	GND
15	GND	15	GPIO: GPIO0/IRQ
16	GND	16	GPIO:GPIO1/IRQ
17	ADC: TWRPI ID 0	17	UART: UART_RX or GPIO: GPIO2

Table 3. General Purpose TWRPI Socket Pinout

18	ADC: TWRPI ID 1	18	UART: UART_TX or GPIO: GPIO3
19	GND	19	UART: UART_CTS or GPIO: GPIO4/Timer
20	Reset	20	UART: UART_RTS or GPIO: GPIO5/Timer

6.12 USB

The MK64FN1M0VMD12 features a fullspeed/low-speed USB module with OTG/Host/Device capability and built-in transceiver. The TWR K64F120M routes the USB D+ and D signals from the MK64FN1M0VMD12 MCU directly to the on-board microUSB connector (J17).

A power supply switch with an enable input signal and overcurrent flag output signal is used to supply power to the USB connector when the MK64FN1M0VMD12 is operating in host mode. Port pin PTC8 is connected to the flag output signal and port pin PTC9 is used to drive the enable signal. Both PTC8 and PTC9 port pins can be isolated with jumpers (J23 and J26, respectively) if needed.

6.13 Secure Digital Card Slot

A Secure Digital (SD) card slot is available on the TWR-K64F120M connected to the SD Host Controller (SDHC) signals of the MCU. This slot will accept standard format SD memory cards. See the following table for the SDHC signal connection details.

Table 4. SD Card Socket Connection

Pin	Function	TWR-K64F120M Connection
1	SDHC0_D3	PTE4/LLWU_P2/SPI1_PCS0/UART3_TX/SDHC0_D3/TRACE_D0
2	SDHC0_CMD	PTE3/ADC0_DM2/ADC1_SE7A/SPI1_SIN/UART1_RTS/SDHC0_CMD/TRACE_D1/SPI1_SOUT
3	VSS1	GND
4	VDD	3.3 V Board supply (V_BRD)
5	SDHC0_DCLK	PTE2/LLWU_P1/ADC0_DP2/ADC1_SE6A/SPI1_SCK/UART1_CTS/SDHC0_DCLK/TRACE_D2
6	VSS2	GND
7	SDHC0_D0	PTE1/LLWU_P0/ADC1_SE5A/SPI1_SOUT/UART1_RX/SDHC0_D0/TRACE_D3/I2C1_SCL/SPI1_SIN
8	SDHC0_D1	PTE0/ADC1_SE4A/SPI1_PCS1/UART1_TX/SDHC0_D1/TRACE_CLKOUT/I2C1_SDA/RTC_CLKOUT
9	SDHC0_D2	PTE5/SPI1_PCS2/UART3_RX/SDHC0_D2/FTM3_CH0
10	SD_CARD_DETECT	PTB20/SPI2_PCS0/FB_AD31/CMP0_OUT
11	CD_WP_COMMON	GND
12	SD_CARD_WP	PTB21/SPI2_SCK/FB_AD30/CMP1_OUT

6.14 External Bus Interface – FlexBus

The device features a multi-function external bus interface called Flexbus, which is capable of interfacing to slave-only devices.. The FlexBus interface is not used directly on the TWR-K64F120M. Instead, a subset of the FlexBus signals are connected to the Primary Connector on the TWR-ELEV so that the external bus can access devices on Tower peripheral modules. Refer to sheet 8 of the TWR-K64F120M schematic for more detail.

6.15 Ethernet and 1588

The MK64FN10MVDC12 features a 10/100 Mbps Ethernet MAC with MII and RMII interfaces. The TWR-K64F120M routes MII/RMII interface signals from the K64 MCU to the Primary Connector which allows a connection to an external Ethernet PHY that can be found on some Tower peripheral modules.

When the K64 Ethernet MAC is operating in RMII mode, synchronization of the MCU clock and the 50 MHz RMII transfer clock is important. The MCU input clock must be kept in phase with the 50 MHz clock supplied to the external PHY. Therefore, the TWR-K64F120M provides the option (see Table 5, Ethernet operation jumper settings) to clock the MCU from an external clock from CLKIN0 pin on the Primary Connector. The Tower peripheral module implementing the RMII PHY device should drive a 50 MHz clock on the CLKIN0 pin that is kept in phase with the clock supplied to the RMII PHY.

The TWR-SER1 module that comes as part of the TWR-K64F120M-KIT provides a 10/100 Ethernet PHY that can operate in either MII or RMII mode. By default, the PHY is boot strapped to operate in MII mode; therefore, jumper configuration changes may be required. Table shows the settings for proper interoperability between the Ethernet interface on the TWR-SER and the TWR-K64F120M.

Table 5. Ethernet operation jumper settings

Tower Module	Jumper	Setting
TWR-K64F120M	J32	ON
—	J33	OFF
TWR-SER	J2	3-4
—	J3	2-3
—	J11	9-10

6.16 TWR-K64F120M Jumper Options and Headers

The following is a list of all the jumper options on the TWR-K64F120M. The default installed jumper settings are indicated by white text on a black background.

Table 6. Jumper options and headers

Option	Jumper	Setting	Description
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Table 6. Jumper options and headers

50MHz Clock OSC power	J33	1-2	Enable V_BRD power supply to 50MHz OSC
	J32	1-2	Disable V_BRD power supply to 50MHz OSC
JTAG Board Power Selection	J14	ON	Connect 5V output (P5V_TRG_USB) to JTAG port (supports powering board from JTAG pod supporting 5V supply output)
		OFF	Disconnect OSJTAG 5V output (P5V_TRG_USB) from JTAG port
UART4_TX	J36	ON	Connect PTE24 as UART4_TX to Secondary TWR_ELEV
		OFF	Disconnect PTE24 as UART4_TX to Secondary TWR_ELEV
UART4_RX	J27	ON	Connect PTE25 as UART4_RX to Secondary TWR_ELEV
		OFF	Disconnect PTE25 as UART4_RX to Secondary TWR_ELEV
SDHC_WP / UART4_RTS_B	J34	ON	Connect PTE27 as UART4_RTS_B to Secondary TWR_ELEV or as SDHC_WP to SD card slot as write protect signal
		OFF	Disconnect PTE27 as UART4_RTS_B to Secondary TWR_ELEV or as SDHC_WP to SD card slot as write protect signal
GPIO3_ELEV	J35	ON	Connect PTE28 as General Purpose IO to TWR_ELEV
		OFF	Disconnect PTE28 as General Purpose IO to TWR_ELEV
UART_CTS / RTC_CLKOUT/ 1588_CLKIN	J31	ON	Connect PTE26 as UART_CTS to Secondary TWR_ELEV or as RTC_CLKOUT to primary TWR_ELEV or as Clock input for 1588
		OFF	Disconnect PTE26 as UART_CTS to Secondary TWR_ELEV or as RTC_CLKOUT to primary TWR_ELEV or as Clock input for 1588
TAMPER0	J21	ON	Connect Tamper0 signal to test point
		OFF	
K64 VREG IN Selector	J19	1-2	VBUS Signal on micro_USB connector J17 connects to K64_VREGIN to allow standalone USB operation
		2-3	VBUS signal from TWR ELEV connector connects to K64_VREGIN to allow USB operation with complete Tower System
3.3 V Voltage Regulator Input Selector	J18	1-2	Output of USB power switch controlled by the VTRG_EN signal from the K20 MCU. Provides input to 3.3V regulator.
		2-3	Output of USB power from primary elevator Pin A57 to 3.3V regulator.
		5-6	Output of USB power from K64 VREGIN to 3.3 regulator

Table 6. Jumper options and headers

Board Power Selector	J29	1-2	Connect K20 USB regulator output (VOUT_3V3) to on-board supply (V_BRD)
		3-4	Connect K64 USB regulator output (VOUT_3V3) to on-board supply (V_BRD)
		5-6	Connect 3.3V on-board regulator output (P3V3) to on-board supply (V_BRD)
		7-8	Connect 1.8 V on-board regulator output (P1V8) to on-board supply (V_BRD)
MCU Power connection	J28	ON	Connect on-board 3.3V or 1.8V supply (V_BRD) to MCU VDD
		OFF	Disconnect on-board 3.3V or 1.8V supply (V_BRD) to MCU VDD
MCU Power VDDA for current measurement	J22	ON	Connect MCU_PWR (3.3V or 1.8V) to VDDA and VREFH
		OFF	Disconnect MCU_PWR (3.3V or 1.8V) to VDDA and VREFH
VBAT Power Source	J20	1-2	Connect VBAT to on-board 3.3 V or 1.8 V supply
		2-3	Connect VBAT to the higher voltage between MCU supply (MCU_PWR) or coin cell supply (VBATD)
Accelerometer IRQ Connection	J7	ON	Connect PTA8 to INT2 pin of accelerometer
	J8	ON	Connect PTA6 to INT1 pin of accelerometer
		OFF	Disconnect PTA6 and/or PTA8 from INT1 and/or INT2 of accelerometer
External Pull down on SDHC D3	J13	ON	External 10K ohm Pull down on SDHC_D3
		OFF	No pull down on SDHC_D3
LED connections	J30	1-2	Connect PTE6 to Yellow/Green LED (D5)
		3-4	Connect PTE7 to Yellow LED (D6)
		5-6	Connect PTE8 to Orange LED (D7)
		7-8	Connect PTE9 to Blue LED (D8)
5V power selection	J38	1-2	Connect 5V power from OpenSDA (mini USB) to power switch MIC2026
		2-3	Connect 5V power from Elevator to power switch MIC2016
Micro USB power enable	J26	ON	Connect PTC9 to USB power enable on power switch MIC2026
		OFF	Disconnect PTC9 from USB power enable on power switch MIC2026
Micro USB overcurrent flag	J23	ON	Connect PTC8 to overcurrent flag on power switch MIC2026
		OFF	Disconnect PTC8 from overcurrent flag on power switch MIC2026
Micro USB ID selection	J25	ON	USB Host / Device ID selection is controlled by PTE12
		OFF	No ID selection USB Host / Device

Table 6. Jumper options and headers

Potentiometer connection	J24	ON	Connect potentiometer to ADC1_SE18
		OFF	Disconnect potentiometer from ADC1_SE18
General Purpose TWRPI V_BRD power enable	J6	ON	Connect on-board 1.8 V or 3.3 V supply (V_BRD) to TWRPI 3V power (GPT_VBRD)
		OFF	Disconnect fromboard 1.8 V or 3.3 V supply (V_BRD) to TWRPI 3V power (GPT_VBRD)
GPIO RESET_OUT_B connection	J1	1-2	Connect PTB7 to RESET_OUT_B signal
		2-3	RESET_OUT_B signal resets the target MCU
Target MCU UART1_RX output selection	J10	1-2	Connect MCU's UART1_RX to OpenSDA virtual COM RX port
		2-3	Connect MCU's UART1_RX to primary Elevator (A41) UART0_RX
Target MCU UART1_TX output selection	J15	1-2	Connect MCU's UART1_TX to OpenSDA virtual COM TX port
		2-3	Connect MCU's UART1_RX to primary Elevator (A42) UART0_RX
SWD_CLK_TGTMCU output selection	J39	ON	Enable the SWD_CLK_TGTMCU connection between the OpenSDA and target MCU
		OFF	Isolate the SWD_CLK_TGTMCU connection between the OpenSDA and target MCU
Reset selection for SW2 Reset button	J16	1-2	Connect the reset button to target MCU before level shifter
		2-3	Connect the reset button to target MCU without passing through level shifter

7 Useful links

www.freescale.com/twr-k64f120m

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