TWR-VF65GS10 Tower Module User's Guide

1 TWR-VF65GS10 Overview

The TWR-VF65GS10 Tower Controller Module is compatible with the Freescale Tower System (see Figure 1) and features the heterogeneous dual-core Vybrid VF6xx family member with characteristics listed in section 2.1.

TWR-VF65GS10 is available either separately or inside the Tower System Kit (TWR-VF65GS10-KIT, TWR-VF65GS10-DS5, or TWR-VF65GS10-PRO) consisting of the below blocks in various combinations:

- Tower Elevator Modules (TWR-ELEV),
- Either Tower Serial Module (TWR-SER),
- Tower Serial2 Module (TWR-SER2),
- Tower LCD Display (TWR-LCD-RGB).

TWR-VF65GS10 can also be combined with other Tower peripheral modules to create development platforms for a wide variety of applications. Visit freescale.com/tower for details.

Contents

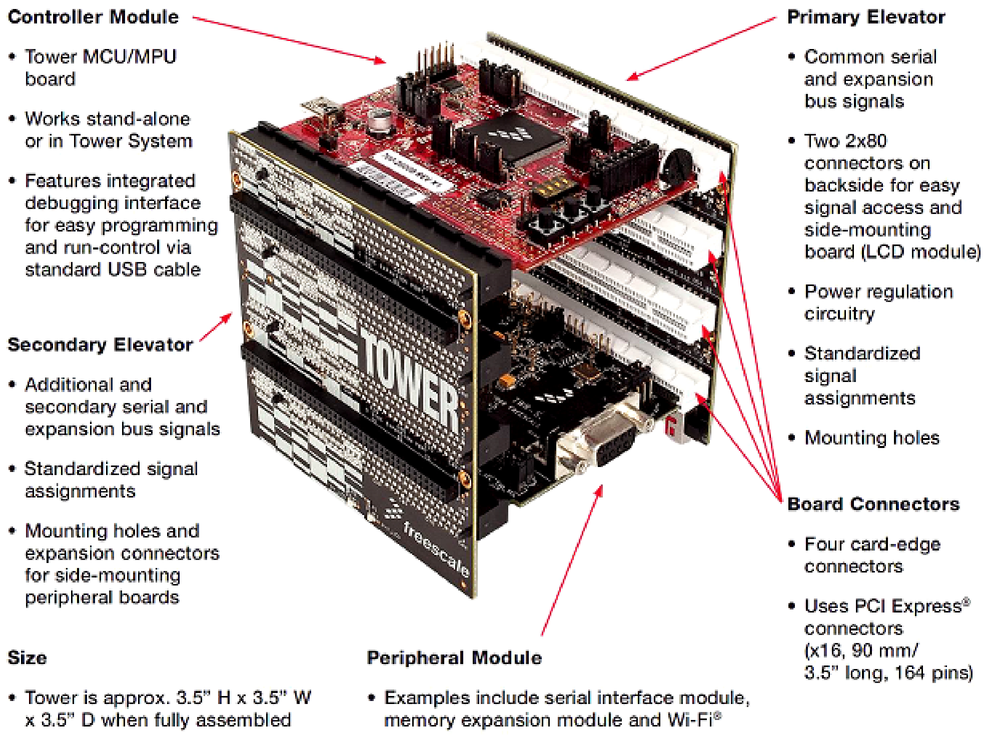

Figure 1. Freescale Tower System overview

Each Tower module features two expansion edge connectors - for the primary and secondary elevator modules (see Figure 1). Proper Tower operation is only guaranteed with the elevator modules of Rev. F or later.

1.1 Tower Kit contents

Provided below are details of the available TWR-VF65GS10 kits.

TWR-VF65GS10:

- TWR-VF65GS10 - MPU Module,
- Dual-head USB cable,
- Printed DS-5 license and links for software tools,
- Quick Start Guide.

TWR-VF65GS10-KIT:

- TWR-VF65GS10 - MPU Module,
- TWR-ELEV – Primary and Secondary Elevator Modules,
- TWR-SER – Serial module including Host/Peripheral/OTG USB, Ethernet, CAN, RS232, and RS485,
- Dual-head USB cable,
- Printed DS-5 license and links for software tools,
- Quick Start Guide.

TWR-VF65GS10-DS5:

- TWR-VF65GS10 MPU module,
- TWR-ELEV – Primary and Secondary Elevator Modules,
- TWR-SER2 – Serial module including Host/Peripheral USB, Dual Ethernet, CAN, RS232 and RS485,
- TWR-LCD-RGB display,
- Dual-head USB cable,
- Printed DS-5 license and links for software tools,
- Quick Start Guide.

TWR-VF65GS10-PRO:

- TWR-VF65GS10 MPU module,
- TWR-ELEV – Primary and Secondary Elevator Modules,
- TWR-SER2 – Serial module including Host/Peripheral USB, Dual Ethernet, CAN, RS232 and RS485,
- TWR-LCD-RGB display,
- Dual-head USB cable,
- Printed DS-5 license and links for software tools,
- Quick Start Guide.

1.2 Tower features

Shown in Figure 2 and Figure 3, the TWR-VF65GS10 Tower Module possesses following key features:

- Vybrid MVF61NS151CMK50 Controller,
- Kinetis K20DX128VFM5 Controller (provides OpenSDA Debug function),
- 1 Gb (64Mx16) DDR3 in 96 FBGA package,
- 2 Gb (128MX16) NAND Flash,
- Two 128 Mb (16 MB) Quad-I/O Serial Flash,
- Dual USB with on-chip PHY,
- Interfaces to TWR-LCD-RGB board,
- Four user-controlled status LEDs,
- Three mechanical push buttons for user input, and one for reset,
- Potentiometer and three-axis digital accelerometer,
- Micro SD Card slot,
- Battery-based power supply for Vybrid Real-Time Clock (RTC) and Tamper Detection modules.

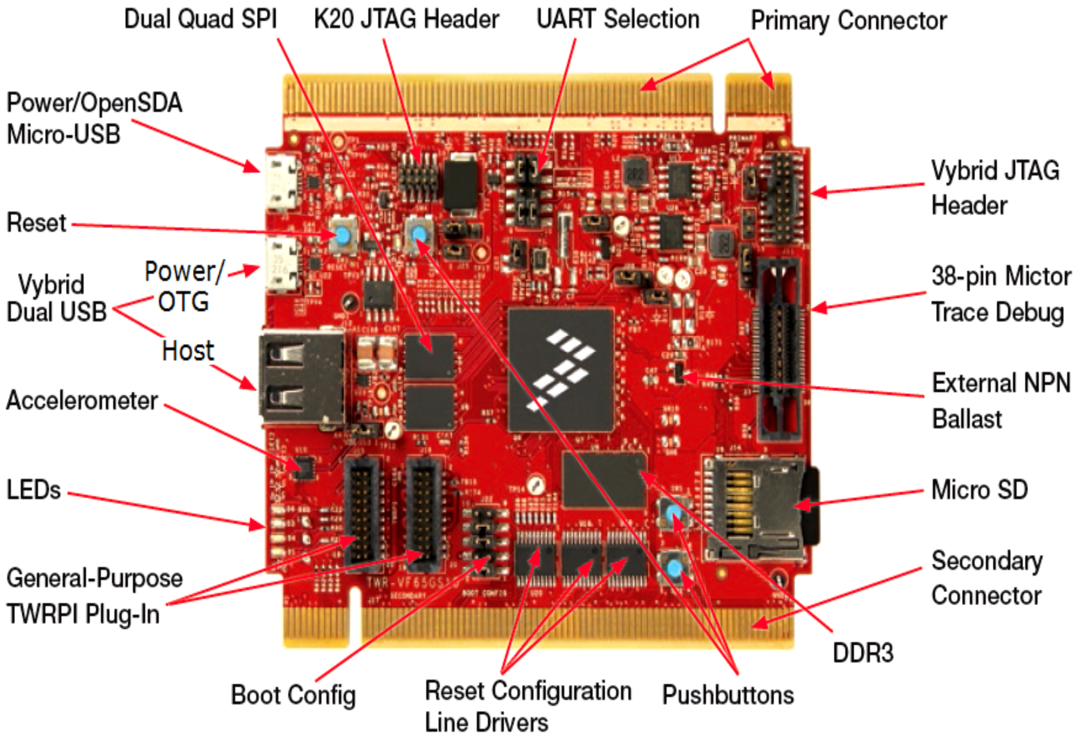

Figure 2. Top side of TWR-VF65GS10

Figure 3. Bottom side of TWR-VF65GS10

1.3 Getting Started

To get started, follow the steps in the TWR-VF65GS10 Quick Start Guide. A video walk-through guide, "Introduction to the Vybrid Tower System Module," is also available on the tool support page (freescale.com/TWR-VF65GS10).

1.4 Reference Documents

More information on the Vybrid family, Tower System, and Peripheral Modules can be found in the below documents located in the documentation sections of freescale.com/Vybrid, freescale.com/TWR-VF65GS10, and freescale.com/Tower:

- *VYBRIDVF6FS: Vybrid Family Fact Sheet,*
- *VYBRIDRM: Vybrid Reference Manual,*
- *VYBRIDSRM: Vybrid Security Reference Manual,*
- *TWRVF65GS10QSG: Quick Start Guide,*
- *TWR-VF65GS10_SCH: Schematic,*
- *TWR-VF65GS10-PWB: Design Package,*
- *TWRFS: Tower Fact Sheet,*
- *TWR-ELEV-PRI-SCH: Primary Elevator Schematic,*
- *TWR-ELEV-SEC-SCH: Secondary Elevator Schematic,*
- *TWR-SER-SCH: Serial (USB, Ethernet, CAN, RS232/485) Peripheral Module Schematic,*
- *TWR-SER2-SCH: Enhanced Serial Connectivity, Dual Ethernet, High-Speed USB Peripheral Module Schematic*
- *OPENSDAUG: OpenSDA User Guide.*

2 Hardware Description

The TWR-VF65GS10 Tower Controller Module (block diagram in Figure 4) features:

- Dual-core MVF61NS151CMK50 (ARM Cortex-A5 and ARM Cortex-M4 operating at up to 500 and 167 MHz, respectively) with dual TFT display in 364 BGA package,
- Dual USB OTG with on-chip HS PHY and on-chip HS/FS/LS PHY,
- Dual 10/100 Mbps MAC (Ethernet) with on-chip L2 switch,
- Advanced security,
- Communication peripherals,
- Advanced digital-audio support,
- Tamper detect.

The module can operate either stand-alone or as a part of the Freescale Tower System. Based on the K20-series Kinetis device and referred to as OpenSDA, the on-board debug circuit provides a JTAG interface and a power supply input through a single Micro-B OTG USB connector.

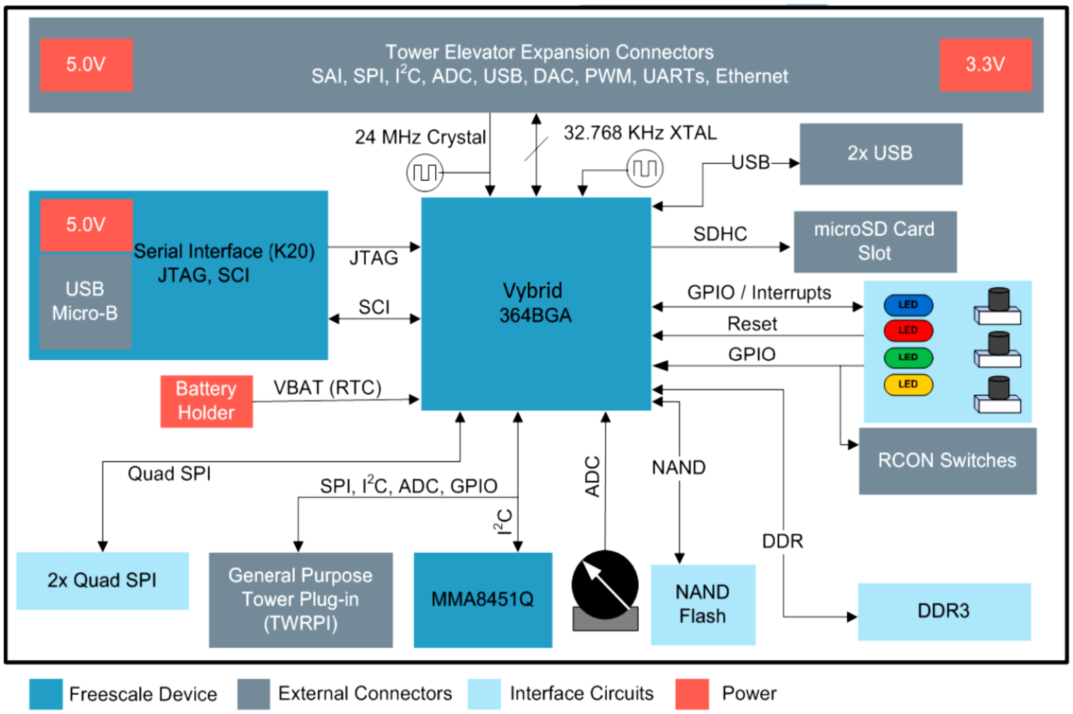

Figure 4. TWR-VF65GS10 block diagram

2.1 Vybrid device

Listed below are the MVF61NS151CMK50 highlights:

- ARM Cortex-A5 core @ 500 MHz (1.57 DMIPS/MHz) with TrustZone, with 32 KB ICache/32 KB D-Cache (L1), and 512 KB of L2 cache,
- NEON Media Processing Engine (MPE) co-processor and double-precision Floating Point Unit (FPU),
- ARM Cortex-M4 @ 167 MHz with 16 KB I-Cache/16 KB D-Cache,
- 1 MB on-chip SRAM, with ECC on 512 KB of it,
- LPDDR2/DDR3 support,
- Support for Dual TFT display up to WVGA,
- Dual 10/100 Mbps MAC (Ethernet) with on-chip L2 switch,
- Dual OTG USB with on-chip HS PHY and on-chip HS/FS/LS on-chip PHY,
- NAND Flash Controller,
- Power management including WAIT, STOP, LPRUN, ULPRUN, and LPSTOPn modes,
- Advanced Security supporting Symmetric and Asymmetric Key Cryptography with on-chip tamper detection,
- Rich set of communication peripherals and general-purpose features,
- Advanced digital-audio support with multiple audio interfaces and hardware asynchronous sample-rate converter co-processor,

- - 40C to + 85C operating temperature range,
- 176 LQFP and 364 BGA package options.

2.2 Clocking scheme

There are two external, crystal-based clock sources on the Vybrid Tower board: 32.768 kHz XOSC and 24 MHz XOSC.

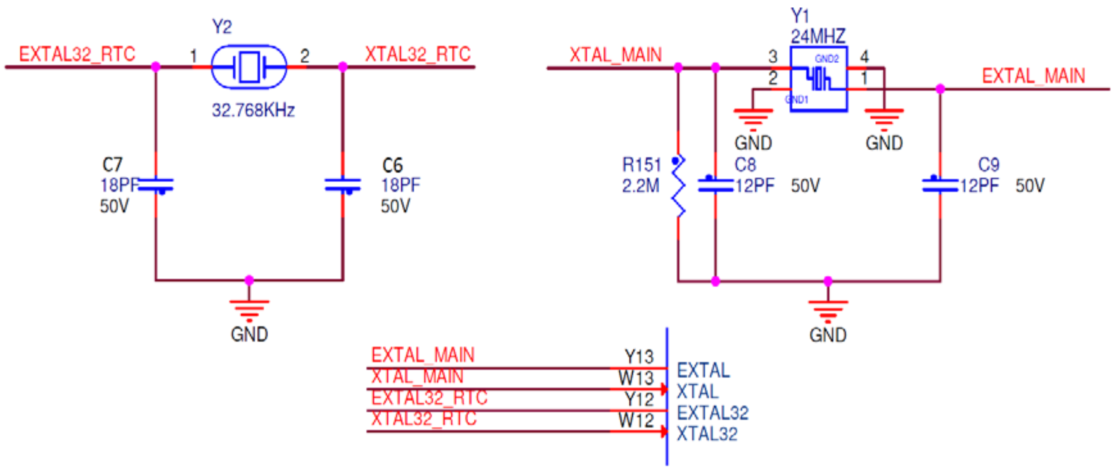

Figure 5. TWR-VF65GS10 external clock options

Internal to the Vybrid device are a slow, 128 kHz internal reference clock (IRC) and a fast, 24 MHz IRC. The 128 kHz IRC signal is divided by four by default providing an internal 32 kHz clock to the device. Refer to Figure 6 for the high-level clocking diagram.

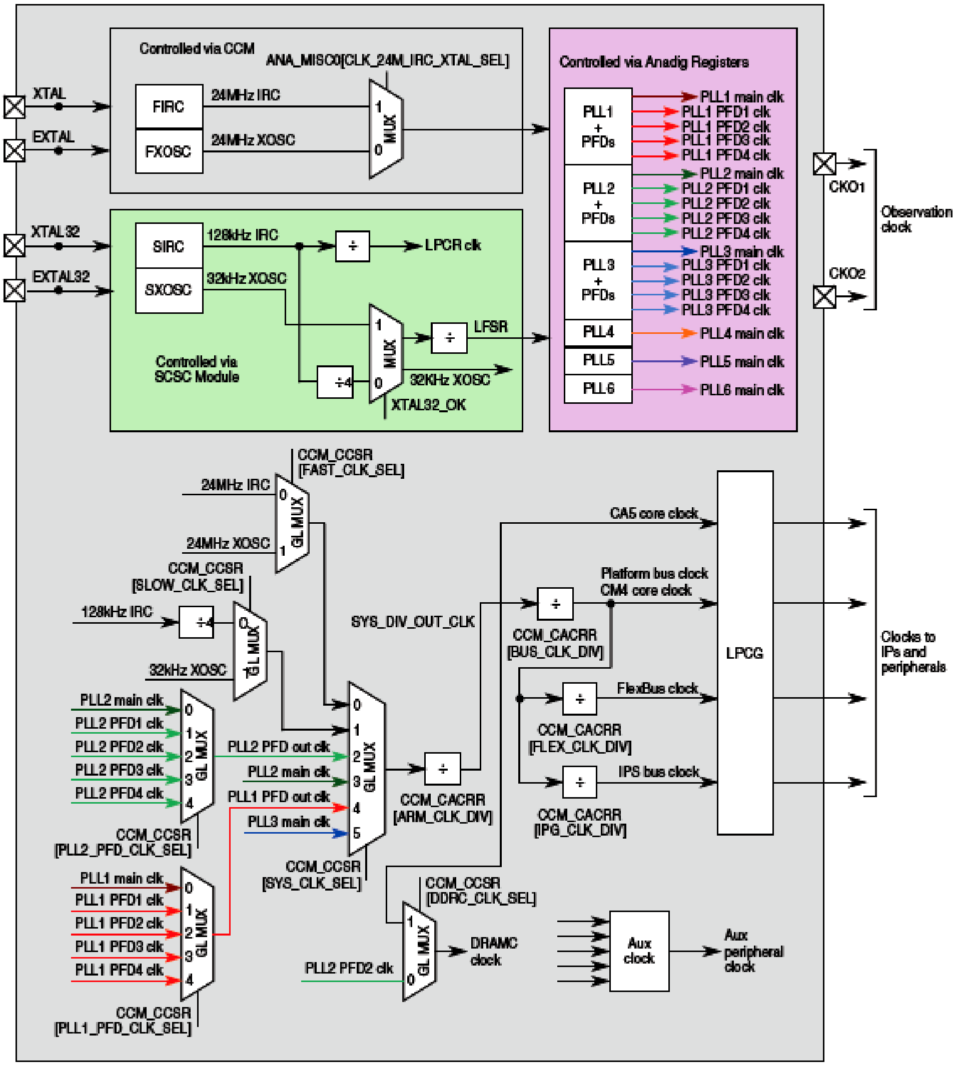

Figure 6. Vybrid clocking diagram

A PLL summary for the MVF61NS151CMK50 device is as follows:

- PLL 1 – System PLL,
- PLL 2 – PLL 528,
- PLL 3 – USB0 PLL,
- PLL 4 – Audio PLL,
- PLL 5 – MAC (Ethernet) PLL,
- PLL 6 – Video PLL,
- PLL 7 – USB1 PLL.

For additional clocking details, refer to the ANADIG and CCM chapters of the *Vybrid Reference Manual*.

2.3 System power

While reading this chapter, refer to Figure 7 and Table 3 as well as the TWR-VF65GS10 schematic.

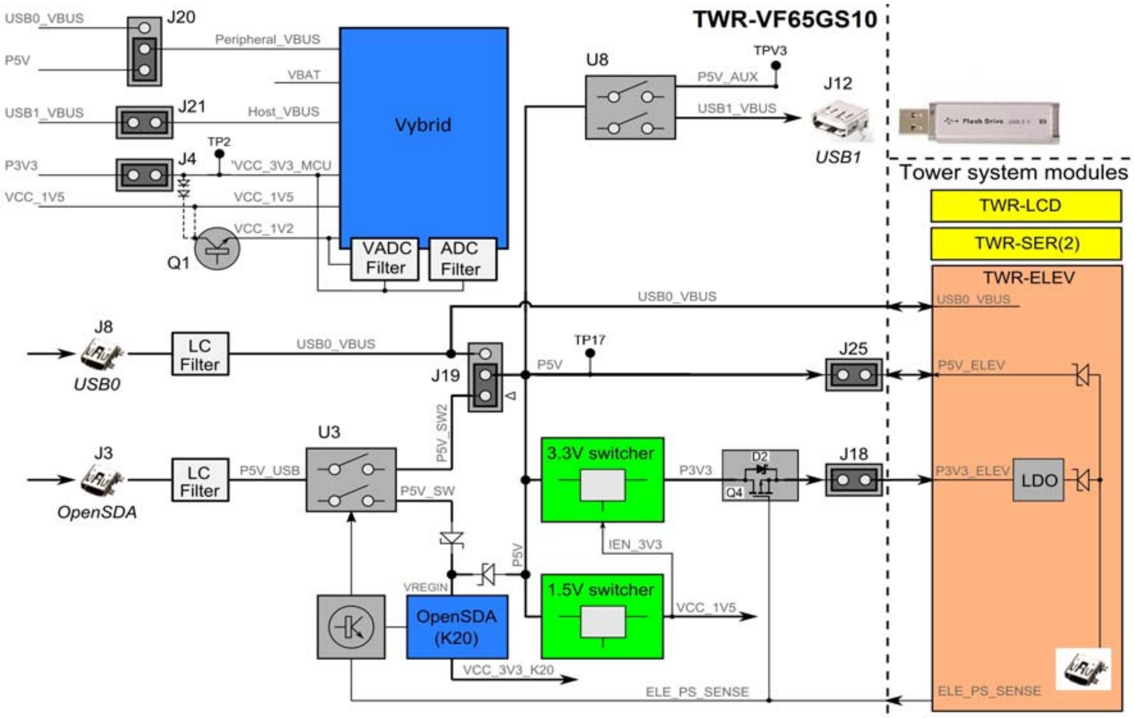

Figure 7. Power distribution scheme

2.3.1 Power options

The only external power source TWR-VF65GS10 needs is 5V (either locally or from the Tower elevator module), the rest of the required rails being generated by TWR-VF65GS10 itself (see section 2.3.3).

NOTE

The USB0_VBUS net routed to J19 (pin 3) and J20 (pin 3) is also present on pin A57 of the primary elevator connector J17A (see Figure 7), which should be taken into account for Tower peripheral modules using this power rail, e.g. TWR-SER or TWR-SER2. To prevent abnormal operation, power conflicts, or even damage caused by undesired sharing of the USB0_VBUS power among the Tower System modules via the elevator, the following measures are recommended:

- Proper settings of the relevant jumpers on all the Tower System modules,
- Proper logic levels of the TWR-VF65GS10 signals controlling power rails on the involved peripheral modules.

Refer to the peripheral modules' schematics for details.

2.3.1.1 Local power options

There are three options for connecting a power source to the TWR-VF65GS10 module:

- “OpenSDA USB” option (main) - 5V on the J3 (Micro-B OTG USB) connector tied to the K20 microcontroller (U13) bearing the “OpenSDA” debug interface, with J19 in the “1-2” position (default); the only one when “OpenSDA” operates; used for application development,
- “Vybrid USB” option - 5V on the J8 (Micro-B OTG USB) connector, with J19 in the “2-3” position; the Tower System powered from the USB0_VBUS power rail belonging to the Vybrid USB port,
- “Non-USB” option - 5V on the TP17 test point, with J19 fully open; the only local option with power provided by a non-USB source; recommended for applications specifying the minimum 5V rail value, e.g. when the Tower System consumption as well as power supplied by the USB Host connector (J12) are close to their maximum levels, which causes significant voltage drop over the USB cable and series on-board components (connectors, switches, ferrite beads, etc.), but, as per the USB specification, the Peripheral device plugged into J12 needs the VBUS value to be at least 4.75V.

If a part of the Tower System, the whole system is powered from TWR-VF65GS10. In this case, J18 and J25 shall be closed to provide 3.3V and 5V, respectively, to the elevator modules.

2.3.1.2 Power from elevator in the Tower System

- The J19 is fully open and J25 closed in this mode, and the 5V power comes either from the Tower elevator USB connector or the screw terminal,
- The J18 state does not matter thanks to the on-board 3.3V DC switch (see section 2.3.1.2).

2.3.1.3 Combined power options in the Tower System

- When 5V power is provided simultaneously by the Tower Elevator module (see section 2.3.1.2) and the local J3 connector (see 1-st option in section 2.3.1.1), the whole Tower System is powered from the elevator module, i.e. 5V coming from J3 is blocked (refer to the AN4649 *Power for the Tower Application Note* for details),
- When 5V power is provided simultaneously by the Tower elevator module (see section 2.3.1.2) and the local J8 connector (see 2-nd option in section 2.3.1.1), TWR-VF65GS10 is powered from J8, and the peripheral Tower modules from the elevator module.

With two 5V sources available simultaneously, having the J25 header open (see Figure 7) prevents a conflict between them - undesired but unlikely to harm TWR-VF65GS10; the J18 state does not matter, thanks to the on-board DC switch (see section 2.3.1.2).

2.3.2 “OpenSDA” option power-up sequencing

In this local-power case (see section 2.3.1.1), 5V power from the USB connector J3 comes directly the K20-series Kinetis microcontroller (U13), which runs the “OpenSDA” firmware and controls power for the rest of the system.

As per the USB power specification, when a Peripheral is first connected, the Host recognizes it as "low-power", allowing it to draw up to 0.1A of current. On the enumeration stage, the Peripheral may ask the Host to recognize it as "high-power", with a 0.5A limit. To meet these requirements, the following power-up sequence is implemented on the TWR-VF65GS10 module (when its "RESET" button SW3 is not pressed):

- USB cable plugged in,
- K20 powered on,
- K20's LED (D5) turned on,
- K20 waiting for USB enumeration,
- K20's LED turned off once enumeration completed,
- OpenSDA started (refer to its User Guide for details),
- 5V for the rest of system enabled by K20,
- "POWER ON" LED (D9) turned on.

2.3.3 On-board power rails

2.3.3.1 Primary power rails

The two power rails external to Vybrid, 3.3V and 1.5V, are generated using powerful high-efficiency switch-mode voltage regulators, 5V "as-is" being used by the Vybrid USB blocks.

When a part of the Tower System, but power is only provided to TWR-VF65GS10 itself, it may power, through the Tower elevator modules, the rest of the system with:

- 5V, if J25 closed,
- 3.3V, if J18 closed.

The TWR-VF65GS10 board never uses other 3.3V than generated on-board. Even when a part of the Tower System, with J18 closed and 5V and 3.3V available from the Tower elevator module, the on-board DC switch (based on Q4/D2) automatically prevents external 3.3V from flowing into the board.

The 3.3V power supplied to the device (P3V3) is routed through the J4 header. TP2 is a test point that can be used to measure the main 3.3V input into the MVF61NS151CMK50 device.

2.3.3.2 Vybrid core power

An external ballast transistor (Q1) is used to generate 1.2V for the Vybrid core, with its collector powered from 1.5V (default) or 3.3V (to test low-power applications without 1.5V rail, e.g. without DDR). Refer to AN4807 *Vybrid Power Consumption and Options Application Note* for details.

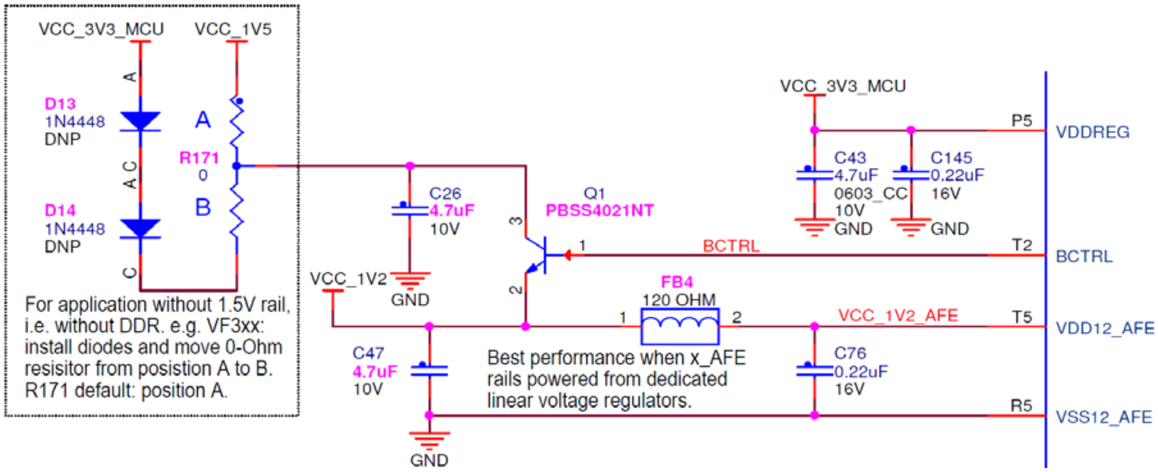

Figure 8. Vybrid core power

2.3.3.3 Backup battery

The Secure Real-Time Clock (SecureRTC) module operates when the external power supply fails. The on-board coin cell battery holder accommodates a round, 20-mm, 3V lithium battery, e.g. 2032 or 2025, and the J1 header selects if the Vybrid VBAT pin is powered from it or the primary 3.3V rail. In the Vybrid VBAT power domain are also the 32 KHz XOSC, Tamper, and Monitors blocks.

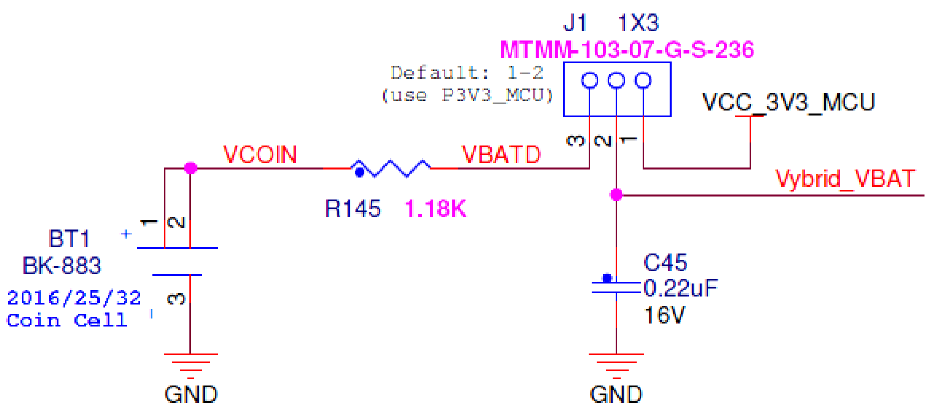

Figure 9. Coin cell

2.4 Debug interfaces

Three debugging interfaces are provided on the TWR-VF65GS10 module:

- OpenSDA with CMSIS-DAP on Micro-B OTG USB connector J3,
- JTAG on header J5,
- ARM ETM (Embedded Trace Macrocell) on connector J11.

2.4.1 OpenSDA with CMSIS-DAP firmware

The OpenSDA circuit consists of a K20 series Kinetis microcontroller and surrounding components to act as a bridge between J3 and Vybrid JTAG, SPI, and UART pins. The firmware is a mass-storage bootloader with a virtual serial-port capability, which allows the demo program to output serial data through the USB from the primary (Cortex-A5) core over UART1.

The CMSIS-DAP (Cortex Microcontroller Software Interface Standard – Debug Access Port) firmware allows a debug connection to be established through J3.

Alternate and/or updated firmware versions might be available; checking relevant links on the TWR-VF65GS10 web page to verify that is recommended.

2.4.2 Cortex JTAG connector

JTAG debugging can be done using the 19-pin Cortex-M header J5.

2.4.3 Cortex JTAG+Trace connector

The 38-pin Mictor connector J11 (Figure 10) provides more robust debugging based on the ARM ETM (Embedded Trace Macrocell) format. Along with the regular JTAG debug pins (TDI, TDO, TMS, TCLK, and RESET), a number of additional Trace pins are used.

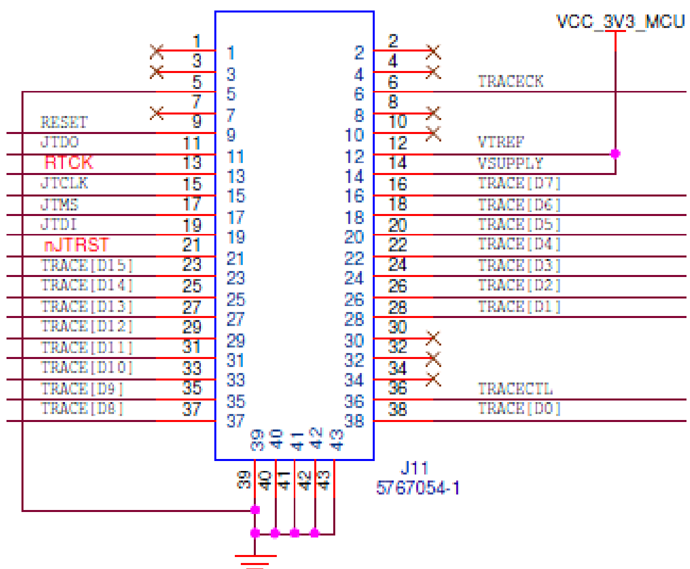

Figure 10. 38-pin Mictor connector

2.5 Graphical interface

- The Vybrid device includes two on-chip Display Control Unit (DCU4) modules, primary DCU0 and secondary DCU1, which can be used to drive graphical content to a TFT LCD screen, such as the abovementioned TWR-LCD-RGB one.

- The DCU0 pins (DCU0_B0-DCU0_B7, DCU0_R0-DCU_R7, DCU_G0-DCU_G7, DCU0_HSYNC, DCU0_VSYNC, and DCU0_PCLK) are connected to the Secondary Tower elevator module.
- DCU1 is not supported on the TWR-VF65GS10 board.
- A different Graphical LCD module type, TWR-LCD, is incompatible with the TWR-VF65GS10 board.

2.6 DDR3 memory

- A single 1 Gb (64Mx16) DDR3 memory chip in the 96-ball FBGA package (K4B1G1646G by Samsung) is installed on the TWR-VF65GS10 board.
- It is powered from the abovementioned 1.5V power rail (along with the ballast transistor Q1).
- A simple resistor divider is good enough to generate the 0.75V DDR3 reference (see Figure 11).

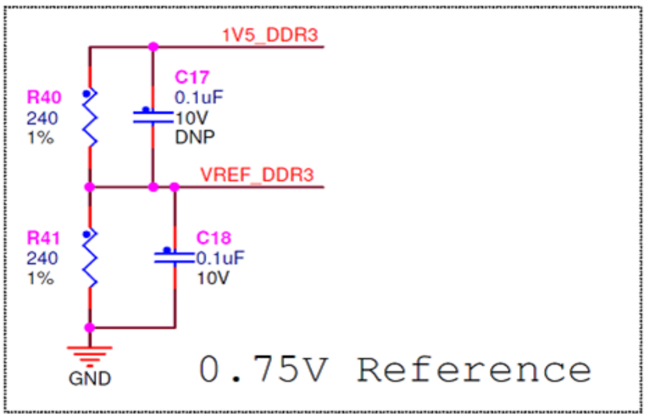

Figure 11. DDR3 0.75V reference supply

- The TWR-VF65GS10 board is laid out so that it needs no external termination resistors, which simplifies its design and lowers power consumption.
- DDR3 Self-Refresh (low-power) mode is supported even when Vybrid is in any of the LPSTOPx modes, in which its I/Os are switched into a high-impedance mode. The on-board pull-up on DDR_RESET and pull-down on DDR_CKE lines keep the DDR3 module in Self-Refresh mode.

2.7 NAND Flash memory

- A single 2 Gb (128MX16) SLC NAND Flash memory (e.g. MT29F2G16ABAEA by Micron) is installed on the TWR-VF65GS10 board.
- NAND Flash cannot operate in the eXecute-In-Place (XiP) mode.
- NAND Flash is supported as a boot device by the internal BootROM.
- Vybrid's NAND Flash data pins are shared between its NAND Flash controller and FlexBus interface. However, due to lack of dynamical switching between the two interfaces, they are dedicated to NAND Flash in the TWR-VF65GS10.

For more information, refer to the *Vybrid Reference Manual*.

2.8 QuadSPI memory

- Two 128 Mb (16 MB) Quad-I/O Serial Flash (e.g. S25FL128S by Spansion) are installed on the TWR-VF65GS10 board.
- QuadSPI eXecute-In-Place (XiP) mode supported.
- QuadSPI interface supports both Single (SDR) and Dual Data Rate (DDR).
- QuadSPI interface supports Parallel QuadSPI operation in DDR mode.
- QuadSPI memory is supported as a boot device by the internal Boot ROM.

2.9 Accelerometer

An MMA8451Q digital accelerometer is connected to the Vybrid device through an I^2C interface (0x1C address) and a GPIO/IRQ signal.

For more information, refer to the TWR-VF65GS10 Schematic.

2.10 Input-output hardware devices

The below input-output hardware devices are provided on the TWR-VF65GS10 board:

- Three pushbutton switches connected to the GPIO/Interrupt signals, out of which SW1 and SW4, are connected to PTB16 and PTD6, respectively, and can be used as wakeup sources from the low power modes,
- One pushbutton switch used for Vybrid manual reset and K20 boot-up mode selection,
- Four user-controllable LEDs,
- Potentiometer connected to the Vybrid ADC input.

For more information, refer to the TWR-VF65GS10 Schematic.

2.11 General Purpose Tower Plug-in (TWRPI) socket

TWR-VF65GS10 features a General Purpose TWRPI interface:

- Based on sockets J15 & J16.
- Pinout provided in Table 1.
- Features sensors, RF transceivers, etc.
- Provides access to:
  - I^2C and SPI interfaces,
  - IRQs,
  - GPIOs,
  - Timers,
  - Analog-conversion signals,
  - TWRPI ID signals,
  - Reset,
  - Voltage supplies.

Table 1. TWRPI connectivity

Pin	Description (J15)		Pin	Description (J16)
1	GND		1	5V
2	GND		2	3.3V
3	I2C0_SCL		3	GND
4	I2C0_SDA		4	3.3V
5	GND		5	GND
6	GND		6	GND
7	GND		7	GND
8	GND		8	ADC0 Input
9	DSPI0_SIN		9	ADC1 Input
10	DSPI0_SOUT		10	GND
11	DSPI0_CS1		11	GND
12	DSPI0_SCK		12	ADC2 Input
13	GND		13	GND
14	GND		14	GND
15	GPIO0/IRQ		15	GND
16	GPIO1		16	GND
17	GPIO2		17	ID0
18	GPIO3		18	ID1
19	GPIO4		19	GND
20	N/C		20	RESET_B

2.12 MAC (Ethernet) interface

The installed Vybrid device features dual 10/100 Mbps Ethernet MAC with IEEE1588 capability, internal L2 Switch block, and supports both MII and RMII interface types.

On the TWR-VF65GS10 board:

- Two RMII interfaces are routed to both the primary and secondary module sides,
- Optional MII one (MII0) is routed to the primary elevator module side only (Table 3). Due to pin sharing, using the MII0 and NAND Flash interfaces simultaneously is impossible.

The TWR-VF65GS10 is compatible with two Ethernet-bearing peripheral module types - Serial Cards TWR-SER and TWR-SER2, having one and two Ethernet ports, respectively. The RMII Mode configuration settings are provided in Table 2.

Table 2. Serial card configuration for RMII mode

TWR-SER - RMII Mode			TWR-SER2 - RMII Mode (1=ON)	
Jumper	Setting		Switch	Setting
J2	3-4		SW1 - PHY A	[1:8] = 11000000
J3	2-3		SW2 - PHY B	[1:8] = 10100000
J12	9-10			

Refer to the TWR-SER and TWR-SER2 User Manuals for additional details.

2.13 Dual USB interface

The installed Vybrid device has two OTG USB ports with on-chip HS/FS/LS PHYs. They are:

- USB0 on the Micro-B OTG connector J8 and optionally on the primary Tower elevator module side,
- USB1 on the Type-A connector J12.

2.14 SD card interface

- The installed Vybrid device has two SD Host Controllers, SDHC0 & SDHC1.
- SDHC1 is connected to a micro Secure Digital (micro SD) card slot, whereas SDHC0 is not used due to that some of its shared pins are already used for the NAND Flash and MAC (Ethernet) connections.
- Refer to Table 4 for SDHC1 connection details.
- A micro SD card can be used as a Vybrid boot device by its internal boot ROM.

2.15 External bus (FlexBus) interface

Since the two Vybrid's interfaces, NAND Flash and FlexBus, share pins, and NAND Flash is used on the TWR-VF65GS10 board, the Flexbus pins are not routed to the Tower elevator module and unavailable for any custom connections.

2.16 Boot device selection

Based on the J22 header settings (Table 3), Vybrid boots from one of the four memory devices – two on-board (QuadSPI or NAND Flash) or two removable (SD card or USB Flash drive) ones.

The USB/UART connection used for the USB Flash option is also utilized by a special tool useful for programming the QuadSPI and NAND Flash on-board memory devices as well as the plugged in SD card. It is called “Manufacturing Tool” and provided in the “Hardware Development Tools” section under the “Software & Tools” tab on the Vybrid family web page.

3 Jumper Table

Table 3 shows available jumper options on the TWR-VF65GS10 module, the default settings are in bold.

Table 3. Jumper table

Component	Option	Jumper Location	Description
J1	Vybrid VBAT power source (SecureRTC, 32kHz XOSC, Tamper, and Monitors)	**1-2** 2-3	**VBAT tied to main Vybrid 3.3V (VCC_3V3_MCU)**. VBAT tied to Coin Cell.
J4	VCC_3V3_MCU - main Vybrid 3.3V supply (VDD33 pins)	**ON** OFF	**P3V3 from on-board 3.3V regulator (see 2.3 above) tied directly to VCC_3V3_MCU.** Current-measuring device connected across.
J6	JTAG 5V supply	**OFF** ON	**Pin 11 & 13 of JTAG connector floating.** Pin 11 & 13 of JTAG connector tied to 5V.
J7	Tamper loopback	**ON** OFF	**EXT_WM0_TAMPER_IN tied to EXT_WM0_TAMPER_OUT.** EXT_WM0_TAMPER_IN open, EXT_WM0_TAMPER_OUT open.
J13	Accelerometer interrupt	**ON** OFF	**MCU PTB9 pin tied to INT1 of accelerometer.** Accelerometer Interrupt input untied.
J18	Connection between TWR-VF65GS10 and Elevator 3.3V rails	**ON** OFF	**P3V3 tied to P3V3_ELEV.** TWR-VF65GS10 and Elevator 3.3V rails untied.
J19	On-board 5V source (also see 2.3 above)	**1-2** 2-3	**P5V comes from OTG USB connector J3.** P5V comes from OTG USB connector J8.
J20	Power source for Vybrid USB0 PHY	**1-2** 2-3	**Self-powered - USB0_VBUS tied to P5V.** Bus-powered - USB0_VBUS tied to VBUS of Peripheral OTG USB connector J8.
J21	Power source for Vybrid USB1 PHY	**ON** OFF	**USB1_VBUS tied to VBUS of Host USB Type-A J12.** USB1 PHY unpowered.
J22	Vybrid Boot Option ON (installed) - 1, OFF - 0 1 2 3 4 5 2 4 6 8 10 1 3 5 7 9	12_345 10_000 **10_110** 10_001 01_xxx 00_xxx	Switch Settings Details QuadSPI Boot **SD Card Boot** NAND Boot UART/USB Boot Boot from Fuses
J23	SCI1_TX, SCI2_TX	1-2 **1-3** **2-4** 3-4	SCI1_TX connected to ELEV_UART1_TX. **SCI1_TX connected to OpenSDA_UART_RX.** **SCI2_TX connected to ELEV_UART1_TX.** SCI2_TX connected to OpenSDA_UART_RX.
	SCI1_RX, SCI2_RX	7-8 **7-9** **8-10** 9-10	SCI1_RX connected to ELEV_UART1_RX. **SCI1_RX connected to OpenSDA_UART_TX.** **SCI2_RX connected to ELEV_UART1_RX.** SCI2_RX connected to OpenSDA_UART_TX.

J25	Elevator 5V supply (also see 2.3 above)	**ON** OFF	**P5V tied to P5V_ELEV.** Board and Tower System 5V power rails untied.
R164, R165	USB0 multiplexer	A B	**Connected to OTG USB connector J8.** Connected to Tower Elevator module.
R21	Optional MII MAC (Ethernet) interface	**A** B	**RMII CLK** MII0 TXCLK
R175 to R181		**Removed** Installed	**RMII Interfaces.** MII0 Interface.
R182		**A** B	**SAI RX BCLK** MII0 RXCLK
SH10	Vybrid SDRAM Controller (SDRAMC) power	**Shorted** Cut	**Power pins tied directly to on-board 1.5V source.** Current-measuring device connected across.

4 Input/Output Connections and Pin Usage

Table 4 describes connection details for the LEDs, switches, and major I/O interfaces.

Table 4. I/O connections and pin usage

Feature	Connection	Port Pin	Pin Function
OpenSDA USB-to-serial Bridge (J3)	OpenSDA Bridge RX Data	PTB4	SCI1 TX
	OpenSDA Bridge TX Data	PTB5	SCI1 RX
TWR-ELEV serial (J17A)	Elevator TX Data	PTB6	SCI2 TX
	Elevator RX Data	PTB7	SCI2 RX
SD Card Slot (J14)	SD Clock	PTA24	SDHC1_DCLK
	SD Command	PTA25	SDHC1_CMD
	SD Data0	PTA26	SDHC1_DAT0
	SD Data1	PTA27	SDHC1_DAT1
	SD Data2	PTA28	SDHC1_DAT2
	SD Data3	PTA29	SDHC1_DAT3
	SD Card Detect	PTA7	SDHC1_SW
Pushbuttons	SW1	PTB16	PTB16/Low-Power Wakeup
	SW2	PTB17	PTB17
	SW3	RESET_B	RESET_B
	SW4	PTD6	PTD6 /Low-Power Wakeup
LEDs	D1 - Blue LED	PTB0	PTB0
	D3 - Yellow LED	PTB1	PTB1

	D4 - Yellow/Green LED	PTB2	PTB2
	D6 - Orange/Red LED	PTB3	PTB3
	D7 - Orange LED	RESET_B	RESET_B
Potentiometer (R60)	ADC Input	PTC30	ADC0SE5
Accelerometer (U10)	Accelerometer Clock	PTB14	I2C0_SCL
	Accelerometer Data	PTB15	I2C0_SDA
	Accelerometer Interrupt	PTB9	GPIO
General Purpose TWRPI Socket (J15)	TWRPI I2C0_SCL	PTB14	PTB14
	TWRPI I2C0_SDA	PTB15	PTB15
	TWRPI DSPI0_SIN	PTB20	PTB20
	TWRPI DSPI0_SOUT	PTB21	PTB21
	TWRPI DSPI0_CS1	PTB18	PTB18
	TWRPI DSPI0_SCK	PTB22	PTB22
	TWRPI GPIO0/IRQ	PTB10	PTB10
	TWRPI GPIO1	PTA20	PTA20
	TWRPI GPIO2	PTB7	PTB7
	TWRPI GPIO3	PTB6	PTB6
	TWRPI GPIO4	PTB8	PTB8
General Purpose TWRPI Socket (J16)	TWRPI ADC0 Input	ADC1SE9	ADC1SE9
	TWRPI ADC1 Input	PTC31	ADC1SE5
	TWRPI ADC2 Input	ADC1SE8	ADC1SE8
	TWRPI RESET_B	RESET_B	RESET_B
USB0 (J8) USB Micro-B OTG	USB0 MICRO_USB_VBUS	USB0_VBUS	USB0_VBUS
	USB0 D-	CON_USB0_DN	CON_USB0_DN
	USB0 D+	CON_USB0_DP	CON_USB0_DP
USB1 (J12) USB Type-A	USB1 ATYPE_USB_VBUS	USB1_VBUS	USB1_VBUS
	USB1 D-	USB1_DN	USB1_DN
	USB1 D+	USB1_DP	USB1_DP
Boot Configuration (J22)	Jumper 1&2	PTE0	BOOTMOD1
	Jumper 3&4	PTE1	BOOTMOD0
	Jumper 5&6	PTE12	RCON5 / DCU0_R7

	Jumper 7&8	PTE15	RCON6 / DCU0_G2
	Jumper 9&10	PTE16	RCON7 / DCU0_G3
NAND Flash	NAND Flash Data	PTD16 - PTD31	NF_D[0] - NF_D[15]
	NAND Flash Write Enable	PTB24	NF_WE_b
	NAND Flash Chip Enable	PTB25	NF_CE_b
	NAND Flash Read Enable	PTB27	NF_RE_b
	NAND Flash Read/Busy	PTC26	NF_RB_b
	NAND Flash Address Latch Enable	PTC27	NF_ALE
	NAND Flash Command Latch Enable	PTC28	NF_CLE
QuadSPI Flash	QuadSPI0 Data	PTD5	QSPI0_A_DATA0
	QuadSPI0 Data	PTD4	QSPI0_A_DATA1
	QuadSPI0 Data	PTD3	QSPI0_A_DATA2
	QuadSPI0 Data	PTD2	QSPI0_A_DATA3
	QuadSPI0 Chip Select	PTD1	QSPI0_A_CS0_B
	QuadSPI0 Clock	PTD0	QSPI0_A_SCK
	QuadSPI1 Data	PTD12	QSPI0_B_DATA0
	QuadSPI1 Data	PTD11	QSPI0_B_DATA1
	QuadSPI1 Data	PTD10	QSPI0_B_DATA2
	QuadSPI1 Data	PTD9	QSPI0_B_DATA3
	QuadSPI1 Chip Select	PTD8	QSPI0_B_CS0_B
	QuadSPI1 Clock	PTD7	QSPI0_B_SCK

5 Revision history

Table 5. Revision history

Rev.	Date	Substantive change(s)
1.0	May 2013	Release for revision G design.
1.1	June 2013	Optional DDR3 self-refresh for Vybrid in LPStop modes added.
1.2	August 2014	Release for revision H design.

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