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# FDD86102LZ

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

100 V, 35 A, 22.5 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 22.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 8$  A
- Max  $r_{DS(on)}$  = 31 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 7$  A
- HBM ESD protection level > 6 kV typical (Note 4)
- Very low  $Q_g$  and  $Q_{gd}$  compared to competing trench technologies
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

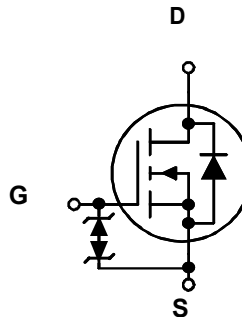
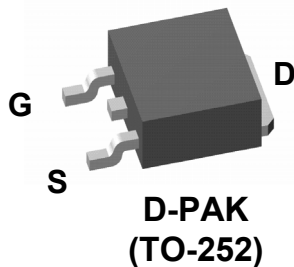


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

### Applications

- DC - DC Conversion
- Inverter
- Synchronous Rectifier



### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	35	A
	-Continuous $T_A = 25$ °C (Note 1a)	8	
	-Pulsed	40	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	84	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	54	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86102LZ	FDD86102LZ	D-PAK(TO-252)	13 "	16 mm	2500 units

FDD86102LZ N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		69		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$		17.8	22.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 7\text{ A}$		23.2	31	
		$V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		31.1	40	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 8\text{ A}$		31		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1157	1540	pF
$C_{oss}$	Output Capacitance			181	245	pF
$C_{rss}$	Reverse Transfer Capacitance			7.7	15	pF
$R_g$	Gate Resistance			0.6		$\Omega$

### Switching Characteristics

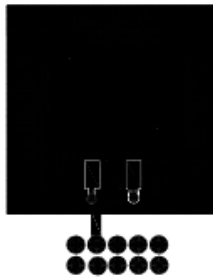
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 8\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6.6	14	ns
$t_r$	Rise Time			2.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			20	32	ns
$t_f$	Fall Time			2.3	10	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		18	26
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 50\text{ V}$ , $I_D = 8\text{ A}$	8.7	13	nC
$Q_{gs}$	Gate to Source Gate Charge			2.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.4		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 8\text{ A}$ (Note 2)		0.82	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 2.6\text{ A}$ (Note 2)		0.75	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		43	70	ns
$Q_{rr}$	Reverse Recovery Charge			43	70	nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a.  $40\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $96\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 13\text{ A}$ ,  $V_{DD} = 90\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

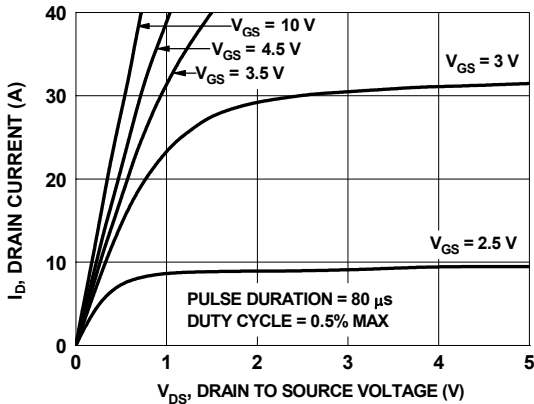


Figure 1. On-Region Characteristics

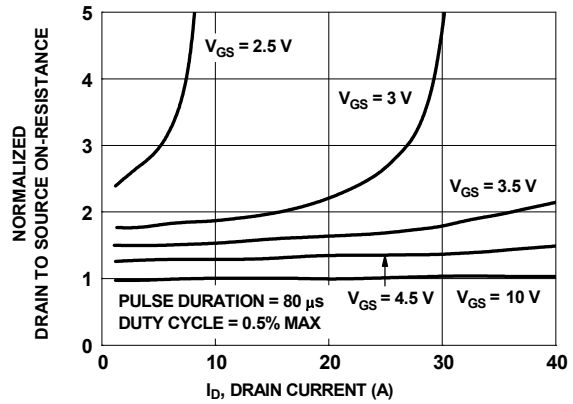


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

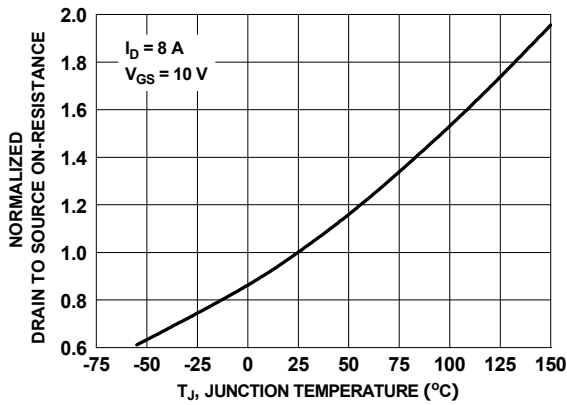


Figure 3. Normalized On-Resistance vs Junction Temperature

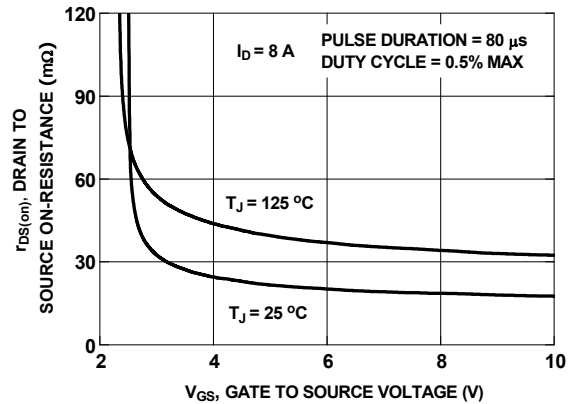


Figure 4. On-Resistance vs Gate to Source Voltage

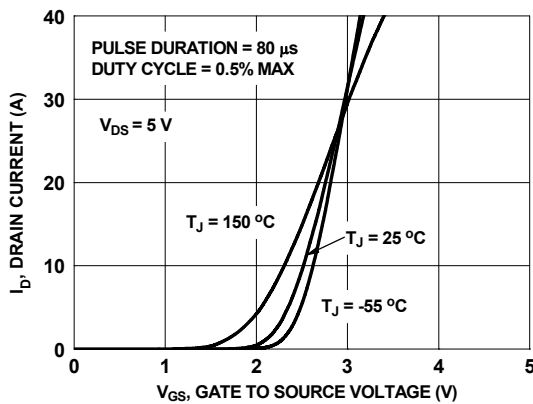


Figure 5. Transfer Characteristics

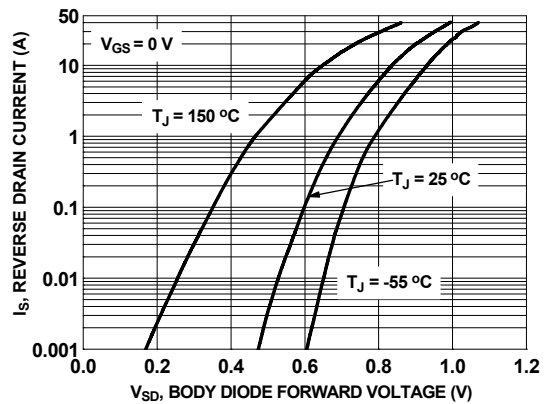
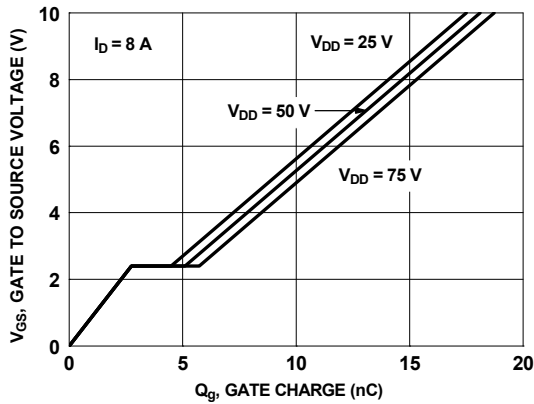
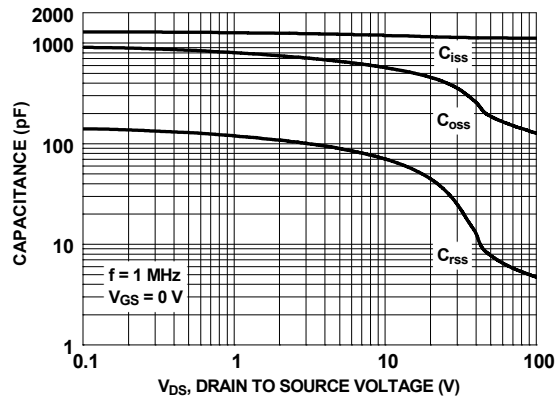


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

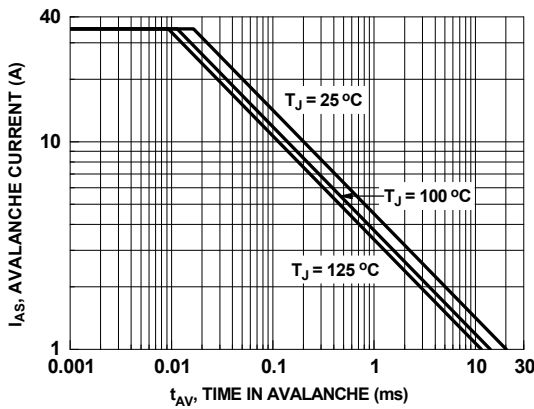
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



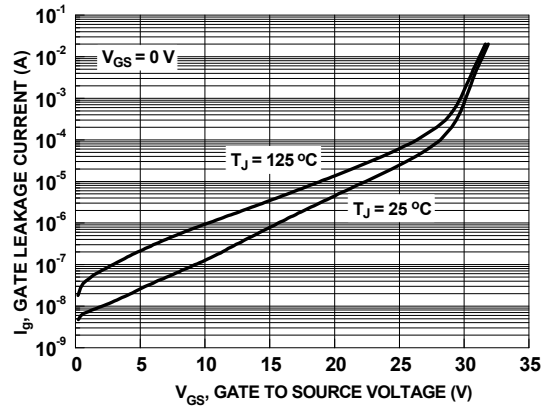
**Figure 7. Gate Charge Characteristics**



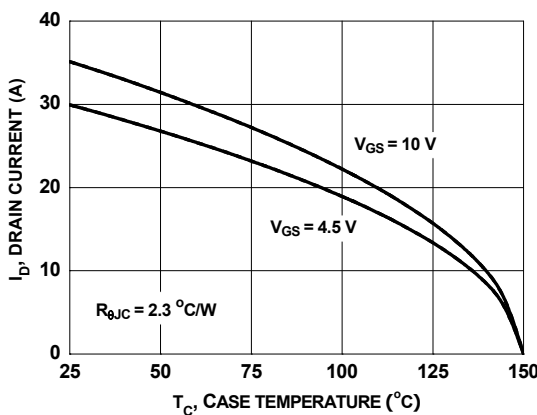
**Figure 8. Capacitance vs Drain to Source Voltage**



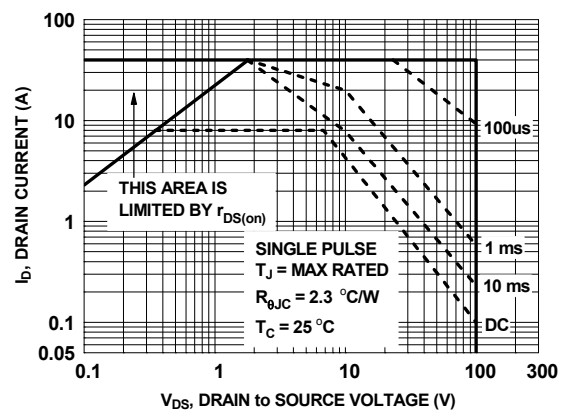
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

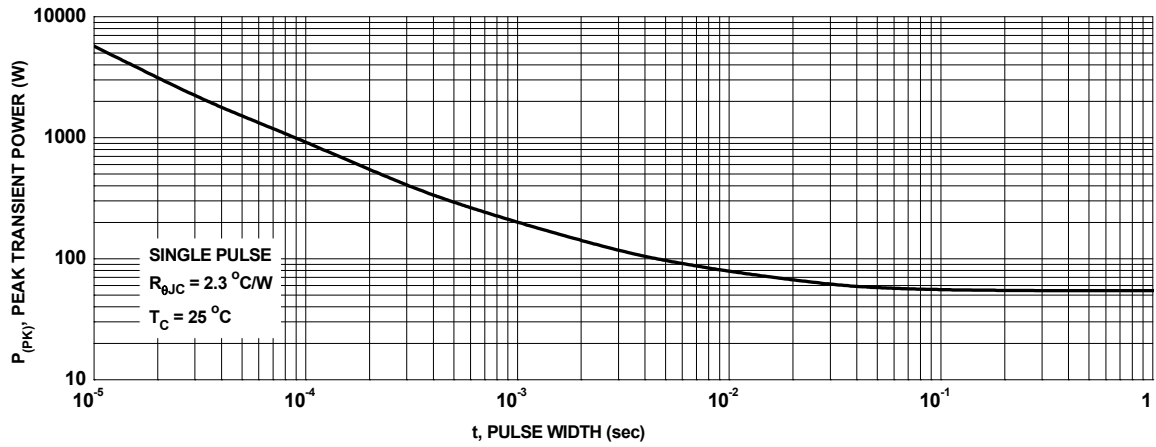


**Figure 11. Maximum Continuous Drain Current vs Case Temperature**

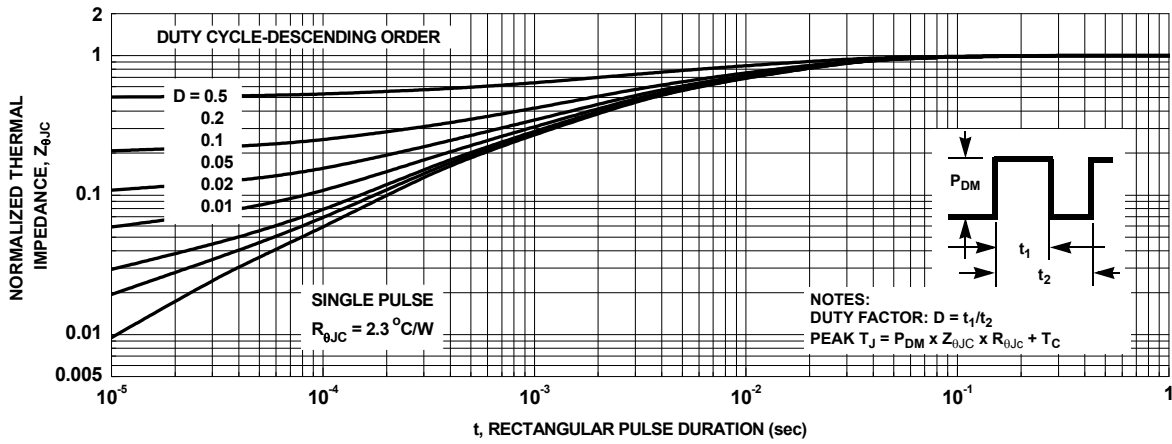


**Figure 12. Forward Bias Safe Operating Area**

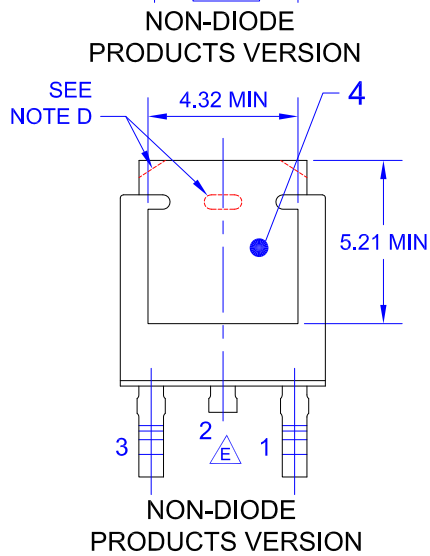
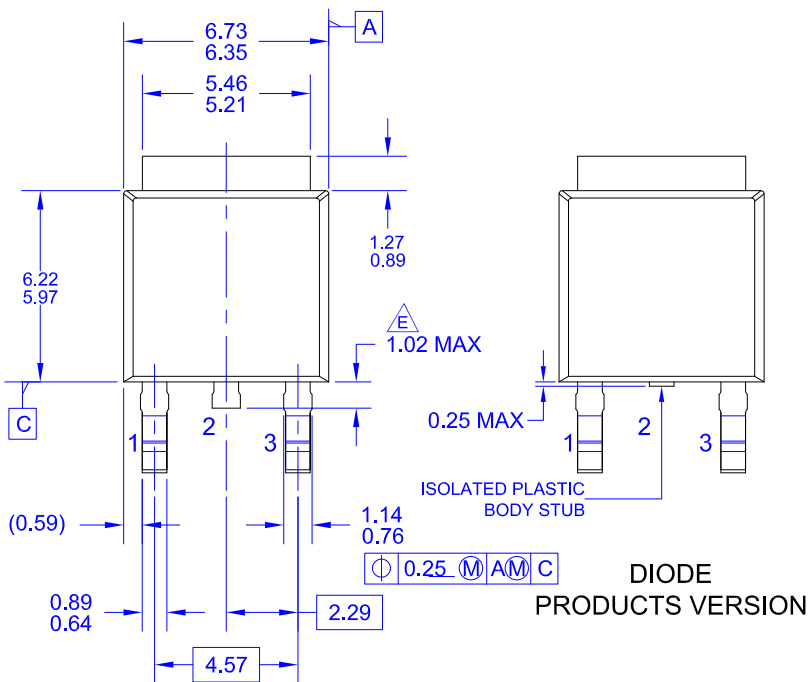
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction-to-Case Transient Thermal Response Curve**



**NOTES: UNLESS OTHERWISE SPECIFIED**

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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