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# FDC3535

## P-Channel Power Trench<sup>®</sup> MOSFET -80 V, -2.1 A, 183 mΩ

### Features

- Max  $r_{DS(on)}$  = 183 mΩ at  $V_{GS} = -10$  V,  $I_D = -2.1$  A
- Max  $r_{DS(on)}$  = 233 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -1.9$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

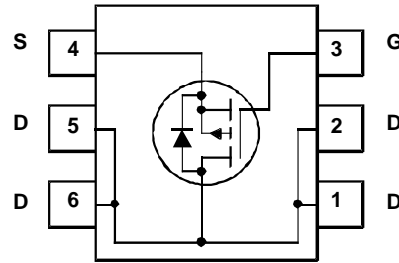
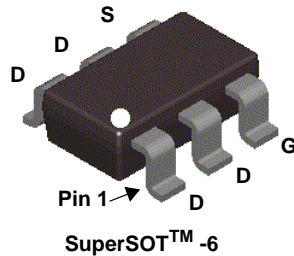


### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- Load Switch
- Synchronous Rectifier



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	-80	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Note 1a)	-2.1	A
	-Pulsed	-10	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	37	mJ
$P_D$	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	30	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.535	FDC3535	SSOT-6	7"	8 mm	3000 units

FDC3535 P-Channel Power Trench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-64		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -64\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}$ , $I_D = -2.1\text{ A}$		147	183	m $\Omega$
		$V_{GS} = -4.5\text{ V}$ , $I_D = -1.9\text{ A}$		176	233	
		$V_{GS} = -10\text{ V}$ , $I_D = -2.1\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		246	307	
$g_{FS}$	Forward Transconductance	$V_{DD} = -10\text{ V}$ , $I_D = -2.1\text{ A}$		6.3		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		659	880	pF
$C_{oss}$	Output Capacitance			49	65	pF
$C_{rss}$	Reverse Transfer Capacitance			24	40	pF
$R_g$	Gate Resistance			5.7		$\Omega$

### Switching Characteristics

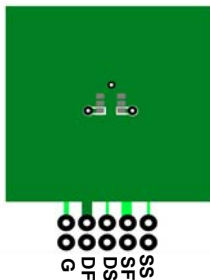
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -40\text{ V}$ , $I_D = -2.1\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6.5	13	ns
$t_r$	Rise Time			3.1	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	38	ns
$t_f$	Fall Time			2.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$		14	20
	Total Gate Charge	$V_{GS} = 0\text{ V to } -4.5\text{ V}$	$V_{DD} = -40\text{ V}$ $I_D = -2.1\text{ A}$	6.8	10	nC
$Q_{gs}$	Total Gate Charge			1.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.7		nC

### Drain-Source Diode Characteristics

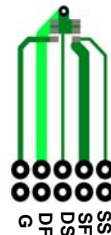
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -2.1\text{ A}$ (Note 2)		-0.81	-1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = -2.1\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		25	40	ns
$Q_{rr}$	Reverse Recovery Charge			23	38	nC

#### NOTES:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



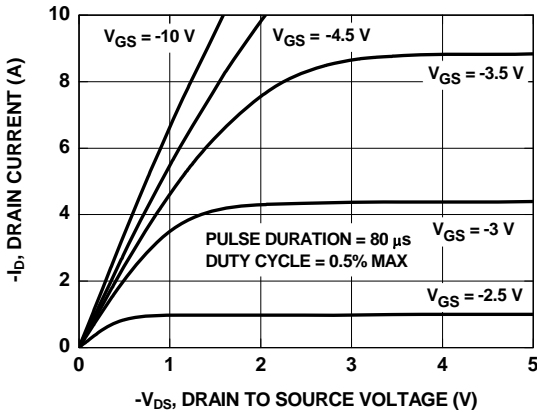
a. 78  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



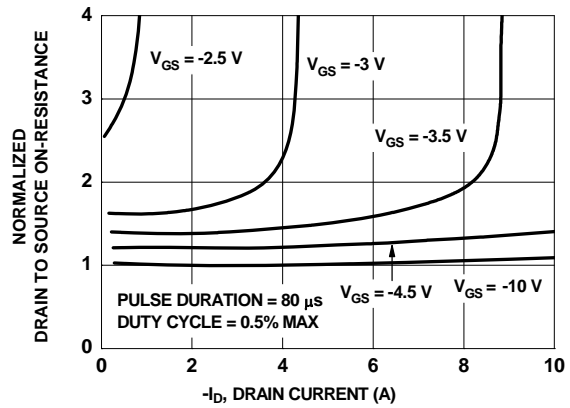
b. 175  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = -5\text{ A}$ ,  $V_{DD} = -80\text{ V}$ ,  $V_{GS} = -10\text{ V}$ .

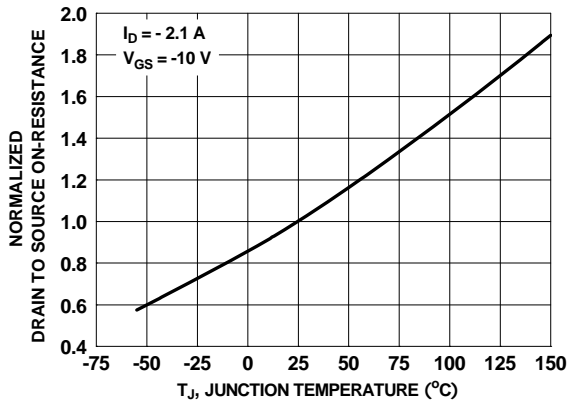
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



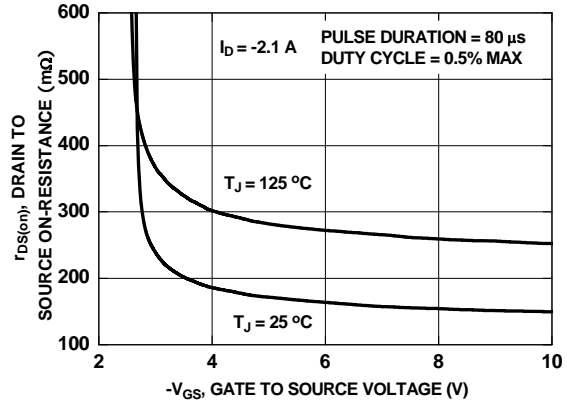
**Figure 1. On-Region Characteristics**



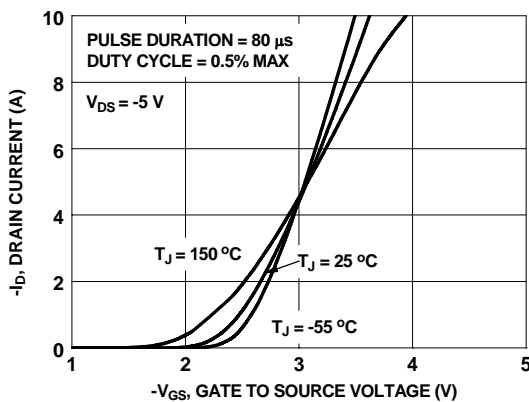
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



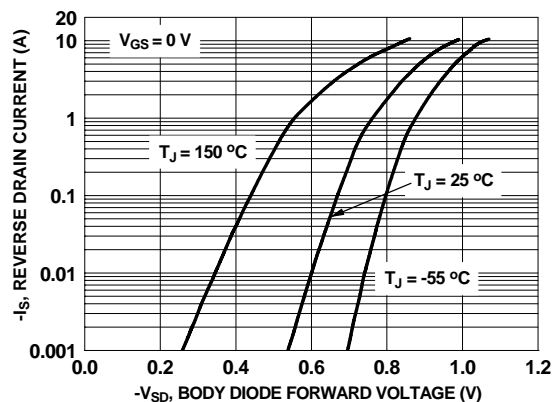
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

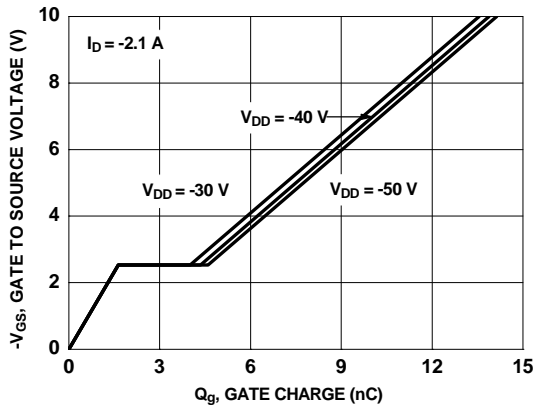


**Figure 5. Transfer Characteristics**

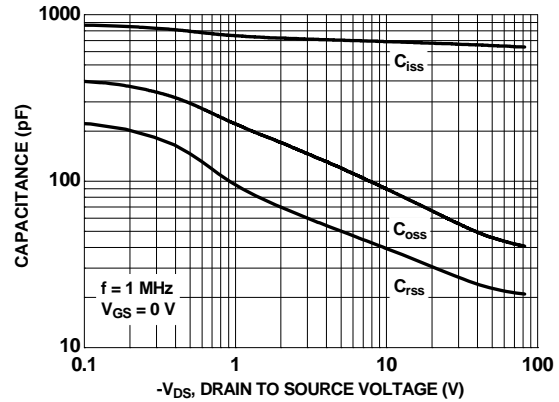


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

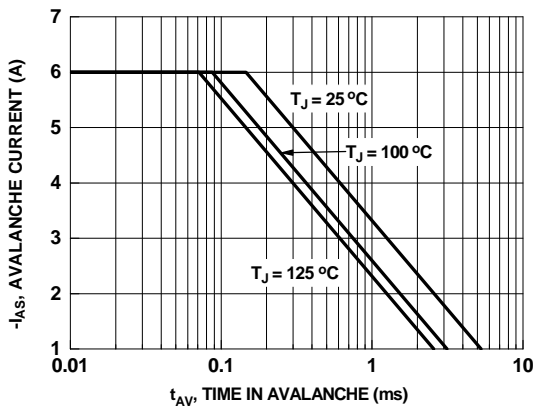
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



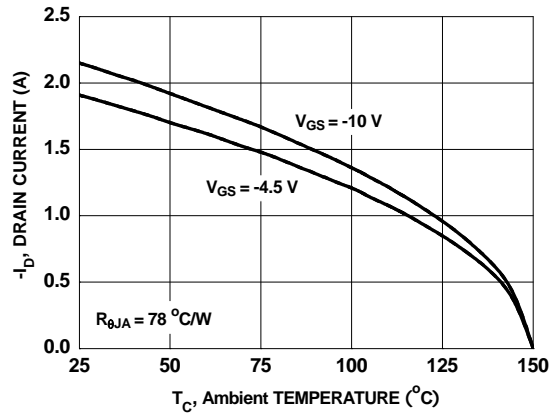
**Figure 7. Gate Charge Characteristics**



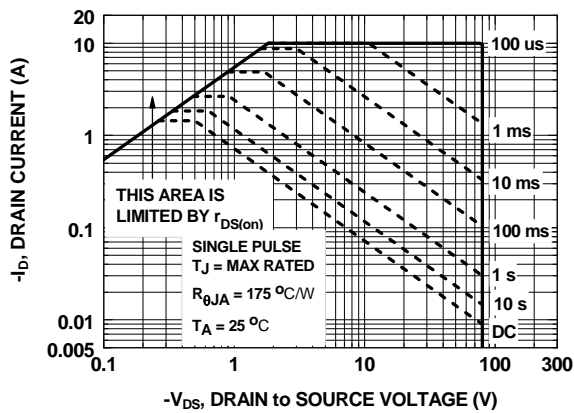
**Figure 8. Capacitance vs Drain to Source Voltage**



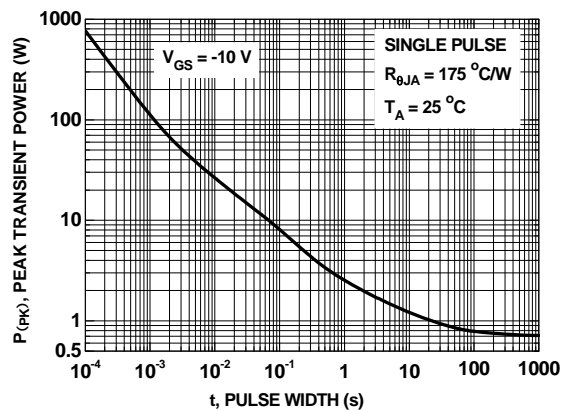
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

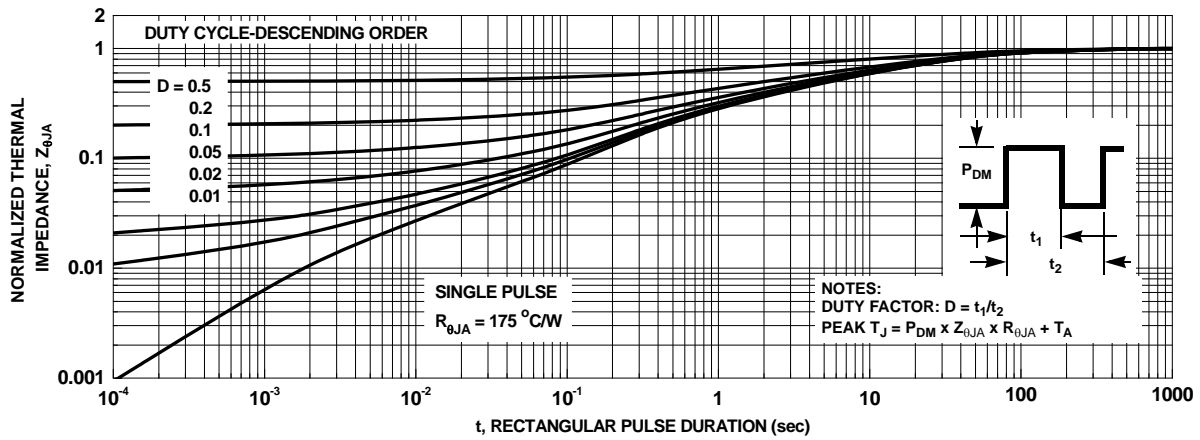


**Figure 11. Forward Bias Safe Operating Area**

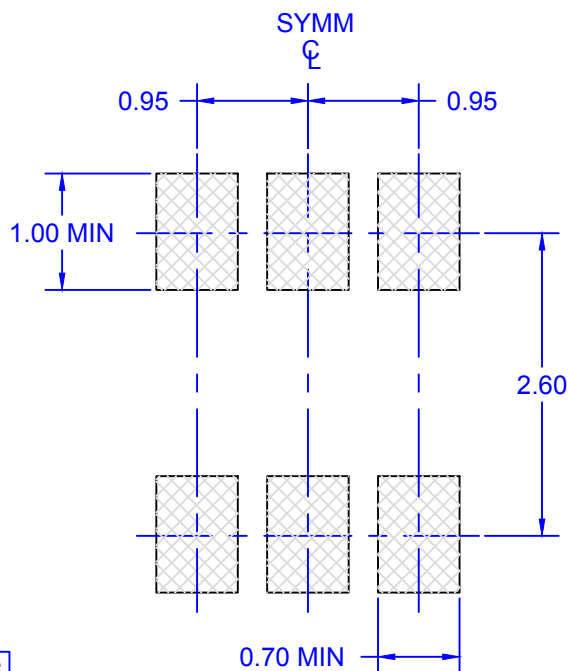
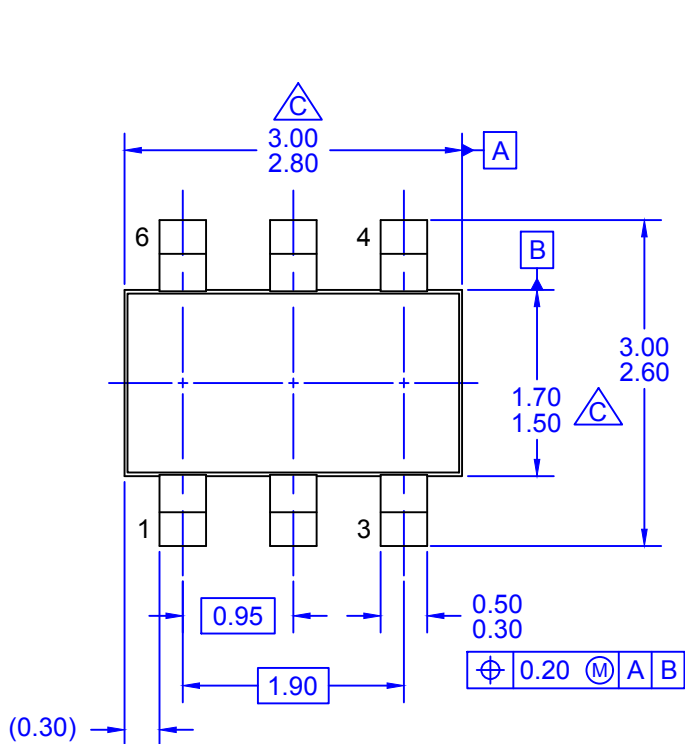


**Figure 12. Single Pulse Maximum Power Dissipation**

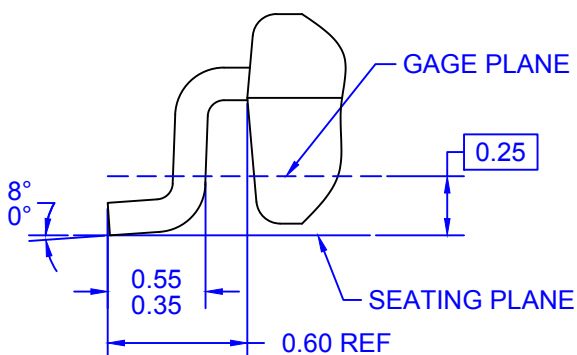
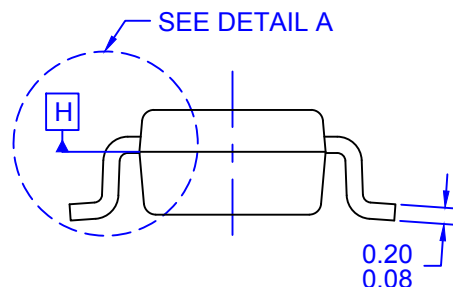
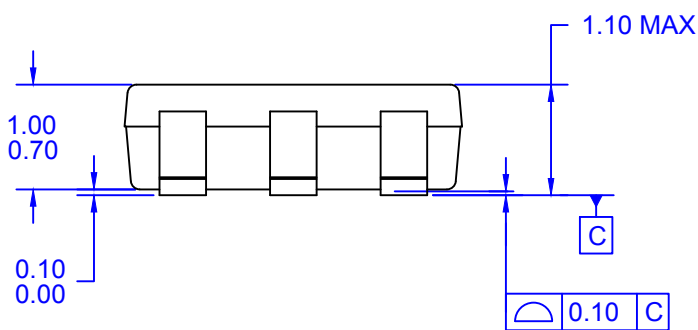
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



LAND PATTERN RECOMMENDATION



DETAIL A  
SCALE: 50X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE E.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25mm PER END. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS ARE DETERMINED AT DATUM H.
  - D) DRAWING FILE NAME: MKT-MA06AREVF

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