CoolMOS™

Detailed MOSFET Behavioral Analysis

Using Parameters Extracted from Models

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Application Note

About this document

Scope and purpose

Low $R_{DS(on)}$ vs. die size is one of the major benefits of **S**uper **J**unction MOSFETs. Smaller silicon influences price and enables higher power density in switching power converters. As the power density in SJ MOSFET grows, so does complexity – both of the construction of the MOSFET and the interaction with application. Of particular interest is the non-linearity of the inherent parasitic MOSFET capacitances.

Most (all) modern SJ MOSFET **D**ata **S**heets are structured in a two-tiered approach; The typical values given in the first, tabular section are reflecting the center-point of the process tuning, while the min and max values listed are often guaranteed values. However, many parameters of interest are functions of operating conditions. These parameters are listed only for a preselected set of conditions. This is why DS have the second tier graphing these parameters. These curves list 2-dimensional data, and show a parameter as a function of a single operating condition change. The presented curves provide great insight into *trends*, but not necessarily into specific behavior. Therefore, it is beneficial to the design engineer to have the ability to generate the data behind the curves for specific operating conditions. This application note aims to arm the power converter designer with appropriate tools to generate – and use – these data.

Attention: ***This Application Note does not guarantee validity of the data exemplified herein, the data of any data sheets or accuracy of Simulation models or Simulation tools. Please refer to specific data sheets and model/Simulation SW documentation for proper guidance on accuracy and/or validity of data used or produced employing the methods described in present Application Note.***

Intended audience

This Application Note aims to enable the power design engineer to extract – and make use of – MOSFET parameters that are not present in the DS. We do this by means of reasonably accurate behavioral models available for download. Our goal is to use SPICE models and simulation tools in versatile ways to enable a deeper level of analytical understanding in power design engineering (than possible with DS alone).

This document will benefit power engineers who are familiar with Mathcad® (or similar math tool) and simulation environments (such as SIMetrix™) that can run models using PSPICE style behavioral syntax. Examples are given throughout intended to enhance the engineer's understanding of MOSFET behavior – specifically Super Junction MOSFETs. Some detailed information and insights are provided on SJ MOSFET behavior in **Q**uasi-**R**esonant Flyback application, which might be of value to power engineers interested in this topology.

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1 Summary

Parameters (similar as given in Data Sheet) were extracted for an example MOSFET via the downloaded simulation model. Examples were given for extracting multiple Datasheet parameters at operating points different than those given in the Datasheet.

Typical loss mechanisms associated with power MOSFETs working in Switched Mode Power Supplies were categorized into four major groups; Conduction-, Gate charge-, E_{oss}- and Switching -loss. For each group, the relevant MOSFET DS parameters were identified, but potential short comings of information in DS were uncovered.

In order to complement HV MOSFET data sheets, where it is not possible to convey all information for all operating conditions, several simulation test benches were developed with the purpose of extracting relevant data at application specific operating conditions (not only the graphed data in the DS at a set of pre-defined operating points) using Infineon's simulation models for HV SJ MOSFETs.

Specific examples were given – using Mathcad® as the basis for theoretic/mathematic analysis – on how to use the extracted data for detailed behavior and loss analysis in SMPS designs. The techniques discussed herein enable quantitative and qualitative analysis and mathematical manipulations not directly possible with conventional circuit simulations and not possible from manual interpretation of DS.

The methods described herein thus significantly extend the use of accurate models from topology/circuit simulation in a specific simulation environment (SIMetrix™) to theoretical/mathematical manipulation and elaboration on a level otherwise unobtainable.

2 How Infineon's MOSFET models are constructed

Infineon's HV SJ MOSFET models are behavioral models based on actual device physics (excluding level 0 models), such that behavior observed in simulation corresponds fairly well to behavior observed in physical application (within normal operating conditions for a typical device). This makes the models particularly useful for simulating real-world behavior for example during switching transitions etc., and can create great value for investigations that are not possible in reality (such as deep understanding of loss mechanisms enabled by integration of instantaneous power in a completely noise free environment as well as non-loading probes with "infinite" dynamic range to name a few). However, with highly accurate behavioral models comes also the possibility to set up test-benches similar to what is used in actual device characterization, and extract valuable parameters as can be found in the second tier of data sheets as detailed above.

Attention: ***This Application Note does not guarantee validity or accuracy of any or all Infineon's MOSFET models or other models or any other vendors' models.***

Models provided by Infineon are not warranted by Infineon as fully representing all the specifications and operating characteristics of the semiconductor product to which the model relates. The models describe the characteristics of typical devices. In all cases, the current data sheet information for a given device is the final design guideline and the only actual performance specification.

Although models can be a useful tool in evaluating device performance, they cannot model exact device performance under all conditions, nor are they intended to replace bread boarding for final verification. Infineon therefore does not assume any liability arising from their use.

Infineon reserves the right to change models without prior notice.

For basic operation of models in a simulation environment, description of different device model levels and guidance on the availability and installation of Infineon's HV SJ MOSFET models, please refer to **[1]**.

3 MOSFET Loss Mechanisms

Usually losses are of greatest interest in theory/modeling of SJ MOSFETs. Power switch related losses in switching power supplies can generally be placed in 4 major contributing categories:

1. Conduction loss: Defined by specific $R_{DS(on)}$ at a given set of operating conditions (e.g. RMS current, $T_{junction}$)
2. Gate-driver loss: This is the energy (from the gate-driver power supply) expended every switching cycle to drive the MOSFET channel on and off
3. E_{oss} loss: this is the energy stored in the output capacitance (C_{oss}) of the switching power MOSFET, which is dissipated in the channel at MOSFET turn-on in hard-switching applications. Efficiency increase by way of preventing E_{oss} losses is a common motivation for soft-switching
4. Switching loss: this is the instantaneous power dissipation in the MOSFET channel during switching transitions caused by simultaneous current through and voltage across the channel of the MOSFET

Of course these four categories can be further elaborated, and additional 2^{nd} order effects may have to be considered when detailing the power switch loss contributions. These effects are outside the scope of this document.

4 Examples of MOSFET parameter extraction

In this section various simulation test bench examples for extracting and using data from Infineon's Level 1 and Level 3 MOSFET SPICE models are shown.

4.1 $R_{DS(on)}$ extraction simulation test bench

Perhaps the easiest parameter to extract is the MOSFET $R_{DS(on)}$. In this example the SPA11N80C3 SJ MOSFET model is used in SIMetrix™ simulation tool. From the DS we get:

Table 1 Excerpt of SPA11N80C3 Data-sheet detailing the typical $R_{DS(on)}$ at 10 V_{GS} gate drive, 25°C junction temperature and 7.1 A drain current

Drain-source on-state resistance	**$R_{DS(on)}$**	V_{GS}=10 V, I_D=7.1 A. T_j=25°C	-	0.39	0.45	Ω
		V_{GS}=10 V, I_D=7.1 A, T_j=150°C	-	1.05	-	

In a simulation test bench, the test conditions given are emulated to reproduce the expected typical $R_{DS(on)}$. As detailed in **[1]** the (Level 3) model has 5 terminals: Gate, source and drain terminals and additional terminals T_j and T_{case}. T_j is meant for monitoring the junction temperature (Voltage in volts represents temperature in °C), whereas T_{case} represents the thermo-electrical equivalent case-node, where a heat sink would normally be connected (and where an R-C network representing the thermo-electrical properties of a specific heat sink would be connected in the simulation schematic). An ideal voltage source can be connected to the T_{case}-pin to represent an ideal heat sink with a temperature (in °C) equal to its voltage.

A very small resistor (1 µΩ to 1 mΩ) between T_j and T_{case} ensures significantly reduced temperature delta from junction to case. This keeps the junction temperature close to the specified case temperature in simulation.

An ideal current source feeds the specified current into the drain, while the gate-source voltage is held at the specified V_{gs} (by an ideal voltage source). We will be using "Analog behavioral non-linear transfer functions" quite extensively throughout this document in order to mathematically manipulate simulation outputs (voltage/current) into the specific values under investigation (resistance, charge, energy, power, etc.). In such a calculation block – ARB1 as shown in Figure 1 – the drain-source voltage is divided by the amplitude of the ideal current source (voltage divided by current) and RC-filtered to get rid of any simulation resolution artifacts. A transient simulation is used instead of a DC operating point forming the basis for further development of the test bench.

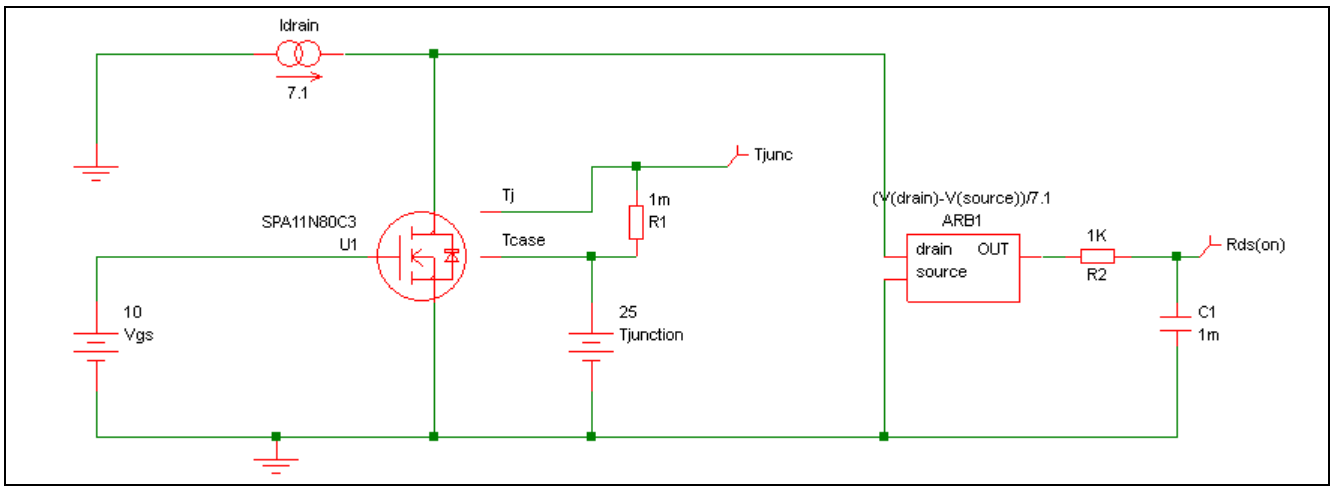


Figure 1 Suggested test-bench for static $R_{DS(on)}$ extraction

The simulation output is expected to show a junction temperature close to 25°C (volts) and an $R_{DS(on)}$ close to 390 mΩ (mV). The simulation result is shown below in Figure 2:

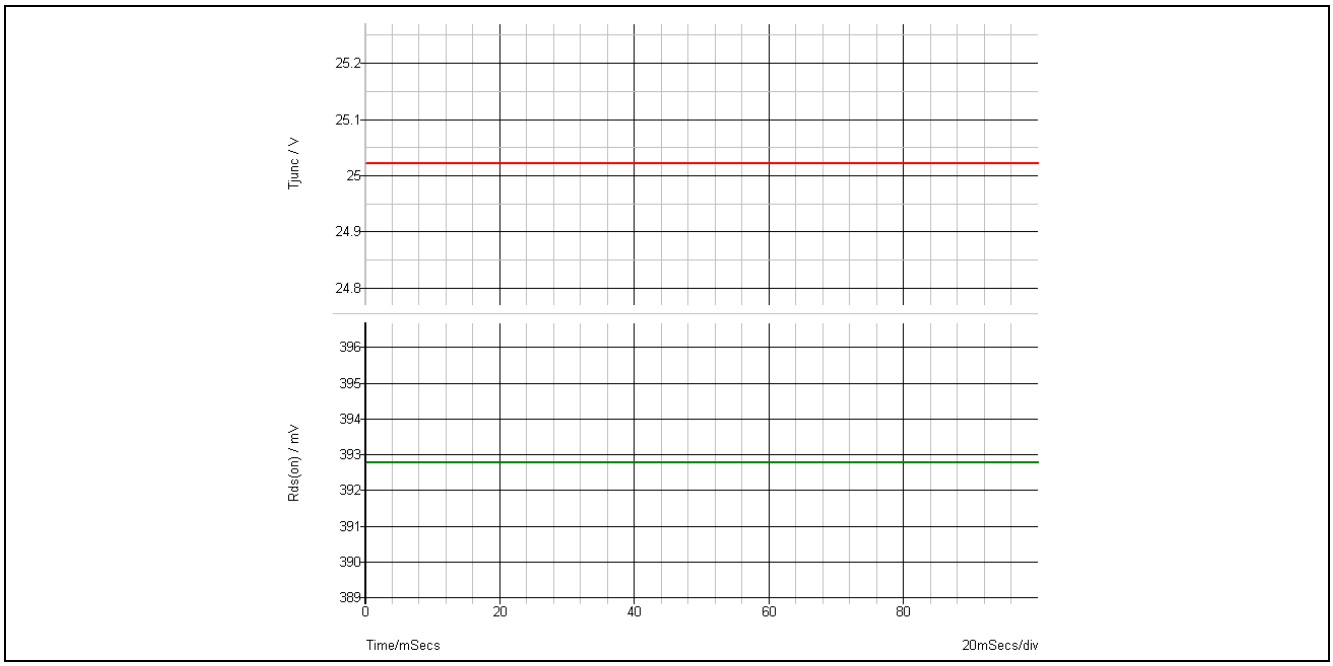


Figure 2 Simulation output proving the typical $R_{DS(on)}$ of ~390 mΩ at T_j=25°C, V_{GS}=10 V and I_D=7.1 A

The basis has now been laid to enhance the parameter extraction, and get the $R_{DS(on)}$ vs. T_j. The transient simulation can be run with a sweeping voltage instead of constant 25 V at the T_{case}. If T_{case} voltage (and by extension T_j) is swept from 0-150 V in exactly 150 ms, then the $R_{DS(on)}$ at t=0 s corresponds to $R_{DS(on)}$ at T_j=0°C, and at t=1 ms corresponds to $R_{DS(on)}$ at T_j=1°C etc. In this case we need to remove – or make sufficiently small – the RC filter on $R_{DS(on)}$ measurement pin.

The simulation output in that case becomes rather useful:

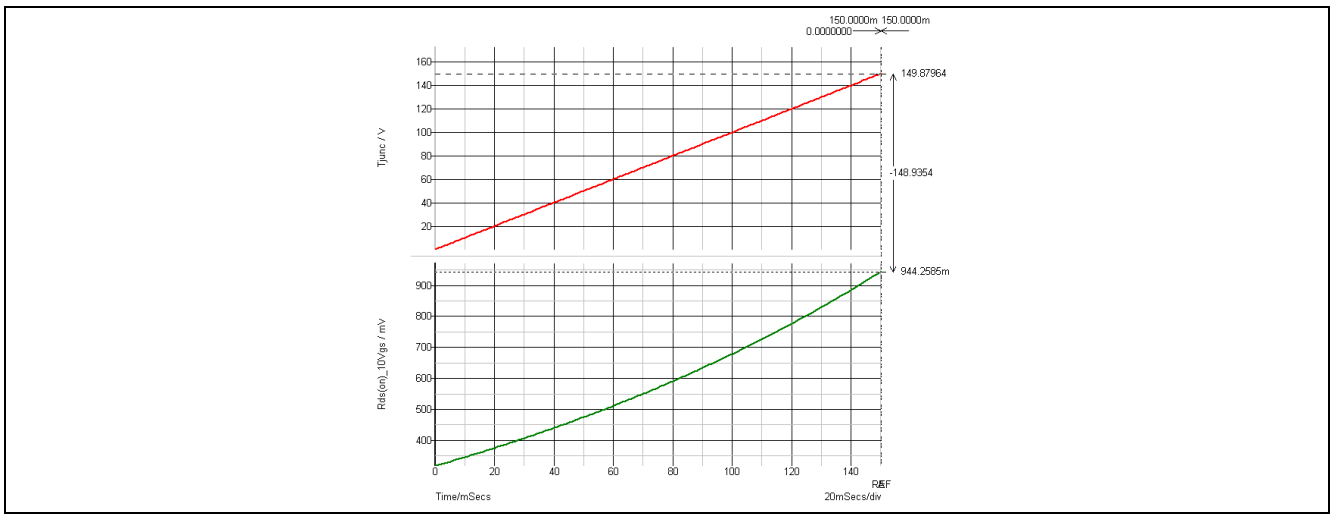


Figure 3 Extracted $R_{DS(on)}$ vs. junction temperature (T_j)

Now we can observe the ~1.05 Ω $R_{DS(on)}$ given in DS at 150°C under conditions that are otherwise the same.

Depending on simulation tool, the data (to generate the graph) is stored and can be retrieved and exported (i.e. to MS Excel®. The resolution of the exported data is determined by the simulation parameters. The data which can now be used as a look-up table provides more accurate estimation of the $R_{DS(on)}$ than estimations based on reading a curve in the DS. Moreover, the data can be imported into math programs (such as Mathcad®, which will serve as the example **S**oft-**W**are throughout this document) and used for dynamic calculations with junction temperature (or other chosen stimulus) as an input. Since some circumstances might be different in a particular application (One could possibly want to investigate consequences of driving with lower gate-voltage or drain-current for example), the influence of these conditions on the parameters are easily investigated and data can be extracted at other operating points.

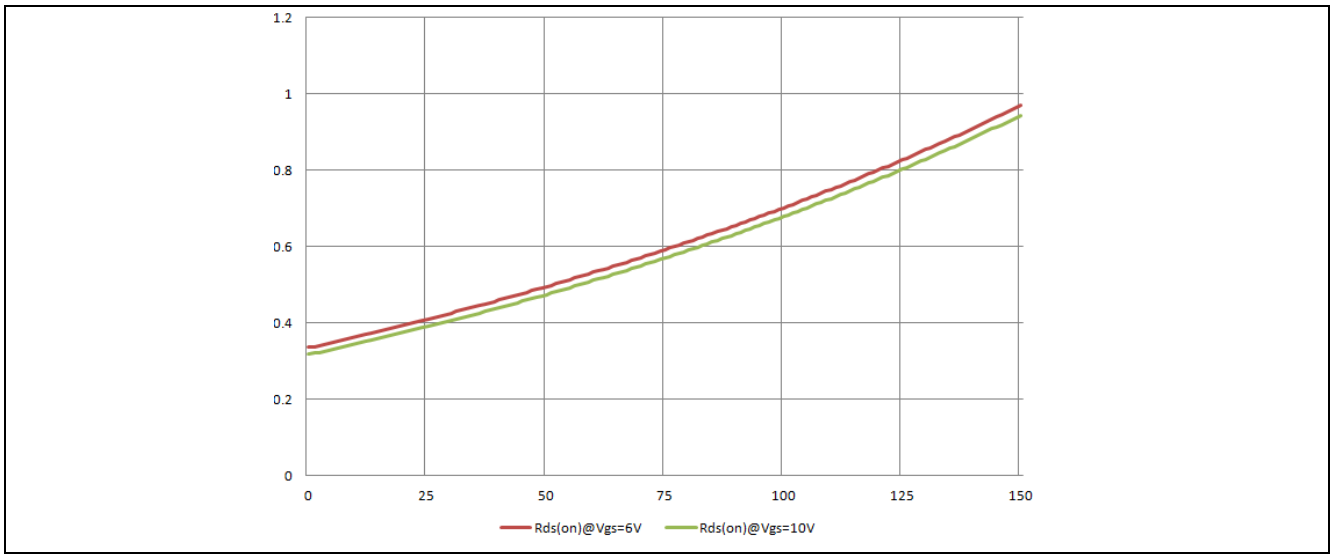


Figure 4 Example Excel® chart with imported $R_{DS(on)}$ vs. T_j data for 6 V gate drive and 10 V gate drive

In the excel data, the difference in $R_{DS(on)}$ at 25°C whether driven by 6 V_{GS} or 10 V_{GS} can be easily determined:

Table 2 As an example, $R_{DS(on)}$ at 25°C can typically be expected to increase from 390 mΩ to 410 mΩ for SPA11N80C3 if driven to 6 V_{GS} rather than 10 V_{GS}

Time [s]	T_{junc} [°C]	$R_{DS(on)}$ @V_{GS}=6 V [mΩ]	$R_{DS(on)}$ @ V_{GS}=10 V [mΩ]
0.023	23	0.403	0.384
0.024	24	0.406	0.387
0.025	25	0.410	0.390
0.026	26	0.413	0.394
0.027	27	0.416	0.397

With a reasonable estimation of the maximum working junction temperature in the application, a more accurate (than reading a graph in DS) estimation of the typical $R_{DS(on)}$ at that particular junction temperature can perhaps inspire more confidence in the theoretically derived conduction loss ($I_{RMS}^2 \cdot R_{DS(on)}$ loss).

4.1.1 Exploiting additional model parameter $dR_{DS(on)}$ for Worst Case (WC) losses

Referring to [1], the model can be made to emulate the corner case $R_{DS(on)}$ by selecting "additional parameter" delta-$R_{DS(on)}$ as shown below in Figure 5.

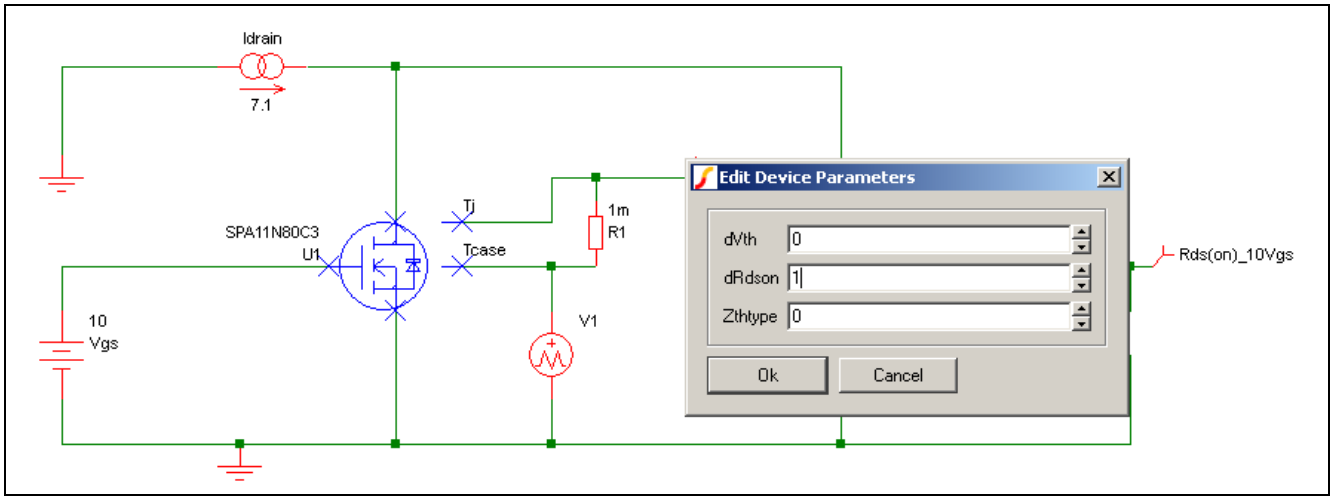


Figure 5 Setting the model to reflect maximum $R_{DS(on)}$ for WC investigations

The simulation output can again be imported for easy manipulation and usage, and for example, the max $R_{DS(on)}$ at 100°C T_j can be used for loss evaluation at harsh operating conditions with a device of extreme tolerance.

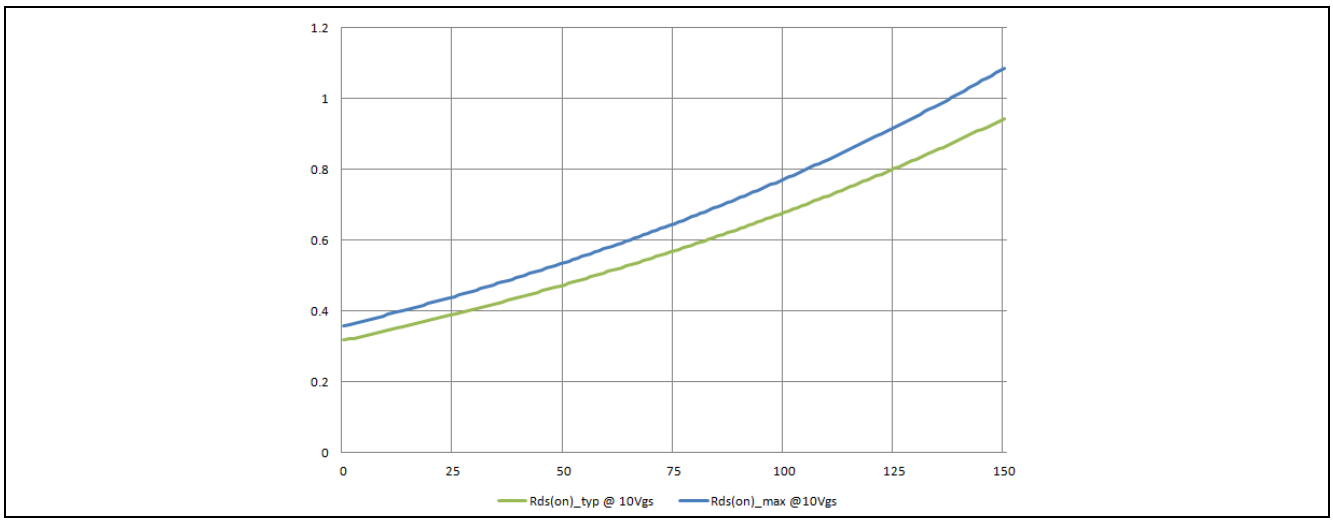


Figure 6 $R_{DS(on)}$ typical and max vs. temperature for SPA11N80C3 (V_{GS} = 10 V)

The absolute value for $R_{DS(on)}$ at T_j = 100°C of SPA11N80C3 is thus estimated from the model to be

- $R_{DS(on)\_typ}$ = 679 mΩ for T_j = 100°C and V_{GS} = 10 V and
- $R_{DS(on)\_max}$ = 773 mΩ for T_j = 100°C and V_{GS} = 10 V

4.1.2 Exploiting additional parameter dV_{th} for WC analysis

In some scenarios it could be beneficial (or even necessary) to drive the MOSFET with a lower driver voltage (with a penalty to $R_{DS(on)}$) as suggested above. We could imagine this might be worth-while in light-load conditions, where the $R_{DS(on)}$ is less significant and the driver-losses themselves become more influential on overall losses. First we develop the test-bench to be more universal by utilizing parameterization in SIMetrix™.

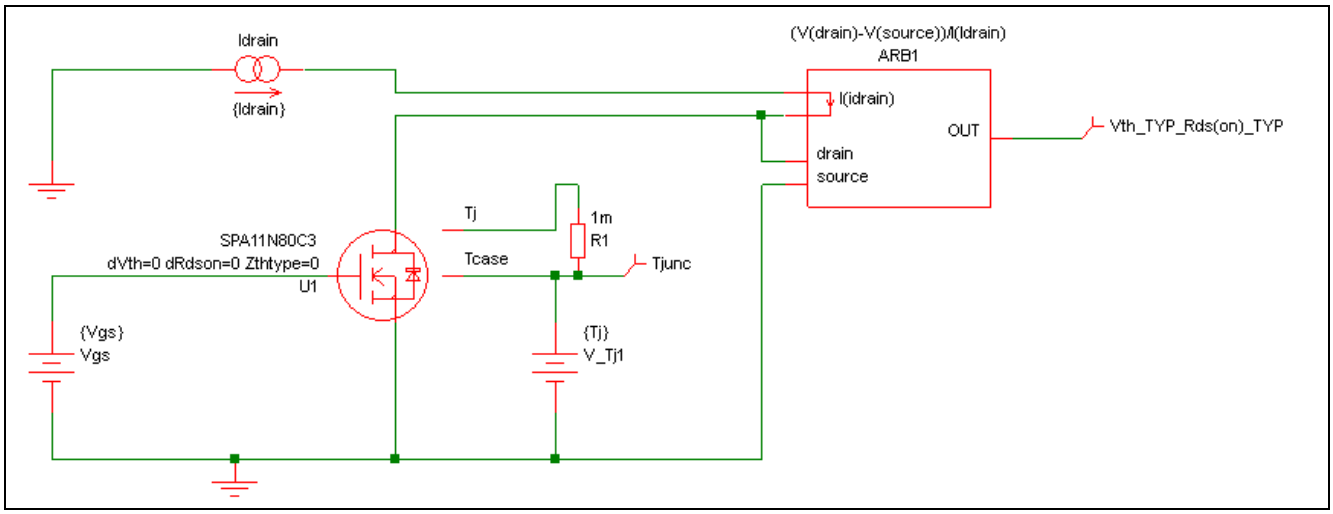


Figure 7 Universal simulation test bench for various $R_{DS(on)}$ investigations

Now we can do a “DC sweep” of drain current (Idrain) with various V_{GS} to learn how $R_{DS(on)}$ changes with drain current at various gate-source voltages.

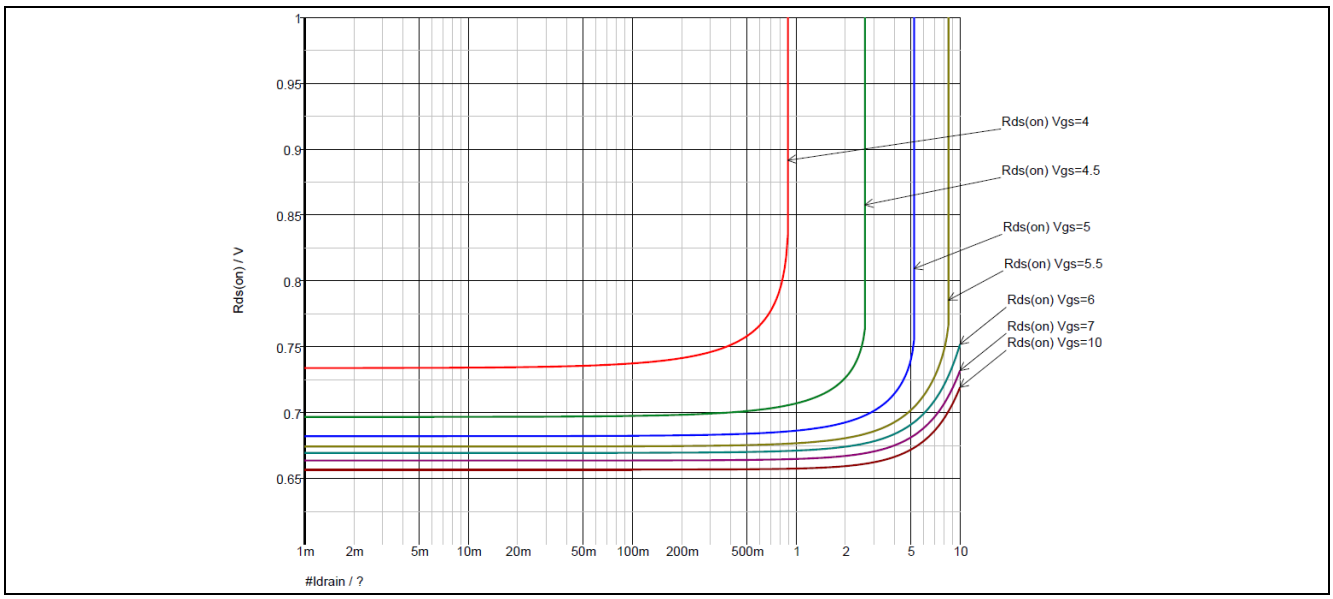


Figure 8 Simulation output when DC sweeping drain-current logarithmically from 1 mA to 10 A at T_j=100°C for various V_{GS}

If at light load the maximum targeted drain-current is 1 A and $R_{DS(on)}$ can be allowed to increase to 1 Ω, we can see that a typical MOSFET will perform satisfactory when driven with only 4.5 V_{GS}.
Let us now change the model's "extra parameter" dV_{th} to its MAX value and evaluate the $R_{DS(on)}$ vs. V_{GS} at various junction temperatures for a drain current of 1 A.

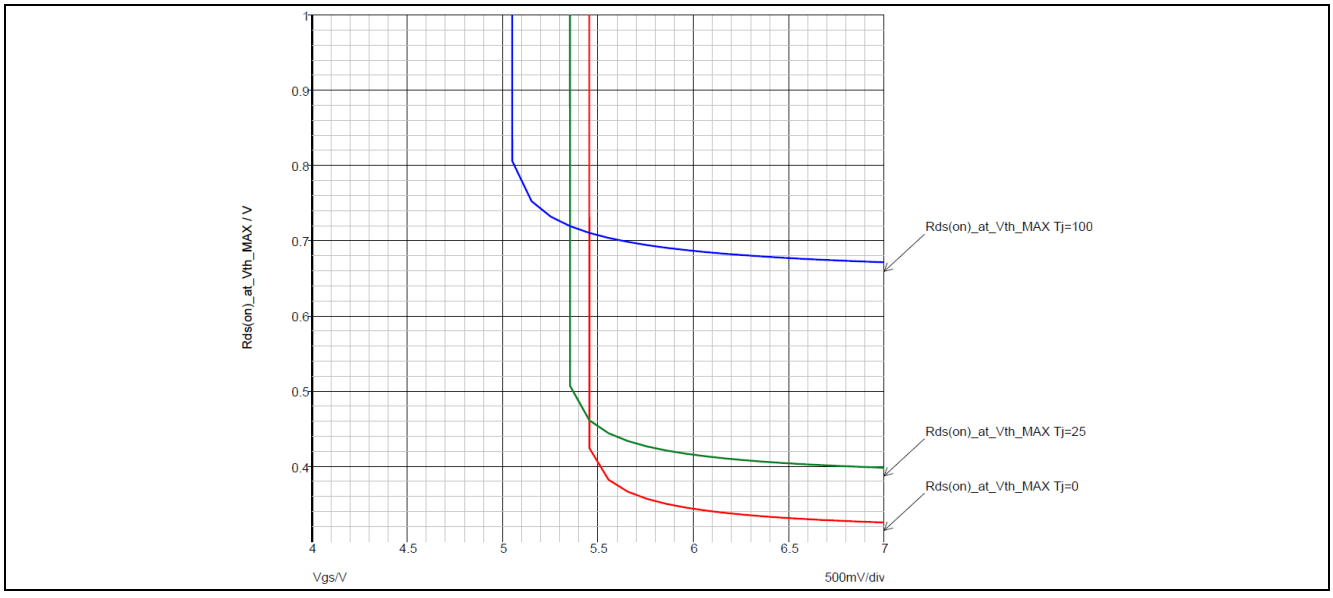


Figure 9 Simulation output when sweeping V_{GS} from 4 V to 7 V for various T_j at I_{DS}=1 A and threshold voltage set to MAX (dV_{th}=1)

We can now see (Figure 9) that the worst case occurs at low temperature (T_j=0°C) and on a corner part (V_{th} at DS specified MAX). The minimum necessary V_{GS} is in fact 5.5 V rather than the 4.5 V one might have suggested based on typical part spec for exemplified SPA11N80C3.

Analysis of worst-case $R_{DS(on)}$ at lower temperatures is also relevant even if there is no intention to lower the V_{GS} at lighter loads for energy savings. Let us imagine a controller IC with a built-in driver working in a peak-current control topology using a current-sense resistor. A typical example of such is the lower power Flyback.

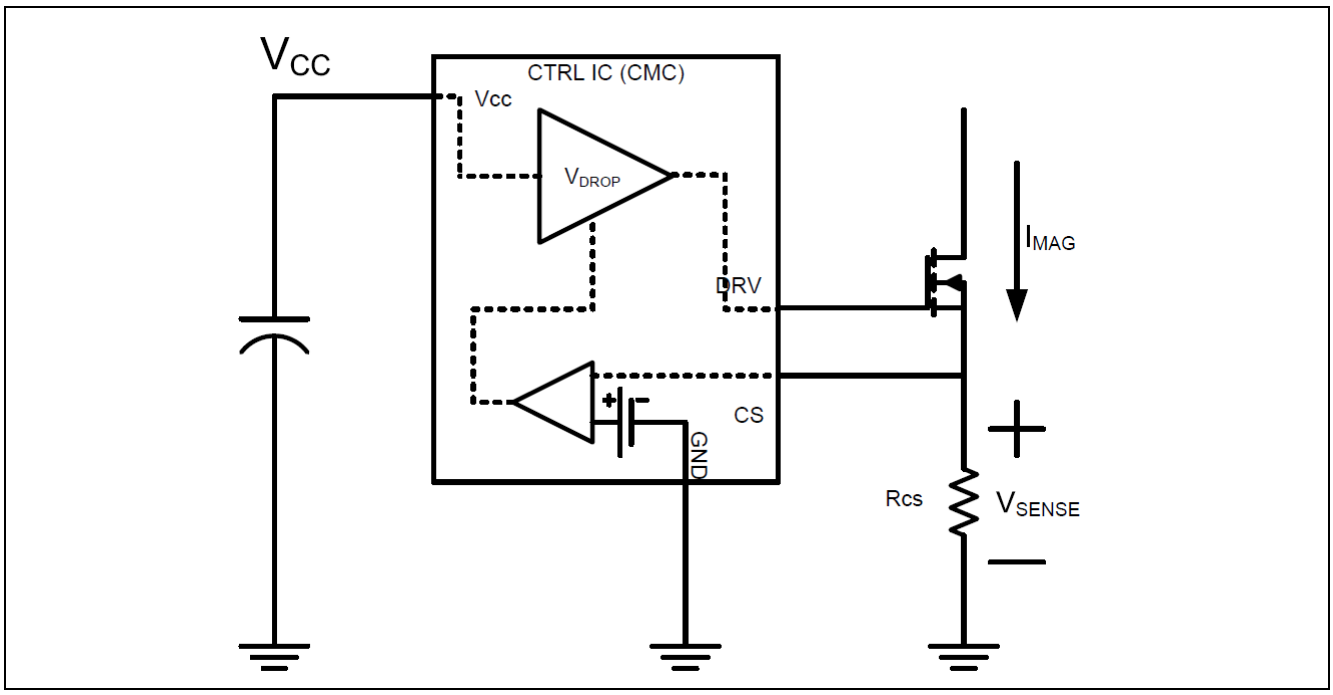


Figure 10 Typical controller/driver combo using current-sense resistor for peak current control

Let us assume a controller IC with **U**nder**V**oltage **L**ock-**O**ut set to a minimum of 6.2 V (not unusual). A normal specification for the maximum voltage drop between V_{CC} and DRV (V_{DROP}) is ~500 mV. At a desired (maximum) controlled peak current of 1 A the R_{CS} is now constrained, since the minimum allowable V_{GS} is ~5.5 V. This leaves only 200 mV of peak (**F**ull-**S**cale) voltage across R_{CS} for proper control (R_{CS} < 200 mΩ) – a constraint that could result in increased sensitivity to noise (more jitter) or in extreme situations even a zero-solution space for dimensioning of the system.

4.2 Gate charge extraction simulation test bench

With MOSFET power loss Category 1 from Chapter 3 (conduction loss) already addressed attention is focused on category 2 (gate-driver loss). A quick estimate uses the given DS value for Q_g (total gate charge) as shown in example of Figure 13. Charge is converted to energy by utilizing $E = ½ Q \cdot V$. The energy is multiplied by 2 since it [the energy] is moved into a capacitor through a series resistor (Equal amount of energy dissipated in resistor and stored in capacitor). Evaluating in terms of power at a given switching frequency yields a rough estimate of loss. Looking again at SPA11N80C3 as an example, we get the DS values shown below in Figure 11.

Gate Charge Characteristics

Gate to source charge	Q_{gs}	V_{DD}=640 V, I_D=11 A, V_{GS}=0 to 10 V	-	8	-	nC
Gate to drain charge	Q_{gd}		-	30	-	
Gate charge total	Q_g		-	64	85	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

Figure 11 Excerpt of SPA11N80C3 DS detailing Gate Charge Characteristics

If driving V_{GS} to 10 V, we could thus expect an energy expenditure of

$$E_{g\_drv} \approx \frac{1}{2} \cdot Q_g \cdot V_{gs} \cdot 2 = 640 \ nJ[typ]$$

Multiplying with switching frequency will give a good first-order approximation of the resulting power dissipation based on gate-charge. However; there could be many reasons for extracting the gate-charge characteristics from the model for detailed evaluation at specific operating conditions in e.g. a Mathcad® work-sheet, where evaluations are made in a mathematical/theoretic environment (rather than simulation environment). Some such examples will be given later in this subsection.

Figure 12 shows V_{GS} as a function of Gate Charge.

In order to extract V_{GS} vs. Q_g from the model, a test bench is set up to emulate the same conditions given for switching voltage and –current. The bench will utilize the relationship

$$i(t) = \frac{dQ(t)}{dt} \Rightarrow Q(t) = \int i(t)dt$$

to arrive at a linearly increasing charge vs. time (when keeping current constant), and V_{GS} will be the measured value (plotted vs. charge).

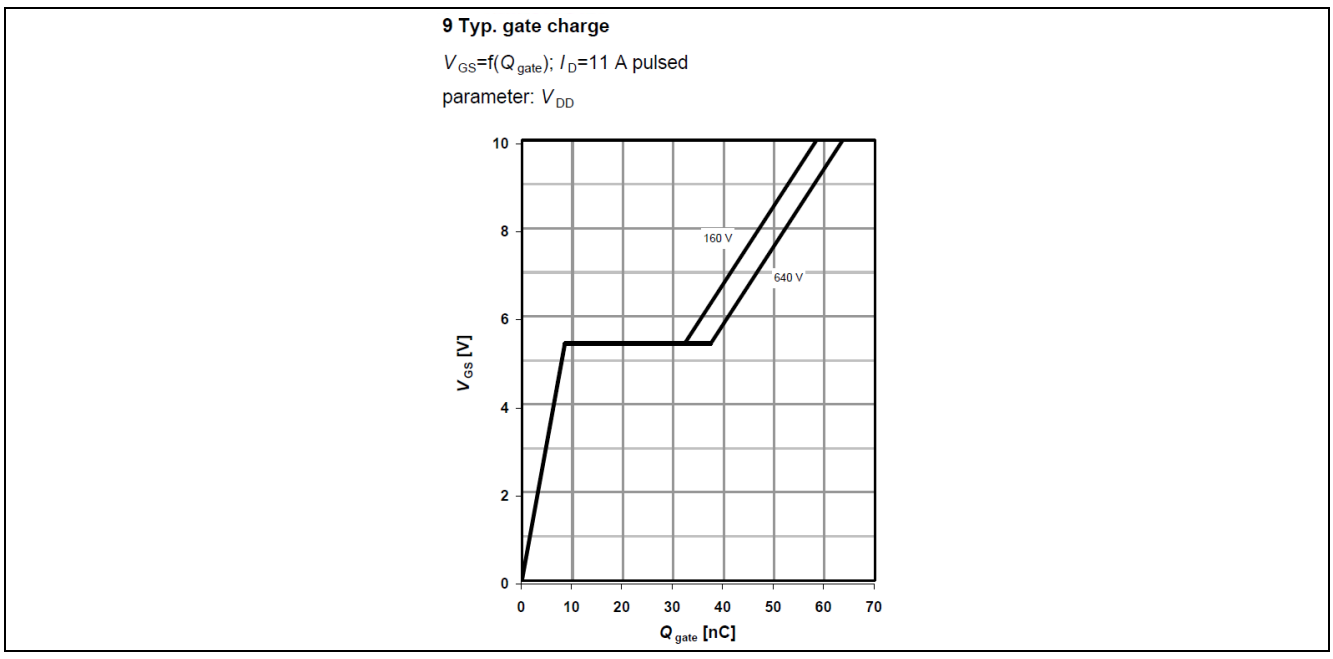


Figure 12 Excerpt of SPA11N80C3 DS detailing the graphical representation of typical V_{GS} vs. Q_g

Examples of MOSFET parameter extraction

One proposed test bench implemented for the SPA11N80C3 in SIMetrix™ is shown below in Figure 13.

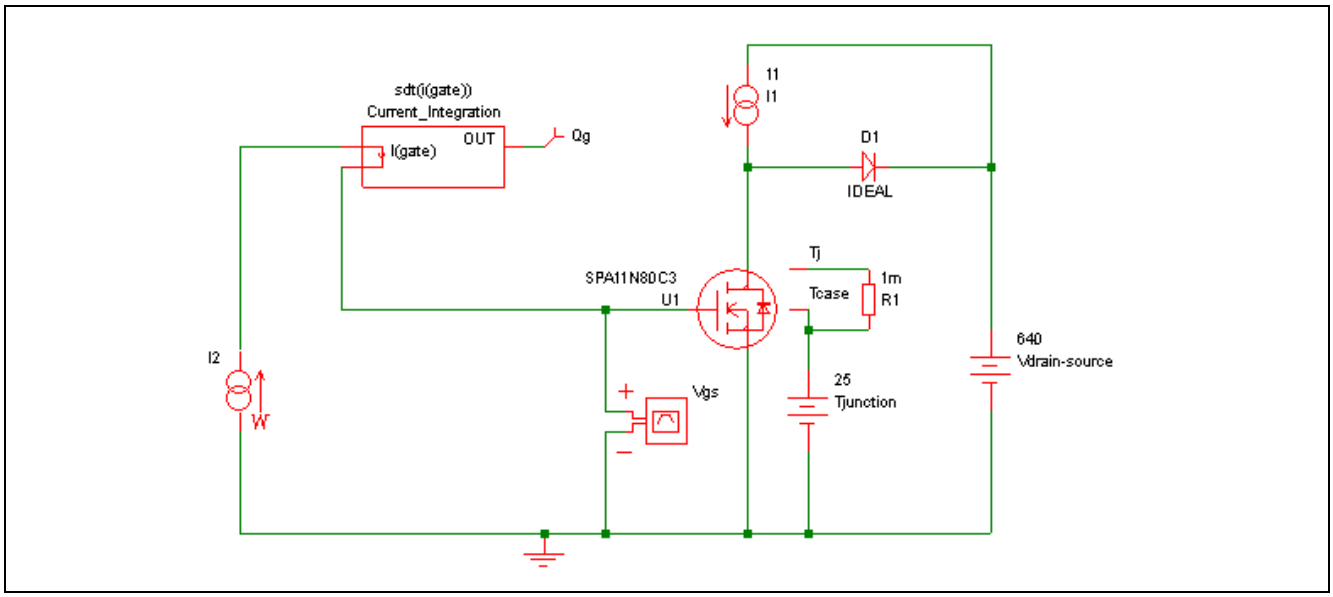


Figure 13 One proposed test bench for extracting V_{GS} vs. Q_g at specified conditions

The gate-current has to be an appropriate value in order not to cause errors – e.g. the gate resistor internal to the MOSFET would represent a significant gate-source voltage error (non-charge related) at a high gate current. For this particular simulation, a gate current of 1 mA is selected. This also means the accumulated charge will be a factor 1000 different in magnitude than the time; and thus time in µs represents charge in nC.

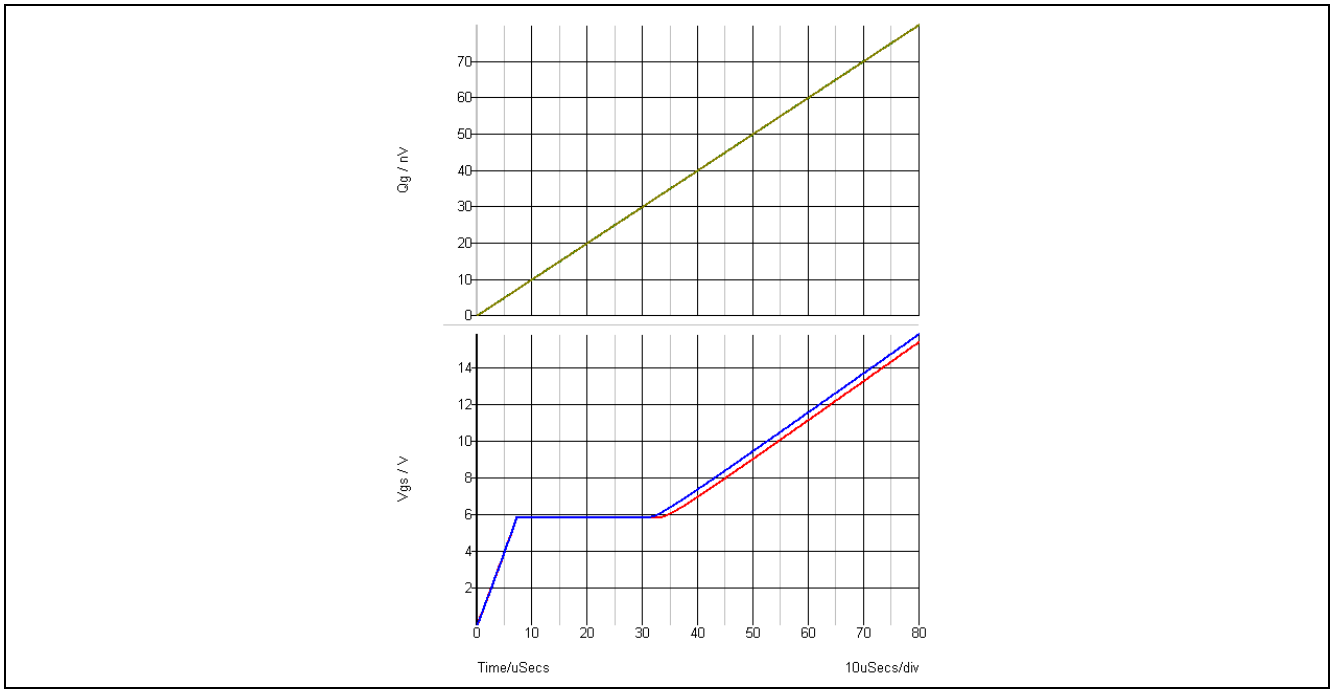


Figure 14 Simulation output from gate charge test bench; blue is V_{DS}=160 V and red is V_{DS}=640 V

Examples of MOSFET parameter extraction

Effects of switching the different voltages are clearly seen in the simulation result as well as the equivalent graph in DS (compare DS graph in Figure 12 with Simulation graph in Figure 14). The gate-charge data is captured with a 0.1 nC resolution in this example (simulation options: output data at 100 ns intervals) in a simulated application, where the drain-current is 1 A and 275 V is switched (quasi-arbitrarily chosen values). The data is imported in Mathcad and converted from array form to function form. This allows easy plotting in a 2-D plot (see Figure 15 below) similar to simulation and DS graphs shown above.

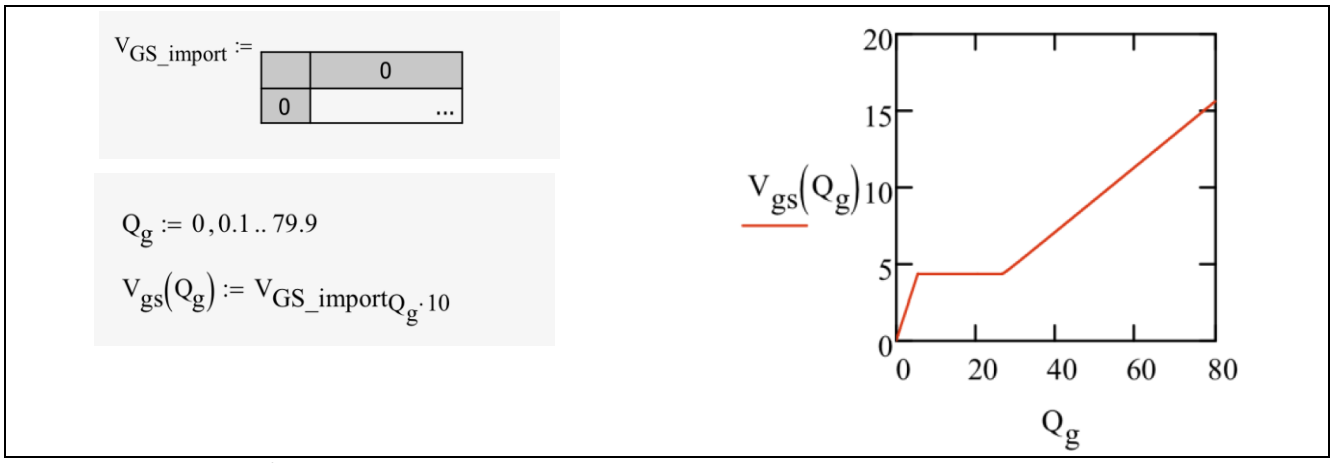


Figure 15 Mathcad® example import, conversion and plotting of V_{GS} vs. Q_g

The data is kept unit-less for easier operation in Mathcad®, but of course units could be put on all values that are not used for indexing a vector or matrix or argumenting a function call.

The data can now be utilized to mathematically retrieve important information, such as gate-source turn-on waveform, turn-on time delay etc. In this example, we will first retrieve the plateau voltage (a function of switched drain-current) as well as Q_{GS} and Q_{GD} as given in DS (see Figure 11), albeit for a different set of switching current/voltage than that of the DS given values. One possible method of doing so is shown in Figure 18 below:

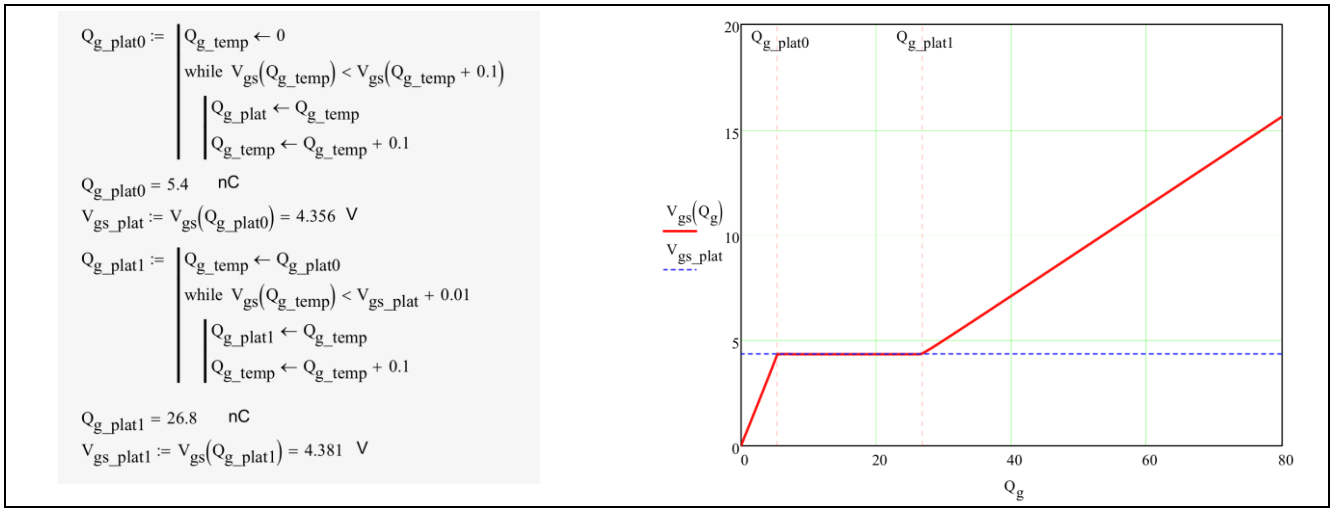


Figure 16 One possible Mathcad® implementation and graph of MOSFET gate characteristics

Examples of MOSFET parameter extraction

Of course all charges (variables Q_X) have the unit nC and all the voltages (V_X) have unit V. From the derived variable values above, Q_{GS} and Q_{GD} can be determined for the particular operating condition simulated in the test bench, since Q_{GS} is defined as the gate charge at the beginning of the Miller plateau and Q_{GD} is defined as the charge at the end of the Miller plateau less Q_{GS}. We therefore get

$$Q_{gs} := Q_{g\_plat0} = 5.4 \quad nC$$

$$Q_{gd} := Q_{g\_plat1} - Q_{gs} = 21.4 \quad nC$$

(both in nC), which are clearly smaller values than the DS specified ones due to the amplitude of the switched voltage and current. It is also possible by similar methodology to derive the total gate charge at targeted V_{GS}. One could e.g. contemplate driving to a different voltage than the DS specified 10 V. If driving to a higher (than 10 V) V_{GS}, the value cannot even be read in the DS, since the curve is only graphed until 10 V. We find

$$VGS := 12 \quad V$$

$$Q_{g\_VGS} := \left| \begin{array}{l} Q_{g\_temp} \leftarrow 0 \\ \text{while } V_{gs}(Q_{g\_temp}) < VGS \\ \quad \left| \begin{array}{l} Q_{g\_temp} \leftarrow Q_{g\_temp} + 0.1 \\ Q_{g\_VGS} \leftarrow Q_{g\_temp} \end{array} \right. \end{array} \right.$$

$$Q_{g\_VGS} = 63 \quad nC$$

We could thus typically expect a total gate charge of 63nC for the SPA11N80C3, when driving it to 12 V_{GS} and switching 275 V_{DS}.

If we considered driving the MOSFET from an ideal 12 V voltage source through a 10 Ω external gate resistor as an example, we could reproduce the estimated the driving waveforms based on the extracted gate-charge data by assuming an RC filter response to a 12 V input step voltage in the time domain (assuming the input capacitance is constant until the Miller Plateau is reached; which is a fair assumption).

The DS gives an internal gate resistance (for the example part, SPA11N80C3) of 1.2 Ω as shown in Figure 17.

Gate resistance	R_G	f=1 MHz, open drain	-	1.2	-	Ω

Figure 17 Excerpt from SPA11N80C3 DS tabular section showing typical internal gate resistance

Let us derive the equivalent *time-related* gate-source and total input capacitances by utilizing

$$C_{tr} = \frac{dQ}{dv}$$

On the Miller plateau, the gate current is constant and we can utilize:

$$I(t) = \frac{dQ(t)}{dt} \underset{I\ constant}{\Rightarrow} dt = \frac{dQ}{I}$$

This information is used in Mathcad® to derive the gate-source voltage waveform (over time) as could be measured on a scope in application.

First the RC circuit parameters are defined (as discussed above), and the RC response to an ideal gate-driver voltage step from 0 V to V_{GS} is derived until the Miller Plateau voltage is reached. After this we determine the time duration of the Miller plateau. At last we evaluate the RC response of the voltage from Miller Plateau to target V_{GS} based on the previously extracted gate charge characteristics. The three pieces of the response can then be assembled. Below is a walk-through applying this method in Mathcad®:

$R_{g\_int} := 1.2$ Ohms — Internal gate resistance (internal to the MOSFET)

$R_{g\_ext} := 10$ Ohms — External gate resistance (discrete resistance between driver output and MOSFET gate-pin)

$$C_{gs\_tr} := \frac{Q_{gs}}{V_{gs\_plat}} = 1.24 \text{ nF}$$

Find the time-related gate-source capacitance based on charge at beginning of Miller Plateau

$$C_{gsgd\_tr} := \frac{Q_{g\_VGS} - (Q_{gd} + Q_{gs})}{VGS - (V_{gs\_plat})} = 4.736 \text{ nF}$$

Find the time-related gate-drain and gate-source parallel capacitance value above Miller Plateau

$$V_{gs\_1}(t) := VGS \cdot \left[1 - e^{\frac{-t}{(R_{g\_int}+R_{g\_ext}) \cdot C_{gs\_tr}}}\right] V$$

RC response for Vgs rising to the start of Miller Plateau (t is time in nano-seconds)

$$i_{plat} := \frac{VGS - V_{gs\_plat}}{R_{g\_int} + R_{g\_ext}} = 0.682 \text{ A}$$

Constant drive current during Miller Plateau

$$t_{plat} := \frac{Q_{gd}}{i_{plat}} = 31.357 \text{ ns}$$

Time spent at Miller Plateau

$$V_{gs\_3}(t) := (VGS - V_{gs\_plat}) \cdot \left[1 - e^{\frac{-t}{(R_{g\_int}+R_{g\_ext}) \cdot C_{gsgd\_tr}}}\right] V$$

RC response for Vgs rising beyond Mille plateau (up to target VGS) (t is time in ns)

Identify the time, when the first RC response reaches the Plateau voltage,

Given

Solver-block to return time (in ns), when gate-source voltage has reached the Miller Plateau

$V_{gs\_1}(t\_guess) = V_{gs\_plat}$

$t\_guess := 15$ ns

$t_{plat1} := Minerr(t\_guess) = 6.262$ ns

Time from Vgs=0v to Vgs=Vplateau

$t := 0, 0.1 .. 1000$

Combine the three pieces of voltage waveforms:

$$V_{gs\_on}(t) := \begin{cases} V_{gs\_1}(t) & \text{if } 0 < t < t_{plat1} \\ V_{gs\_plat} & \text{if } t_{plat1} < t < (t_{plat1} + t_{plat}) \\ \left[V_{gs\_plat} + V_{gs\_3}\left[t - (t_{plat1} + t_{plat})\right]\right] & \text{if } t_{plat1} + t_{plat} < t \end{cases}$$

The total gate-source turn-on waveform can now be plotted and used for further analysis and evaluation

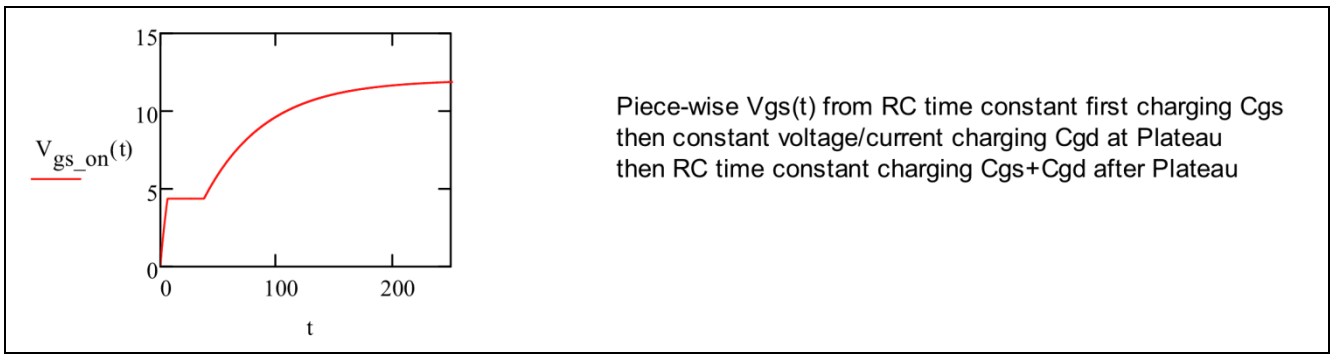


Figure 18 Piece-wise constructed $V_{GS}(t)$ waveform from three regions calculated individually

4.2.1 Detailed gate-drive evaluations

The gate turn-on waveform derived above provides a great foundation for a detailed look at gate-drive energy during the turn-on transition. A comprehensive look into energy dissipation in the (internal and external) resistors will not only give a fairly accurate picture of the losses (for efficiency calculations), but also where these losses occur. This insight enables more accurate evaluation of thermals and potential over-temperature conditions. Since the MOSFET gate charge fundamentally consists of non-dissipative (reactive) elements, the energy expended to charge and discharge it will only be dissipated in the resistive elements of the circuit.

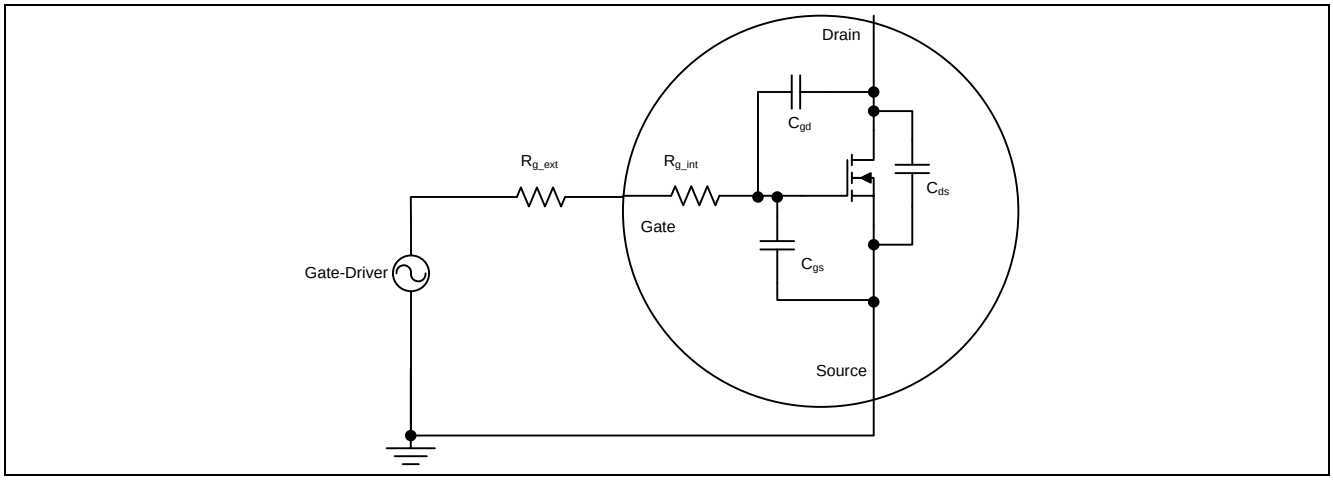
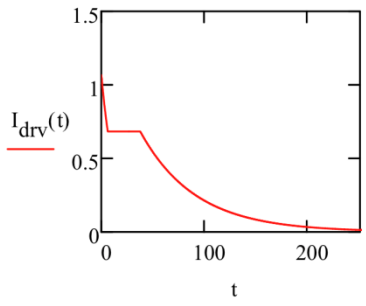


Figure 19 Gate-drive current loop with relevant MOSFET parasitics explicitly shown

Current flows from the Gate-driver through the resistors and either through C_{GS} or through C_{GD} and the MOSFET channel – or both – back to the Gate-driver. In any case, the current through the loop can be calculated and plotted as the gate-driver voltage less the gate-source voltage (derived above) across the series gate resistors.

$$I_{drv}(t) := \frac{VGS - V_{gs\_on}(t)}{R_{g\_int} + R_{g\_ext}} \quad A$$

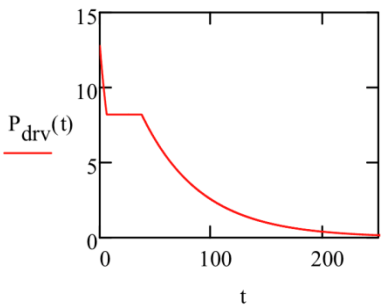


Gate-driver current derived by Ohm's law when knowing gate-driver voltage, gate-source voltage and gate resistors

Figure 20 Gate turn-on current constructed from $V_{gs}(t)$ and Ohm's law

The instantaneous power can be evaluated, using the instantaneous current and –voltage.

$$P_{drv}(t) := VGS \cdot I_{drv}(t) \quad W$$



Instantaneous power is voltage * current

Figure 21 Instantaneous gate driver power

The energy leaving the gate-driver is the integral of its power, so a more accurate evaluation of the energy expended to switch the MOSFET can be plotted. The energy curves for each individual component can also be assessed.

$P_{Rg\_int}(t) := I_{drv}(t)^2 \cdot R_{g\_int}$ W Instantaneous power dissipation in Rg_int

$P_{Rg\_ext}(t) := I_{drv}(t)^2 \cdot R_{g\_ext}$ W Instantaneous power dissipation in Rg_ext

$P_{ciss}(t) := P_{drv}(t) - P_{Rg\_int}(t) - P_{Rg\_ext}(t)$ W Instantaneous power in the gate charge

$E_{drv}(t) := \int_0^t P_{drv}(t)\,dt$ nJ

$E_{Rg\_int}(t) := \int_0^t P_{Rg\_int}(t)\,dt$ nJ

Cummulative energies integral of power

$E_{Rg\_ext}(t) := \int_0^t P_{Rg\_ext}(t)\,dt$ nJ

$E_{ciss}(t) := \int_0^t P_{ciss}(t)\,dt$ nJ

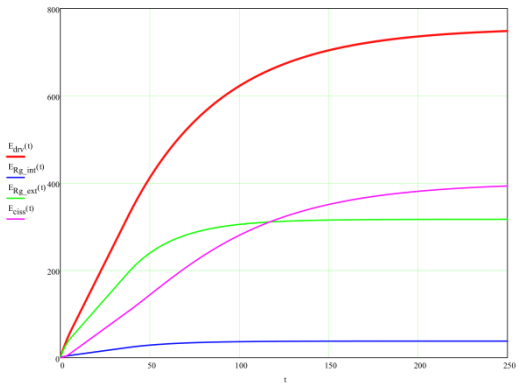


Figure 22 Various energies dissipated or stored in resistive or capacitive elements – plotted vs. time during turn-on transition. Red is total energy taken by driver from its supply, Blue is energy dissipated in MOSFET internal gate resistor, Green is energy dissipated in discrete series gate resistor and Magenta is energy stored in C_{iss}

Examples of MOSFET parameter extraction

The energy stack-up can be easily disseminated graphically or mathematically with this data/plot. Determining the energies (at end of turn-on interval) will give the complete picture of distribution:

$t_{E\_drv\_final} :=$ | $t_{temp} \leftarrow 0$
| while $E_{drv}(t_{temp} + 1) - E_{drv}(t_{temp}) > 0.01$
| | $t_{temp} \leftarrow t_{temp} + 1$
| | $t_{E\_drv\_final} \leftarrow t_{temp}$

Quasi-arbitrarily chosen dE/dt criterion for slope to be very near "flat" is defined (in this particular case, the desired slope "flatness" is less than 10pJ per ns).

$t_{E\_drv\_final} = 271$ ns

Time at which the criterion for dE/dt is met (energy difference over 1 ns is less than 10pJ)

$E_{drv\_final} := E_{drv}(t_{E\_drv\_final}) = 750.789$ nJ

$E_{Rg\_int\_final} := E_{Rg\_int}(t_{E\_drv\_final}) = 38.029$ nJ

$E_{Rg\_ext\_final} := E_{Rg\_ext}(t_{E\_drv\_final}) = 316.91$ nJ

$E_{ciss\_final} := E_{ciss}(t_{E\_drv\_final}) = 395.728$ nJ

Final gate drive energies at completed turn-on for all components

Total drive energy for this particular case is thus ~750 nJ, whereas the initial rough estimation in the beginning of this chapter put the energy at ~640 nJ. Moreover, we can begin to get a very clear idea of where the power dissipation takes place (thermal constraints). As a first estimation, let us assume that the gate-charge characteristics look the same for turn-off as we extracted for turn-on. This might not be exactly the case in actual applications, but will suffice for the purpose of this exercise.

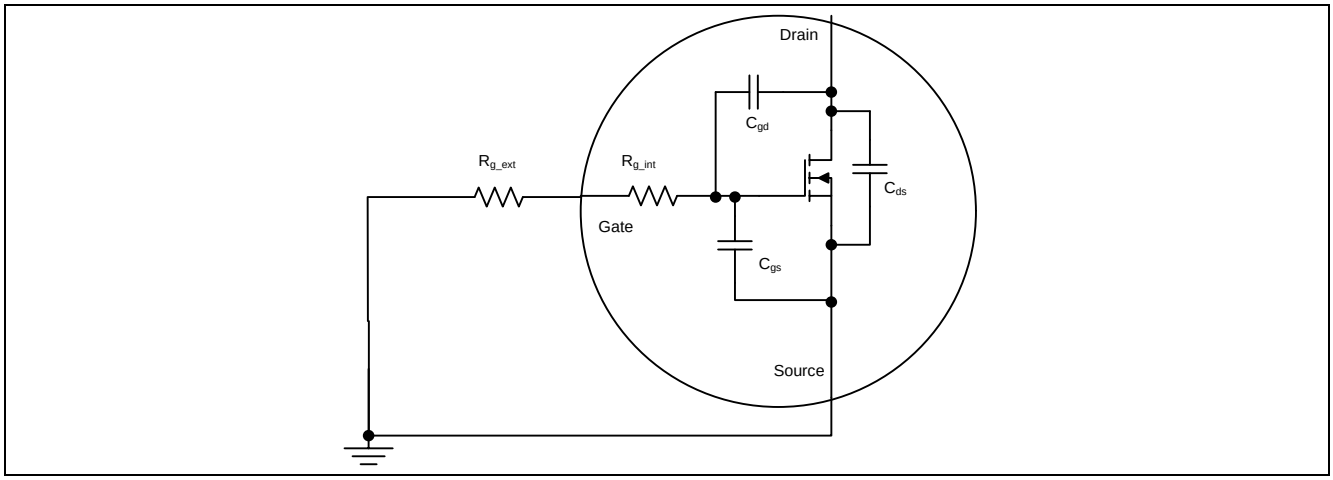


Figure 23 Equivalent turn-off circuit for ideal short (driver) including simple parasitic MOSFET elements

During turn-off, the energy stored in Q_G is dissipated in the (internal and external) gate-resistors. Current will first flow through C_{gs} and C_{gd} through R_{g_int} and R_{g_ext} to ground until the Miller Plateau is reached. Then – during the Miller Plateau – constant current (at constant V_{GS}) will flow only through C_{gd} and through the gate-resistors to ground. After the Miller Plateau is at its conclusion, current will flow mainly through C_{gs} (at high V_{GD}, C_{gd} is very small, and the charge is dominated by C_{gs} in this interval).

$$V_{gs\_off1}(t) := VGS \cdot e^{\frac{-t}{(R_{g\_int}+R_{g\_ext})\cdot C_{gsgd\_tr}}} \quad V$$

RC logarithmic decay from inital voltage (standard RC circuit response)

$t_{Miller1} :=$ | $t_{temp} \leftarrow 0$ | while $V_{gs\_off1}(t_{temp}) > V_{gs\_plat}$ | $t_{temp} \leftarrow t_{temp} + 0.1$ | $t_{Miller1} \leftarrow t_{temp}$

Identify the time (in ns), when Vgs (on its first RC-trajectory from VGS) reaches the Miller Plateau voltage

$t_{Miller1} = 53.8$ ns

Record the time (in ns)

$$t_{Miller} := \frac{Q_{gd}}{\frac{V_{gs\_plat}}{R_{g\_int}+R_{g\_ext}}} = 55.018 \quad ns$$

Calculate the time spent at Miller Plateau (by I(t)=dQ(t)/dt => t=Q/I

$$V_{gs\_off3}(t) := V_{gs\_plat} \cdot e^{\frac{-t}{(R_{g\_int}+R_{g\_ext})\cdot C_{gs\_tr}}} \quad V$$

RC logarithmic decay from Miller Plateau voltage (standard RC circuit response)

$V_{gs\_off}(t) :=$ | $V_{gs\_off1}(t)$ if $0 < t < t_{Miller1}$ | V_{gs_plat} if $t_{Miller1} < t < (t_{Miller1} + t_{Miller})$ | $V_{gs\_off3}[t - (t_{Miller1} + t_{Miller})]$ if $(t_{Miller1} + t_{Miller}) < t$

Combine the three segments

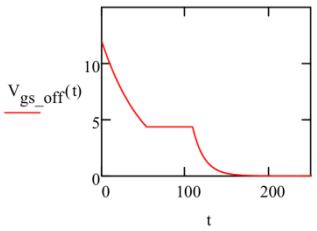


Figure 24 Derivation and plot of estimated gate-source voltage waveform during turn-off

In a similar fashion as during turn-on, the turn-off current waveform can be derived from the gate-source voltage existing across the series resistors. The turn-off power curves can be derived and the energy plotted:

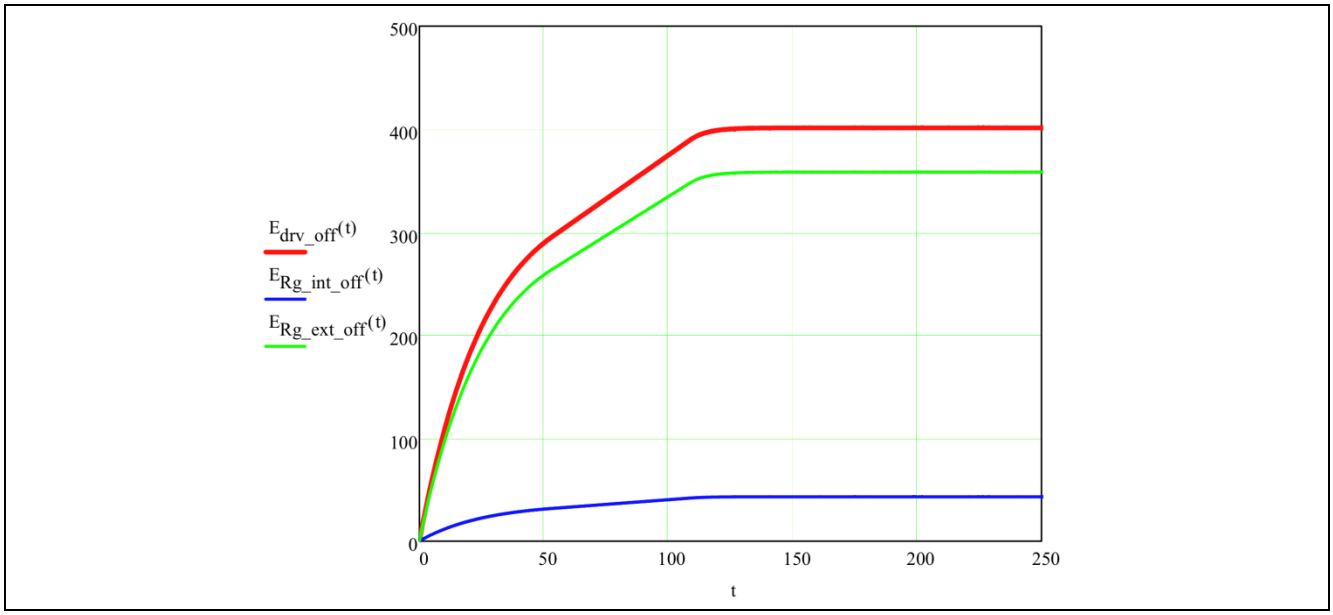


Figure 25 Energy in nJ vs. time in ns for internal, external and total gate resistor during turn-off

$t_{E\_drv\_off\_final} :=$ | $t_{temp} \leftarrow 0$
while $E_{drv\_off}(t_{temp} + 1) - E_{drv\_off}(t_{temp}) > 0.01$
$t_{temp} \leftarrow t_{temp} + 1$
$t_{E\_drv\_off\_final} \leftarrow t_{temp}$

Quasi-arbitrarily chosen dE/dt criterion for slope to be very near "flat" is defined (in this particular case, the desired slope "flatness" is less than 10pJ per ns).
The time of which that criterion is first met is recorded

$t_{E\_drv\_off\_final} = 141$ ns

Time at which the criterion for dE/dt is met (energy difference over 1 ns is less than 10pJ)

$E_{drv\_off\_final} := E_{drv\_off}(t_{E\_drv\_off\_final}) = 401.016$ nJ

$E_{Rg\_int\_off\_final} := E_{Rg\_int\_off}(t_{E\_drv\_off\_final}) = 42.966$ nJ

$E_{Rg\_ext\_off\_final} := E_{Rg\_ext\_off}(t_{E\_drv\_off\_final}) = 358.05$ nJ

Difference in energy content (401 nJ initially on Ciss for turn-off vs. 396 nJ finally after turn-on)
is due to the slope criterion for "final time", where t=∞ would represent the "accurate" value
for a logarithmically converging function

With the chosen values we end up with total gate-charge related energy dissipation of ~750 nJ per switching period broken up into great detail:

Table 3 Summary with detailed breakdown of gate charge related energy- and equivalent power -loss for 100 kHz switching rate (example)

	E turn-on [nJ]	E turn-off [nJ]	Total [nJ]	PWR (100 kHz) [mW]
R_{g_int}	38	43	81	8.1
R_{g_ext}	317	358	675	67.5
Total	355	401	756	75.6

Having a comprehensive overview such as presented here facilitates much more than only efficiency estimations, since the location of the losses can be pin-pointed. More thorough and accurate thermal evaluation is enabled. More-over, specific trade-offs for different MOSFET families/technologies can be evaluated. To mention one such comparison, some SJ MOSFETs employ a much larger internal gate-resistor than the herein exemplified SPA11N80C3. If targeting the same total gate resistance such MOSFETs would essentially dissipate all gate-charge related losses internally (inside the MOSFET). These losses would thereby need to be considered in the thermal management of the MOSFET (heat sinking).

Of course these calculations are still estimations, and cannot substitute real measurements/experiments. For example, the capacitances involved (particularly C_{GD} – also referred to as C_{rss}) are non-linear (meaning non-constant vs. drain-source voltage). In the preceding calculations (time related) equivalent linear capacitances were assumed. The estimated timings are close to accurate; however the assumed (RC) voltage trajectory is not strictly accurate.

4.2.2 Detailed gate drive evaluation enables complex comparisons

The gate-driver current from the “ideal voltage source gate-driver” was investigated in previous subsection. Current ramped very quickly (instantly) to a level above 1 A at in beginning of turn-on interval before RC-ramping down to the Miller Plateau. ~680 mA flowed during the Miller Plateau for the values and operating conditions given. The resulting turn-on delay time and time spent at the Miller Plateau (transition time) was found, and the gate-source voltage was plotted vs. time.

There are two fundamental ways to drive a charge, however, and instead of the ideal voltage source, one could drive the gate with an ideal current source. We will exploit this proposition to gain some insight.

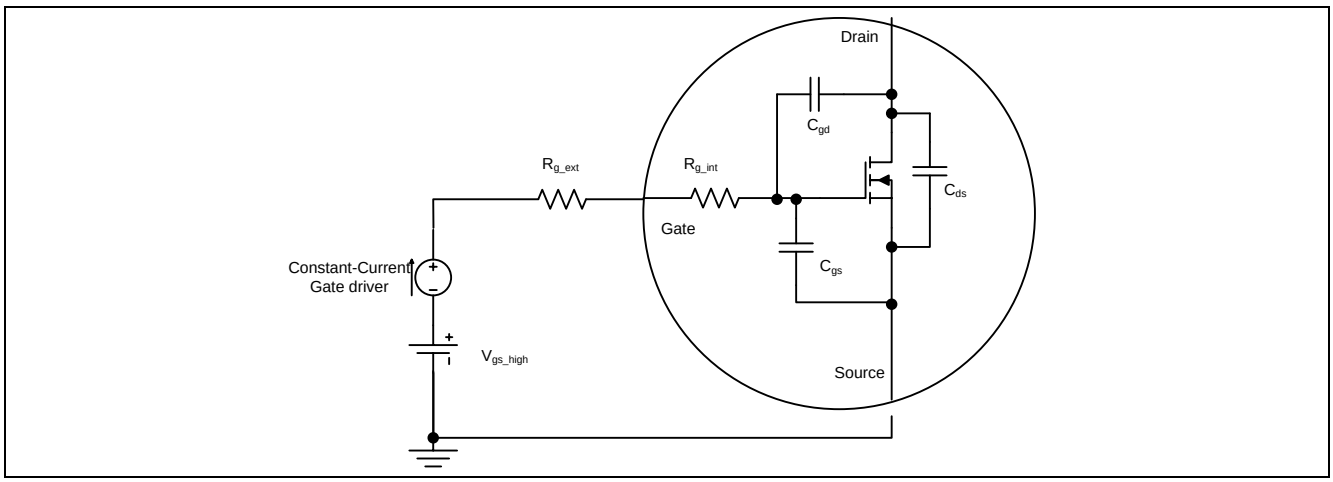


Figure 26 During turn-on, gate driver could act as a constant current source (until target V_{gs} is reached)

A constant current turn-on gate driver could drive the MOSFET with a constant current of similar magnitude to the ~680 mA during the Miller Plateau found in the previous section. To simplify calculations we use an ideal current of 0 A for t≤0, then ~680 mA until V_{GS} reaches the target voltage and then 0 A again. Such a driver would be assumed to have an input voltage a bit greater than the target voltage (to allow for voltage drop across it and across the gate resistors).

$I_{gd\_cc} := i_{plat} = 0.682$ A — Assuming same current-driving capability as the former Miler-plateau current

$V_{gs\_drop} := I_{gd\_cc} \cdot (R_{g\_ext} + R_{g\_int}) = 7.644$ V — Voltage-source voltage (in addition to target Vgs) required for supplying real, physical current-drive gate driver

$V_{gs\_high} := VGS + V_{gs\_drop} = 19.644$ V — Voltage source required to power gate-driver current source

$t_{Qgs\_on} := \frac{Q_{gs}}{I_{gd\_cc}} = 7.912$ ns — Time it will take to get to beginning of Miller Plateau

$t_{Miller\_cc\_on} := \frac{Q_{gd}}{I_{gd\_cc}} = 31.357$ ns — Time spent at the Miller Plateau

$t_{VGS\_cc\_on} := \frac{Q_{g\_VGS} - (Q_{gs} + Q_{gd})}{I_{gd\_cc}} = 53.043$ ns — Time it will take to get to the target gate-source voltage

$t_{cc\_Miller1} := t_{Qgs\_on}$ ns

$t_{cc\_Miller2} := t_{Qgs\_on} + t_{Miller\_cc\_on}$ ns — Time points of interest; total elapsed time at ends of intervals

$t_{cc\_VGS} := t_{cc\_Miller2} + t_{VGS\_cc\_on}$ ns

$$V_{gs\_cc\_on}(t) := \begin{cases} \left(\frac{V_{gs\_plat}}{t_{Qgs\_on}} \cdot t\right) & \text{if } 0 < t < t_{cc\_Miller1} \\ V_{gs\_plat} & \text{if } t_{cc\_Miller1} < t < t_{cc\_Miller2} \\ \left[V_{gs\_plat} + \frac{VGS - V_{gs\_plat}}{t_{VGS\_cc\_on}} \cdot (t - t_{cc\_Miller2})\right] & \text{if } t_{cc\_Miller2} < t < t_{cc\_VGS} \\ VGS & \text{if } t_{cc\_VGS} < t \end{cases}$$

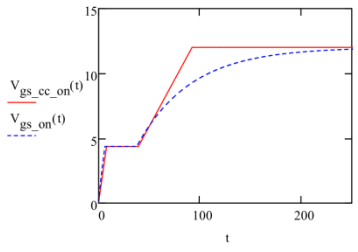


Figure 27 Plot of gate-source voltage for current drive (*Red*) and voltage drive (*Blue*) {V} vs. time {ns}

It can be seen that the transient time is exactly equivalent in the two cases, since the Miller Plateau has exactly the same duration. This means the switching (overlap) losses are similar in the two cases.

Due to a much higher peak current, the ideal voltage drive reaches the Miller Plateau faster than the current-drive. However this does not result in losses, since the MOSFET remains off until the threshold voltage and does not start carrying significant current through its channel until the Plateau voltage has been reached. The much lower peak current (of the constant current-drive) could easily manifest itself as an EMI advantage though. Full enhancement of the channel is reached quicker with the current drive, which could result in (marginally) lower conduction losses at the very beginning of the conduction interval.

The turn-on power and -energies can be explored in detail:

$$I_{cc\_gd}(t) := \begin{cases} I_{gd\_cc} & \text{if } 0 < t < t_{cc\_VGS} \\ 0 & \text{otherwise} \end{cases}$$

$$P_{cc\_Rg\_ext}(t) := I_{cc\_gd}(t)^2 \cdot R_{g\_ext}$$

$$P_{cc\_Rg\_int}(t) := I_{cc\_gd}(t)^2 \cdot R_{g\_int}$$

$$P_{cc\_drv\_on}(t) := I_{cc\_gd}(t) \cdot V_{gs\_high}$$

W

Instantaneous power in the various dissipative and reactive elements of gate driver loop during turn-on for current-drive

$$P_{cc\_src}(t) := \left[V_{gs\_high} - V_{gs\_cc\_on}(t) - I_{cc\_gd}(t) \cdot \left(R_{g\_ext} + R_{g\_int}\right)\right] \cdot I_{cc\_gd}(t)$$

$$P_{cc\_ciss}(t) := P_{cc\_drv\_on}(t) - P_{cc\_Rg\_ext}(t) - P_{cc\_Rg\_int}(t) - P_{cc\_src}(t)$$

$$E_{cc\_Rg\_ext}(t) := \int_0^t P_{cc\_Rg\_ext}(t)\,dt$$

$$E_{cc\_Rg\_int}(t) := \int_0^t P_{cc\_Rg\_int}(t)\,dt \qquad E_{cc\_src}(t) := \int_0^t P_{cc\_src}(t)\,dt$$

Turn-on energies (nJ) over time (ns) during turn-on with constant current drive

$$E_{cc\_drv}(t) := \int_0^t P_{cc\_drv\_on}(t)\,dt \qquad E_{cc\_ciss}(t) := \int_0^t P_{cc\_ciss}(t)\,dt$$

…and plotted:

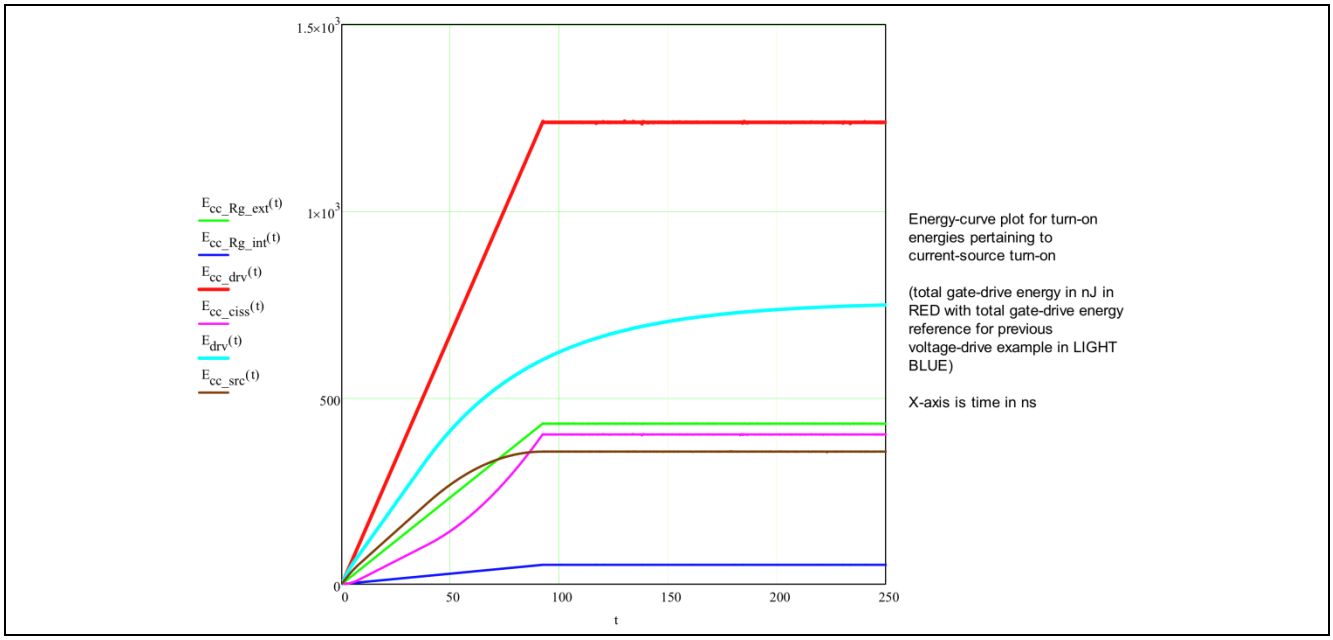


Figure 28 Energies (dissipated and stored) during current-source turn-on – with total drive energy (loss) for the ideal voltage-drive as reference (*Cyan*) and for the current-drive (*Red*)

We can assume identical turn-off behavior in the two cases (gate-driver output shorted), resulting in identical turn-off loss. The total gate charge related energy and loss might be compared for the two driver approaches:

Table 4 Total gate-drive energy and loss comparison for different gate-drive methods

	Voltage drive [nJ]	Current drive [nJ]	Delta [nJ]	ΔPWR [mW]
R_{g_int}	81	95	14	1.4
R_{g_ext}	675	788	113	11.3
Driver	0	355	355	35.5
Total	756	1237	482	48.2

In some applications the voltage drive might be advantageous. This is particularly true when the high peak current capability of the “ideal” voltage source enables fast switching behavior (such as in above example). This could result in the lowest transient turn-on loss in hard-switched applications, if higher currents are switched (multiple or even tens of amperes). In products, where EMI can be handled effectively (metal enclosure) the voltage drive could be a reasonable choice.

Current drive might find advantages in applications where fast switching is not a must (low- or zero-current turn-on or zero-voltage turn-on). In these applications there may be a need to slow down switching transients due to EMI requirements anyway. Here a large gate-resistor would be required for turn-on – with a faster diode-resistor turn-off – in the voltage-source drive. For constant current turn-on, a much smaller current could be programmed to begin with. An example of such an application (where constant current drive is relevant) is a low power flyback adapter working in **D**iscontinuous **C**onduction **M**ode or QR mode within a plastic enclosure. (Plastic enclosures pose difficult challenges for EMI control. Constant current drive limits maximum current amplitudes, di/dt and dv/dt during turn-on transients.

4.3 C_{oss}, Q_{oss} and E_{oss} extraction simulation test bench

The tabular section of a MOSFET data sheet contains capacitance values for input- and output capacitance. Sometimes the reverse transfer capacitance, or C_{rss}, is also listed. One example is given here (continuing the example SPA11N80C3 part as referenced hereto).

Dynamic characteristics

Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	1600	-	pF
Output capacitance	C_{oss}		-	65	-	
Effective output capacitance, energy related[5)]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 480 V	-	50	-	
Effective output capacitance, time related[6)]	$C_{o(tr)}$		-	140	-	

Figure 29 DS excerpt from SPA11N80C3 detailing input- and output capacitance values

As can be seen, similarly as for $R_{DS(on)}$ and gate charge, these parameters are specified for a given point; namely a specific drain-source voltage (and frequency).

The formula for charge (in a linear capacitor) is

$$Q = C \cdot V$$

And for a (linear) capacitor's energy the formula is

$$E = \frac{1}{2} \cdot C \cdot V^2$$

Charge is an expression of time and energy is self-explanatory. We can see quantities in the DS given as energy- and time-related capacitance respectively (in this example given for a drain-source voltage range of 0-480 V). The charge in C_{oss} back-calculated to yield capacitance results in a different value than back-calculating the capacitance based on energy contained in C_{oss}. It is therefore easy to conclude that C_{oss} must not be a linear capacitance. This is especially true for any Super Junction MOSFET due to the physical structure of the silicon. In such structures (SJ structures) the degree of non-linearity depends on the geometry of the charge compensation columns and epitaxial region. To aid in the understanding of the non-linearity of this capacitance, most modern data sheets show a graphical representation of the capacitances (typically showing curves of C_{iss} as well as C_{oss} and C_{rss}).

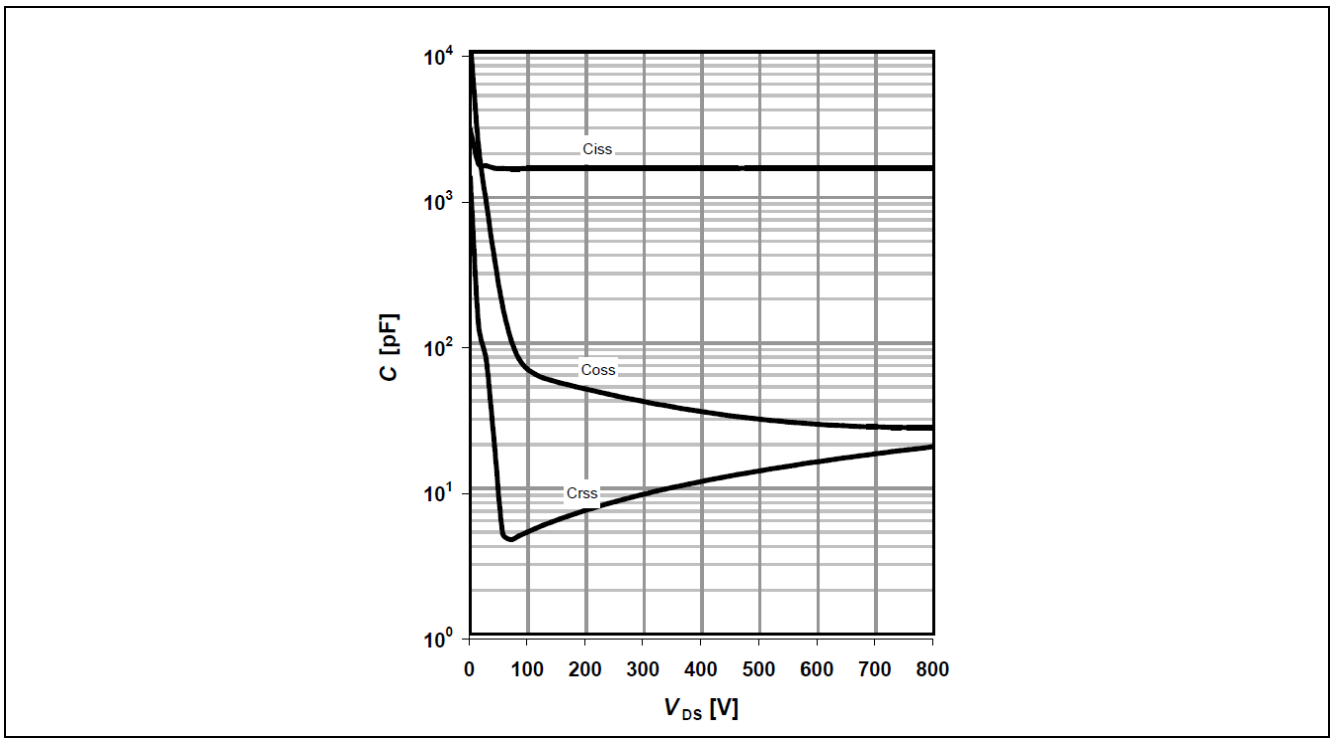


Figure 30 Excerpt of SPA11N80C3 DS detailing the (non-linear) parasitic capacitances vs. V_{DS}

C_{iss} is mostly linear. C_{iss} is defined as the parallel capacitance of C_{GS} and C_{GD}. In the geometrical/physical structure of the Super Junction the main contributor to C_{GS} is formed by the area and “thickness” of overlap of the source and the gate. In below diagram (Figure 31, left) C_{GS} comprises C_{oxm} (biggest contributor), C_{oxN+} and C_{oxP}. The part of C_{iss} consisting of C_{gs} does not vary with drain-source voltage (or any other parameter/condition for that matter). At drain-source voltages beyond a few tens of volts (in modern SJ MOSFETs) C_{gs} is the dominating contributor to C_{iss}. At least this should be the case, since the high dv/dt capacitive voltage divider between C_{gd} and C_{gs} could otherwise cause undesired turn-ons during commutation. At very low drain-source voltage C_{gd} becomes comparatively large and begins to have a significant influence on C_{iss}.
C_{rss} is defined as C_{gd} and is highly non-linear vs. V_{DS} in Super Junction structures.

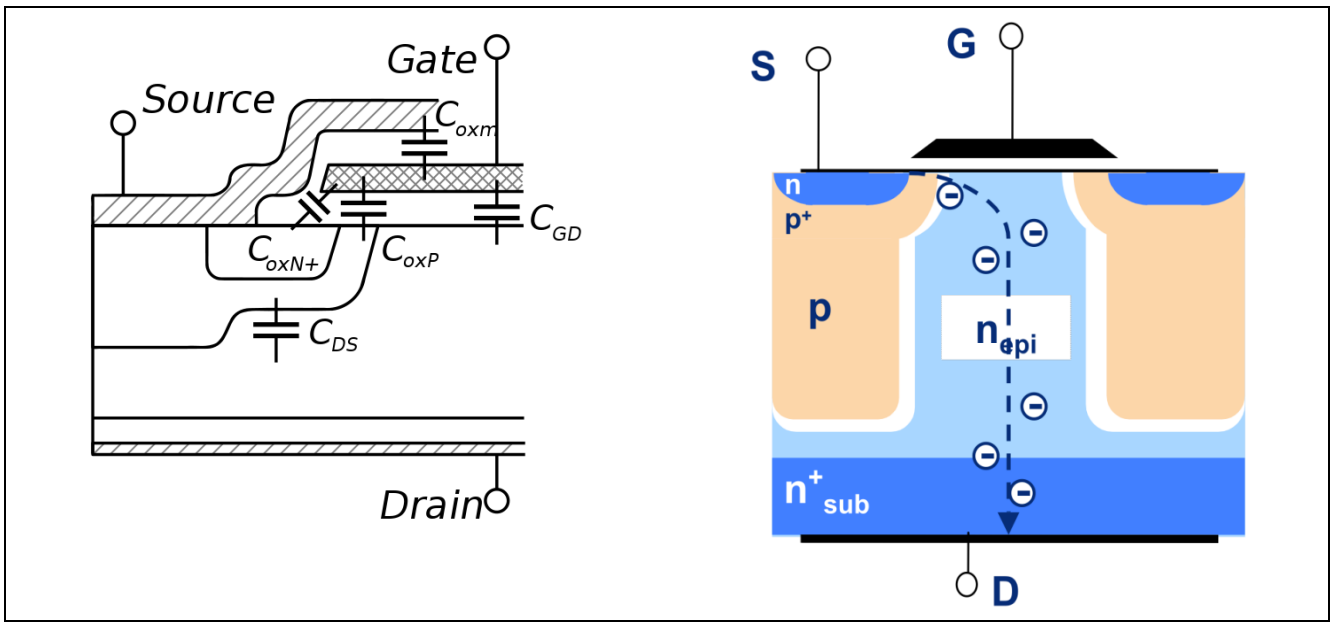


Figure 31 Example representation of MOSFET silicon structure. Left: location of parasitic capacitances (courtesy of Wikipedia). Right: Super Junction structure with deep p-columns for charge compensation

Looking at the SJ structure this non-linearity becomes clearer: At low V_{DS} the (small) drain-source potential is dropped sharply across the boundary between charge-compensation columns and the epi-region (outlined as white border between red p-column and blue epitaxial region in above Figure 31). This means the part of the epi-region positioned directly underneath the gate metallization carries the drain-potential. In physical dimensions the capacitor plates between drain-potential and gate-potential are thus relatively large and in close proximity.

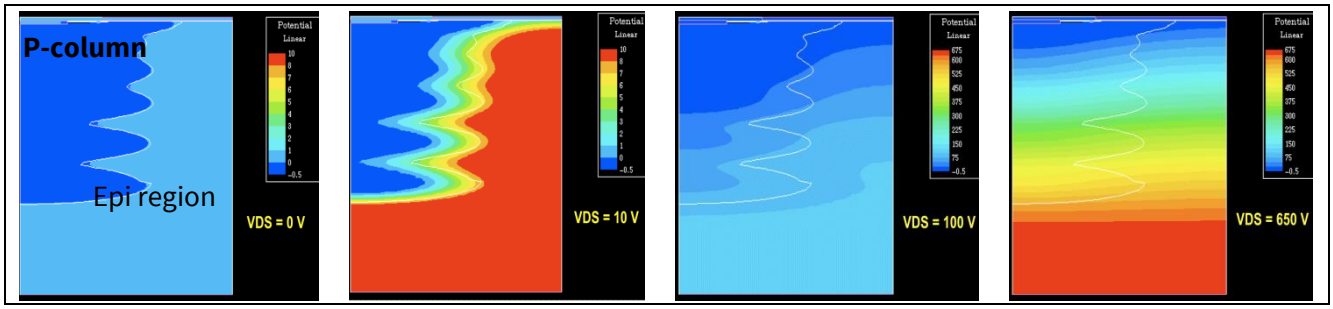


Figure 32 Simulated electrical fields inside the SJ structure at varying V_{DS} detailing capacitance non-linearity. Source: Internal simulation prepared in Taurus-Medici.

At higher drain-source potential on the contrary, the voltage is dropped gradually vertically across the epi-region (and p-column region). The physical distance between the drain- and gate capacitor plates is increased greatly (compared to the case for low drain-source voltage). This makes for a much lower capacitance at increasing drain-source voltage potential (see rightmost picture in Figure 32 above).

Examples of MOSFET parameter extraction

C_{oss} is defined as the parallel capacitance of C_{gd} and C_{ds} both of which are highly non-linear. C_{ds} at low V_{DS} consists of two capacitor plates in very close proximity with a relatively huge overlap area. This area is highlighted as the white border between red p-columns and blue epi-region in Figure 31 on the right. As detailed in Figure 32 (left to right) increasing V_{DS} decreases the area (towards flat/planar at highest V_{DS}) and increases the "distance" of the voltage drop. As the distance between the capacitor plates increases (vertically across the thickness of the multi-epi layers) and their area decreases (charge-compensation columns "collapse"), the capacitance value (C_{ds}) greatly diminishes.

The "collapse" of C_{ds} happens at a rate (dC/dV) and voltage (V_{DS}) defined by the specific geometry of the SJ cells. This makes it extremely technology dependent (what rate at what voltage). More dense (small geometry) MOSFETs will have a more non-linear C_{ds} and C_{gd} characteristic; starting from a higher capacitance value at low V_{DS} and dropping off steeper and deeper at a lower V_{DS} (for a given comparable $R_{DS(on)}$).

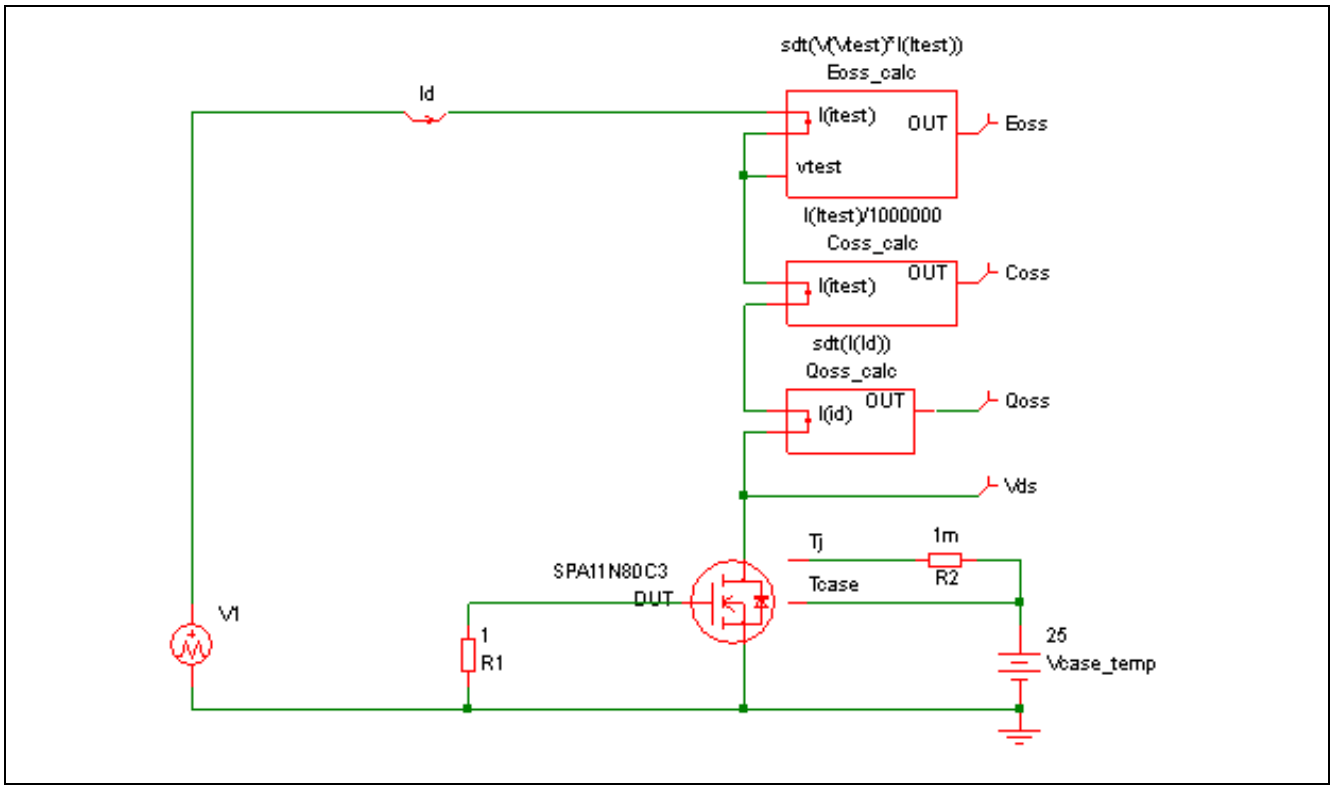


Figure 33 Example of simulation test bench for extracting C_{oss}, Q_{oss} and E_{oss} vs. V_{DS} from the Spice model of SJ MOSFET (DUT is SPA11N80C3 in this example like in previous ones)

In Figure 30 we can identify the (arbitrarily chosen?) capacitance value for C_{oss} at V_{DS} = 100 V, as often given in the data sheet. However, with the understanding that C_{oss} is extremely non-linear, there is clearly a need to extract the data. Only with the data extracted can it be properly manipulated in a math-environment for deeper understanding of its influence in applications.

The relevant data-points revolve around an x-axis of V_{DS}, so the starting point for simulation test bench is to force a specific voltage across V_{DS} at a specific time.

From

$$i(t) = C \cdot \frac{dV(t)}{dt}$$

we can generate C_{oss} if gate is held at source potential (by 1 Ω + R_{g_int} for convergence aid). In order to run an appropriately quick transient simulation, V_{DS} is ramped (by V1) from 0V to 800 V ($V_{(BR)DSS}$ specified for SPA11N80C3) in 800 µs. The analog behavioural non-linear transfer function “Coss_calc” compensates for the 10^6 factor (seconds/microseconds ratio) and outputs C_{oss} (in F) as volts.

In order to generate Q_{oss}, one can exploit the fact that

$$i(t) = \frac{dQ(t)}{dt}$$

The integral of the current over time then equals the charge. This function is handled by “Qoss_calc” in the test bench, which puts out charge in volts representing Coulombs.

Energy is the integral of instantaneous power over time, and power is voltage by current. “Eoss_calc” handles this calculation and outputs E_{oss} in volts representing energy in Joules.

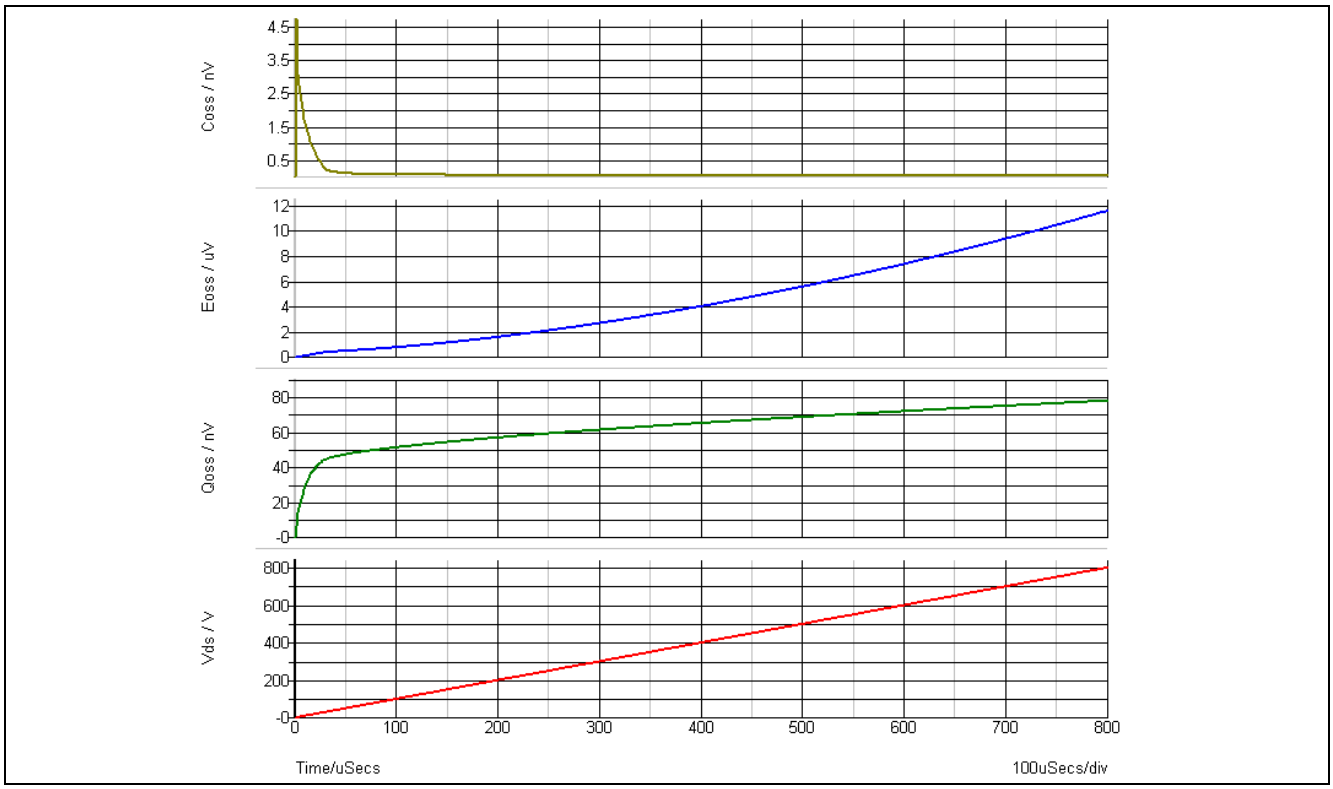


Figure 34 Simulation output proving the validity of V_{DS} on x-axis and detailing C_{oss}, Q_{oss} and E_{oss} vs. V_{DS}

C_{oss}, Q_{oss} and E_{oss} all return 0 at t=0, since the simulation setup is such that DC-operating point settings etc. accommodates integration from a known starting point. However, it is clear that while Q_{oss} and E_{oss} both must be 0 at 0 V_{DS}, C_{oss} clearly should not be. When exporting the data (in 1V increments), a manual correction can be made for C_{oss} at 0 V_{DS} that assumes the same percentage-wise dC_{oss}/dV_{DS} for 0 V_{DS}-to-1 V_{DS} as from 1 V_{DS}-to-2 V_{DS}. This approximation will provide sufficient accuracy for the purpose of this exercise and for most of what this data would be used.

Table 5 Manual correction of extracted 0 V_{DS} data

V_{DS}	Q_{oss}	E_{oss}	C_{oss}		V_{DS}	Q_{oss}	E_{oss}	C_{oss}
0	-7.36E-44	0	2.74E-33	→	0	0.00E+00	0	6.20E-09
1	6.23E-09	2.80E-09	4.74E-09		1	6.23E-09	2.80E-09	4.74E-09
2	1.03E-08	8.84E-09	3.62E-09		2	1.03E-08	8.84E-09	3.62E-09

The data can now be imported into an appropriate math program (Mathcad®), and used for detailed analysis. This is done in the following subsections (4.3.1 to 4.3.4).

4.3.1 Data import and verification (against DS) in Mathcad™

The import is done in Mathcad® via the data import wizard as detailed previously in this note (Figure 15 and further elaborated in accompanying step-by-step guide), and the imported data is converted to an easy-to-plot format. In order to verify the imported data, it should be checked against the DS. A C_{oss} of 65 pF is expected at V_{DS}=100 V according to Figure 29. The imported data yields:

$C_{oss\_100Vds} := C_{oss}(100)\cdot F = 65.667\cdot pF$ Data sheet cross-check for data verification (check against 65pF data sheet value)

Also given in the DS is the $C_{o(er)}$=50 pF and $C_{o(tr)}$=140 pF for V_{DS}=0 V to 480 V as seen in Figure 29. These values are the back-calculated equivalent values of linear capacitance when using the energy- respective charge-differences from 0 V_{DS} to 480 V_{DS}. We can back-calculate these values for cross-verification as well using the standard formulae for energy and charge:

$$dE = \frac{1}{2}\cdot C\cdot dV^2 \Rightarrow C = \frac{2\cdot dE}{V_2^{\,2} - V_1^{\,2}} \quad , \quad dQ = C\cdot dV \Rightarrow C = \frac{dQ}{dV}$$

For the imported data, we get

$C_{o\_er} := \frac{2\cdot\left(E_{oss}(480) - E_{oss}(0)\right)}{480^2 - 0^2} F = 45.553\cdot pF$ Data sheet cross-check for data verification (check against 50pF data sheet value)

$C_{o\_tr} := \frac{\left(Q_{oss}(480) - Q_{oss}(0)\right)}{480 - 0}\cdot F = 141.188\cdot pF$ Data sheet cross-check for data verification (check against 140pF data sheet value)

With all the values falling into line (or close enough for comfort), we can plot the data for quick reference.

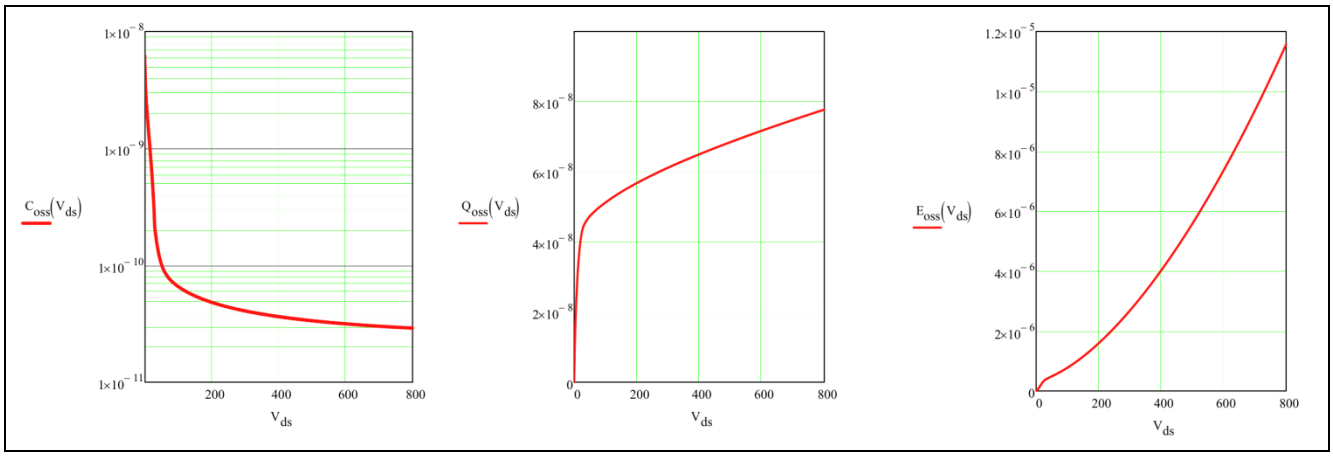


Figure 35 C_{oss}, Q_{oss} and E_{oss} vs. V_{DS} for SPA11N80C3 example SJ MOSFET from extracted data

We also now have the ability to plot (and investigate) Q_{oss} vs. V_{DS}, which is typically not given in the DS for high voltage MOSFETs (such as $E_{oss}(V_{DS})$ is).

The C_{oss} and E_{oss} curves are graphed in a similar way as in a typical data sheets. However, since C_{oss} changes most at lower voltage, and becomes relatively linear at higher voltages, a zoom-in of the “interesting” part can be achieved by plotting on a logarithmic x-axis.

In the resulting graph, the linearly extrapolated value that was manually put in for $C_{oss}(0V_{DS})$ looks reasonable compared to the general $dC_{oss}(V_{DS})/dV_{DS}$ near that voltage level.

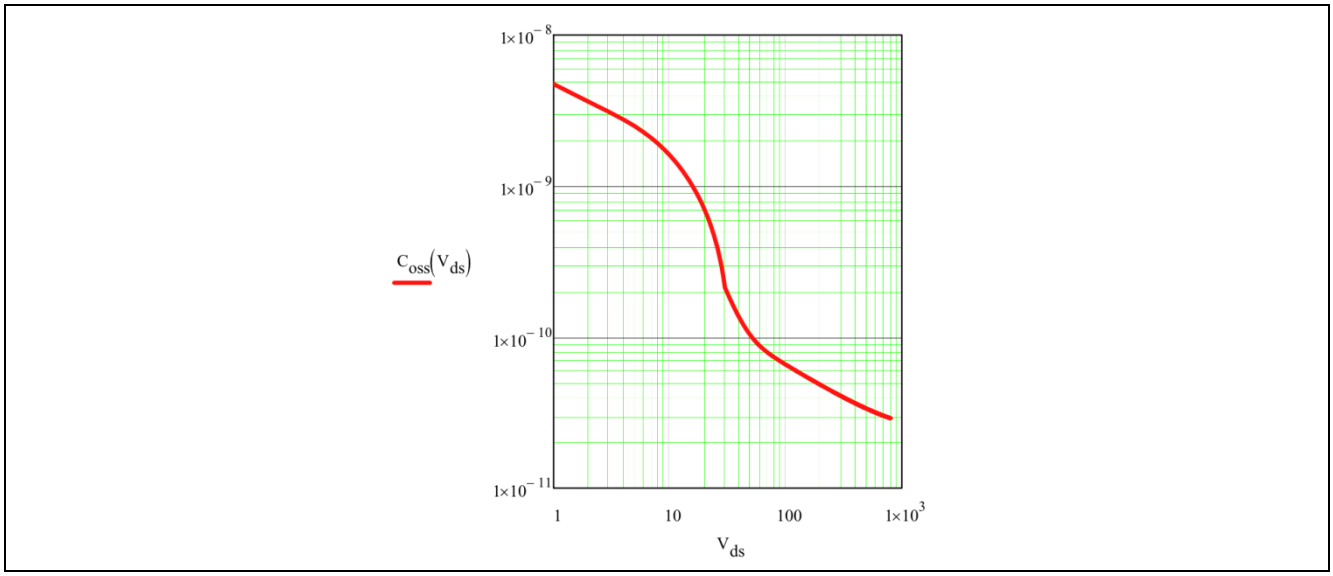


Figure 36 „Zoom-in“ on the lower-voltage part of the $C_{oss}(V_{DS})$ curve by using double-log graph

To exemplify some valuable use of this data, an application is dreamt up, where both energies and charges (timing) could be of great importance. One such application is the QR Flyback converter.

4.3.2 Example of use of imported C_{oss}, Q_{oss} and E_{oss}

For the Flyback operating in QR mode, it might be desired to predict how deep the QR valley would be at some operating conditions. It is also of great interest to know how long time it would take to reach the valley. And the projected E_{oss} loss caused by non-0V turn-on in that valley is of particular interest as well. A simplified schematic containing the relevant components is presented below in Figure 36 for reference.

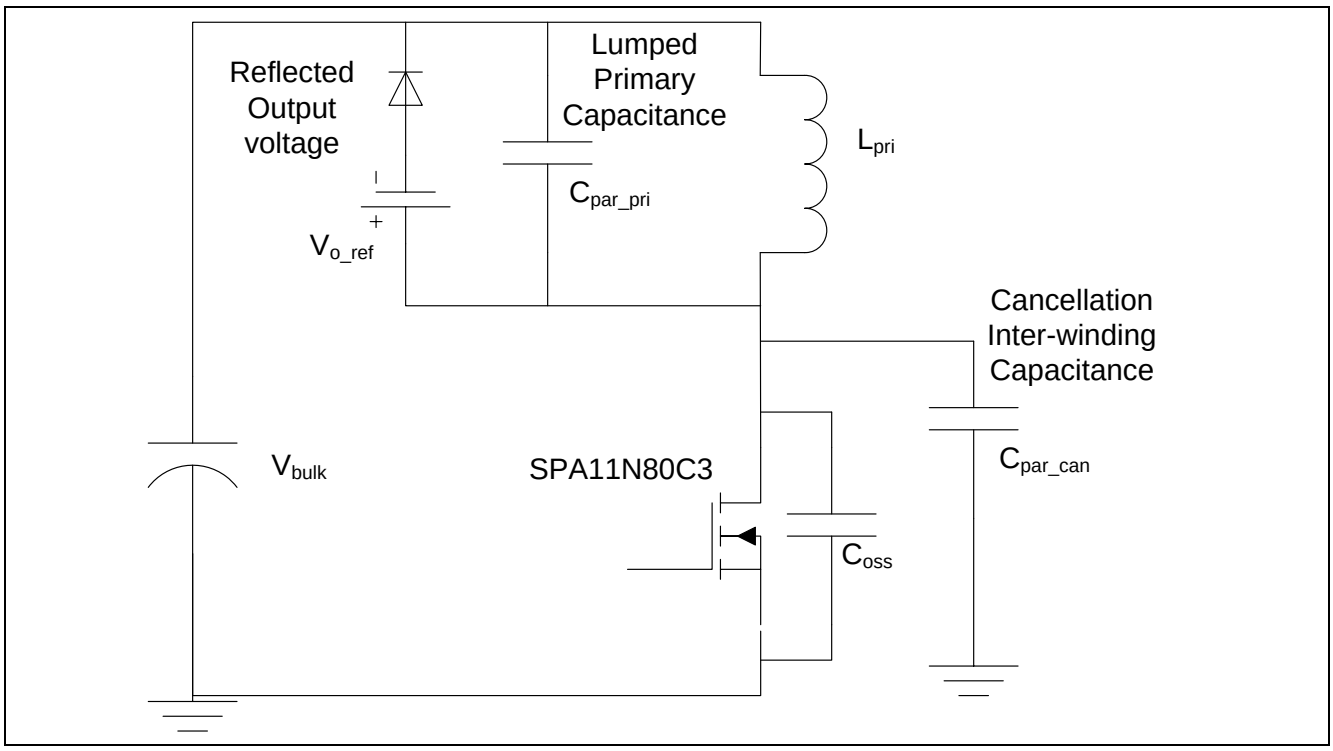


Figure 37 Components of interest for considering the 1st order effects influencing the QR period in a QR flyback application

Three steady-state intervals will be considered:

1. T_{off}: During the time when the primary side MOSFET is off ("off-time", T_{off}), the "secondary side" diode is conducting, keeping approximately the reflected output voltage across the magnetizing inductance. Polarities are such that the MOSFET V_{ds} is the sum of V_{bulk} and V_{0_ref}.
2. T_{QR}: If no rectifiers are conducting (and have not been for a long enough time to be considered steady-state), the voltage across the magnetizing inductance will be 0V (since any voltage would result in di/dt, which cannot be the case when no rectifiers can conduct said current). During the QR interval, the "DC-offset" of V_{DS} is thus equal to V_{bulk}.
3. T_{on}: When the primary side MOSFET is conducting, its drain-source voltage is approximately $0V_{DS}$. Flyback operating in QR-mode (DCM) obviously has a turn-on current of approximately 0A, which means voltage drop across $R_{DS(ON)}$ is negligible. In lower power applications this is the case for the enire conduction interval (relatively low peak current).

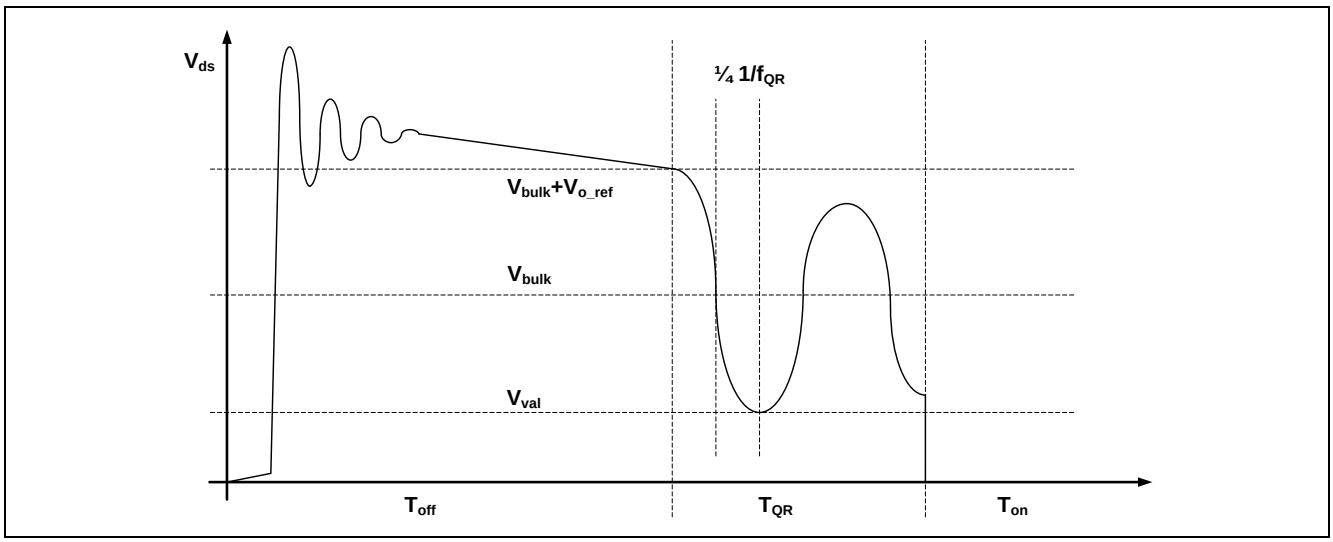


Figure 38 Example simplified V_{DS} waveform for QR flyback converter working in 2nd valley mode.

From transformer characterization, the magnetizing inductance can be accurately measured, and its tolerance is fairly low. The primary-to-cancellation inter-winding capacitance, however, can be a bit tricky – and an estimate might be necessary. The primary side referenced lumped capacitance comprises primary side intra-winding capacitance of the transformer (which can be measured/estimated), but also reflected contributions from all secondary side recitifiers (and snubbers). Rather than attempting to theoretically estimate the total capacitance, a measurement approach in-application is often a more well-suited procedure. A transformer with ~300 µH of primary side magnetizing inductance, ~5µH of primary-referenced leakage inductance and turns-ratio of 5 is subjected to an equivalent bulk-voltage with a 264V_{ac} input in a flyback with 5V of output voltage. From transformer characterization, the primary-to-cancellation inter-winding capacitance is known (assumed 75 pF in this example). The QR period is investigated, and the voltage-range (from valley to peak) is recorded as is the QR period.

The information of V_{DS} waveforms and the known value of C_{oss} vs. V_{DS} can be used to determine approximate value for C_{par_pri}.

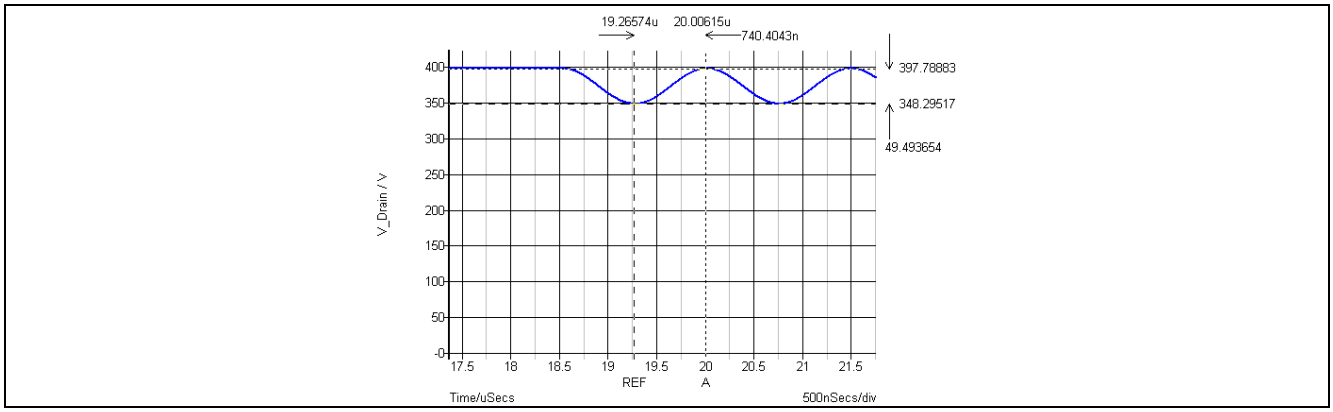


Figure 39 Example V_{DS} waveform during QR interval (simulated waveform representing measurement)

In Figure 37 we can clearly see that C_{oss} and C_{par_can} appear in parallel. It is equally clear that C_{par_pri} and L_{pri} are connected in parallel. Both parallel connections appear in series and in series with V_{bulk}, the impedance of which is comparatively negligible at frequencies relevant to the other impedances (since it ideally is an infinitely large capacitor – forcing a DC voltage at any relevant frequency). The effective equivalent resonant circuit (during T_{QR}) can thus be redrawn accordingly.

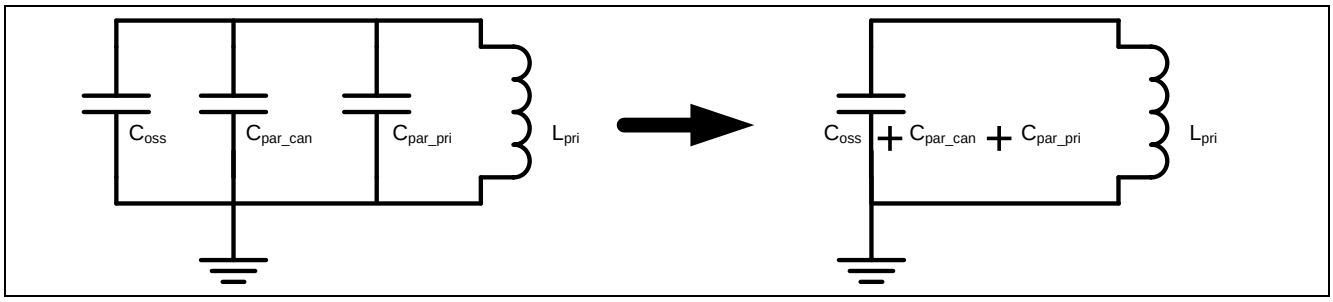


Figure 40 Equivalent resonant circuit during T_{QR} redrawn in simple form

Now the standard LC resonant frequency formula combined with some known values will produce a reliable estimate of C_{par_pri}. C_{oss} time-related (since we are investigating time-domain phenomena) over the voltage range can be found by the relation to charge {C_{oss_tr} is the equivalent linear capacitance that would result in the same charging time as the (non-linear) C_{oss}}.

$V_{pk} := 398$	V	Recorded peak and valley voltages on the primary side (Vds)
$V_{val} := 348$	V	
$t_{QR} := 1.48 \cdot 10^{-6}$	s	Recorded QR full-period time
$f_{QR} := \frac{1}{t_{QR}} = 6.757 \times 10^{5}$	Hz	QR frequency (based on time-measurement)
$L_{mag} := 300 \cdot 10^{-6}$	H	Known/measurable resonant component values
$L_{lkg} := 5 \cdot 10^{-6}$	H	
$L_{pri} := L_{mag} + L_{lkg} = 3.05 \times 10^{-4}$	H	
$C_{par\_can} := 75 \times 10^{-12}$	F	
$C_{oss\_tr} := \frac{Q_{oss}(V_{pk}) - Q_{oss}(V_{val})}{V_{pk} - V_{val}} = 3.728 \times 10^{-11}$	F	Calculated time-related MOSFET Coss over voltage range (based on charge difference over voltage range)
$C_{par\_pri} := \frac{\left(\frac{1}{2 \cdot \pi \cdot f_{QR}}\right)^2}{L_{pri}} - C_{oss\_tr} - C_{par\_can} = 6.963 \times 10^{-11}$	F	Primary-reference lumped capacitance only un-known quantity in formula

The resulting primary-referenced lumped capacitance (from all contributions) is effectively 70 pF in this example.

To verify the results, we will also investigate at low-line (90 V_{AC}), where the valley voltage is lower and C_{oss} consequently enters the more non-linear V_{DS} region.

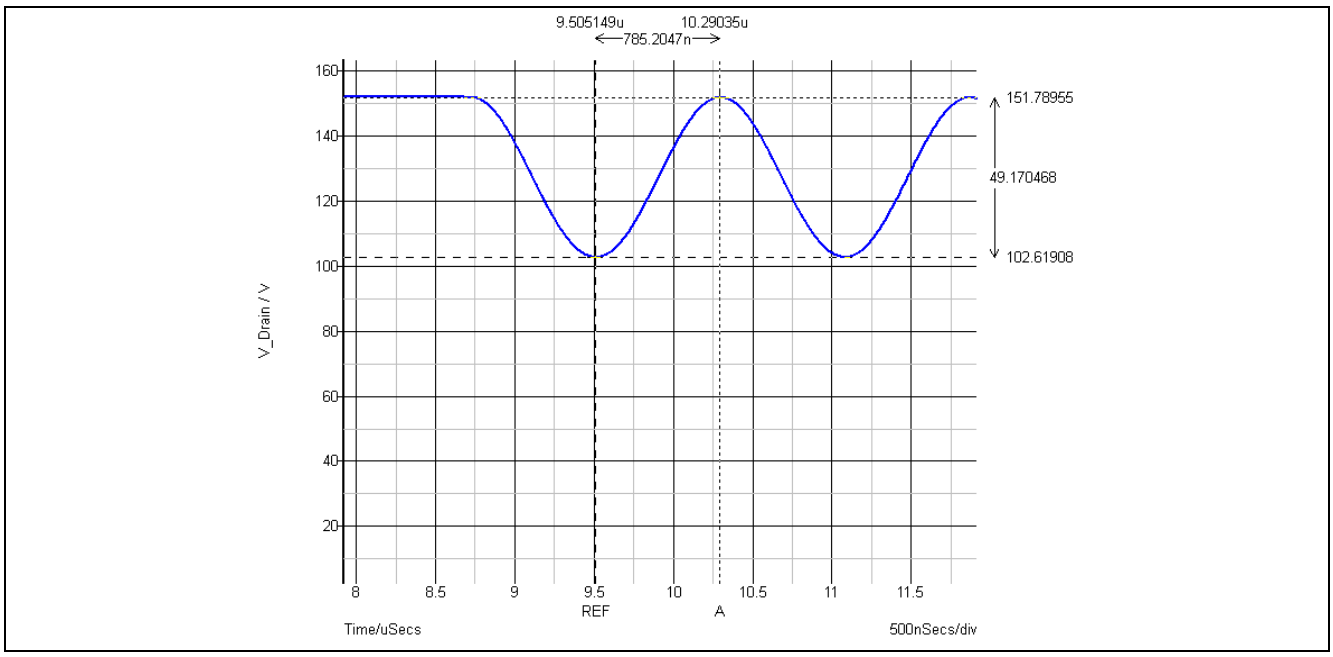


Figure 41 Example V_{DS} waveform during QR-ringing interval with low input voltage.

The procedure is exactly the same as before

$V_{pk2} := 152$ V

$V_{val2} := 103$ V

Values pertaining to QR period with low-line input voltage

$t_{QR2} := 1.570 \cdot 10^{-6}$ s

$f_{QR2} := \frac{1}{t_{QR2}} = 6.369 \times 10^{5}$ Hz

$C_{oss\_tr2} := \frac{Q_{oss}(V_{pk2}) - Q_{oss}(V_{val2})}{V_{pk2} - V_{val2}} = 5.9 \times 10^{-11}$ F

$C_{par\_pri2} := \frac{\left(\frac{1}{2 \cdot \pi \cdot f_{QR2}}\right)^2}{L_{pri}} - C_{oss\_tr2} - C_{par\_can} = 7.071 \times 10^{-11}$ F

Equivalent lumped primary-side referenced capacitance under low-line input

…and the resulting primary referenced lumped capacitance is similar at ~71 pF (70 pF found under high-line conditions).

A small difference might be expected, since any damping and loss mechanisms are neglected and primary reflected lumped capacitance could comprise non-linear elements itself (such as the C_{oss} of secondary side Synchronous Rectifier).

The last remaining un-known quantity related to the QR operation has been revealed; enabled by the data for Q_{oss} vs. V_{DS}. With all the relevant quantities known, the energies during the QR interval can be estimated. At the switch-over between T_{off} and T_{QR} the energy in the magnetizing inductance is 0A. The QR ringing wave shape can be estimated to be a sinusoid (assume linear C_{oss} with value C_{oss_tr} during the QR ringing interval and no damping effects) with the amplitude of the reflected output voltage and a frequency determined by the parasitic elements (and L_{pri}).

$_N := 5$ T — Transformer turns-ratio

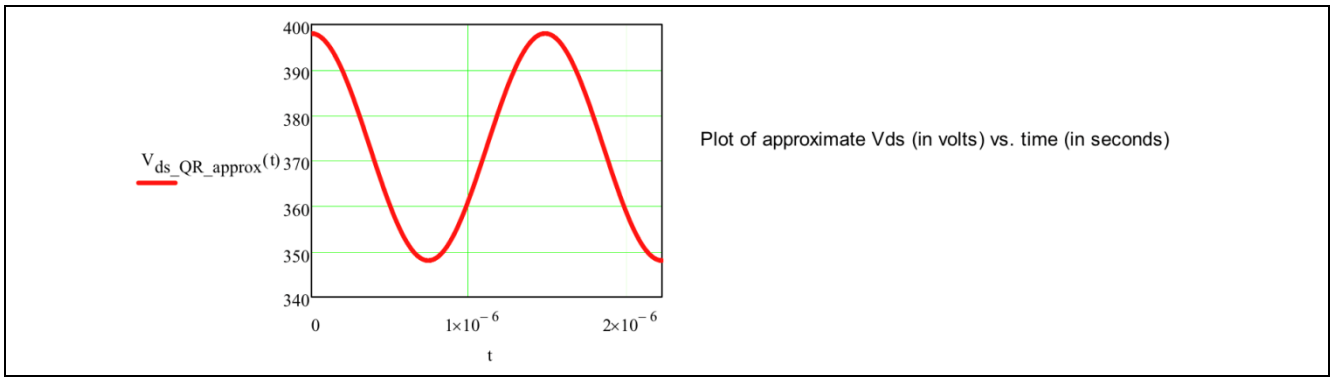
$V_{bulk} := 373$ V — Simulated bulk voltage measurement

$V_o := 5$ V — Output voltage

$V_{o\_ref} := V_o \cdot _N$ V — Output voltage reflected through transformer to primary side

$$V_{ds\_QR\_approx}(t) := V_{bulk} - V_{o\_ref} \cdot \sin\left[\frac{1}{\sqrt{L_{pri}\cdot(C_{oss\_tr} + C_{par\_pri} + C_{par\_can})}}\cdot t + \frac{3}{2}\cdot\pi\right]$$

Approximating the QR-period Vds waveform with a sine-wave



Plot of approximate Vds (in volts) vs. time (in seconds)

Figure 42 Graphing V_{DS} as an estimated sinusoidal wave shape of known frequency and amplitude

With deeper and deeper valley – lower V_{bulk}, higher V_{out} and higher turns-ratio – the non-linearity of C_{oss} can cause gross distortion of the wave-shape, and the sinusoidal wave shape approximation becomes untrue. This is particularly true for high-density SJ MOSFETs with very highly non-linear C_{oss}. For this example though, the approximation is reasonable, since the peak- and valley voltages stay within a reasonably linear portion of the C_{oss} curve. When the MOSFET V_{DS} is identified, all resonant currents can be calculated and plotted:

$$i_{QR}(t) := (C_{oss\_tr} + C_{par\_can})\cdot\left(\frac{d}{dt}V_{ds\_QR\_approx}(t)\right)$$

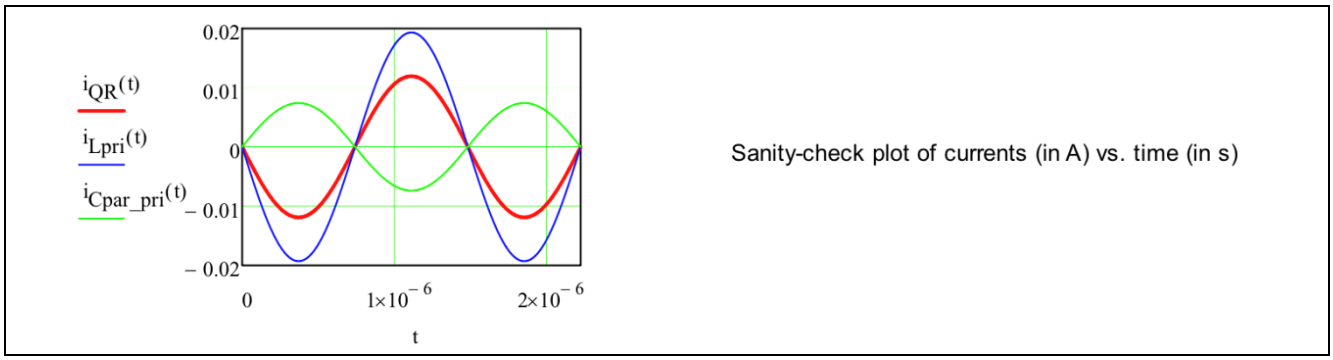
total loop current flows through the parallel combination of Coss and primary-to-cancellation inter-winding capacitance Cpar_can

$$i_{Lpri}(t) := 0 + \frac{1}{L_{pri}}\cdot\int_0^t V_{bulk} - V_{ds\_QR\_approx}(t)\,dt$$

Standard current/voltage relationship for inductors with initial condition of 0A flowing at the start-time of T_QR

$$i_{Cpar\_pri}(t) := i_{QR}(t) - i_{Lpri}(t)$$

Kirchoff's current law applied to find the last unknown current



Sanity-check plot of currents (in A) vs. time (in s)

Figure 43 Calculation of QR related currents as a function of time - based on approximated $V_{DS}(t)$

With all voltages and currents around the QR resonant tank loop known, the various energies can be computed

$E_{cpri\_v}(V_{ds}) := \frac{1}{2}\cdot C_{par\_pri}\cdot(V_{ds} - V_{bulk})^2$	J	Total capacitive energy vs. Vds for Cpar_pri (has Vds - Vbulk across it)
$E_{ccan\_v}(V_{ds}) := \frac{1}{2}\cdot C_{par\_can}\cdot V_{ds}^2$	J	Total capacitive energy vs. Vds for Cpar_can (has Vds across it)
$E_{oss\_can\_v}(V_{ds}) := E_{ccan\_v}(V_{ds}) + E_{oss}(V_{ds})$	J	Total capacitive energy in parallel connection of Coss and Cpar_can Vs. Vds
$E_{Lpri\_i}(i_{Lpri}) := \frac{1}{2}\cdot i_{Lpri}^2\cdot L_{pri}$	J	Total inductive energy in primary inductance vs. current through it

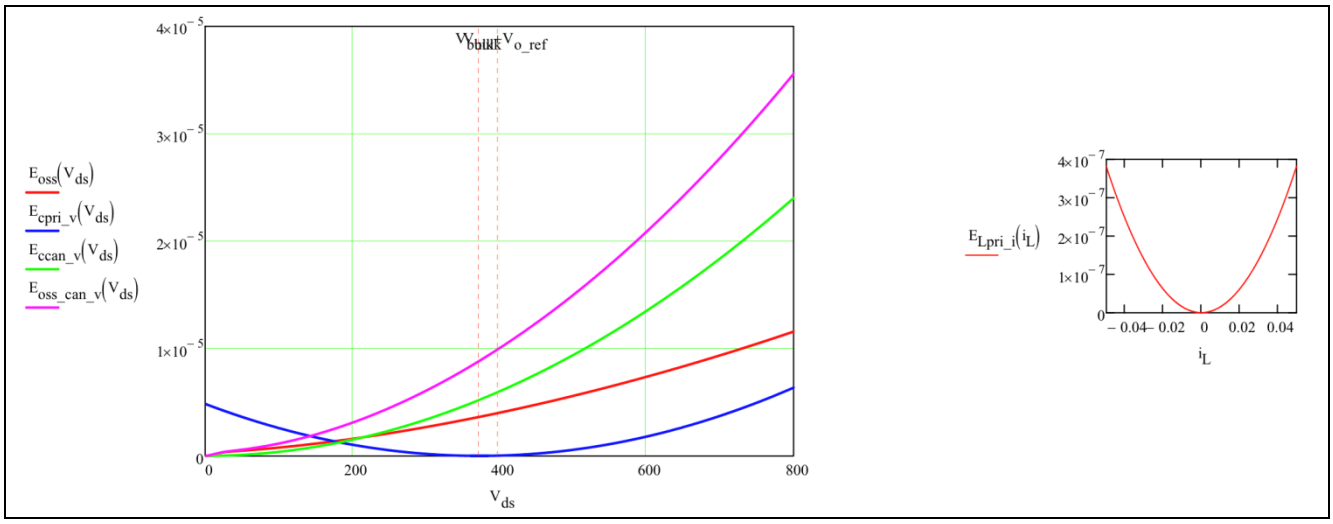


Figure 44 Various capacitive energies vs. V_{DS} (Left) and inductive energy vs. the current through it (Right)

Since the voltages and currents vs. time are known, the energy vs. time can be calculated and plotted for all reactive elements (including bulk-voltage source)

$dE_{oss\_can\_t}(t) := E_{oss\_can\_v}(V_{bulk} + V_{o\_ref}) - E_{oss\_can\_v}(\text{round}(V_{ds\_QR\_approx}(t), 0))$	Energy delta over time for Coss parallel with Cpar_can (referencing initial energy at initial voltage)
$dE_{cpri\_t}(t) := E_{cpri\_v}(V_{bulk} + V_{o\_ref}) - E_{cpri\_v}(V_{ds\_QR\_approx}(t))$	Energy delta over time for primary referenced cap (initial energy based on initial voltage across it)
$E_{oss\_t}(t) := E_{oss}(\text{round}(V_{ds\_QR\_approx}(t), 0))$	Energy in Coss over time (not a delta)
$E_{ccan\_t}(t) := E_{ccan\_v}(V_{ds\_QR\_approx}(t))$	Energy in Cpar_can over time (not a delta)
$E_{Lpri\_t}(t) := E_{Lpri\_i}(i_{Lpri}(t))$	Energy in magnetizing inductance over time (starting energy is exactly 0, so absolute energy over time *is* the delta)
$P_{bulk}(t) := -i_{QR}(t)\cdot V_{bulk}$	Instantaneous power in the bulk-voltage source
$E_{bulk}(t) := \int_0^t P_{bulk}(t)\,dt$	Energy delta in the bulk-voltage source (based on power integrated)
$dE_{LCpri}(t) := (-dE_{cpri\_t}(t) + E_{Lpri\_t}(t))$	Energy delta in the primary side reference lumped capacitance and primary side inductance combined (IC = 0)

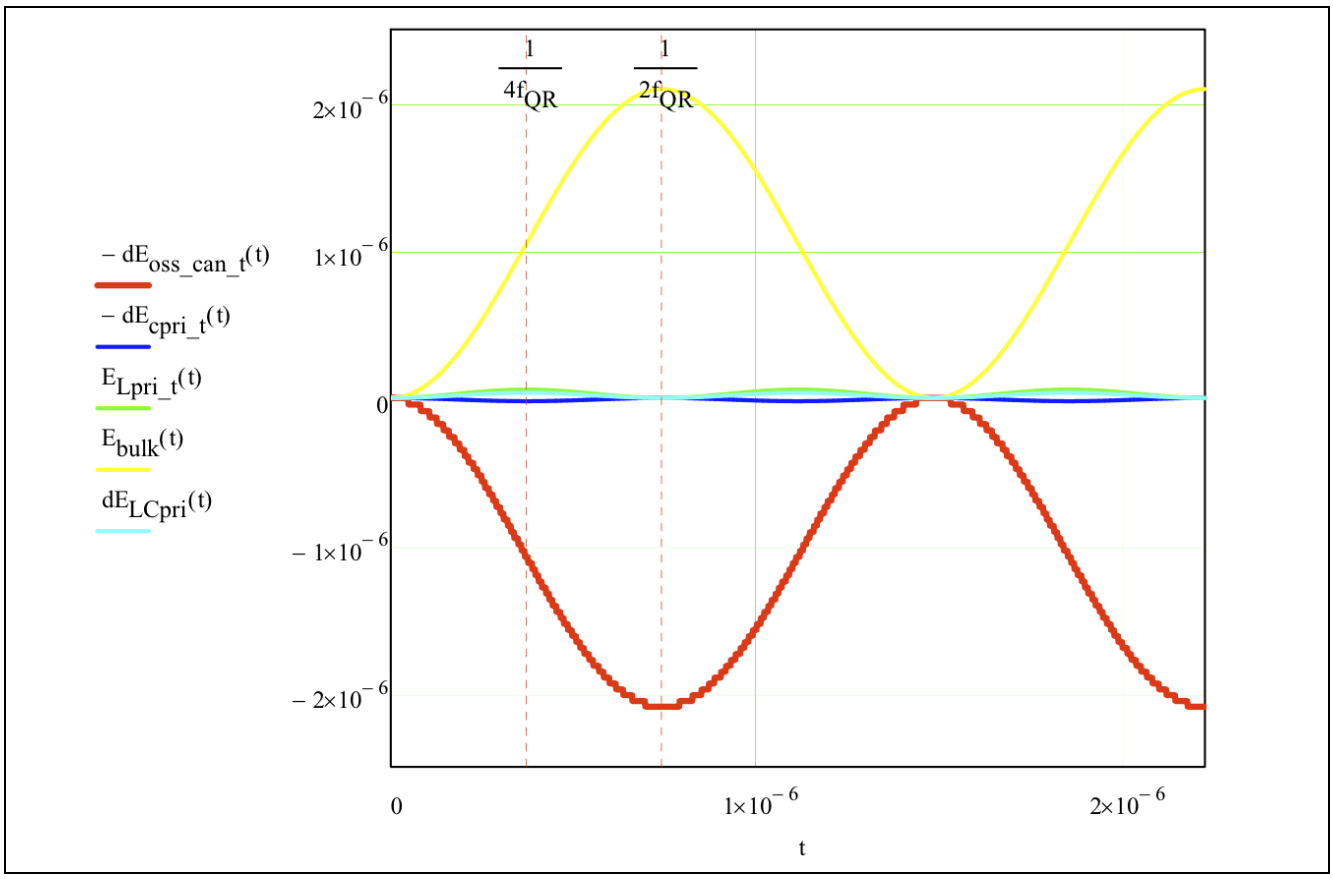


Figure 45 Energy deltas vs. time (t=0 is start of QR period with all dE=0)

In this particular example, the dominant resonant energy is the parallel C_{oss} and C_{par_can} capacitive energy being delivered from the capacitors to the bulk-voltage source during the first ½ period (negative slope indicates energy is removed from reactive element). This energy is then returned to those capacitors (from the bulk-voltage source) during the second ½ period. A small amount of energy from C_{oss} and C_{par_pri} is stored in L_{pri} during the first ¼ period and returned during the second ¼ period.

The energy initially stored on C_{par_pri} is delivered to L_{pri} during first ¼ period and returned during the second ¼ period. At the ½ period point (bottom of the valley), the net energy in the C_{par_pri} and L_{pri} combination is identical to the energy they had stored initially (true when assuming no damping effects). The energy delivery from C_{oss} and C_{par_can} to bulk-voltage source is facilitated by resonant tank operation and depends on the absolute levels of energy (bulk voltage as well as reflected output voltage).

The principle of conservation of energy dictates that the same amount of energy that “changed hands” during the first ½ period ($\omega = 0..\pi$) will “return” in the second ½ period ($\omega = \pi..2\pi$). A false assumption would be that the energy (delivered to the bulk-voltage source from C_{oss} and C_{par_can}) during the first ¼ period ($\omega = 0..1/2\pi$) is the same (quantity) as the for the second ¼ period ($\omega = 1/2\pi..\pi$).

Examples of MOSFET parameter extraction

$E_{oss\_can\_init} := E_{oss\_can\_v}(V_{bulk} + V_{o\_ref})\cdot J = 9.926 \times 10^{-6} J$	Energy stored on capacitance initally
$E_{oss\_can\_bulk} := E_{oss\_can\_v}(V_{bulk})\cdot J = 8.848 \times 10^{-6} J$	Energy stored on capacitace at Vds=Vbulk
$E_{qrt\_diff} := E_{oss\_can\_init} - E_{oss\_can\_bulk} = 1.078 \times 10^{-6} J$	Energy delivered to source during first 1/4 period
$E_{oss\_can\_val} := E_{oss\_can\_v}(V_{bulk} - V_{o\_ref})\cdot J = 7.832 \times 10^{-6} J$	Energy stored on capacitance at Vds=Vval
$E_{2ndqrt\_diff} := E_{oss\_can\_bulk} - E_{oss\_can\_val} = 1.016 \times 10^{-6} J$	Energy delivered to source during second 1/4 period

Energy difference in the first two ¼ periods (1.078 µJ in first ¼ period vs. 1.016 µJ in second ¼ period) is due to the DC-offset of the ringing (not ringing about 0 V, rather ringing about V_{bulk}). Since energy is a function of (absolute) voltage squared, the DC offset influences symmetri. A greater energy 'discrepancy' can be seen, when the ratio of Valley-voltage to Peak-voltage is greater. This is obviously due to the squared dependency of absolute voltage. It is not caused by the non-linearity of C_{oss} – same behavior would be seen with a standard (linear) cap. In the case of higher output voltage and lower bulk-voltage, the non-linearity of C_{oss} influences the wave shapes. In an operating condition like that, the strong non-linearity of C_{oss} also makes the previous assumptions incorrect (to a significant extend) and the distortion of the (sine) wave shapes makes theory/math a bit more involved. Instead of math, simulations are appropriate to use to examine the consequences to energy differences and wave shape distortion due to non-linearity of C_{oss} (example uses V_{bulk} = 100 V and V_{o_ref} = 100 V).

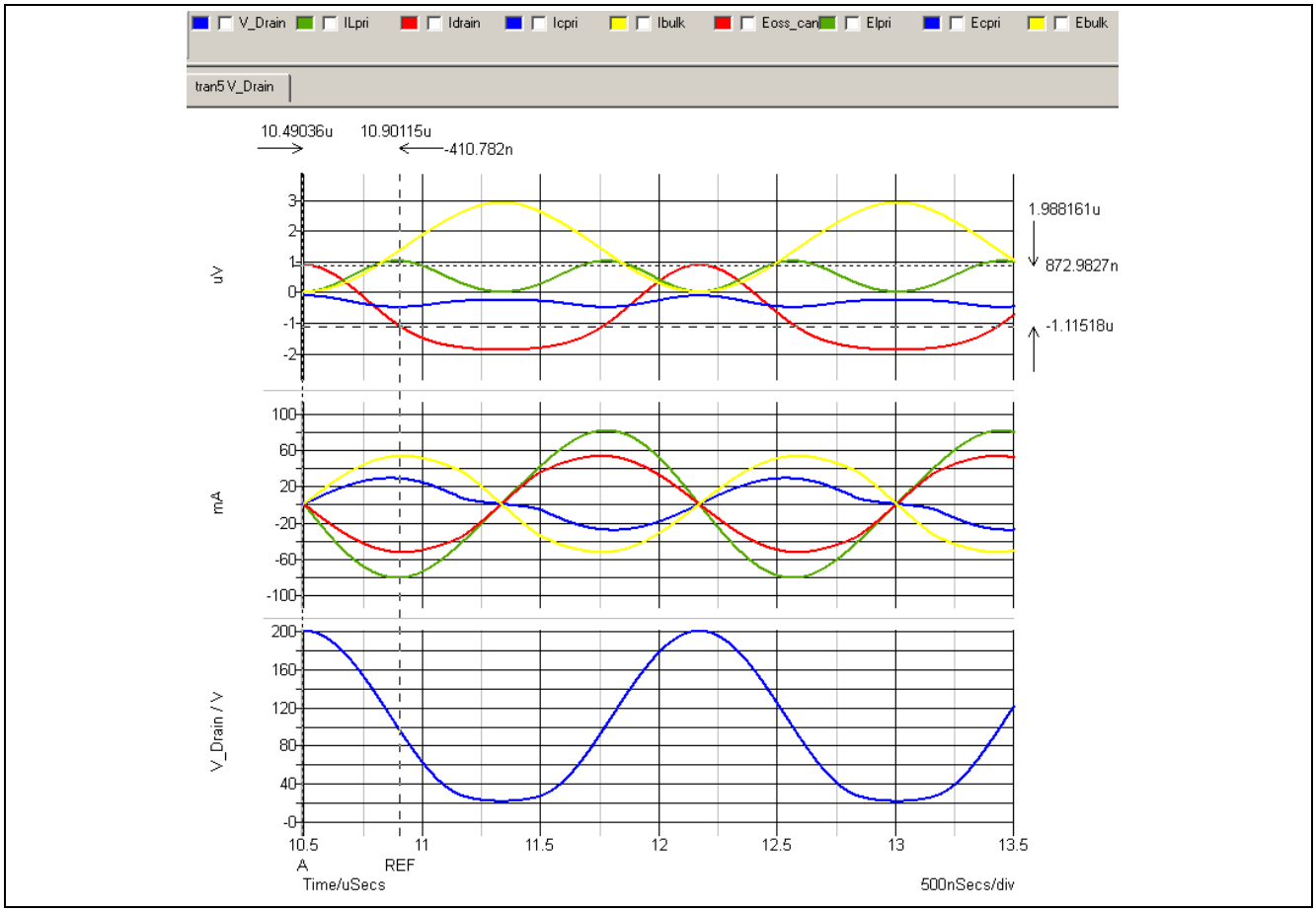


Figure 46 Energies (top graph), Currents (middle graph) and V_{DS} (bottom graph) in QR period with V_{bulk} = 100 V and V_{o_ref} = 100 V {C_{par_pri}=75 pF, L_{pri}=305 µH, C_{par_can}=75 pF and SPA11N80C3}

The energy difference (energy transferred from C_{oss_can}) during the first ¼QR interval {$V_{Bulk}+V_{o\_ref} > V_{ds} > V_{Bulk}$} is ~$E_{QR1}$=1.99 µJ, while it is only ~E_{QR2}=780 nJ in the second ¼ QR interval {$V_{Bulk} > V_{DS} > V_{val}$}. The gross distortion in the V_{DS} waveform is clearly evident – even more so in the current waveform of C_{par_pri}) – with the valley voltage much higher than the "expected" 0 V {~20 V in example}. The distortion is caused by the non-linearity of C_{oss} and would not be present if C_{oss} were linear.

4.3.3 Calculating E_{oss} loss based on imported data

In the above we found all relevant energies at any given time during the QR period (as long as $V_{DS}(t)$ was first calculated). It was also argued that the most relevant energies were the ones of the MOSFET output capacitance and any parasitic capacitances in parallel with it. The energies in the primary-side referenced inductance and the primary-side referenced lumped capacitance were of less significance, when the bulk voltage is high and the output voltage (and transformer turns-ratio) is low.

Exactly at the valley, the energy in the primary-side inductance is 0 J, and can not cause any losses. The MOSFET will turn on, and assuming an instantaneous turn-on, the C_{oss} and C_{par_can} will be "shorted" by the MOSFET $R_{DS(on)}$. The energy contained in these capacitances will thus be dissipated in the MOSFET as E_{oss} loss (referencing Chapter 3). Any energy contained in the primary-side referenced lumped capacitance will be supplemented with additional energy (from the bulk-voltage source) upon MOSFET turn-on (it will be charged from ~(V_{bulk} – V_{val}) to ~V_{Bulk} during MOSFET turn-on). The only energies that result in E_{oss}-type losses are thus the energies contained in C_{oss} and C_{par_can}:

$$E_{turn\_on\_loss} := E_{oss}(round(V_{val}, 0)) + E_{ccan\_v}(V_{val}) = 7.832 \times 10^{-6} \quad J$$

Energy burnt in Rds(on) during MOSFET turn-on

For an example application switching at a rate of 100 kHz, the E_{oss} (and E_{par_can}) power loss then equates to

$$P_{turn\_on\_loss} := E_{turn\_on\_loss} \cdot 100 \cdot 10^{3} \cdot W = 783.19 \cdot mW$$

Expected MOSFET turn-on power loss in 100kHz switching frequency application based on Eoss and Epar_can

…roughly 783 mW, with V_{bulk}=373 V and reflected output voltage V_{o_ref}=25 V.

In comparison with a pure DCM flyback working at an operating point, where the turn-on happens to occur consistently at the following peak (after 1st valley), the energy and power savings achieved by valley-switching can be considerable. Another good reference point is if measures are taken to increase reflected output voltage (either by transformer turns ratio or by increasing output voltage directly) and lower the bulk voltage; the example graphed in Figure 44 (bottom graph) is used.

$$E_{turn\_on\_398V} := E_{oss}(V_{bulk} + V_{o\_ref}) + E_{ccan\_v}(V_{bulk} + V_{o\_ref}) = 9.926 \times 10^{-6} \quad J$$

Energy dissipated if hard-switching at the peak (probabillity in DCM)

$$P_{turn\_on\_398V} := E_{turn\_on\_398V} \cdot 100 \cdot 10^{3} \cdot W = 992.575 \cdot mW$$

Equivalent turn-on power dissipation for peak-switching in DCM at 100kHz

$$E_{turn\_on\_20V} := E_{oss}(20) + E_{ccan\_v}(20) = 2.837 \times 10^{-7} \quad J$$

Energy dissipated if valley voltage is 20V (at low input- and high output-voltage)

$$P_{turn\_on\_20V} := E_{turn\_on\_20V} \cdot 100 \cdot 10^{3} \cdot W = 28.368 \cdot mW$$

Equivalent turn-on power dissipation for lower valley switching

As expected, there is clearly a strong case for ensuring lowest possible valley voltage switching in QR flyback applications.

4.3.4 E_{oss} loss in other applications (general) and significance of Q_{oss}

E_{oss} loss – out of all switching loss mechanisms mentioned in Chapter 3 – is what is mostly targeted in soft-switching applications. In modern SJ MOSFETs, the high C_{oss} at very low V_{DS} provides natural ZVS turn-off (also known as “early channel turn-off”). The MOSFET channel is able to turn off completely before the load current (drain-current) is able to charge the C_{oss} to any appreciable voltage. The MOSFET V_{DS} and I_D waveforms as measured on a scope will show a huge overlap, however the I_D will flow predominantly through C_{oss}, which is ideally a lossless element (purely reactive), and the instantaneous power as shown on the scope as the product of voltage and current will therefore not reflect loss (rather energy stored). In most applications, the gate-charge related losses are negligible compared to overall losses; particularly at full load, where the losses are important for thermal considerations. The turn-on switching loss (overlap between voltage across and current through the MOSFET channel) can be significant depending on the amplitude of the current switched, but in any DCM operation the switched current is 0A and the turn-on switching loss therefore comparatively small (when compared to the other loss mechanisms).

The most significant loss mechanism – and therefore the one targeted by many soft-switching techniques – is thus the E_{oss} loss determined by V_{DS} at turn-on (and the magnitude of which is detailed in example in above paragraph). In order to reduce the magnitude of this loss, the valley-switching is implemented in the Flyback example above. Other topologies – or techniques – aim to achieve full ZVS during turn-on; such as the LLC for example. In case of such topologies, the importance of E_{oss} diminishes (assuming the resonant inductance has much greater energy at transition than the energy required to discharge the C_{oss}), and Q_{oss} becomes much more important (the time it takes to complete such resonant V_{DS} transition). In the case, where the energy in the resonant inductance is much greater than the E_{oss} required for the transition (such as a majority of LLC implementations), C_{oss} is charged by a current that is approximately constant during the switching transition. The resonant transition will have a wave shape that is steep at high V_{DS}, where C_{oss} is small and shallow at low V_{DS}, where C_{oss} is large. However, we can approximate V_{DS} with a linear slope that intersects the actual wave-shape at the time and voltage of interest. If the voltage is known (bulk-voltage), the time can be found from the equivalent time-related C_{oss_tr} and charging current.

$V_{bulk\_llc} := 400$ V

$I_{Lr} := 1$ A

$t_{res\_trans} := \frac{Q_{oss}(V_{bulk\_llc})\cdot 2}{I_{Lr}} \cdot s = 129.93 \cdot ns$

Time it takes for the "constant" resonant inductor current to charge twice (half-bridge) Qoss to the full bulk-voltage (typically 400V in PFC-front stage LLC application)

During this time, all switches in the LLC circuit must be off, and the 1 A charging current does not flow through transformer primary (rather the magnetizing inductance) – so there is no power transfer to the output. Since the charging current causes $I^2 \cdot R$ losses in the parasitic resistances around the resonant loop during this time, it is desirable to keep the dead time to a minimum. It is also clear that the greater the dead-time, the less power transfer “duty cycle”, which means higher peak power transfer when a switch is on – also an efficiency inhibitor.

High density modern SJ MOSFETs have low E_{oss} (less relevant for ZVS turn-on applications), but high Q_{oss} (a disadvantage for ZVS turn-on applications). For most soft-switching applications, the MOSFET technology/family must be chosen carefully to enable proper loss balance/tradeoffs.

4.4 Transfer characteristics extraction simulation test bench

Transistors are amplifiers, which can be clearly realized by looking at the traditional hybrid-π small signal model representation of a typical BJT. The transconductance amplifier delivers an output current that is proportional to the input voltage by a gain (g_m).

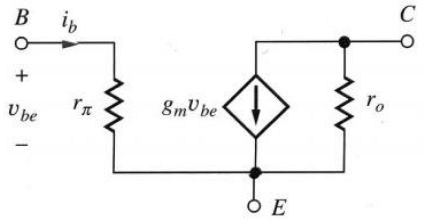


Figure 47 Common „hybrid-π“ small signal model of a typical BJT

Modern SJ MOSFETs can be similarly viewed as transconductance amplifiers, even though they are typically not used in their linear region (not used in small-signal mode, rather large-signal where they are either fully on or fully off). During transitions, however the linear region must necessarily be traversed, in which context the transconductance might be relevant to investigate in greater detail. It is common to see transfer characteristic curves in SJ MOSFET datasheets:

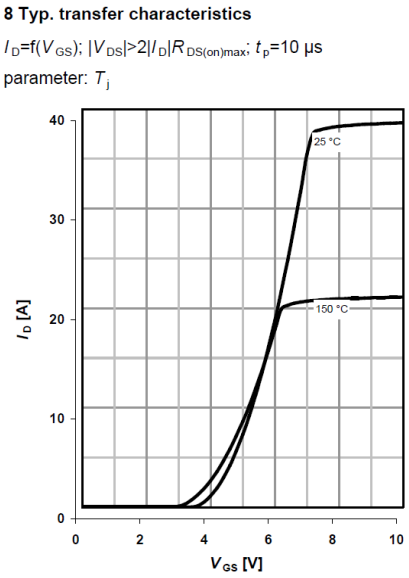


Figure 48 Excerpt of the example SPA11N80C3 datasheet showing typical transfer characteristics graph

To set up a test bench that will mimic these results, a static V_{DS} of some voltage is applied, while V_{GS} is ramped up over a short period (~10 µs). A V_{DS} which is higher than expected drain-current times twice $R_{DS(on)max}$ is required to arrive at a proper saturation point. For I_D=38 A max, a voltage source of

$$V_{ds} > 2 \cdot 0.45\Omega \cdot 38A \Rightarrow V_{ds} > 34.2\ V$$

is used.

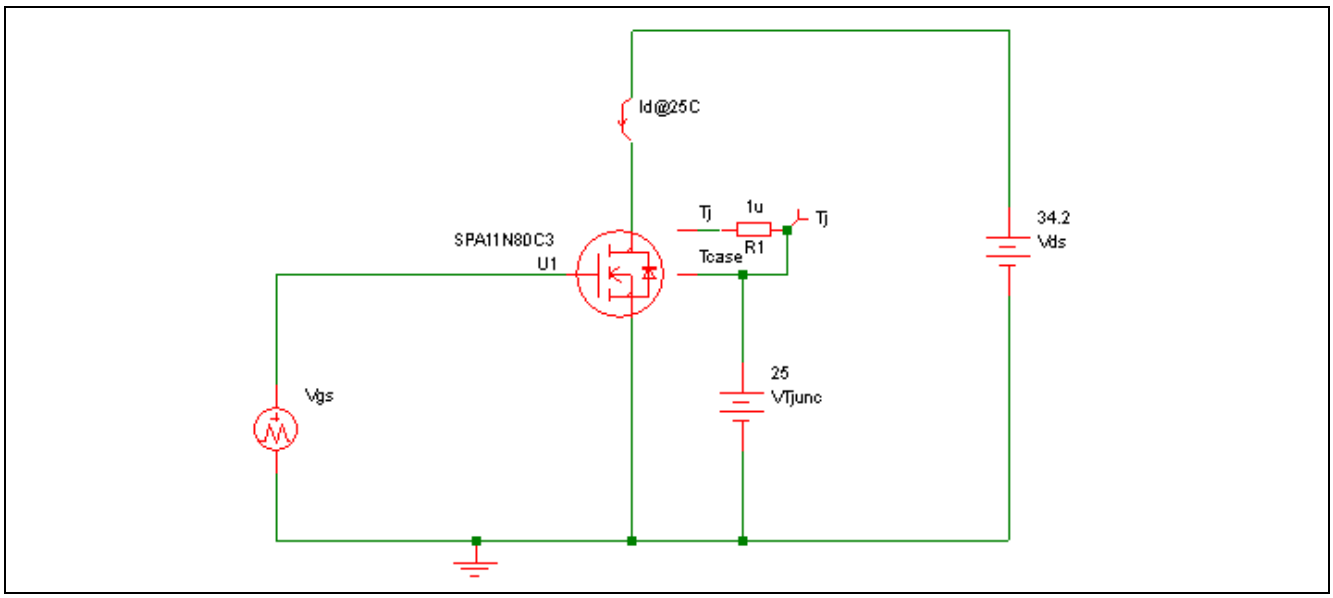


Figure 49 Test bench for extracting transfer characteristics at given I_D and T_j

V_{GS} is ramped from 0 V to 12 V in 12 µs, such that 1 µs on x-axis corresponds to 1 V_{GS}. The resulting output for 25°C and 150°C should be close to DS value

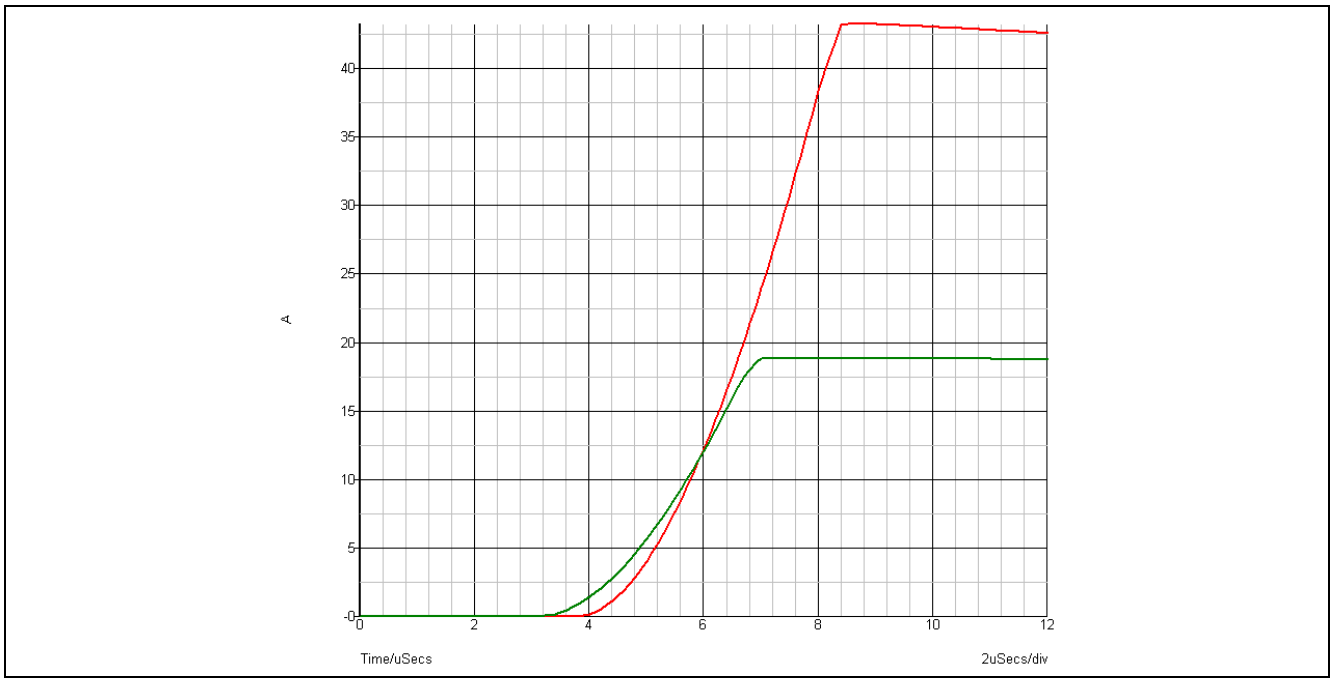


Figure 50 Transfer characteristics extracted from simulation model at 25°C (*Red*) and 150°C (*Green*) for SPA11N80C3 using V_{ds}=34.2 V

The cross-over point between the two can be observed close to 12 A @ 6 V, which might be a bit higher voltage than what it appears to be in DS (Figure 48), but close enough for usage. The saturation current levels are also a bit different than the DS given values, but this should be less consequential to the real usage of this data, since the maximum pulsed drain current is given at 33 A anyway, and this limit is typically a package limit rather than a silicon limit.

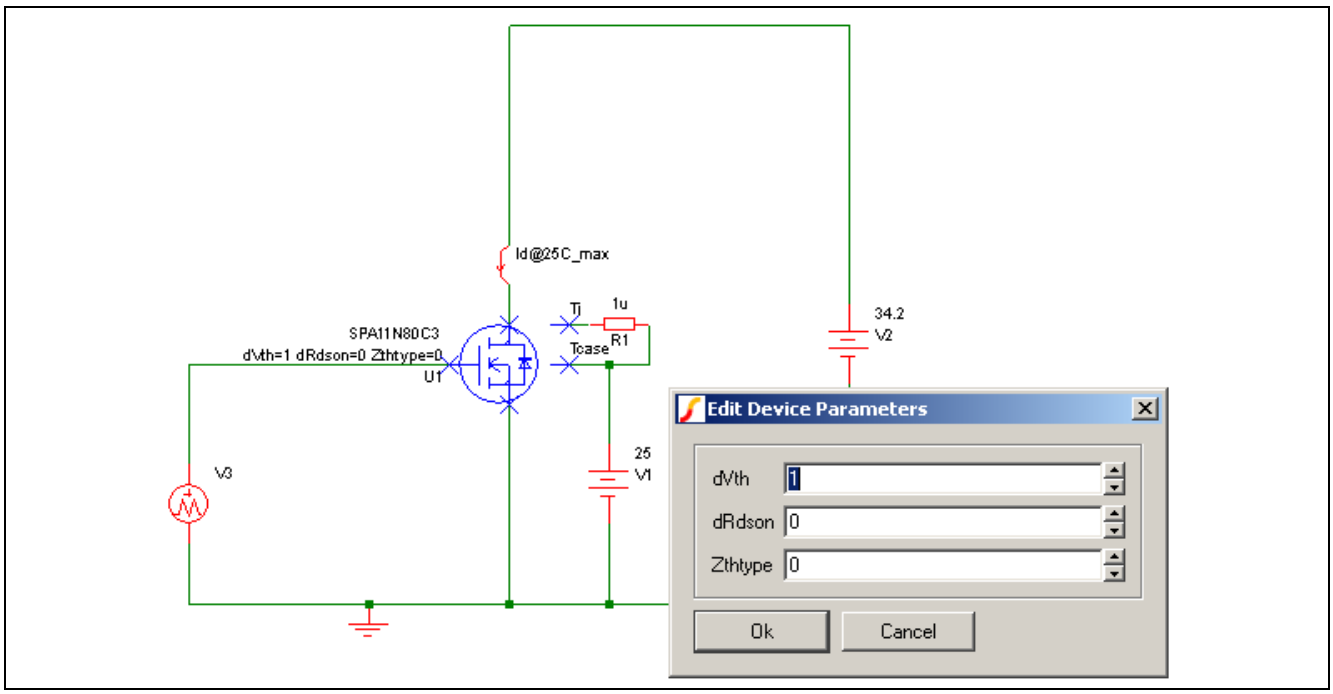


Figure 51 Changing additional parameter dV_{th} in model for min/max variance of threshold voltage

As detailed in **[1]** the model allows for some corner case testing – among others the MOSFET turn-on threshold. The transfer characteristics directly reflect a change in threshold voltage by shifting left or right on the V_{GS} axis.

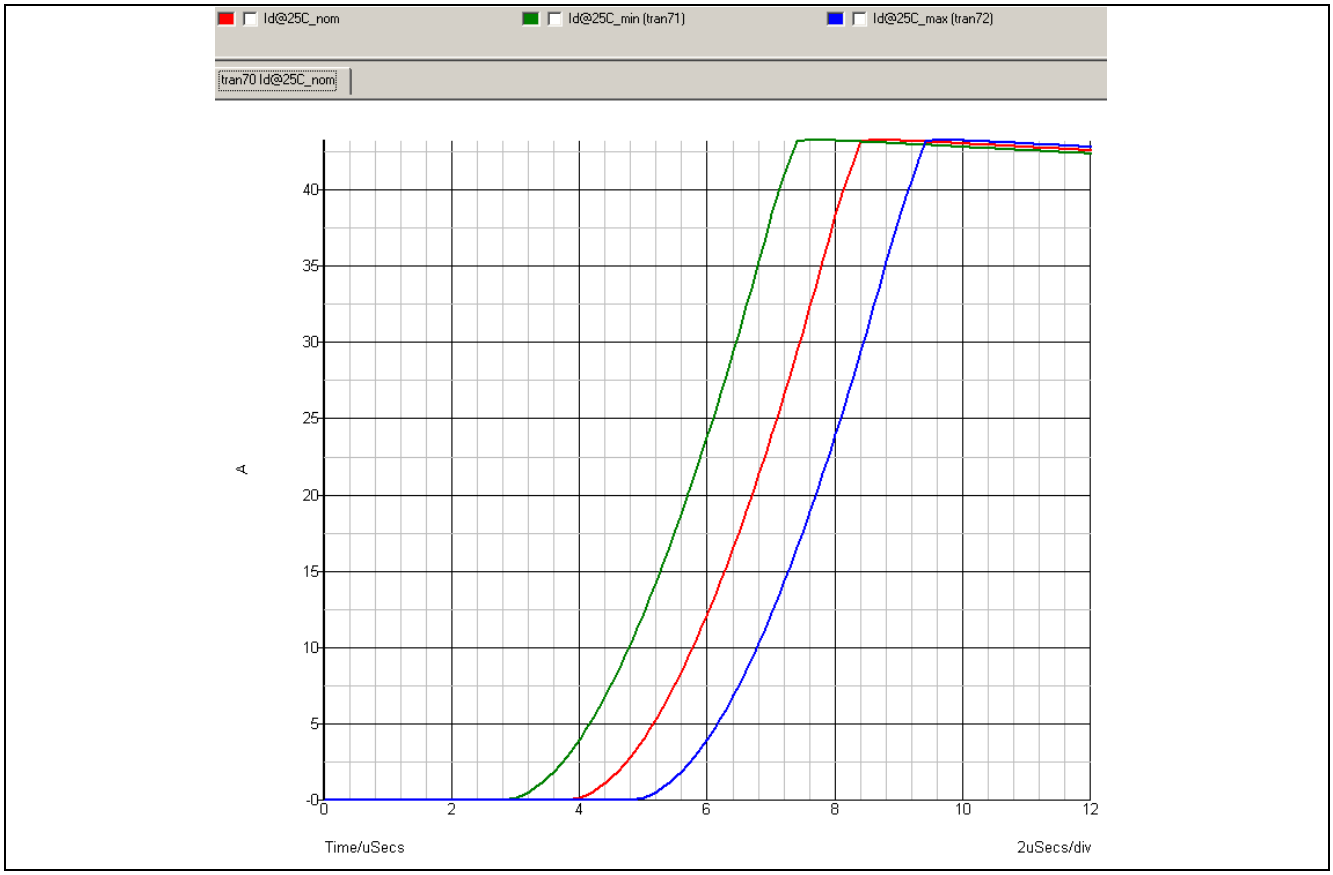


Figure 52 Resulting transfer characteristic curves when changing the model dV_{th} additional parameter

As is the case with (most of) the other parameters, the transfer characteristics are highly influenced by the technology/family of device. In the test bench from Figure 49, the derivative of the drain current can be calculated (divided by a volts-per-second factor) as an expression of the “amplifier” gain – for several technology families – in order to compare current switching abilities as well as stable operating conditions (amplifiers can be brought to instability by employing reactive loading and –feedback; i.e. C_{rss} is in the feedback path from output (drain) back to input (gate)).

4.4.1 Example use of extracted transfer characteristics

One example of valuable use of extracted transfer characteristics could be the comparison of different MOSFETs and technology families in terms of switching speed – which is an expression of the switching losses as outlined in Chapter 3, item 4. The absolute switching speed is best evaluated using simulation, but in order to compare several candidates for expected differences, it might be useful to extract and compare their gains and other parameters that influence switching speed/losses.

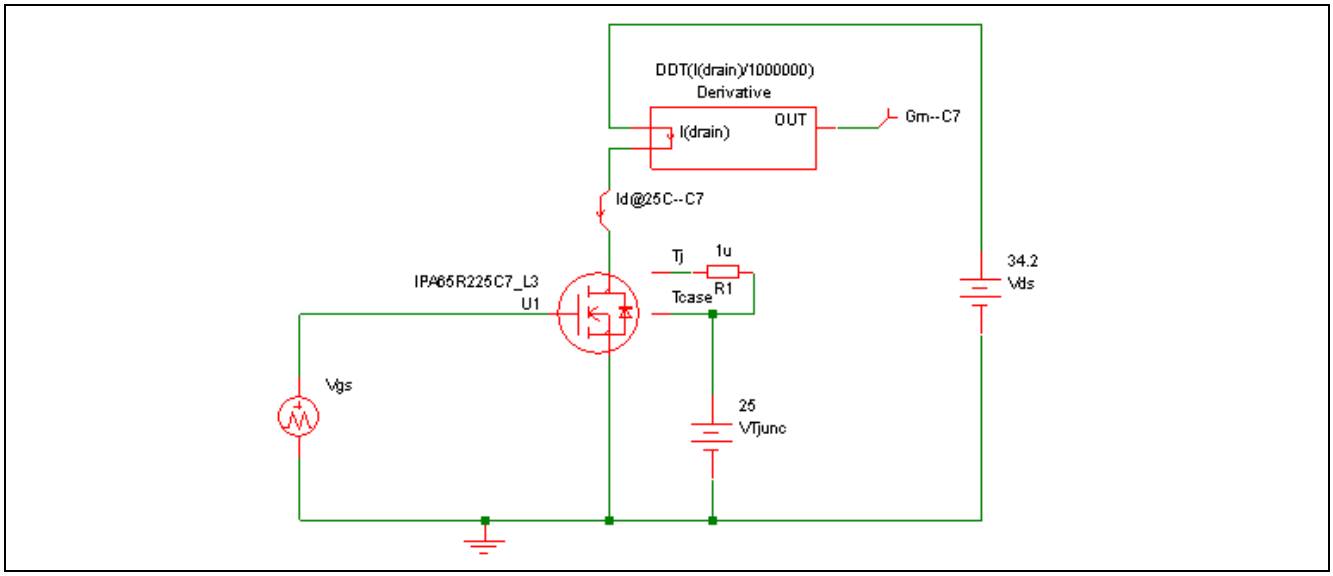


Figure 53 Modified transfer characteristics test bench for gain-evaluation of several SJ MOSFETs

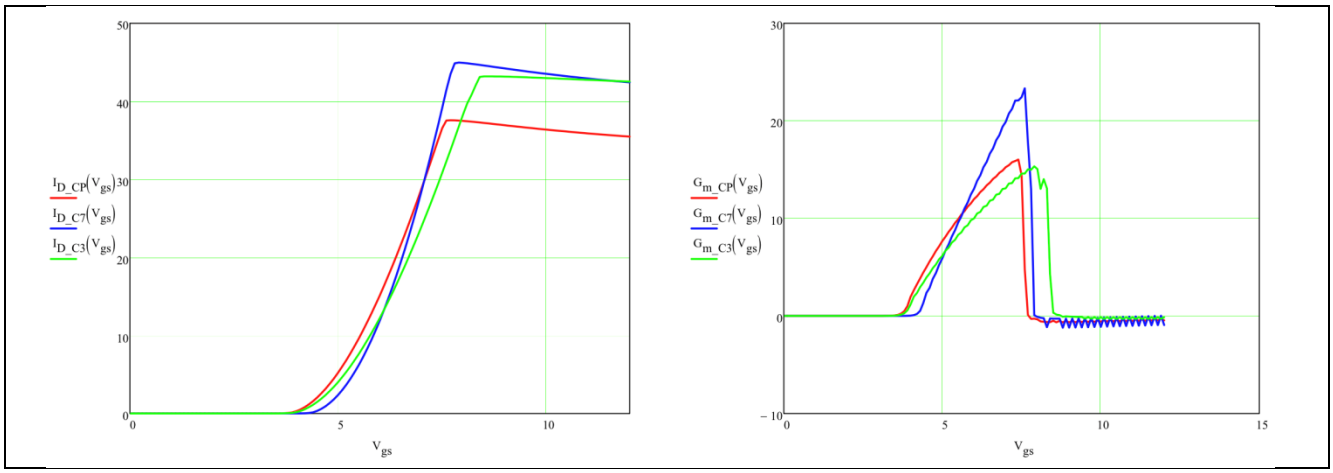


Figure 54 Simulation output (imported in Mathcad®) for Transfer Characteristics (left) and Transconductance Gain (right)

With a small modification to the C_{oss}, Q_{oss}, E_{oss} simulation extraction test bench (reference section 4.3), the $C_{rss}(V_{DS})$can be additionally extracted, which is useful since this parameter influences switching speed.

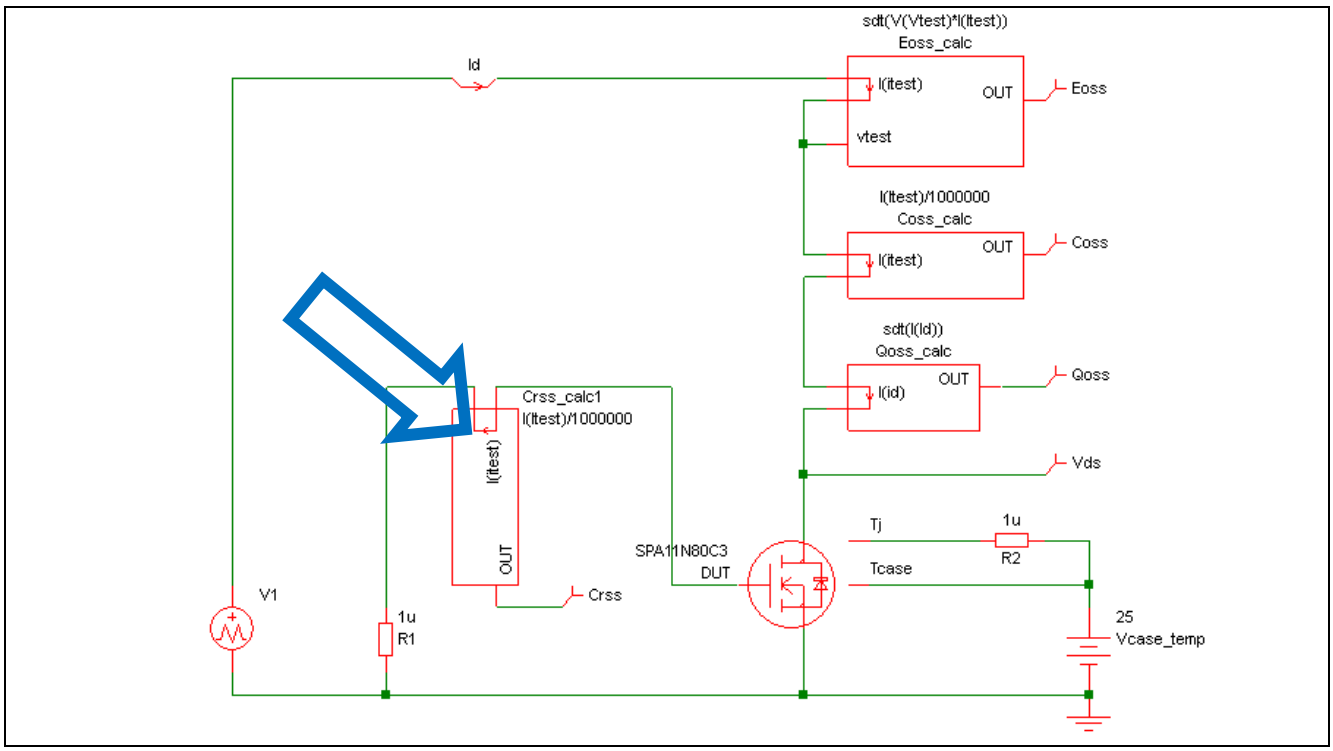


Figure 55 Adding another current integrator to C_{oss} extraction test bench to get C_{rss} as an output

A Mathcad® plot can show the difference in MOSFET technologies in terms of C_{rss}:

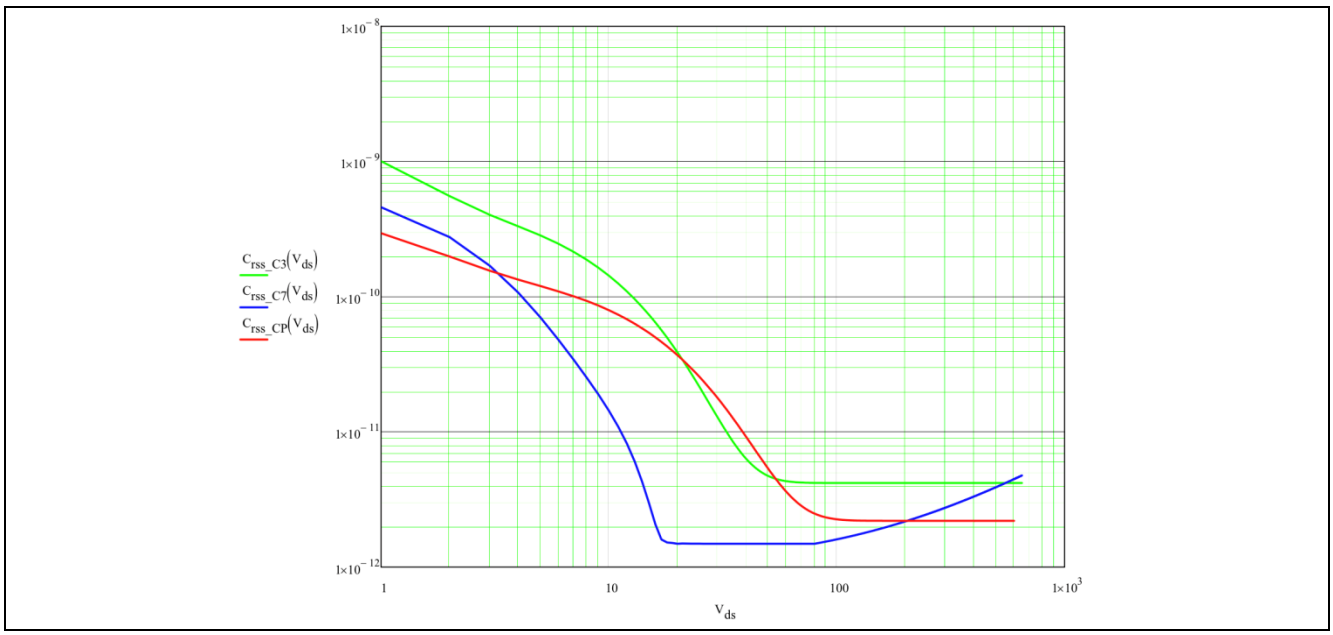


Figure 56 $C_{rss}(V_{DS})$ for different technologies extracted from models and plotted for comparison

At high V_{DS} (greater than ~50 V) C_{rss} is on the order of 4.2 pF for SPA11N80C3. The combination of relatively modest gain (~6.5 A/V for SPA11N80C3) with a somewhat high C_{rss} at V_{DS} of interest (>4.2 pF), makes the SPA11N80C3 a rather slow, but stable MOSFET with a high “ease of use”. And in spite of a much lower $R_{DS(on)}$ (~225 mΩ) than the compared CP and C3 (~400 mΩ), the C7 technology has higher gain combined with a much lower C_{rss} (<2 pF) – making for potentially much faster switching and thus lower switching losses (as outlined in Chapter 3, item 4).

5 References

[1] Application Note AN 2014-02 “Introduction to Infineon’s Simulation Models Power MOSFETs” V2.0 Feb. 2014. F. Stueckler, G. Noebauer, K. Bueyuektas.

5.1 Links

- Infineon Webpage:
  www.infineon.com
- MOSFET models:
  http://www.infineon.com/cms/en/product/promopages/simulationmodels/
- General power MOSFET related material:
  http://www.infineon.com/MOSFET

Revision History

Major changes since the last revision

Page or Reference	Description of change
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--	First Release

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