55 W Flyback converter design using the IRS2982S controller IRXLED04

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About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IRS2982S control IC for LED and general purpose switch mode power supply (SMPS). The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction

The IRS2982S is a versatile SMPS controller IC primarily intended for LED drivers in the 5 to 100 W power ranges suitable for Buck, Buck-Boost and Flyback converters operating in critical conduction mode (CrCM) and discontinuous mode (DCM) at light loads. Flyback converters will be covered in this application note focusing on an isolated voltage regulated design with PFC.

All of the control and protection required for the converter is integrated in the IRS2982S as well as a high voltage start-up cell to enable rapid illumination at switch on over a wide line input voltage range. The IRS2982S is also able to provide power factor correction in a single stage Flyback converter able to meet class C (lighting) line current harmonic limits of the EN61000-3-2 standard.

A 55W isolated voltage regulated PFC Flyback evaluation board based on the IRS2982S controller is described in detail in this application note and detailed test results are presented.

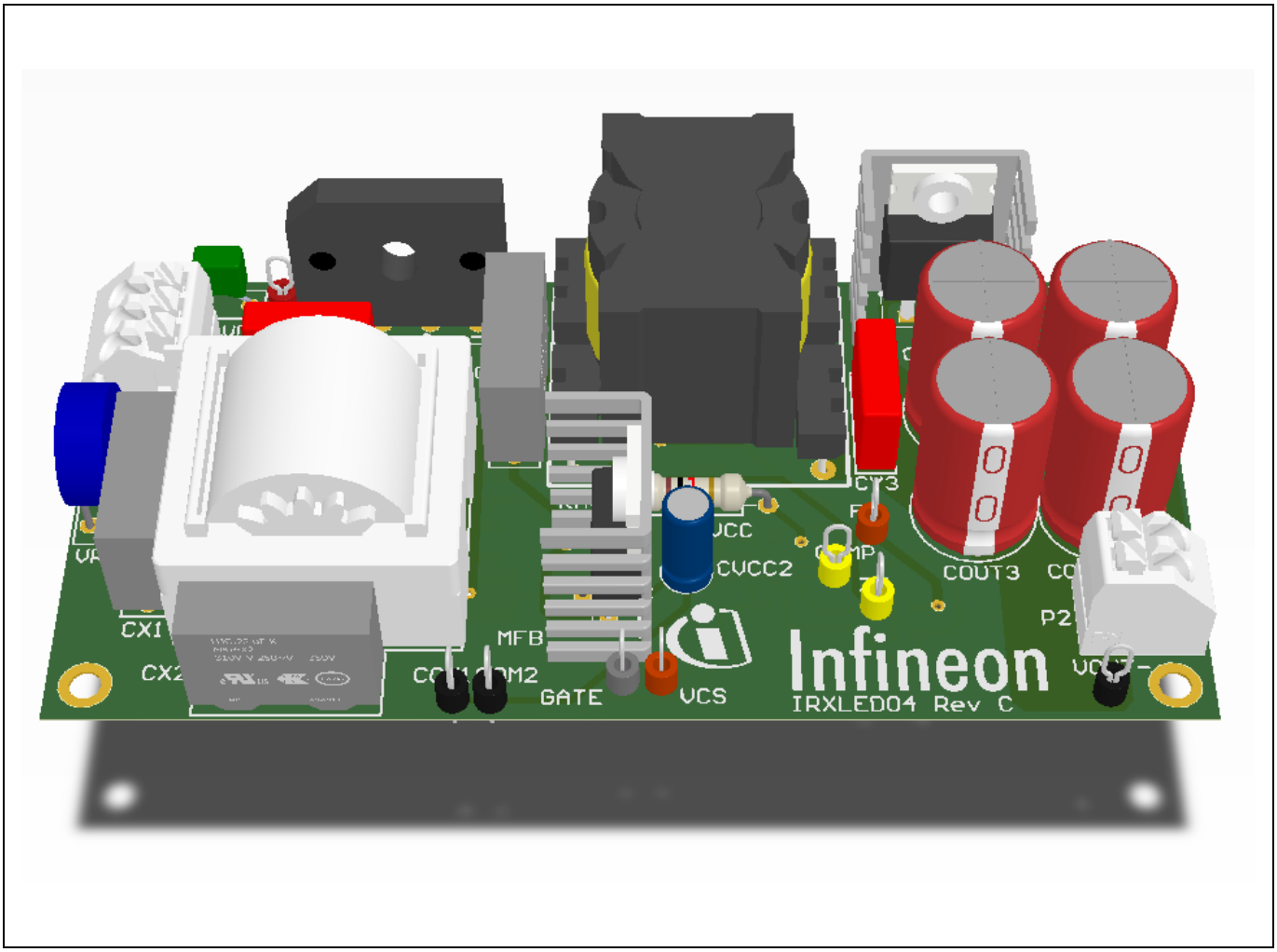


Figure 1 IRXLED04 55 W Flyback evaluation board

2 IRS2982S functional overview

The IRS2982S is comprised of the following functional blocks:

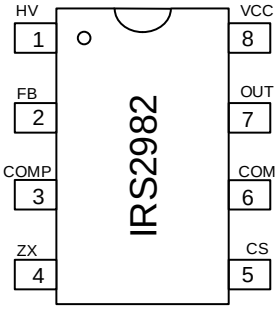
1. *High voltage start-up cell*
   The IC internal functional blocks remain disabled in low power mode until VCC first rises above the V_{CCUV+} under-voltage lock out (UVLO) threshold, continuing to operate while VCC remains above V_{CCUV-}. VCC is initially supplied through the integrated high-voltage start-up cell, which supplies a controlled current from the HV input provided a voltage greater than V_{HVSMIN}, is present. The current supplied is limited to I_{HV_CHARGE} reducing to less than I_{HVS_OFF} when VCC reaches the cut-off threshold V_{HVS_OFF1}. The HV start-up cell switches over from *start-up mode* to *support mode* after the feedback input at FB has exceeded V_{REG} for the first time. In this mode the cut-off threshold becomes V_{HVS_OFF2}. During steady state operation under all line-load conditions VCC is supplied through an auxiliary winding on the Flyback transformer with VCC high enough so that the HV start-up in does not supply current. If the auxiliary supply were unable to maintain VCC, the HV start-up cell operating in support mode would supply current to assist.

2. *PWM controller*
   The SMPS control section operates in voltage mode where the gate drive output on time is proportional to the error amplifier output voltage appearing at the compensation output COMP. An external capacitor CCOMP (shown in figure 4) connected to 0 V (ground) acts with the trans-conductance characteristic of the error amplifier to provide loop compensation and stability. Minimum on time is reached when V_{COMP} falls to $V_{COMPOFF}$ below which the gate drive is disabled. Under very light load conditions V_{COMP} transitions above and below $V_{COMPOFF}$ to produce burst mode operation. Off time is determined by the demagnetization signal received at the ZX input, which is derived from the auxiliary transformer winding that supplies VCC through a resistor divider. Internal logic limits the minimum off time to t_{OFFMIN}, therefore the system transitions from CrCM to DCM at light loads. If the ZX input signal fails to provide triggering the next cycle will start automatically after a re-start period of t_{WD}.

3. *Protection*
   The IRS2982S includes cycle by cycle primary over-current protection, which causes the gate drive to switch off if the voltage detected at the CS exceeds the threshold V_{CSTH}. This prevents the possibility of transformer saturation at low line under heavy load but does not protect against output overload or short circuit.

Over-voltage protection is also provided through the ZX input, which provides a voltage proportional to the output voltage. This disables the gate drive output and pulls the COMP voltage below the $V_{COMPOFF}$ threshold. The error amplifier then starts to charge CCOMP until the gate drive starts up again at minimum on time. Under an open circuit output condition the over voltage protection causes the converter to operate in burst mode preventing the output voltage from rising too high.

The IRS2982S uses an SO-8 package as shown below:



Pin	Name	Description
1	*HV*	High Voltage Start-up Input
2	*FB*	Feedback Input
3	*COMP*	Compensation and averaging capacitor input
4	*ZX*	Zero-Crossing & Over-Voltage Detection input
5	*CS*	Current Sensing Input
6	*COM*	IC Power & Signal Ground
7	*OUT*	Gate Driver Output
8	*VCC*	Logic & Low-Side Gate Driver Supply

Figure 2 IRS2982S pin assignments

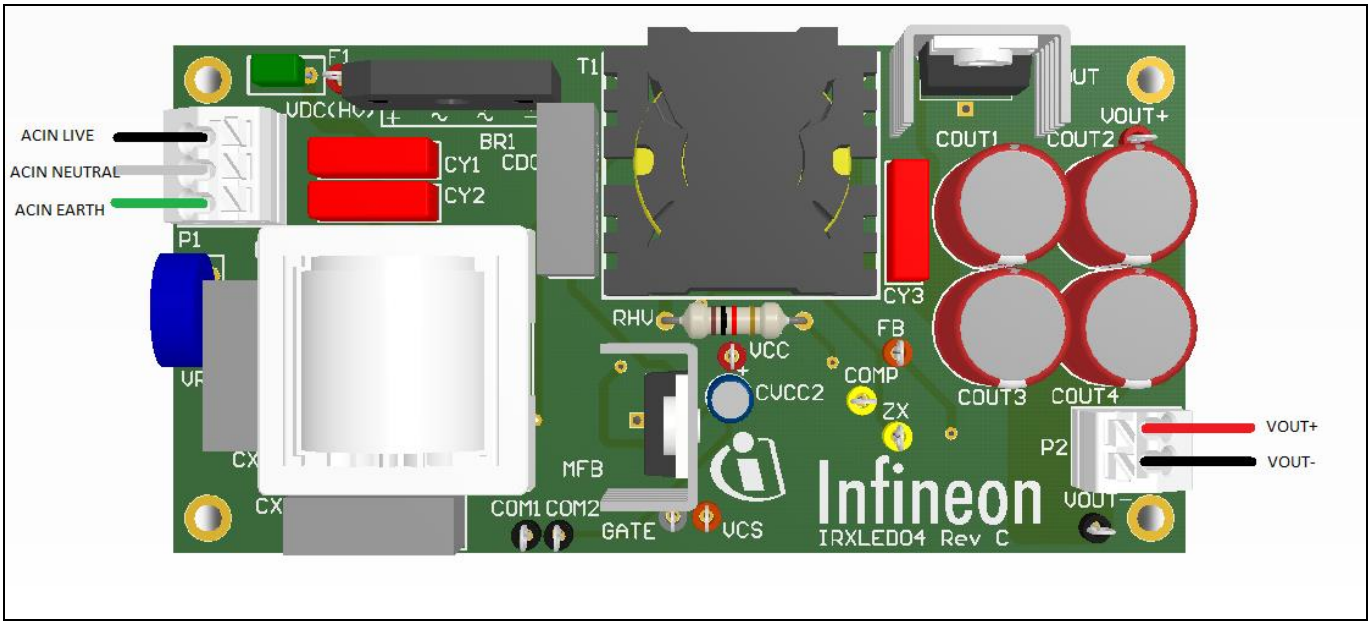


Figure 3 IRXLED04 Wiring Diagram

3 Flyback converter

3.1 Flyback converter types

There are several configurations of Flyback converter that may be used with the IRS2982S depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated,
2. Current or voltage regulation,
   In the case of voltage regulation current limiting is needed for protection against overload or short circuit and in the case of current regulation over-voltage protection is necessary for an open-circuit.

The IRS2982S can operate in any of the four combinations of (1) and (2). Extremely accurate current or voltage regulation is achieved in non-isolated converters since direct feedback to the FB input is possible. Isolation is however required in the majority of Flyback converters. For isolated constant current regulation an opto-isolator is necessary; for isolated constant voltage regulation feedback may be taken from the auxiliary winding as shown in figure 4 with a small loss of line and load regulation accuracy. An opto-isolator is also necessary for highly accurate voltage regulation.

The basic circuit in figure 4 shows the main elements of the IRS2982S based PFC Flyback converter. This can be used as a stand-alone power supply or as a front end stage with a current regulating Buck regulator as the back end stage in a dimmable (or non-dimmable) off line LED driver. This front end stage is able to provide a regulated output voltage over a wide range of line and load with sufficient accuracy for the majority of applications.

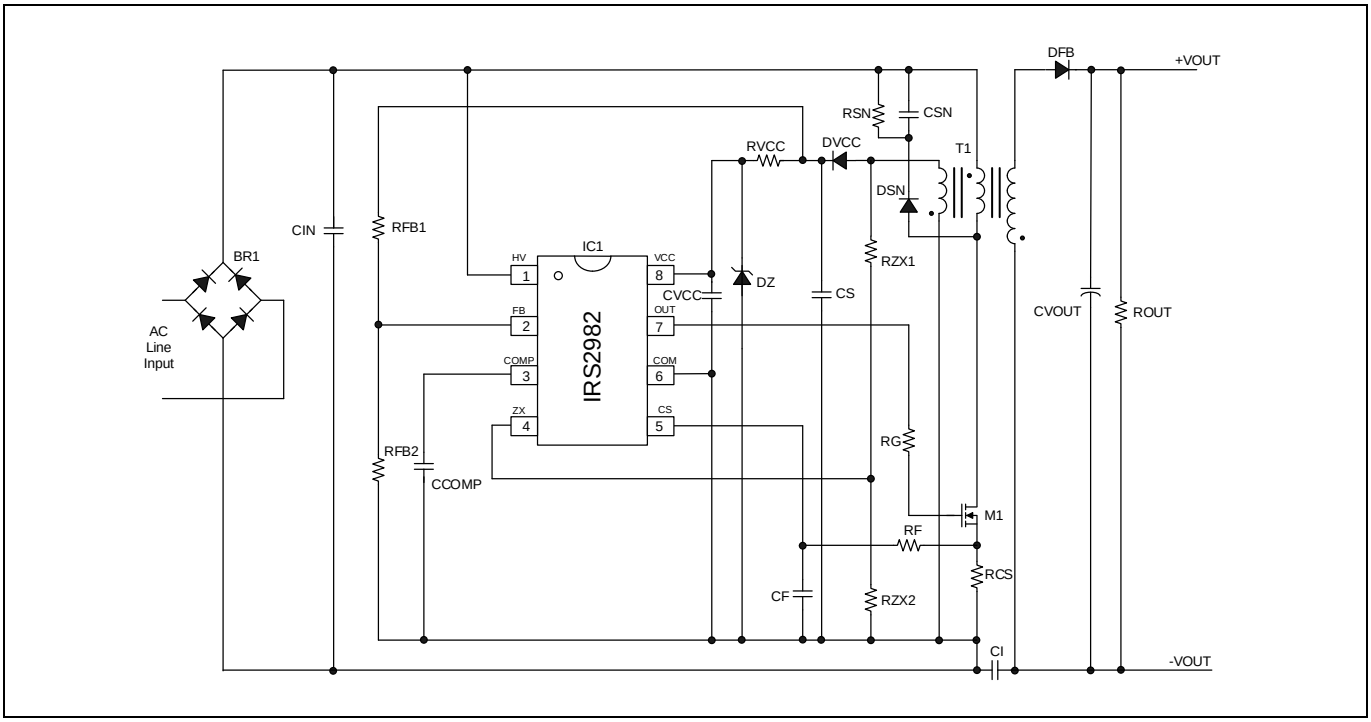


Figure 4 Isolated voltage regulated Flyback converter based on the IRS2982S

A 55 W PFC Flyback voltage regulated design as implemented in the IRXLED04 evaluation board will be discussed in detail in the following sections.

3.2 Eval board specifications

Input and output at normal operation:

- AC Input voltage 100 VAC up to 265 VAC (45 to 65 Hz)
- Output voltage 55 VDC
- Maximum output voltage ripple +/-3 V @ full load
- The tolerance of the nominal output voltage is +/-5% in the power range from 10% up to 100% of the rated output power.
- Maximum output continuous power 55 W
- PF >0.95 @50 W load and 230 VAC input voltage
- THD <10% @50% up to 100% load and < 20% @ 20% load with 230 VAC input voltage
- Efficiency >89% at 80% load and >88% at 100% load @ 230 VAC input voltage.
- Startup time to reach the secondary nominal output voltage of 55 VDC during full load condition and 230 VAC input voltage must be <300 ms.

Protection features

- Primary output over-voltage protection @ VOUT <= 60 VDC
- Cycle by cycle primary over-current protection

WARNING!
Output short circuit and overload protection are not provided on this evaluation board. This board can be damaged by sustained over loading or short circuiting the output!

No load operation

- Burst mode during no load condition.
- Max power losses during no load condition must be <500mW @230VAC input voltage

Max component temperature
During worst case scenario (ambient temperature 60 °C) the max allowed component temperature is:

- Resistor < 105 °C
- Ceramic capacity, film capacity and electrolyte capacity <85 °C
- Flyback Transformer and chokes <105 °C
- MOSFET, transistor and diodes <105 °C
- IC <100 °C

Dimension of evaluation board

- Max width 2.2” (55.9 mm), max length 4.4” (111.8 mm).

Safety Requirements
The single stage Flyback converter should cover the safety requirement regarding EN61347-2-13 and SELV max output voltage 60 VDC. This part of IEC 61347 specifies particular safety requirements for electronic control gear for use in DC supplies up to 250 V and AC supplies up to 1000 V at 50 Hz or 60 Hz and at an output frequency which can deviate from the supply frequency, associated with LED modules.

Note
This evaluation board is designed as a front end stage for a two stage power supply such as an LED driver where the back end stage is a current regulating Buck regulator. The Flyback converter uses primary voltage regulation with no secondary current feedback and is therefore not designed to withstand a sustained overload or short circuit condition. Additional circuitry may be added if such protection is required.

4 Schematic

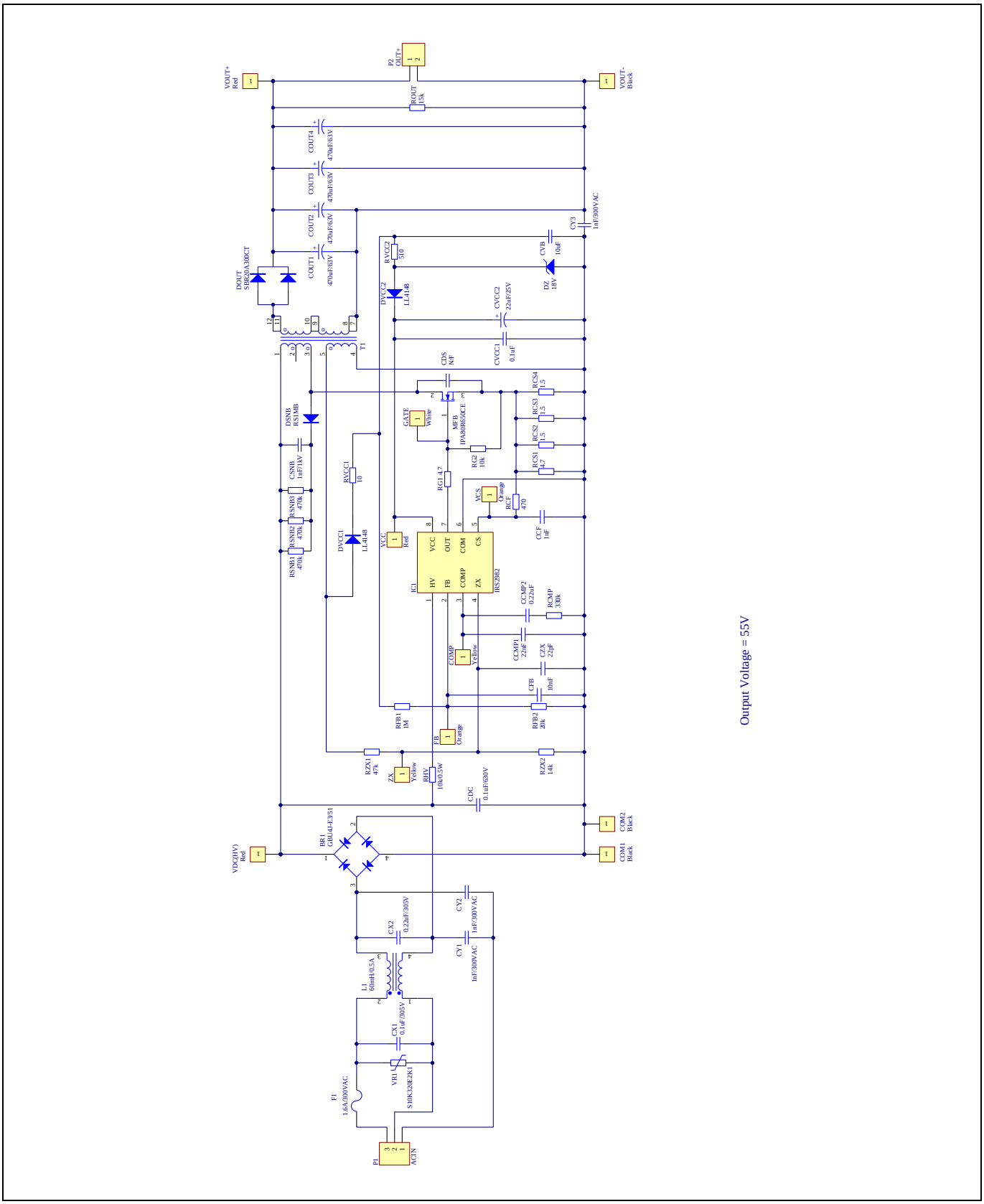


Figure 5 IRXLED04 55 W PFC Flyback schematic

5 Dimensioning

The IRXLED04 eval board is populated for basic voltage regulation from the transformer auxiliary winding as shown in figures 4 and 5.
The Flyback converter is designed for power factor correction with low AC line current total harmonic distortion (iTHD). The MOSFET used is an IPA80R650CE 800 V rated CoolMOS device with 650 mΩ on resistance, 45 nC gate charge and low parasitic capacitances in a TO-220 FullPAK. This device is able to withstand high voltage ringing at switch off with minimal added snubber components and has low conduction and switching losses as well low gate drive current.
The output diode has less than 50 ns reverse recovery and a forward voltage drop less than 900m V at maximum rated current of 10 A at 25 °C temperature, reducing to 700 mV at 150 °C. The blocking voltage is 300 V, necessary to withstand the output voltage under open circuit condition at high line input added to the transformer secondary reflected voltage.
The parameters of the MOSFET and output diode contribute to the overall high efficiency of the converter.
The Flyback transformer (more accurately described as a coupled inductor) consists of three windings; the primary for energy storage during the on time, the secondary for energy transfer to the output during the off time and the auxiliary, which supplies VCC and provides the required de-magnetization and voltage feedback signals. The IRS2982S (IC1) VCC supply is derived from the transformer auxiliary winding through DVCC1 initially charging CVB then CVCC1 and 2 through RVCC and DVCC2 with DZ to clamp the voltage to protect IC1. Voltage feedback is provided through a divider comprised of RFB1 and RFB2, which sets the output voltage. The auxiliary winding voltage is proportional to the output voltage so that:

$$VAUX = VREF \cdot \frac{RFB1+RFB2}{RFB2} = VOUT \cdot \frac{N_A}{N_S} \quad [V] \quad [1]$$

Switching cycle peak current limiting is set by parallel shunt resistors RCS1 to 4, which give a combined resistance of 450 mΩ, setting the peak current to 2.67 A according to the threshold VCSTH of 1.2 V. This limits the inrush current during start-up and also protects against damage under over load or short circuit conditions. The eval board is not designed to withstand a sustained output overload or short circuit.
The maximum peak current at low line and full load, assuming DMAX is 0.58 is calculated as:

$$I_{PMAX} = \frac{2\sqrt{2}\cdot POUT}{D_{MAX}.VAC_{MIN}\cdot\eta} = \frac{2\sqrt{2}\cdot 50}{0.58\cdot 100\cdot 0.9} = 2.71 \quad [A] \quad [2]$$

The transformer turns-ratio is calculated as follows:

$$N = \frac{N_P}{N_S} = \frac{\sqrt{2}\cdot VAC_{MIN}}{V_{OUT}+V_F} \cdot \frac{D_{MAX}}{1-D_{MAX}} = \frac{\sqrt{2}\cdot 100}{55+1} \cdot \frac{0.58}{1-0.58} = 3.49 \quad [3]$$

The primary to auxiliary winding turns-ratio is calculated to provide an auxiliary supply voltage of 20 V:

$$\frac{N_P}{N_A} = \frac{\sqrt{2}\cdot VAC_{MIN}}{V_{AUX}+V_{F(AUX)}} \cdot \frac{D_{MAX}}{1-D_{MAX}} = \frac{\sqrt{2}\cdot 100}{20+1} \cdot \frac{0.58}{1-0.58} = 9.3 \quad [4]$$

The transformer primary inductance is calculated according to the formula:

$$L_{PRI} = \frac{VAC_{MIN}^2\cdot\eta\cdot D_{MAX}^2}{2\cdot P_{OUT}\cdot f_{MIN}} \quad [H] \quad [5]$$

Dimensioning

$$\frac{100^2 \cdot 0.9 \cdot 0.58^2}{2 \cdot 50 \cdot 40000} = 757 \cdot 10^{-6}\ \text{H} = 757 \quad [\mu\text{H}]$$

Where, η is the efficiency assumed to be 0.9 and minimum frequency set to 40 kHz to occur at the peak of the line input voltage at 100 Vrms.

The resistor divider comprising RFB1 and RFB2 sets the output voltage according to:

$$V_{OUT} = \frac{N_P}{N_A} \cdot \frac{1}{N} \cdot V_{REF} \cdot \frac{RFB1+RFB2}{RFB2} \quad [\text{V}] \quad [6]$$

In this design, RFB2=20 k and RFB1=1 M. VREF is 400 mV specified in the IRS2982S datasheet therefore:

$$9.3 \cdot \frac{1}{3.49} \cdot 0.4 \cdot \frac{20k+1000k}{20k} = 54.4 \quad [\text{V}]$$

The threshold for over voltage protection through the ZX input is given by the resistor divider consisting of RZX1 and RZX2, where RZX1=47 k and RZX2=14 k and V_{OVTH} is 5.1 V:

$$V_{OUTOV} = \frac{N_P}{N_A} \cdot \frac{1}{N} \cdot V_{OVTH} \cdot \frac{RZX1+RZX2}{RZX2} \quad [\text{V}] \quad [7]$$

$$9.3 \cdot \frac{1}{3.49} \cdot 5.1 \cdot \frac{47k+14k}{14k} = 59.2 \quad [\text{V}]$$

The maximum reflected voltage appearing at the MOSFET drain is then calculated as follows based on the highest AC line input voltage of 265 Vac:

$$V_{DMAX} = \sqrt{2} \cdot V_{ACMAX} + \left(V_{OUT(MAX)} + V_F\right) \cdot N \quad [\text{V}] \quad [8]$$

$$\sqrt{2} \cdot 265 + (60+1) \cdot 3.49 = 588 \quad [\text{V}]$$

It is recommended to allow 30% headroom on top of the reflected voltage to accommodate the switch off transient and high voltage ringing. This requires a MOSFET with a minimum drain-source maximum rating of 765 V and therefore an 800 V part has been selected.
Four parallel 470 µF output capacitors (COUT1 to 4) have been used with a total capacitance of 1880 µF, combined ripple current rating of 8 A and impedance of 7 mΩ at 100 kHz. The maximum low frequency output ripple can be calculated as follows:

$$V_{RIPPLE} = \frac{I_{OUT}}{2 \cdot \pi \cdot f_{ac(\min)} \cdot C_{OUT}} \quad [\text{Vpp}] \quad [9]$$

$$\frac{1}{2 \cdot \pi \cdot 45 \cdot 1880 \cdot 10^{-6}} = 1.88 \quad [\text{Vpp}]$$

$$C_{OUT} = \frac{I_{OUT}}{2 \cdot \pi \cdot f_{ac(\min)} \cdot V_{RIPPLE}} \quad [\text{F}] \quad [10]$$

6 Control loop

The voltage mode Flyback converter operating in critical conduction mode has a basic error amplifier to output voltage (VCOMP) transfer characteristic with a single pole of the form:

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} \approx \frac{k \cdot f_s}{D} \cdot \frac{1}{1+\frac{s}{\omega_{po}}} \quad [11]$$

Where,

$$\omega_{po} = \frac{2}{R_{LOAD} \cdot C_{OUT}} \quad , \; R_{LOAD} = \frac{V_{OUT}}{I_{OUT}}$$

And 'k' is a constant of approximately 2.5 x 10^{-6} defined by the IRS2982S.

To prevent over-shoot of the output voltage at start up while maintaining good regulation, power factor and line current THD a type 2 compensation network is used at the COMP pin, which is the output of the IRS2982S internal OTA error amplifier. The loop gain needs to cross 0 dB below the minimum line frequency with sufficient margin to achieve good PF/iTHD performance.

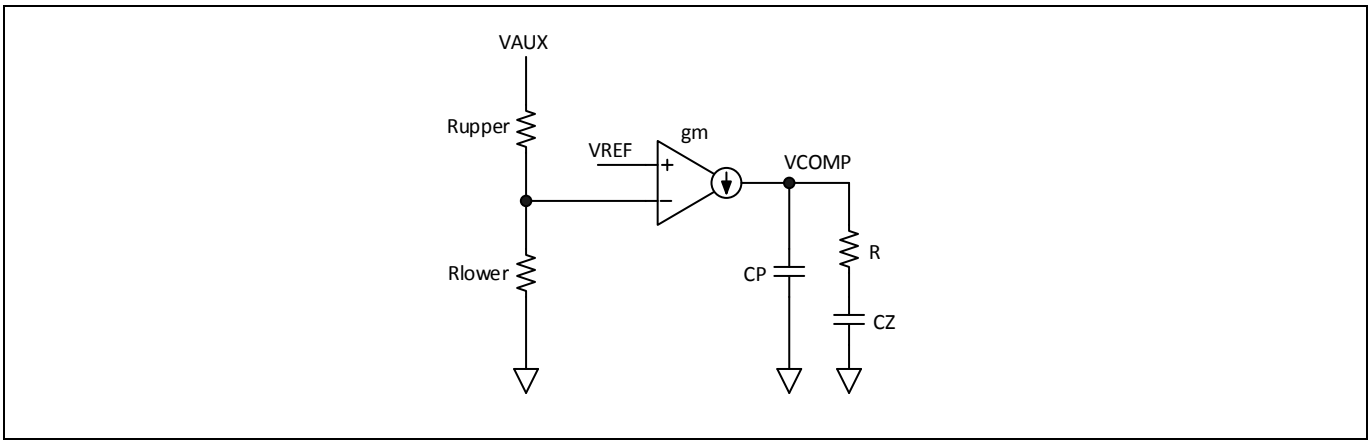


Figure 6 Type 2 OTA compensation

The transfer function has a zero at low frequency formed by R (RCMP) and CZ (CCMP2) and a pole at higher frequency formed by R and CP (CCMP1). The OTA gm is approximately 100 μΩ^{-1} as specified in the data sheet.

The error amplifier transfer function is as follows:

$$\frac{V_{COMP}(s)}{V_{IN}(s)} \approx \frac{R_{LOWER}.g_m.R}{R_{LOWER}+R_{UPPER}} \cdot \frac{1+\frac{1}{sRC_z}}{1+sRC_p} \quad [12]$$

The mid-band gain is given by:

$$G_o = \frac{R_{LOWER}.g_m R}{R_{LOWER}+R_{UPPER}} \quad [13]$$

Control loop

The zero is given by:

$$\omega_z = \frac{1}{R.C_z} \quad [14]$$

The pole is given by:

$$\omega_p = \frac{1}{R.C_p} \quad [15]$$

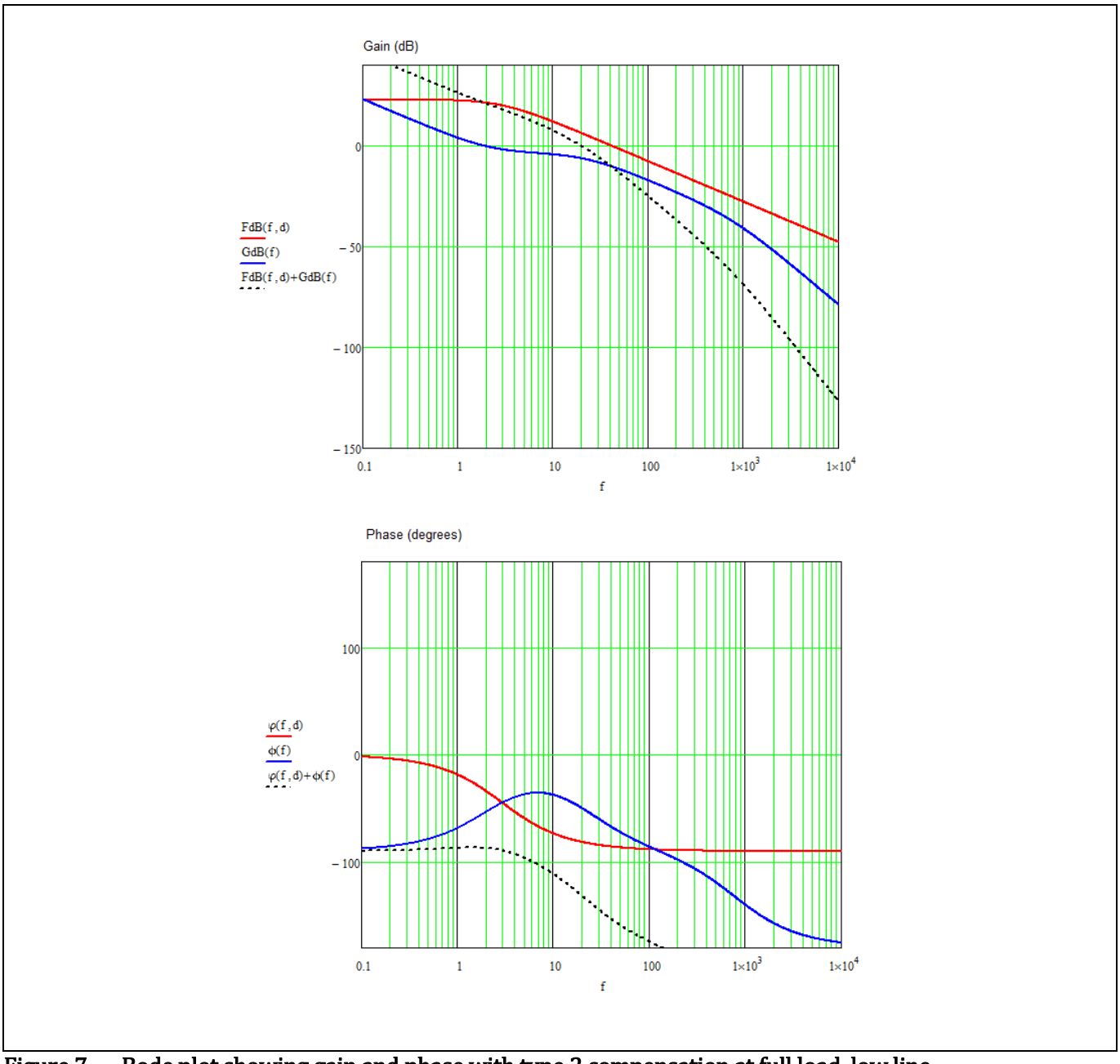


Figure 7 Bode plot showing gain and phase with type 2 compensation at full load, low line

The red lines show the converter plant transfer function from V_{COMP} to V_{OUT} and the blue lines show the feedback network and error amplifier transfer function. These are added together to give the loop transfer function T(s) shown by the dotted line.

It can be seen that at maximum load the gain crosses zero dB at approximately 20 Hz and the phase margin is 87 °, which provides a stable system. Bode plots at different line and load conditions indicate that the system will always be stable.

7 Bill of materials

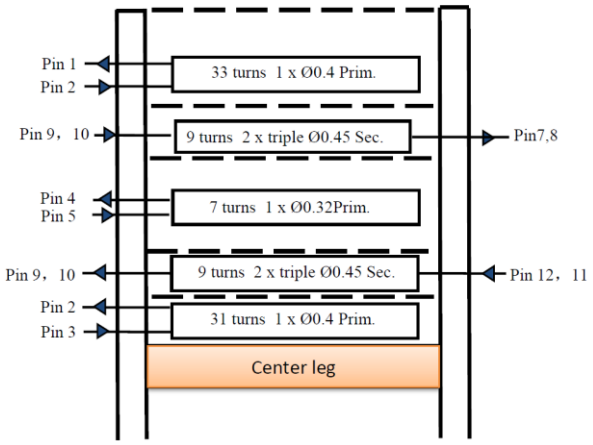
Quantity	Designator	Manufacturer	Part Number	Value/Rating
1	BR1	Vishay	GBU4J-E3/51	600 V/4 A
1	CCF	TDK	C2012X7R2E102K085AA	1 nF/250 V/0805/10%
1	CCMP1	TDK	CGA4C2C0G1H223J060AA	22 nF/250 V/0805/10%
1	CCMP2	TDK	C2012X7R1E224K125AB	0.22 µF/25 V/0805/10%
1	CDC	Epcos	B32922C3104M	0.1 µF/305 VAC/X2
1	CFB	TDK	C3216CH1H103K085AA	10 nF/50 V/1206/10%
1	COM1	Keystone	5001	0.04" dia black
1	COM2	Keystone	5001	0.04" dia black
1	COMP	Keystone	5004	0.04" dia yellow
1	COUT1	Panasonic	EEU-FR1J471B	470 µF/63 V/20%
1	COUT2	Panasonic	EEU-FR1J471B	470 µF/63 V/20%
1	COUT3	Panasonic	EEU-FR1J471B	470 µF/63 V/20%
1	COUT4	Panasonic	EEU-FR1J471B	470 µF/63 V/20%
1	CSNB	TDK	C4532X7R3A102M200KA	1 nF/1 kV/20%/1812/X7R
1	CVB	TDK	C3216X5R1H106K160AB	10 µF/50 V/1206/10%
1	CVCC1	TDK	C3216C0G1H104J160AA	0.1 µF/50 V/1206/5%
1	CVCC2	Panasonic	EEU-EB1H220S	10 µF/50 V/1206/10%
1	CX1	Epcos	B32922C3104M	0.1 µF/305 VAC/X2
1	CX2	Epcos	B32922C3224M	0.22 µF/305 VAC/X2
1	CY1	Vishay	VY2102M29Y5US63V7	1 nF/300 VAC/Y
1	CY2	Vishay	VY2102M29Y5UG63V7	1 nF/300 VAC/Y
1	CY3	Vishay	VY2102M29Y5US63V7	1 nF/300 VAC/Y
1	CZX	Kemet	C0805C220J5GACTU	22 pF/50 V/0805/5%
1	DOUT	Diodes Inc	SBR20A300CT	300 V/10 A/TO-220AB
1	DSNB	Diodes Inc	RS1MB-13-F	1000 V/1 A/SMB
1	DVCC1	Diodes Inc	LL4148-13	75 V/0.15 A/MINIMELF
1	DVCC2	Diodes Inc	LL4148-13	75 V/0.15 A/MINIMELF
1	DZ	Micro Commercial Co	BZV55C18-TP	18 V/0.5 W/MINIMELF
1	F1	Bussman	SS-5H-1.6A-APH	T1.6 A/300 VAC/4-8.5
1	IC1	Infineon	IRS2982S	SMPS Controller
1	IFB	Keystone	5003	0.04" dia orange
1	L1	Kemet	SS24H-R05600-CH	2x60 mH Common Mode
1	MFB	Infineon	IPA80R650CE	800 V/4.5 A/TO-220
1	P1	Phoenix Contact	1985205	3 Position 3.5mm Green
1	P2	Phoenix Contact	1985195	2 Position 3.5mm Green
1	PFC	Keystone	5002	0.04" dia white
1	RCF	Panasonic	ERJ-6GEYJ471V	470/0.125 W/0805/5%
1	RCMP	Panasonic	ERJ-6GEYJ334V	330 k/0.125 W/0805/5%
1	RCS1	Panasonic	ERJ-8GEYJ4R7V	4.7/0.25 W/1206/5%
1	RCS2	Panasonic	ERJ-8GEYJ1R5V	1.5/0.25 W/1206/5%
1	RCS3	Panasonic	ERJ-8GEYJ1R5V	1.5/0.25 W/1206/5%
1	RCS4	Panasonic	ERJ-8GEYJ1R5V	1.5/0.25 W/1206/5%
1	RFB1	Panasonic	ERJ-8GEYJ105V	1 M/0.25 W/1206/5%
1	RFB2	Panasonic	ERJ-8GEYJ203V	20 k/0.25 W/1206/5%
1	RG1	Panasonic	ERJ-8GEYJ4R7V	4.7/0.25 W/1206/5%
1	RG2	Panasonic	ERJ-8GEYJ103V	10 k/0.25 W/1206/5%
1	RHV	Yageo	CFR-50JB-52-10K	10 k/0.5 W/5%
1	ROUT	Panasonic	ERJ-8GEYJ153V	15 k/0.25 W/1206/5%
1	RSNB1	Panasonic	ERJ-8GEYJ474V	470 k/0.25 W/1206/5%

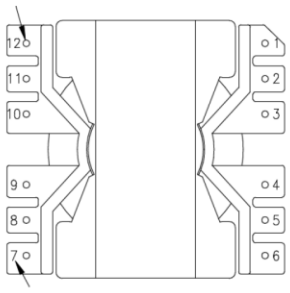
Bill of materials

1	RSNB2	Panasonic	ERJ-8GEYJ474V	470 k/0.25 W/1206/5%
1	RSNB3	Panasonic	ERJ-8GEYJ474V	470 k/0.25 W/1206/5%
1	RVCC1	Panasonic	ERJ-8GEYJ100V	10/0.25 W/1206/5%
1	RVCC2	Panasonic	ERJ-8GEYJ511V	510/0.25 W/1206/5%
1	RZX1	Panasonic	ERJ-8GEYJ473V	47 k/0.25 W/1206/5%
1	RZX2	Panasonic	ERJ-6ENF1402V	14 k/0.125 W/0805/1%
1	T1	Wurth Finepower	750316066 Rev 00 TPT-PQ2627-001A	Flyback Transformer 800 µH 64:18:7
1	VCC	Keystone	5000	0.04" dia red
1	VCS	Keystone	5003	0.04" dia orange
1	VDC(HV)	Keystone	5000	0.04" dia red
1	VOUT+	Keystone	5000	0.04" dia red
1	VOUT-	Keystone	5001	0.04" dia black
1	VR1	Epcos	S10K320E2K1	510 V/3.5 kA/10 mm
1	ZX	Keystone	5004	0.04" dia yellow
4	Z1	Keystone	1902F	Standoff, Hex 0.65"L 4-40THR Nylon
4	Z2	B & F Fastner	NY PMS 440 0025 PH	Screw, Philips 4-40 x 1/4 Nylon
1	Z3	Heatsink (for MFB)	577102B04000G	HEATSINK TO-220 W/TAB .375"
1	Z4	Screw	9900	MACHINE SCREW PAN PHILLIPS 4-40
1	Z5	Nut	4694	HEX NUT 3/16" STEEL 4-40
1	Z6	Washer	4693	WASHER SPLIT LOCK #4 STEEL
1	Z7	Heatsink (for DOUT)	Aavid Thermalloy	591202B00000G

8 Transformer specification

Core type and material: Wurth 150-2239 PQ2625, PC44
Bobbin : THT, Vertical, Wurth p/n: 070-5649
Primary inductance and leakage inductance:
Lp = 795µH (±5%), measured between pin1 and pin3, leakage inductance ≤ 10µH





Start	End	No. of Turns	Wire Size	Layers
3	2	31	1 x φ0.4mm	½ Primary
11,12	9,10	9	2 x triple φ0.45mm	½ Secondary
5	4	7	1 x φ0.32mm	Flyback Auxiliary
9,10	7,8	9	2 x triple φ0.45mm	½ Secondary
2	1	33	1 x φ0.4mm	½ Primary

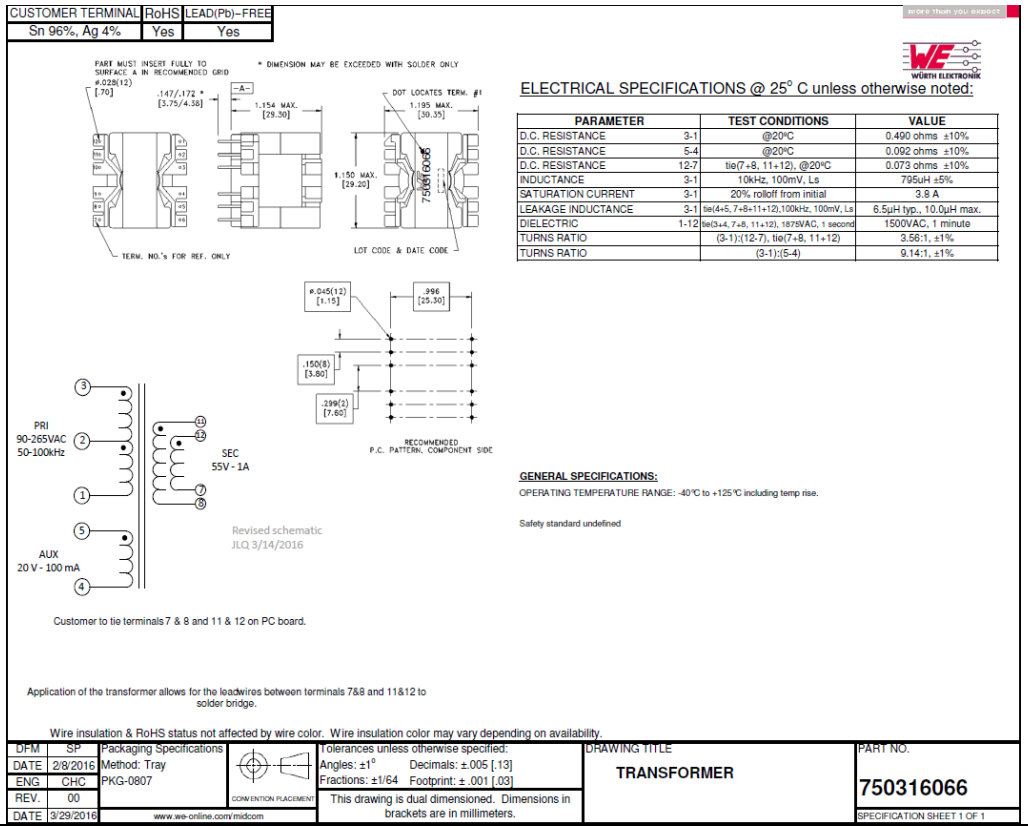


Figure 8 Flyback transformer specification

9 PCB Layout

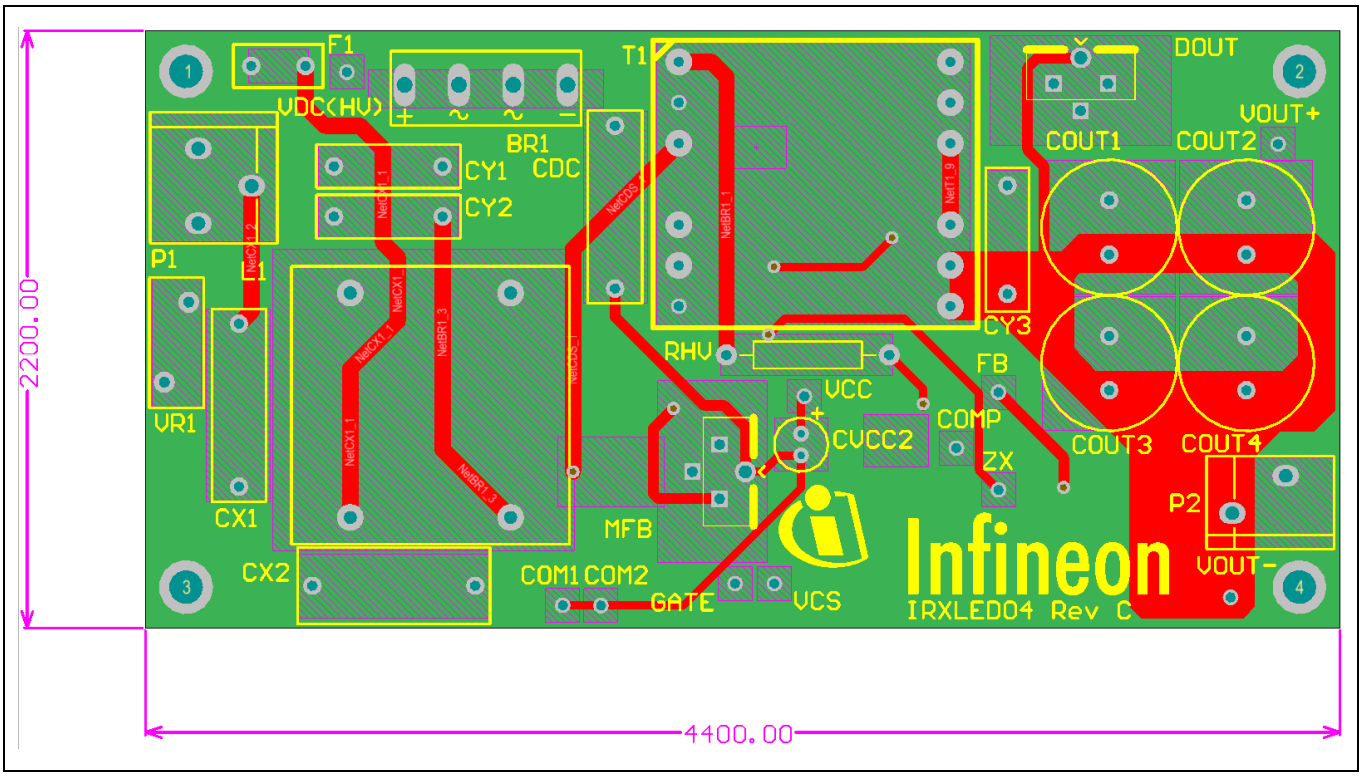


Figure 9 PCB top side components and traces

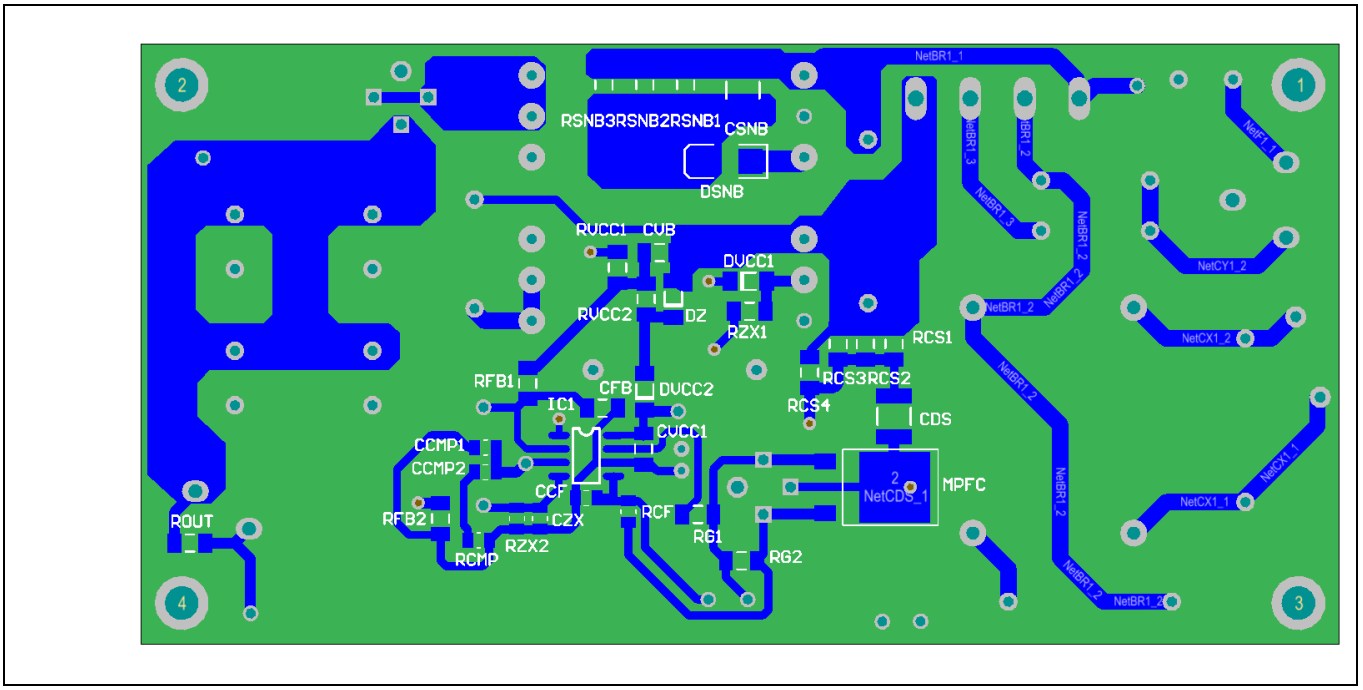


Figure 10 PCB bottom side components and traces

9.1 PCB layout guidelines for system optimization

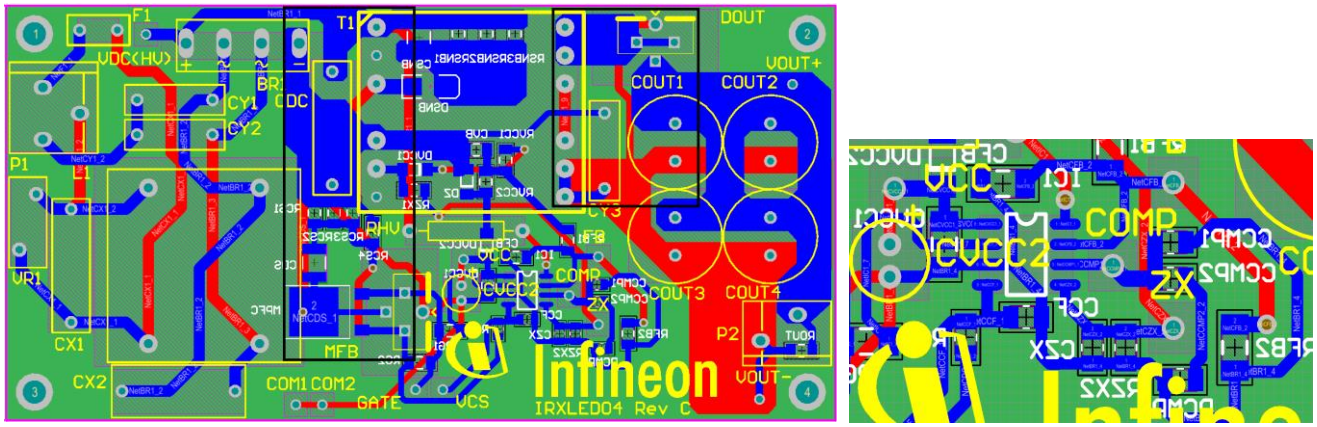


Figure 3 PCB layout

The left side of the above figure shows the primary and secondary high frequency current loops surrounded by a black outline in each case. The primary loop on the left side of the board originates from CDC connecting first to the transformer (T1) primary (pin 1). The other side of the primary winding (pin 3) is connected to the drain of the MOSFET (MFB). To minimize EMI this trace should be kept as short as possible, however in this board due to the shape and the alternative DPAK footprint that has also been included, MFB could not be located directly next to T1. A ground plane has been placed on the other side of the PCB to absorb some of the EMI. The current sense resistors (RC1-4) are located such that the connection to the high frequency 0V bus return of CDC is extremely short with the other end connected to the source of MFC through another short trace. A pad connected to CDC 0V is provided so that a grounded heatsink may be used, provided the MOSFET is in an insulated TO-220 FullPAK. This also absorbs some of the EMI originating from the drain.

The secondary high frequency current loop originates from T1 pins 11 and 12 connecting through a short trace to DOUT, which then connects through another very short trace to COUT1. The negative side of COUT1 returns directly back to T1 pins 7 and 8 again through another short trace providing the tightest possible HF current loop. Parallel output capacitors COUT2-4 are connected to COUT1 through very heavy Copper traces to provide minimum impedance and best possible HF ripple current sharing between the capacitors. A grounding pad is also provided for the DOUT heat sink. The diode must also be in a TO-220 FullPAK to use a grounded heatsink.

The primary-secondary 0V Y capacitor (CY3) is connected directly to each 0V HF point with the shorted possible traces.

The layout techniques described minimize EMI emitted by the converter as much as possible.

Aside from EMI considerations, it is essential to design the PCB so that the IRS2982 is able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. The picture on the right of the above figure shows the area around IC1. Pin 6 is the 0V (ground) connection, which is returned to the 0V side of CDC through a direct connection. It is also essential that decoupling capacitor CVCC1 be located directly next to IC1 with direct connections to the VCC and COM/0V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star point, which is at the negative side of the high frequency capacitor (CDC).

Components associated with IC1 such as CCF, CZX CMP1 and RCMP are connected to the signal ground with the shortest traces possible back to pin 6.

Additionally, clearance distances between high voltage traces and other parts of the circuit are kept as large as possible to comply with safety requirements. For this reason the middle leads of MFB and DOUT are bent forward to connect to a pad located further from the other two pads.

10 Test results

10.1 Operation at maximum load

The following measurements were made with IPA80R650CE MOSFET fitted as MFB.

Parameter	Unit	Results			
VAC	Vrms	100	120	230	265
Vdrain(ref)	V	326	349	510	550
VCSpk	V	1.19	1.06	0.73	0.69
ICSpk	A	2.63	2.35	1.62	1.53
Ton	µs	16.00	12.03	4.39	3.68
Toff	µs	12.16	10.87	8.22	7.76
D		0.57	0.53	0.35	0.32
Fs	kHz	35.51	43.67	79.30	87.41
ZXmax	V	4.7	4.7	4.7	4.7

Table 1 Test result summary

10.2 Test measurements under different line and load conditions

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vpp]
100%	51.98	51.98	1.00	57.79	89.95%	0.993	5.60%	1.50
50%	26.39	52.77	0.50	28.94	91.17%	0.994	6.10%	0.75
20%	10.80	54.02	0.20	12.10	89.29%	0.981	8.70%	0.30
0.50%	2.80	56.09	0.05	3.67	76.42%	0.855	n/a	0.08
0	0.00	59.30	0.00	0.68	0.00%	n/a	n/a	0.02

Table 2 Input 100 VAC

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vpp]
100%	52.02	52.02	1.00	57.01	91.25%	0.994	5.60%	1.50
50%	26.43	52.85	0.50	28.81	91.72%	0.992	6.10%	0.75
20%	10.82	54.12	0.20	12.14	89.16%	0.971	8.50%	0.30
0.50%	2.82	56.38	0.05	3.81	73.99%	0.802	n/a	0.08
0	0.00	59.20	0.00	0.63	0.00%	n/a	n/a	0.02

Table 3 Input 120 VAC

Test results

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vpp]
100%	52.19	52.19	1.00	56.09	93.05%	0.983	9.10%	1.50
50%	26.51	53.01	0.50	28.89	91.74%	0.954	8.80%	0.75
20%	10.83	54.17	0.20	12.51	86.60%	0.825	15.40%	0.30
0.50%	2.79	55.83	0.05	3.76	74.24%	0.360	50.00%	0.08
0	0.00	56.00	0.00	0.33	0.00%	n/a	n/a	0.02

Table 4 Input 230 VAC

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vpp]
100%	52.22	52.22	1.00	56.12	93.05%	0.975	9.90%	1.50
50%	26.52	53.04	0.50	29.00	91.45%	0.929	9.90%	0.75
20%	10.82	54.09	0.20	12.69	85.25%	0.755	16.70%	0.30
0.50%	2.78	55.53	0.05	3.61	76.91%	0.267	50.00%	0.08
0	0.00	55.70	0.00	0.31	0.00%	n/a	n/a	0.02

Table 5 Input 265 VAC

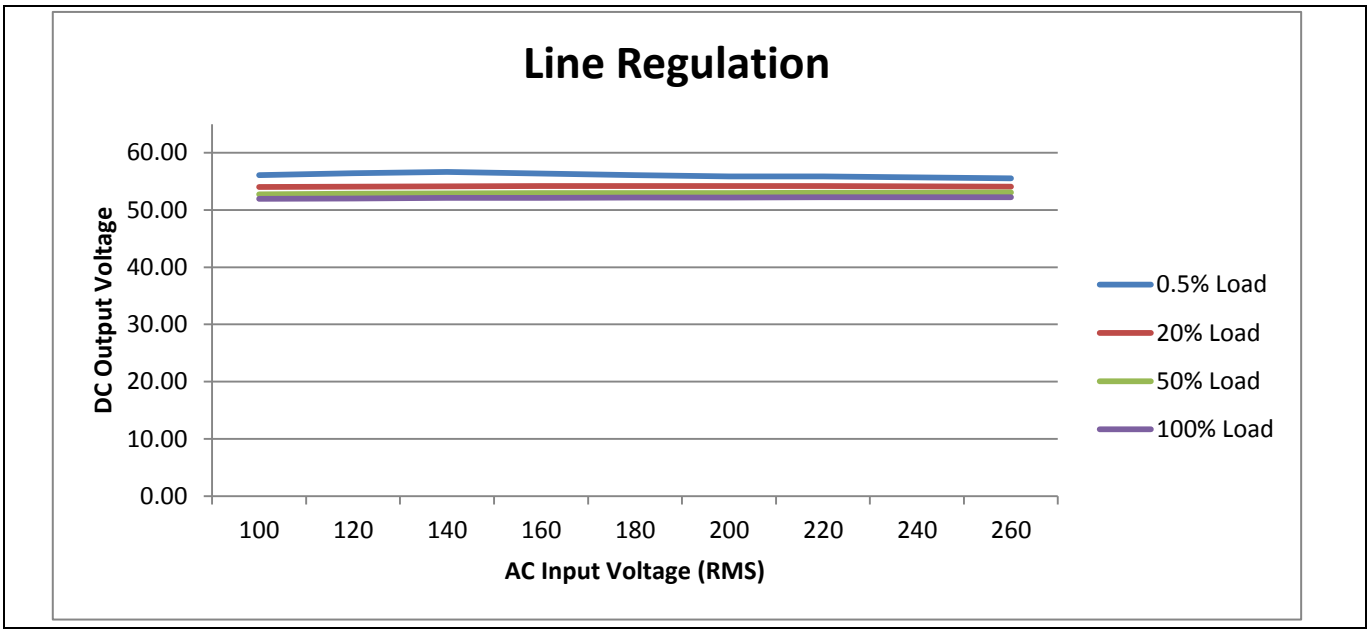


Figure 4 Line regulation at different loads

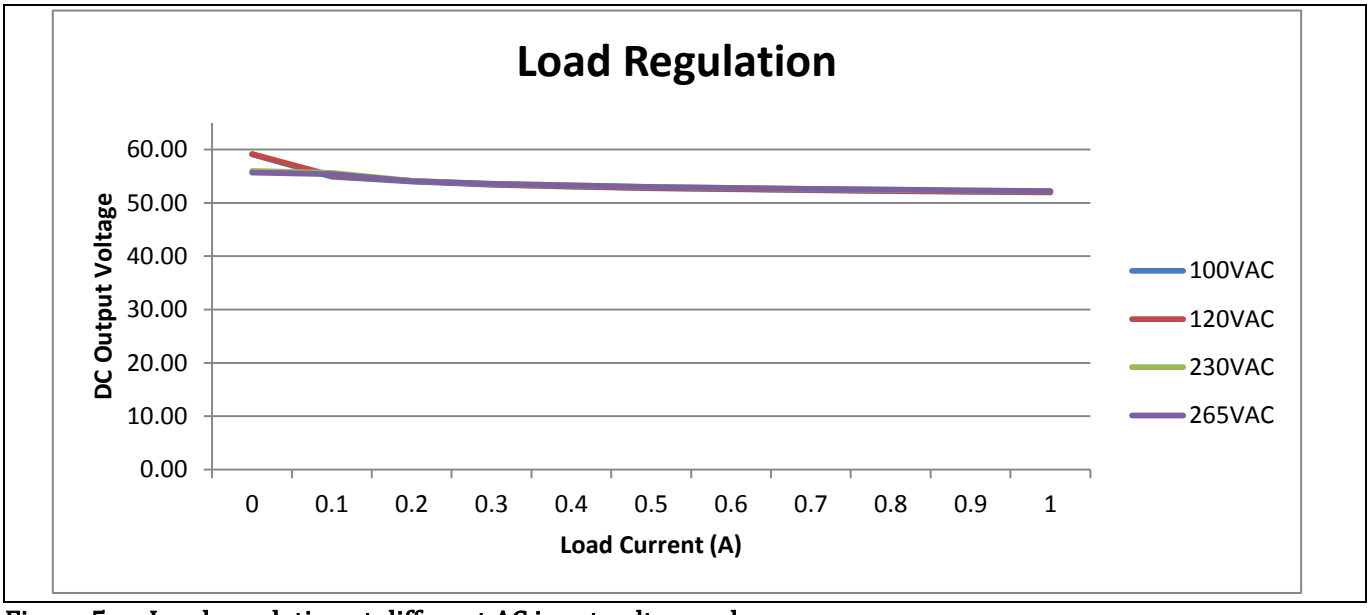


Figure 5 Load regulation at different AC input voltage values

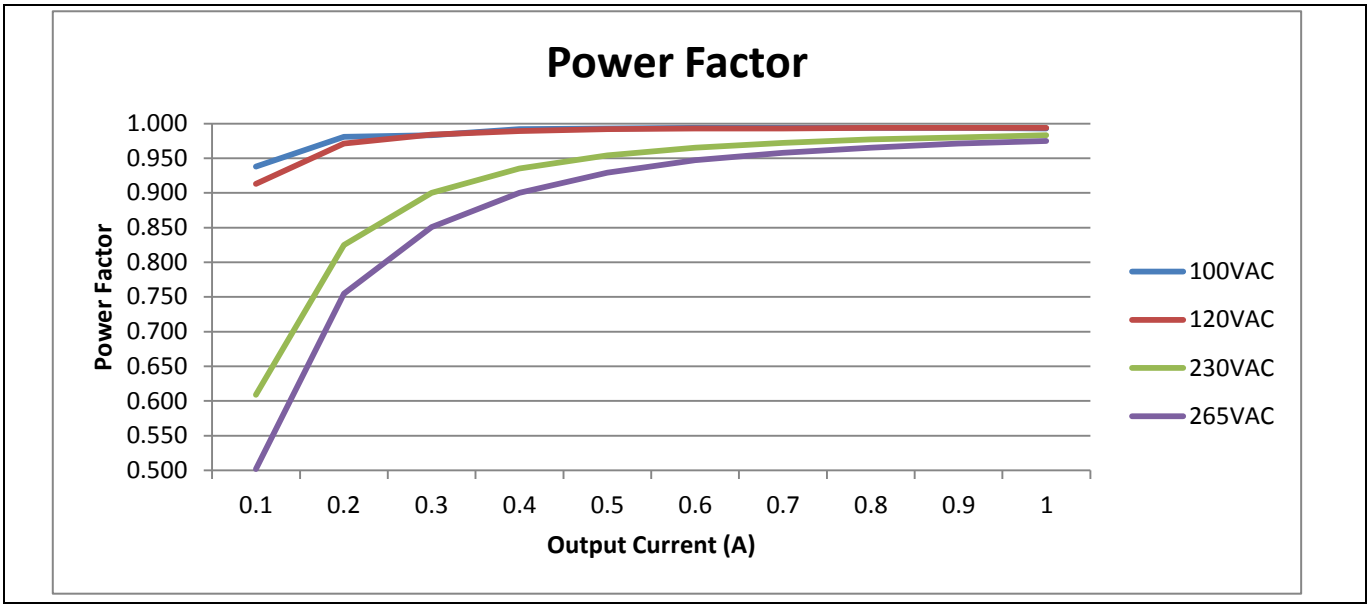


Figure 6 Power factor vs load

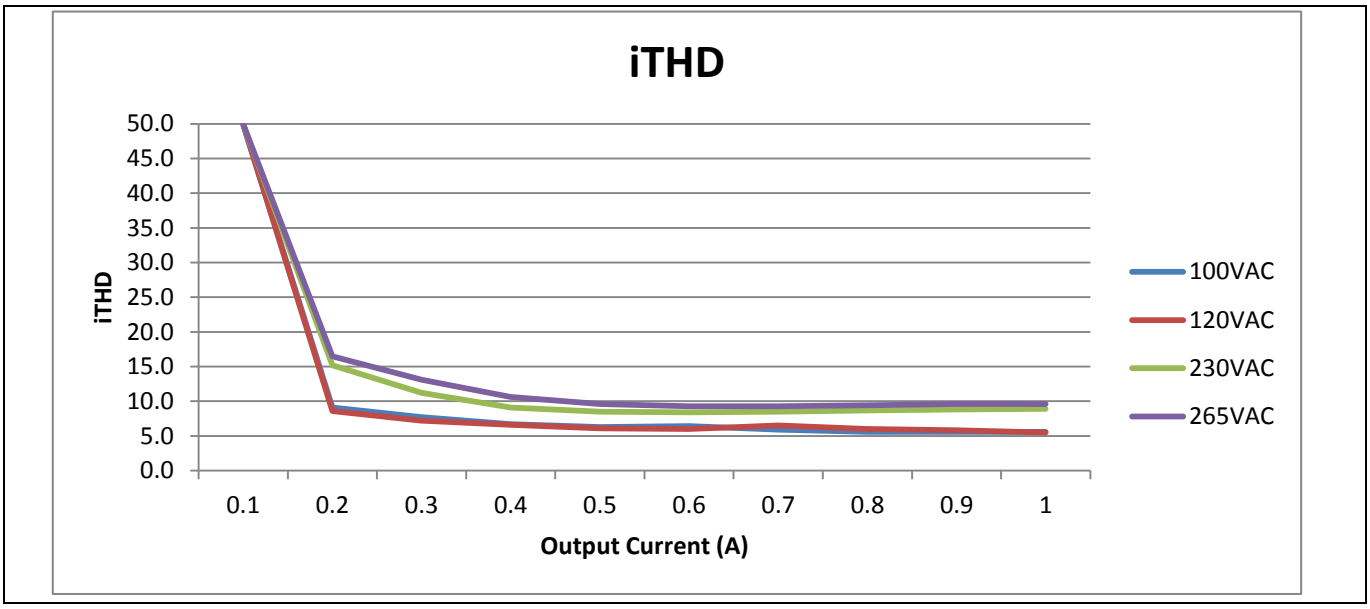


Figure 7 THDi vs load

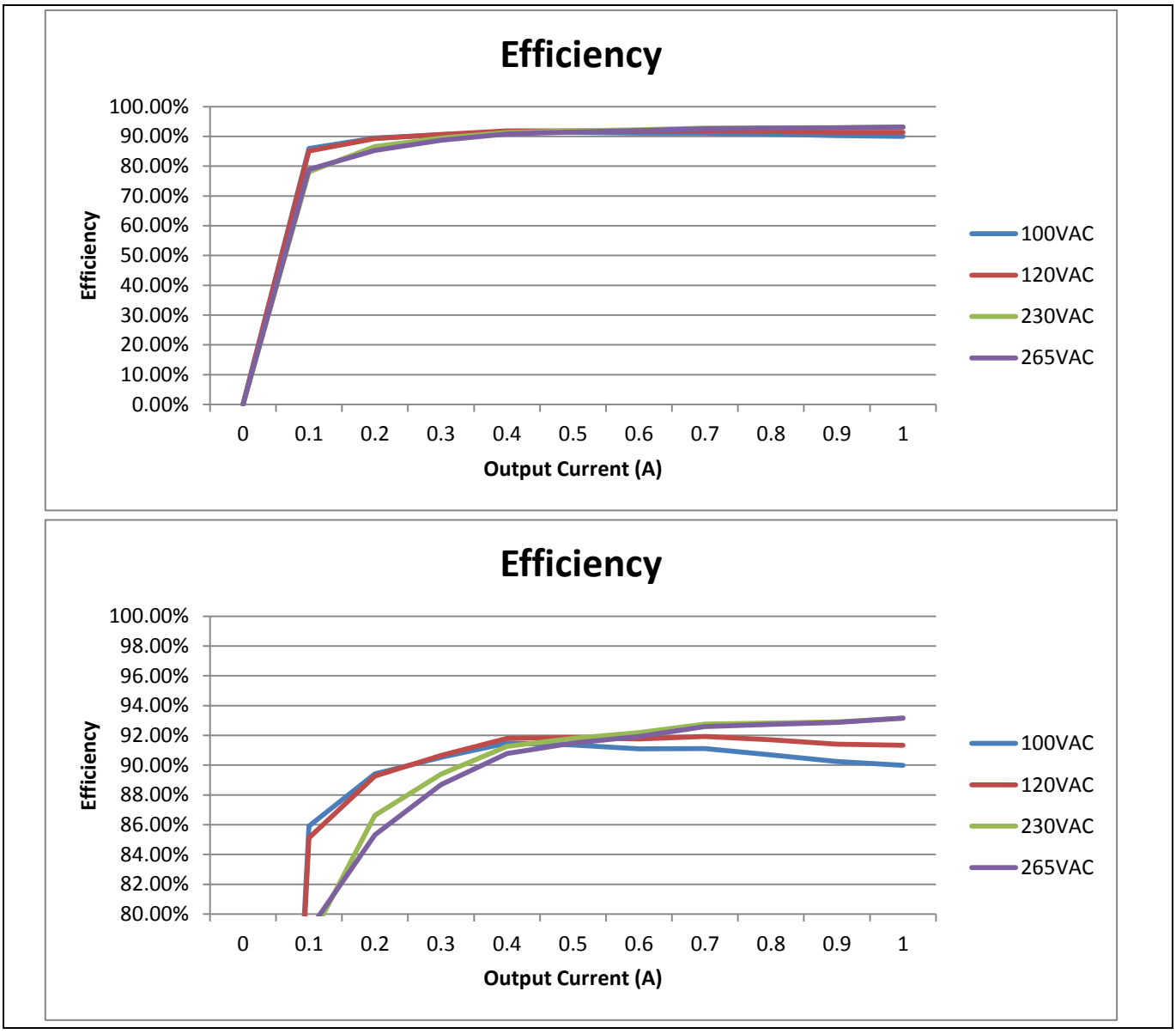


Figure 8 Efficiency vs load

10.3 Start and steady state operation at maximum load

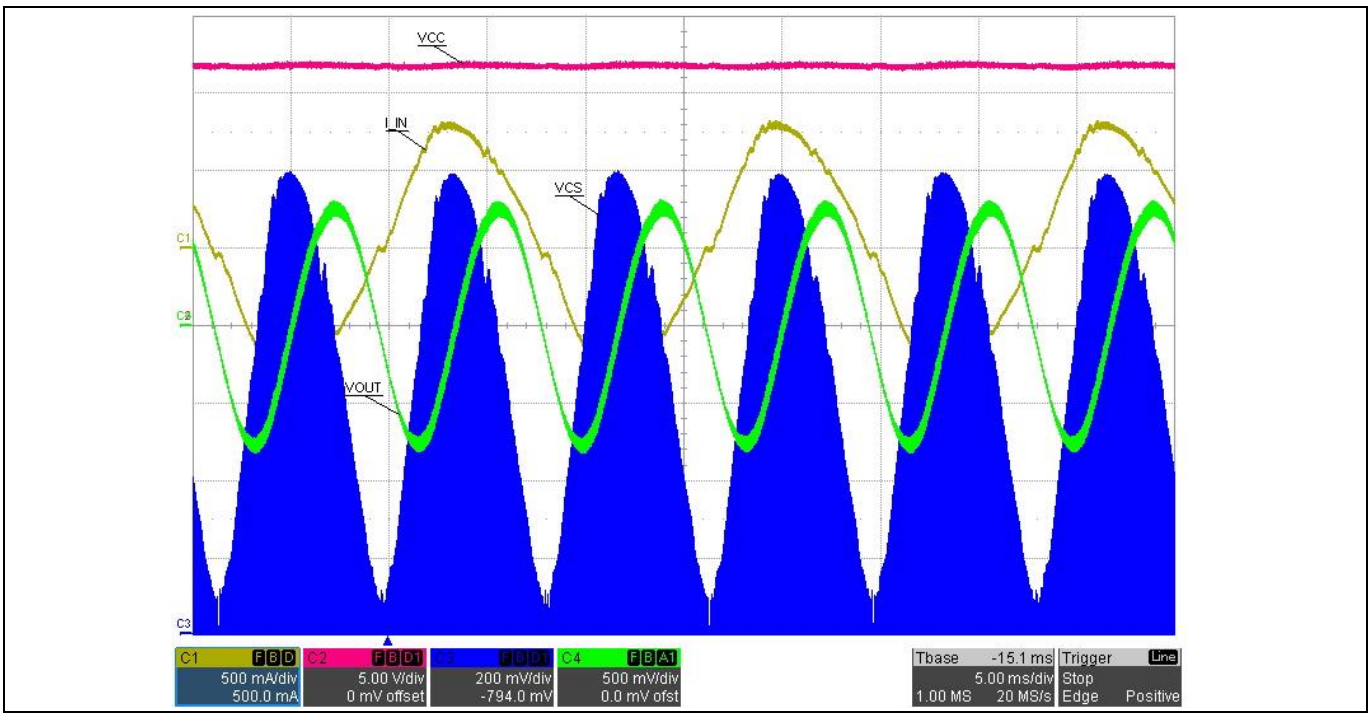


Figure 9 100 VAC steady state operation at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT ripple (green)

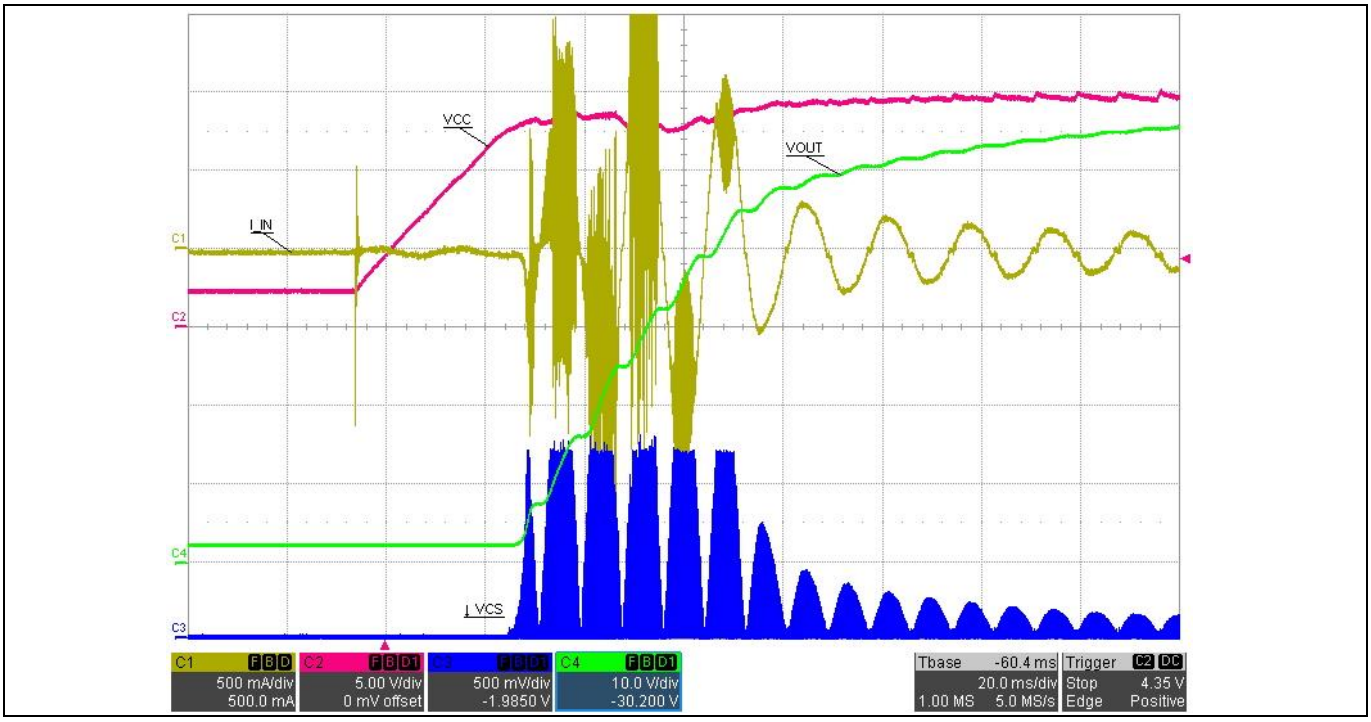


Figure 10 100 VAC start-up at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT (green)

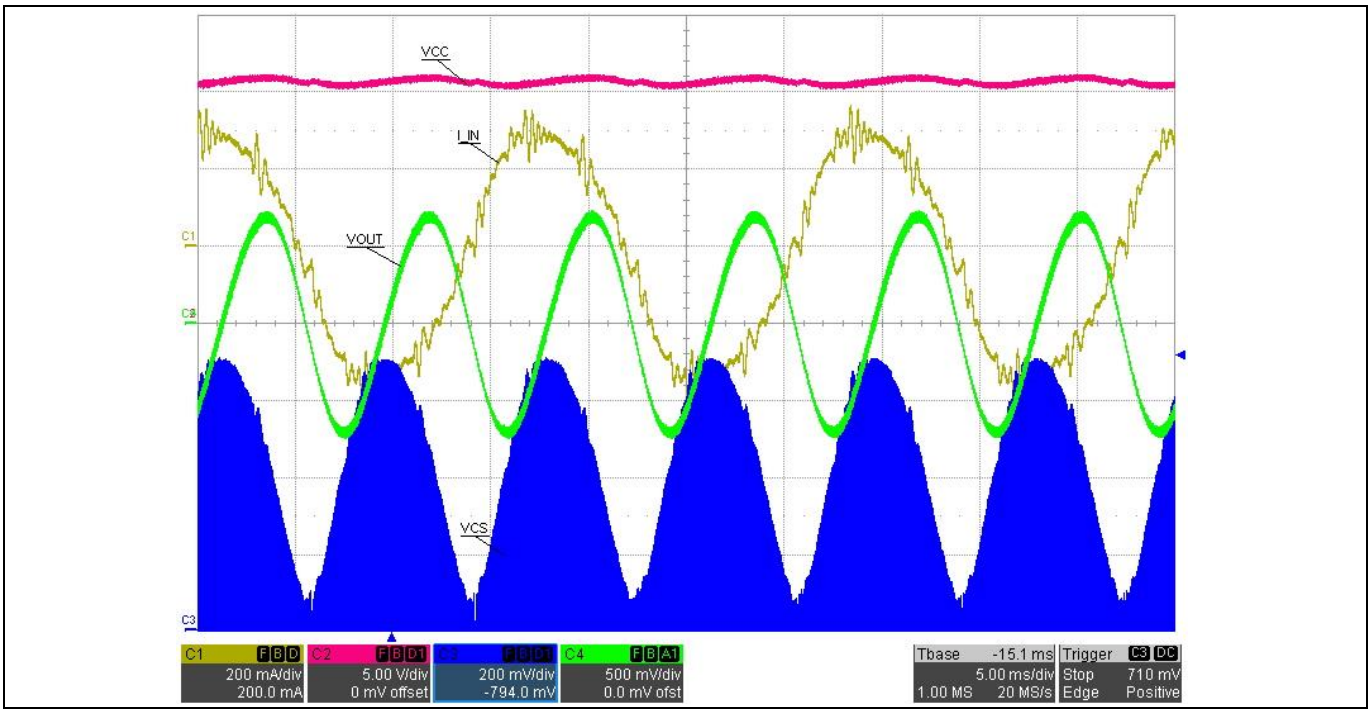


Figure 11 230 VAC steady state operation at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT ripple (green)

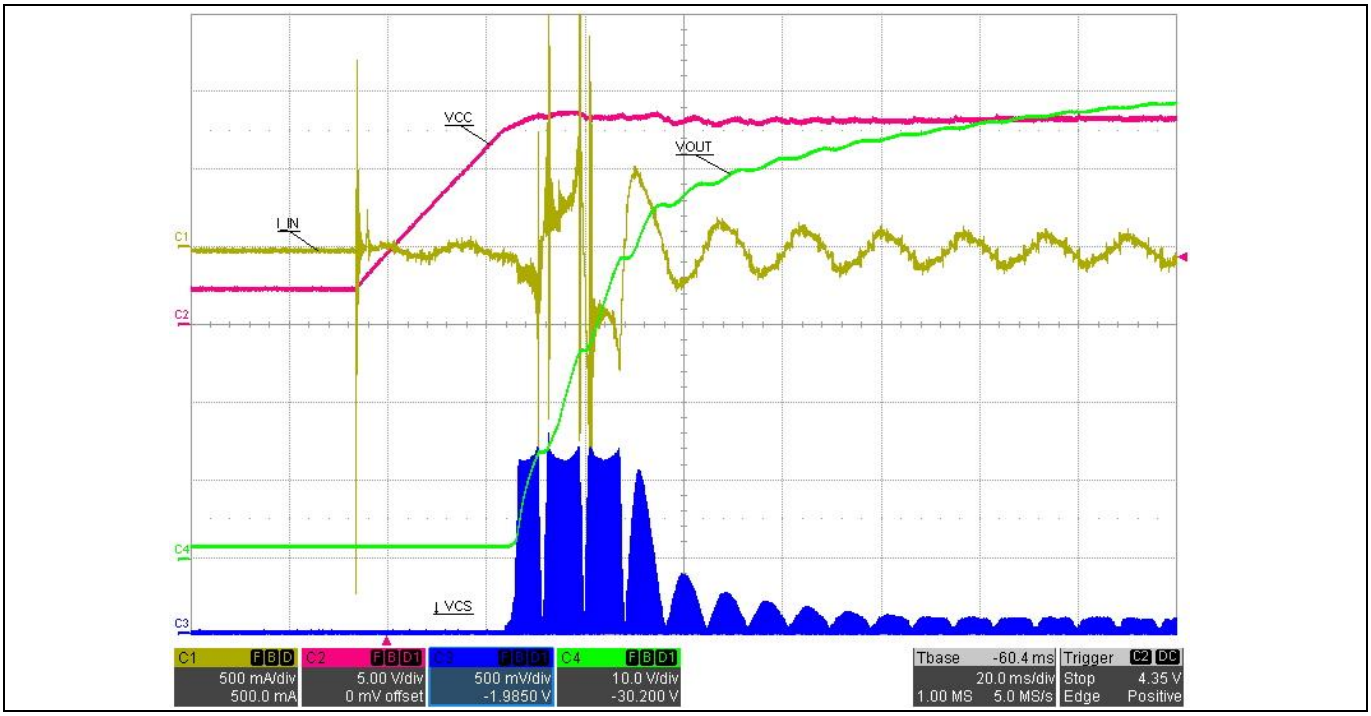


Figure 20 230 VAC start-up at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT (green)

At both 120VAC and 230VAC with full load the output voltage rises within the specified time with minimal or no over-shoot. Cycle by cycle current limit operates for the first few AC line half-cycles limiting inrush current.

10.4 Start-up under different line and load conditions

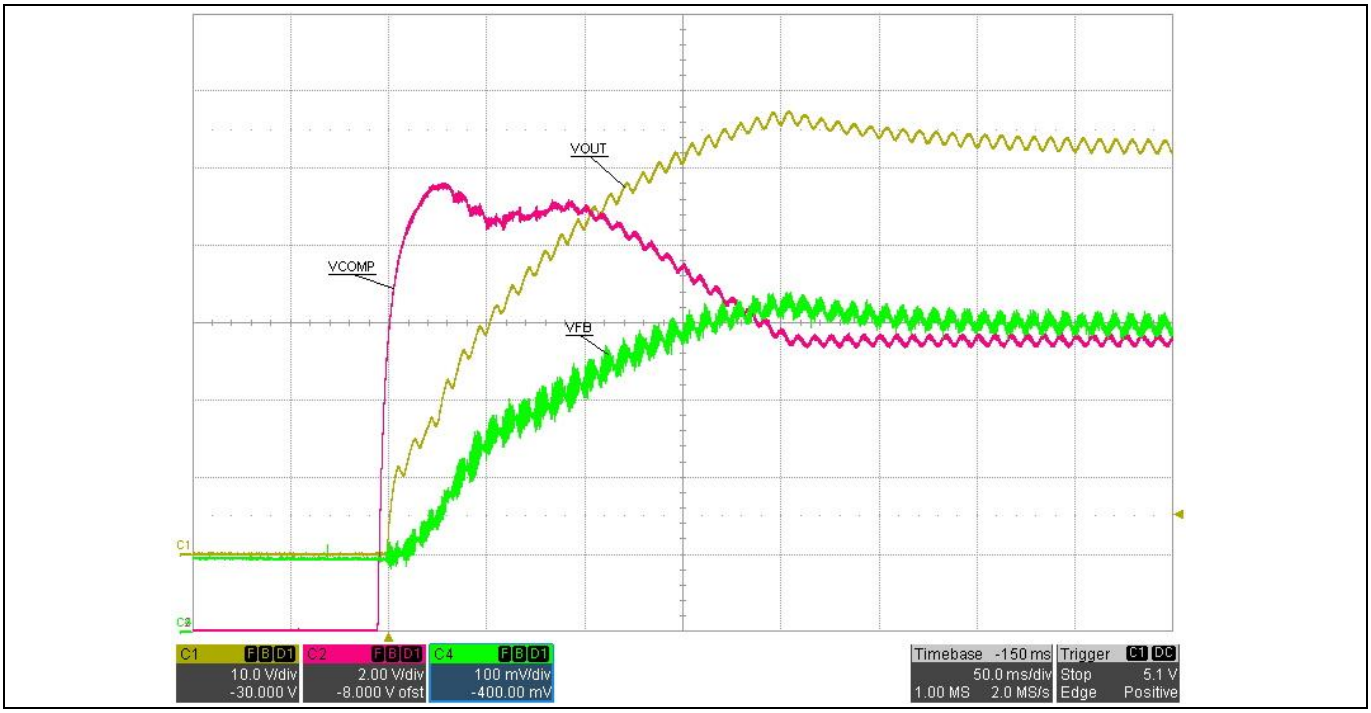


Figure 12 100 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)

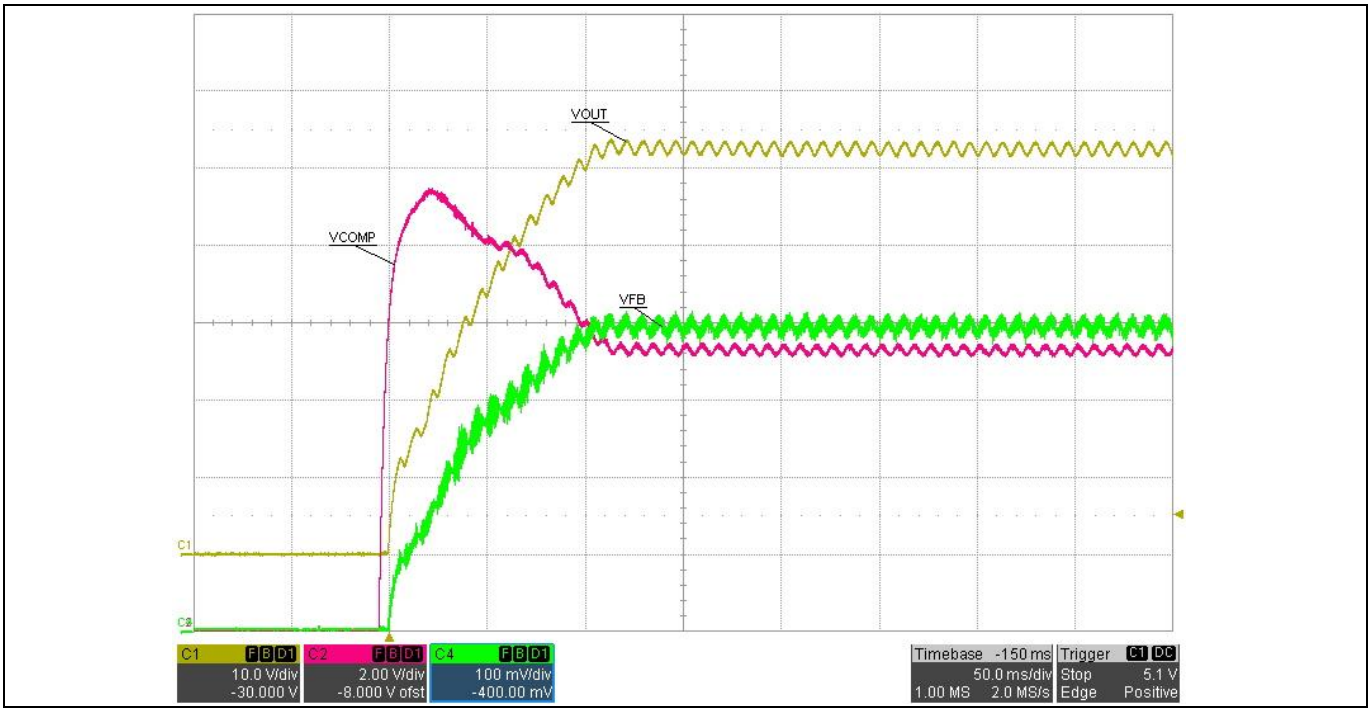


Figure 13 120 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)

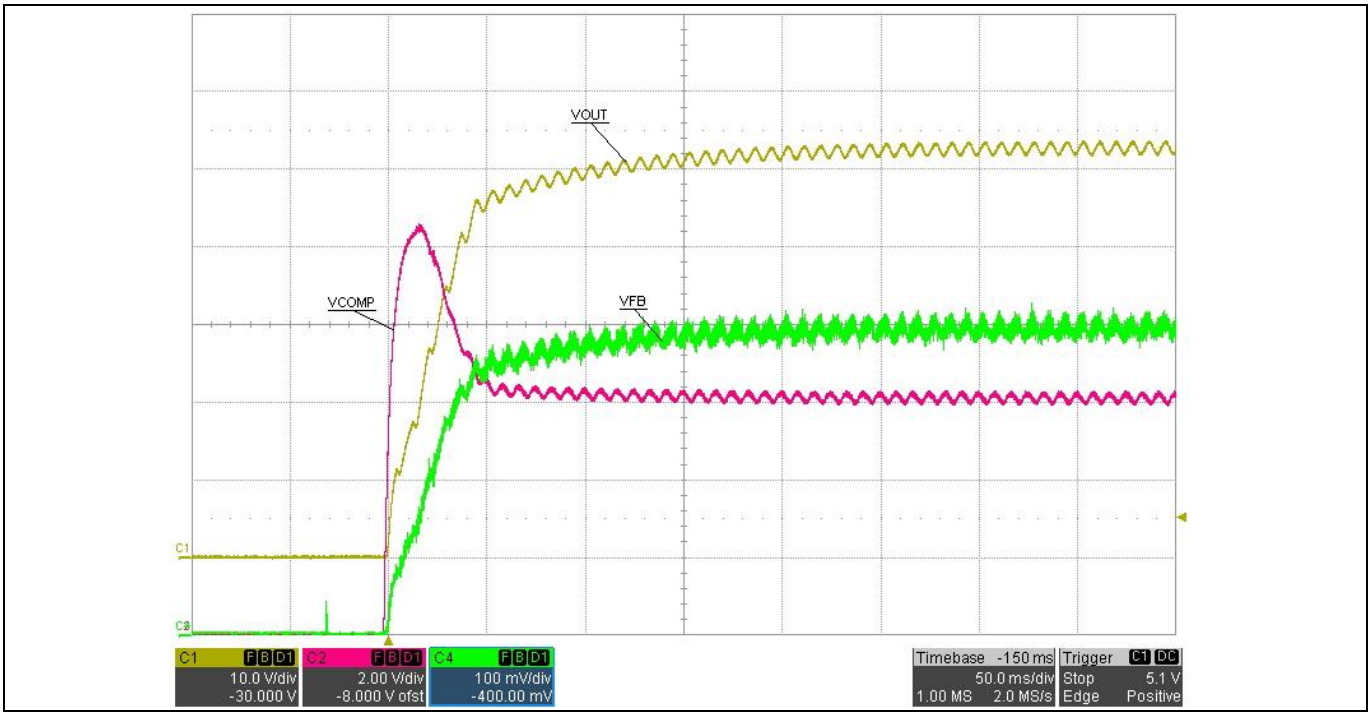


Figure 14 230 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)

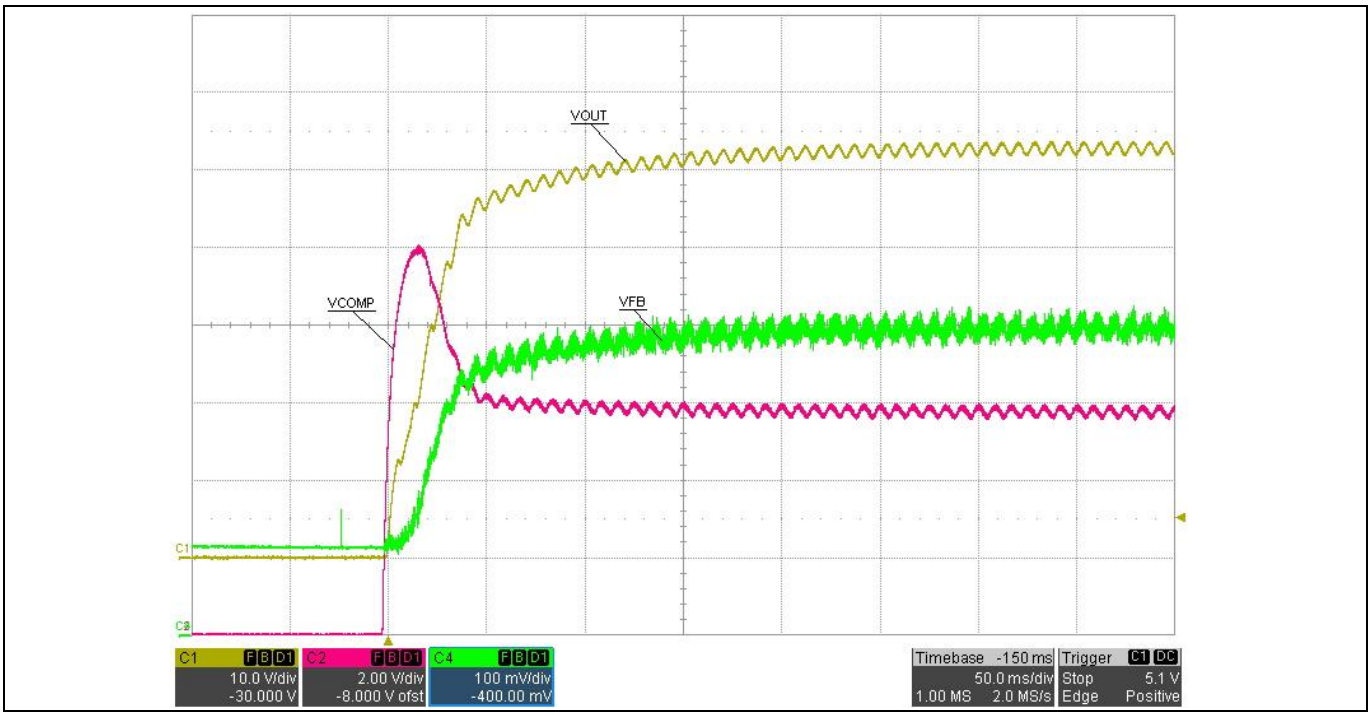


Figure 15 265 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)

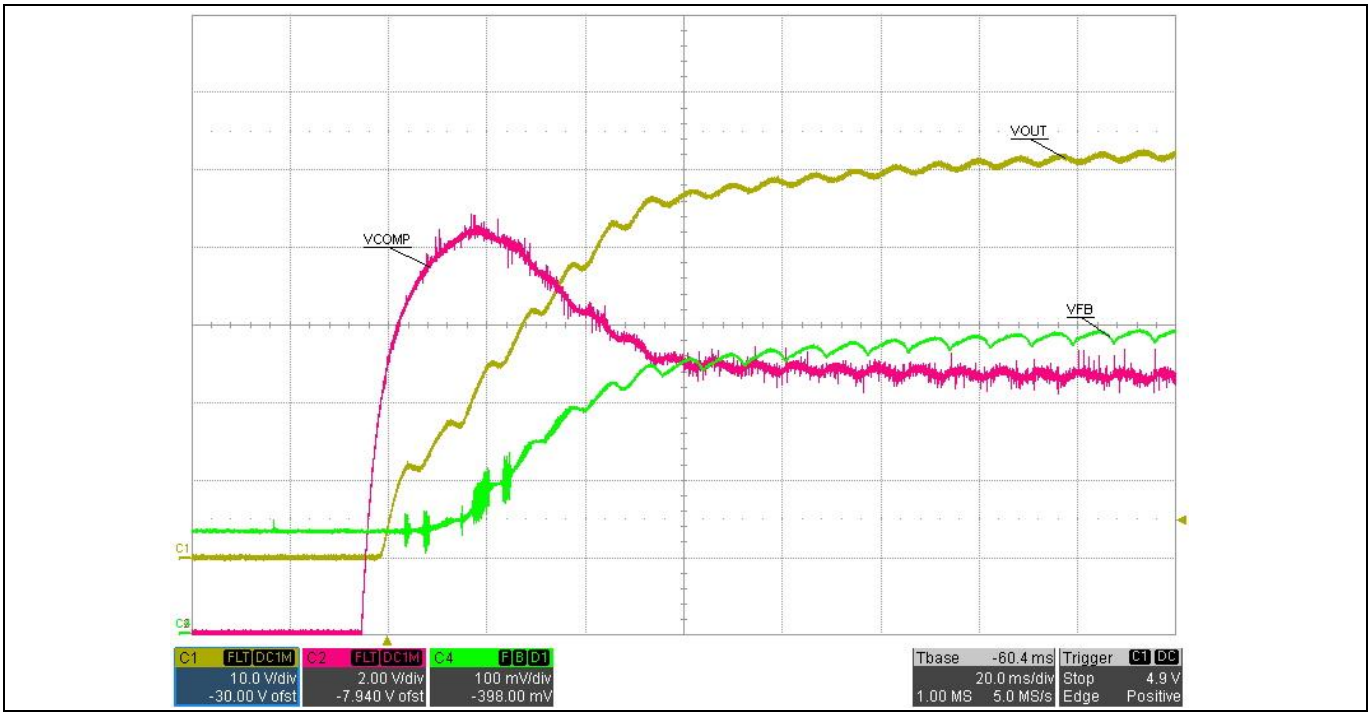


Figure 16 120 VAC start-up at 50% load
Output voltage (yellow), VCOMP (red), VFB (green)

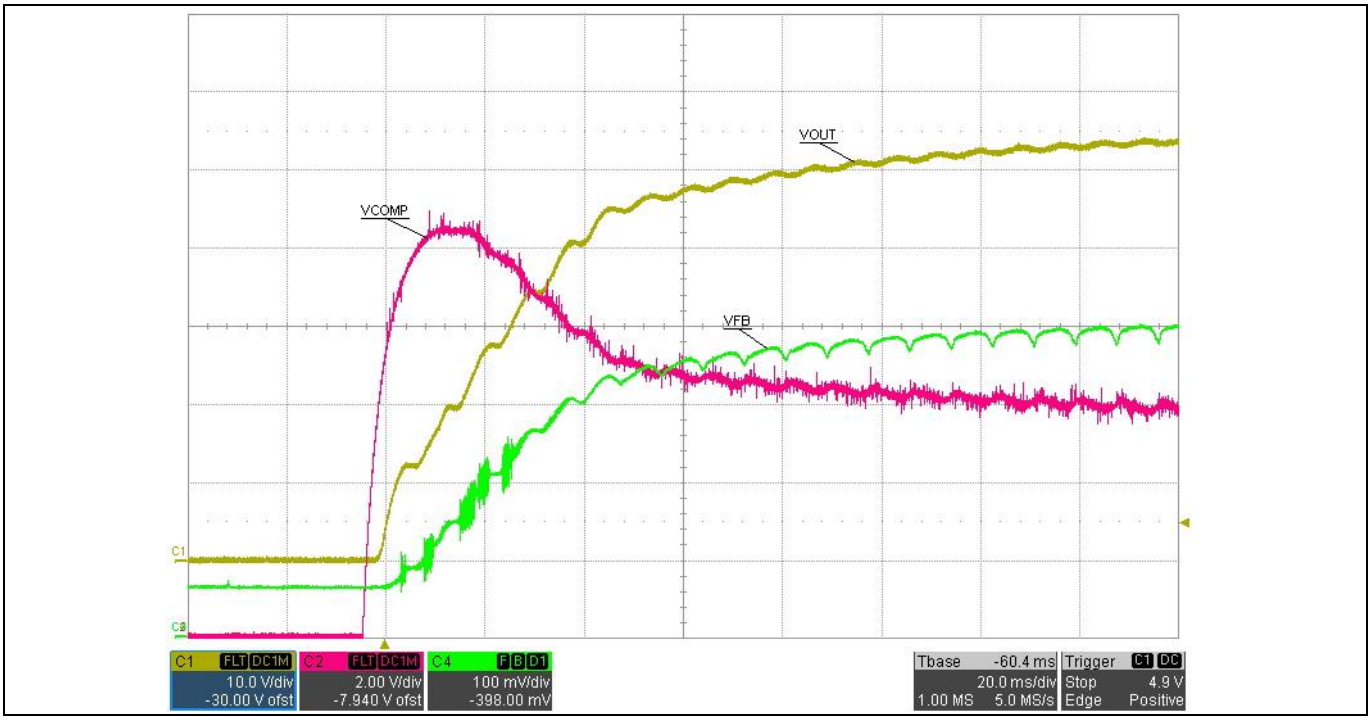


Figure 17 120 VAC start-up at 20% load
Output voltage (yellow), VCOMP (red), VFB (green)

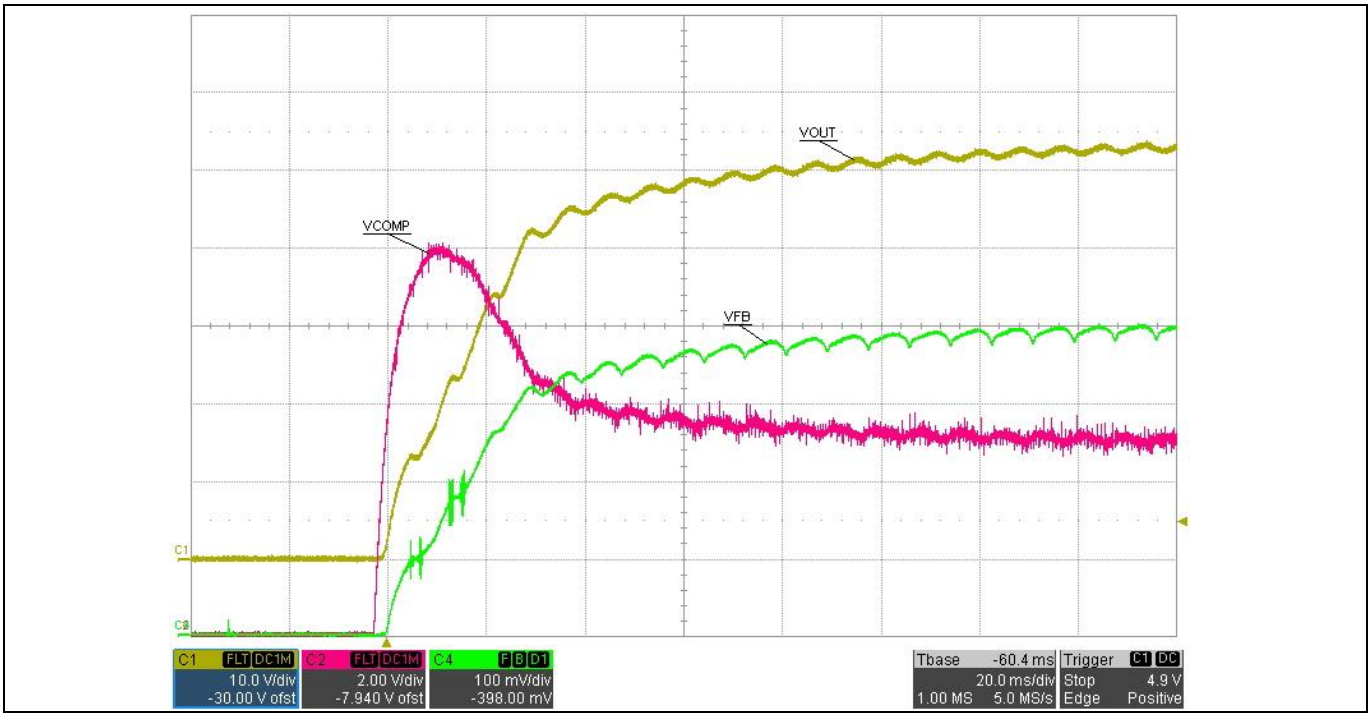


Figure 18 230 VAC start-up at 50% load
Output voltage (yellow), VCOMP (red), VFB (green)

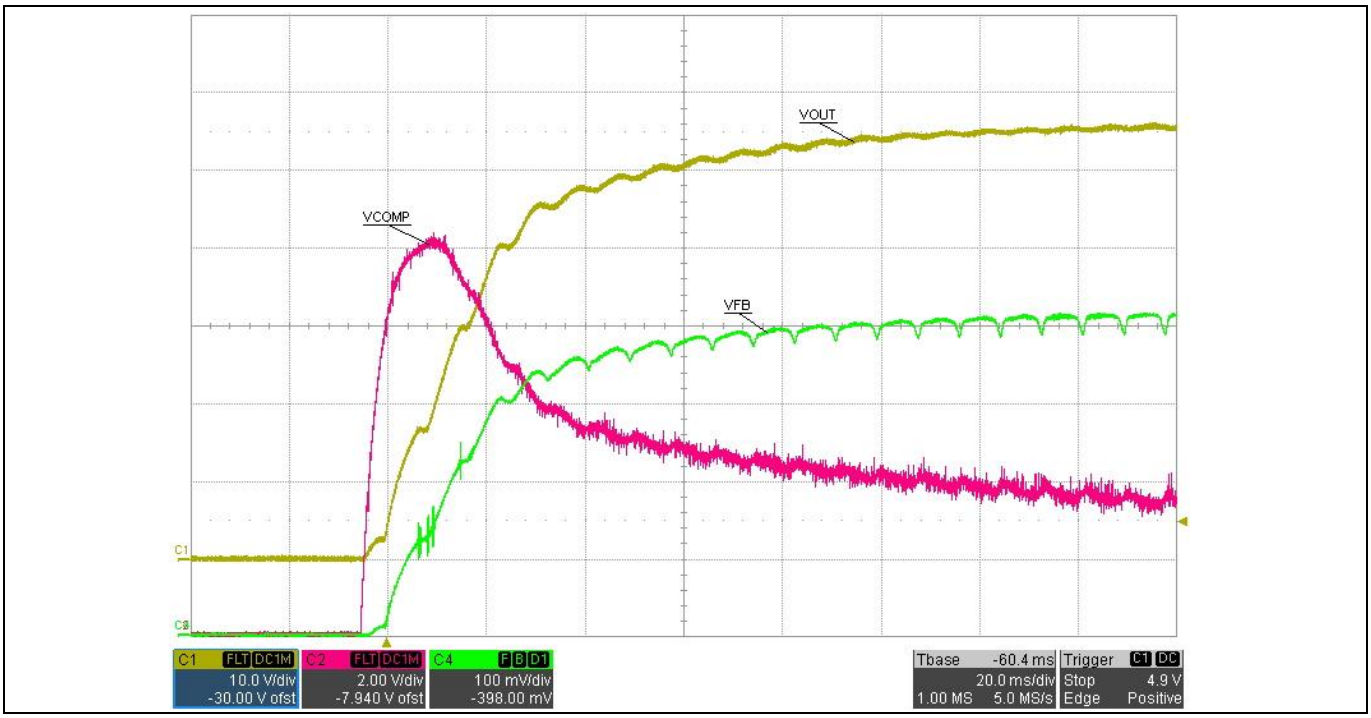


Figure 19 230 VAC start-up at 20% load
Output voltage (yellow), VCOMP (red), VFB (green)

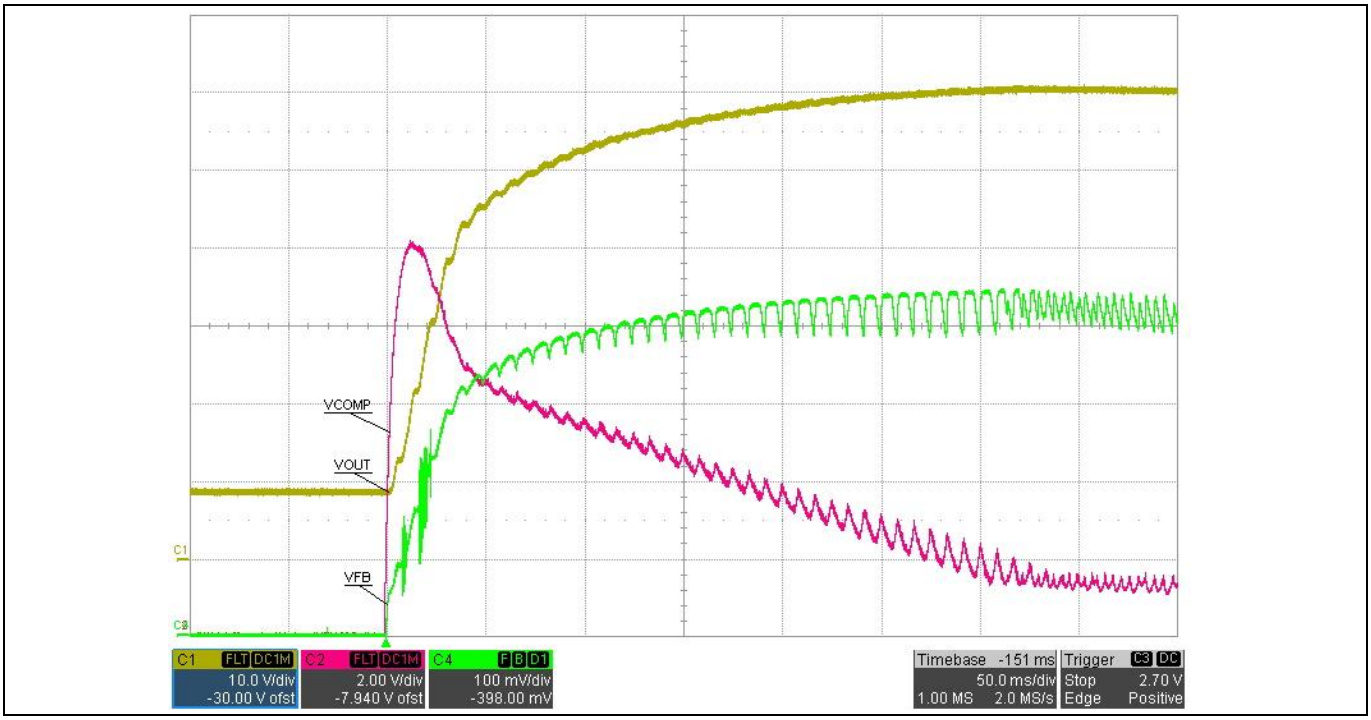


Figure 20 120 VAC start-up at 0% load
Output voltage (yellow), VCOMP (red), VFB (green)

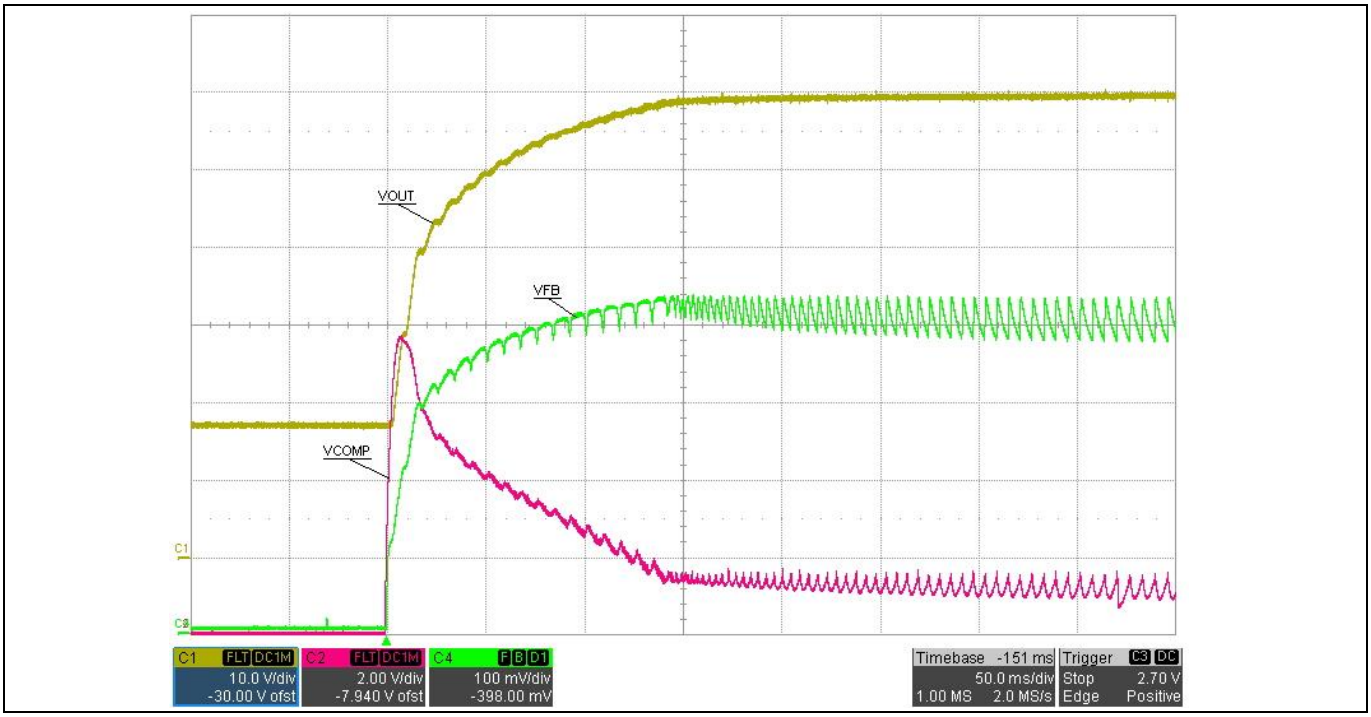


Figure 30 265 VAC start-up at 0% load
Output voltage (yellow), VCOMP (red), VFB (green)

10.5 Operation at line peak and zero crossing

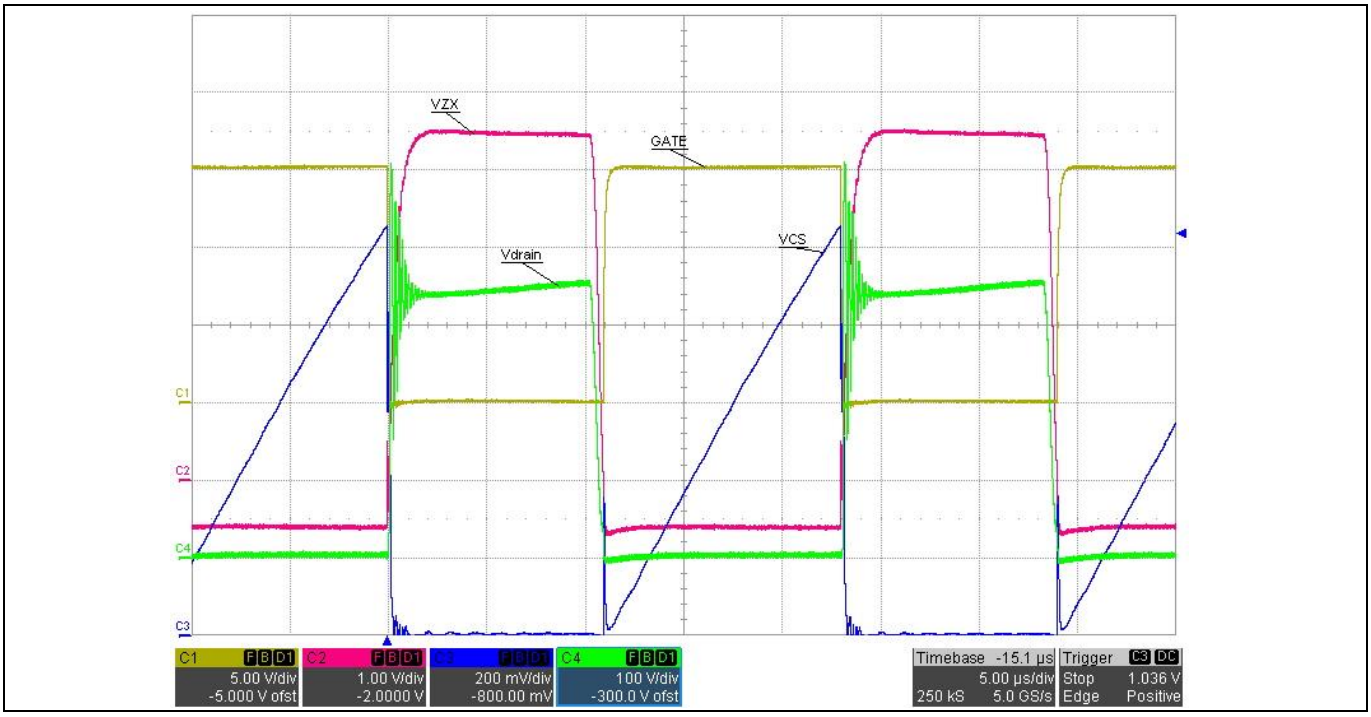


Figure 21 120 VAC at 100% load, AC line peak
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

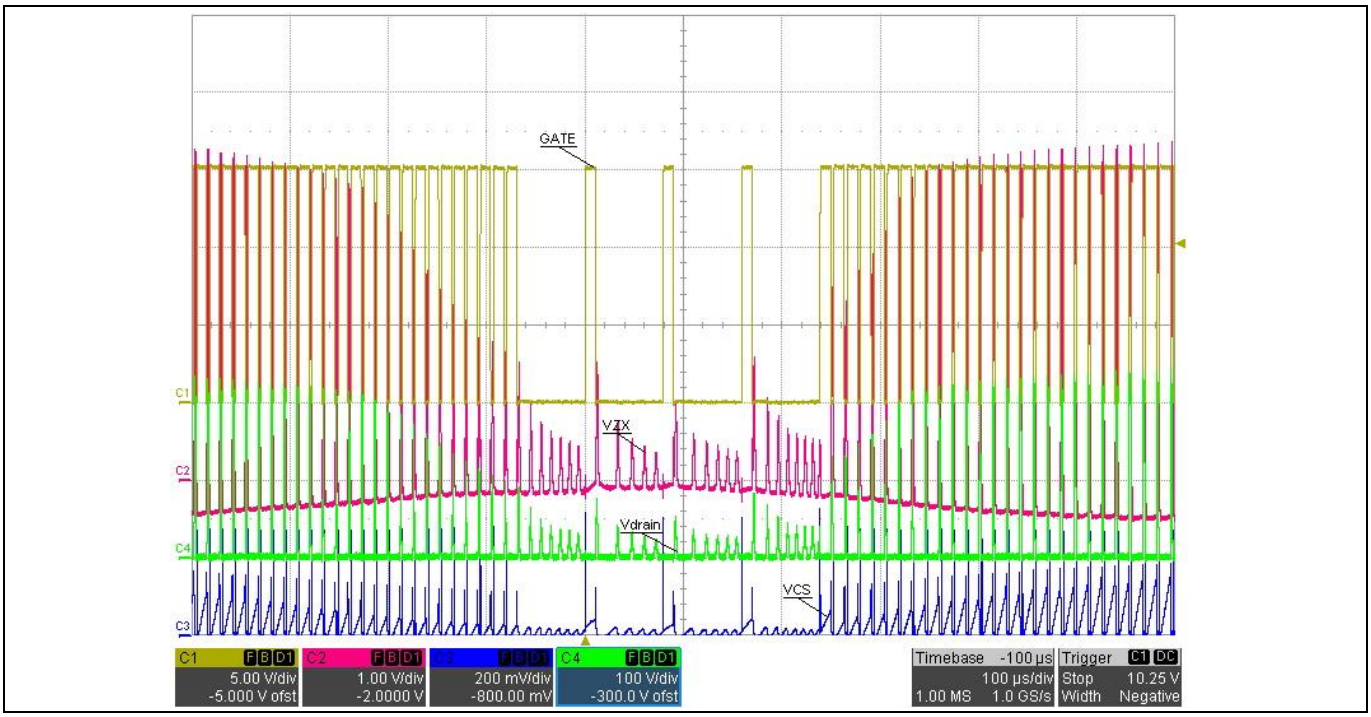


Figure 22 120 VAC at 100% load line zero-crossing
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

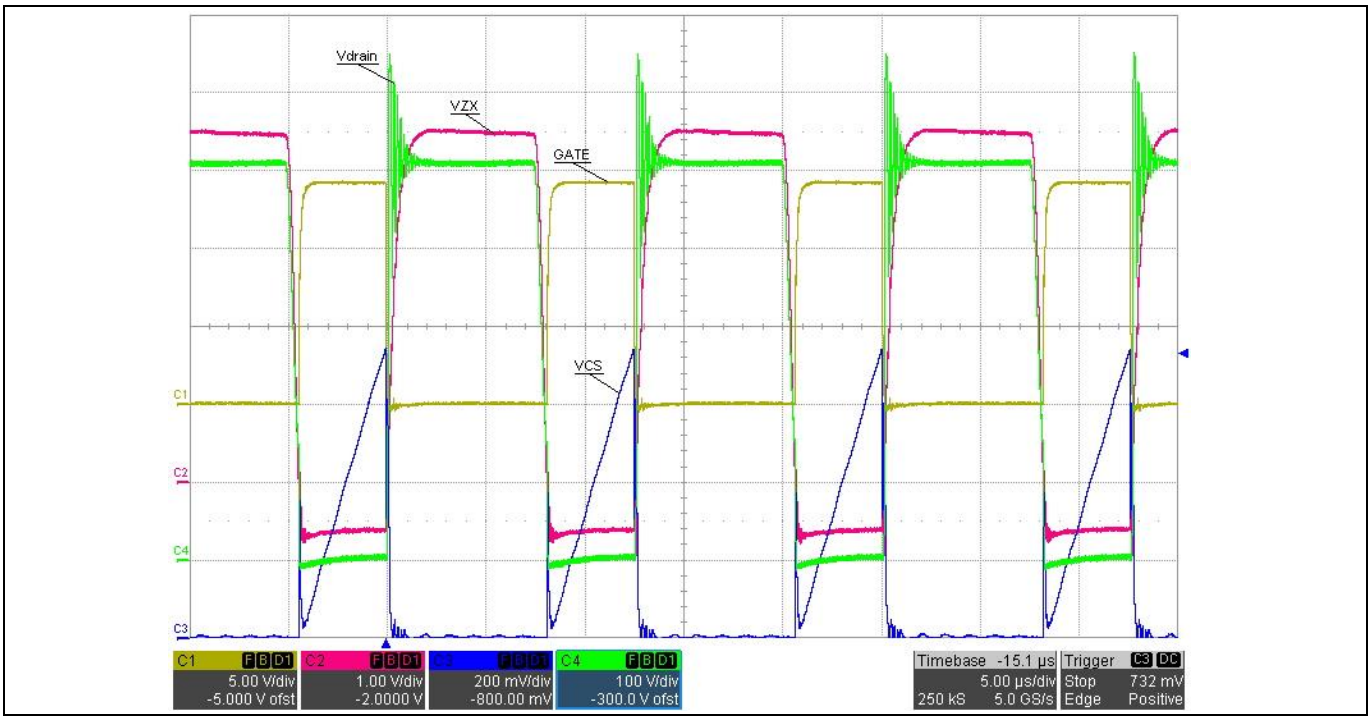


Figure 23 230 VAC at 100% load line peak
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

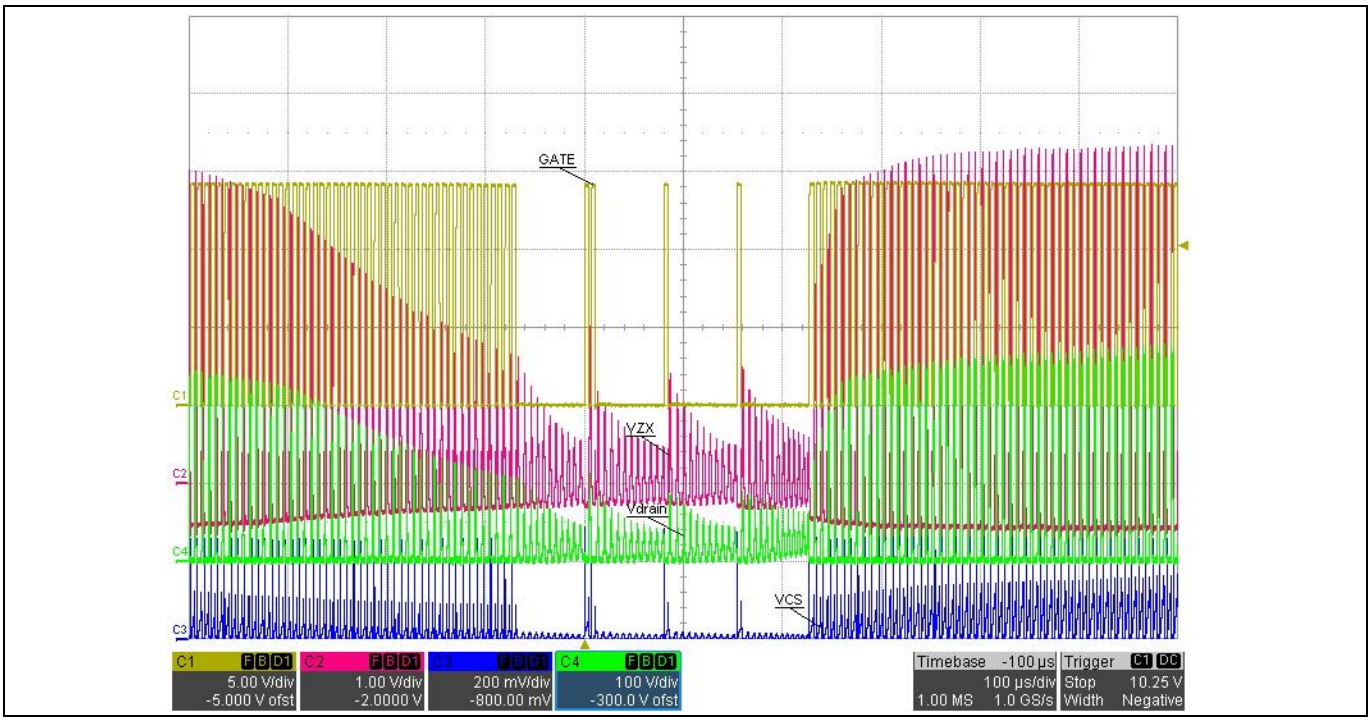


Figure 24 230 VAC at 100% load line zero-crossing
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

Close to the line zero-crossing the amplitude of VZX is below the VZX+ threshold of 1.54 V so the next switching cycle is not started until the restart interval timeout period t_{WD}. This does not significantly impact power factor and THD.

10.6 Burst mode operation at zero load

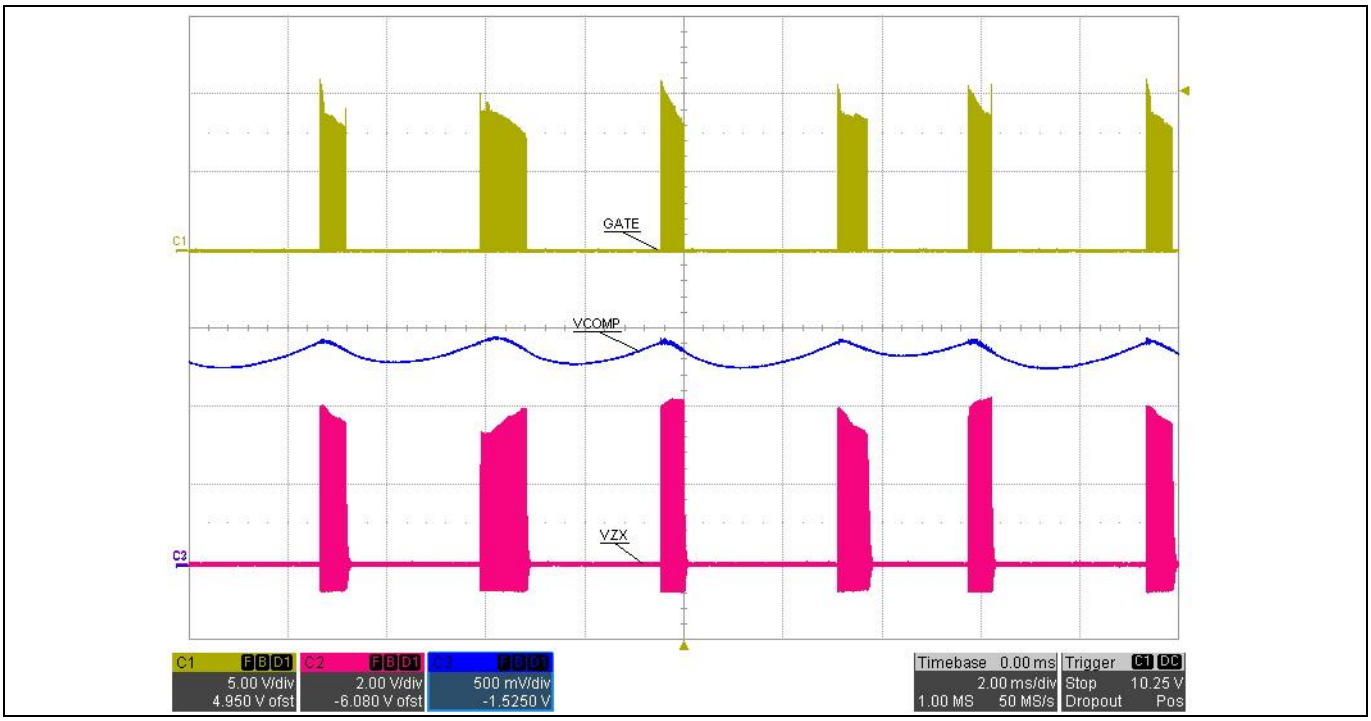


Figure 25 120 VAC start-up at 0% load burst mode operation
Gate drive (yellow), VCOMP (blue), VZX (red)

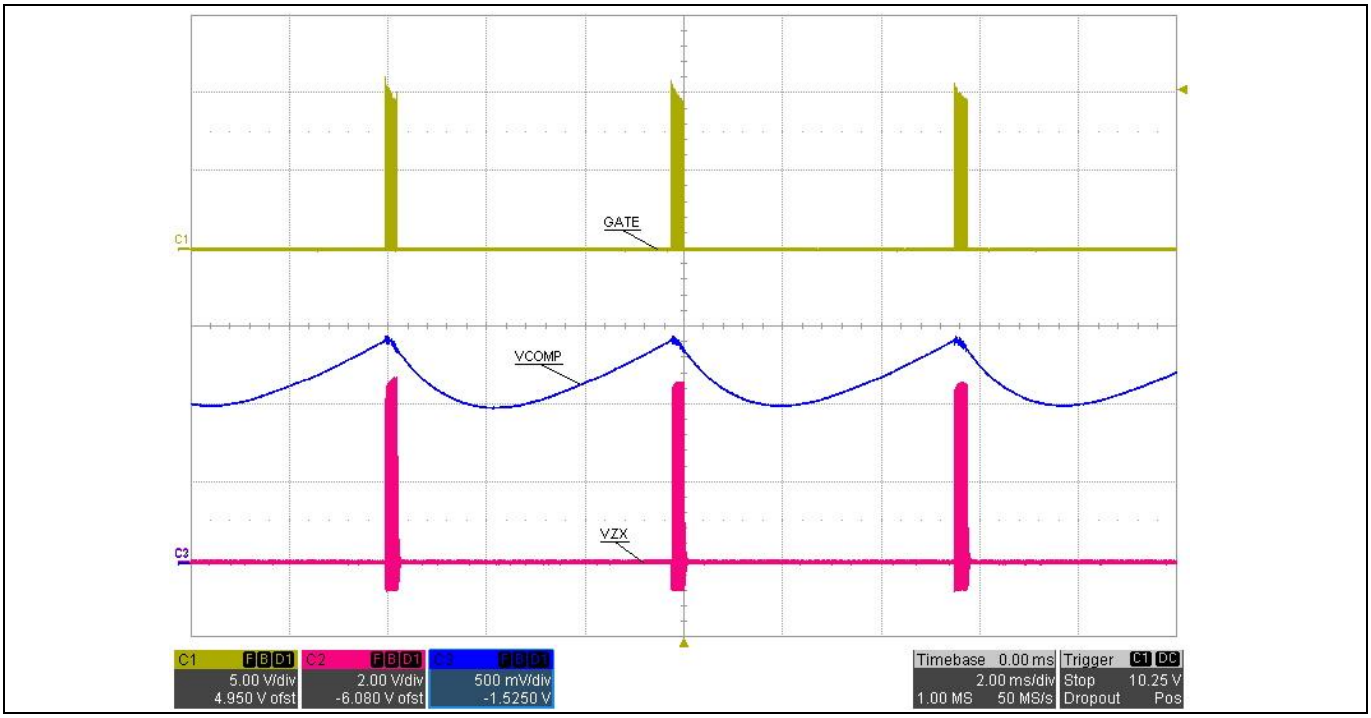


Figure 26 230 VAC start-up at 0% load burst mode operation
Gate drive (yellow), VCOMP (blue), VZX (red)

10.7 Light load DCM operation

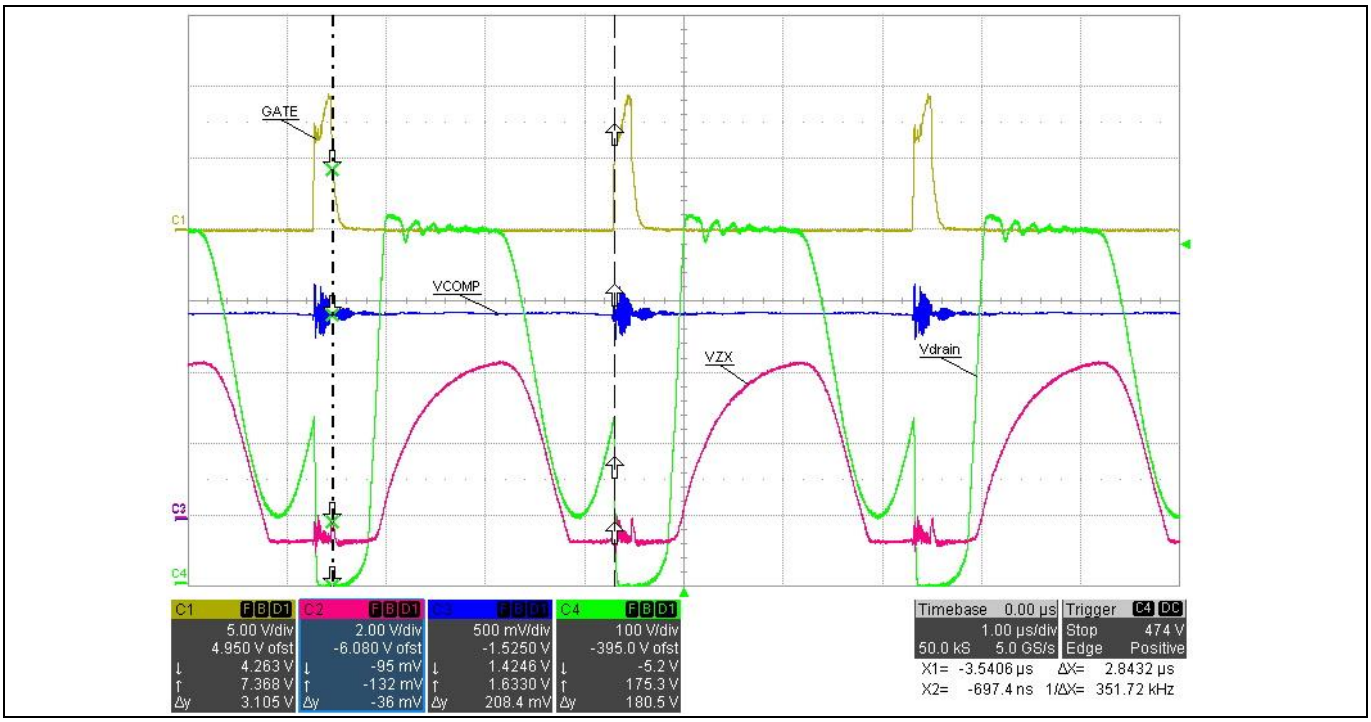


Figure 27 100 VAC start-up at zero load
Gate drive (yellow), VCOMP (blue), VZX (red), Vdrain (green)

10.8 Over-voltage protection through ZX

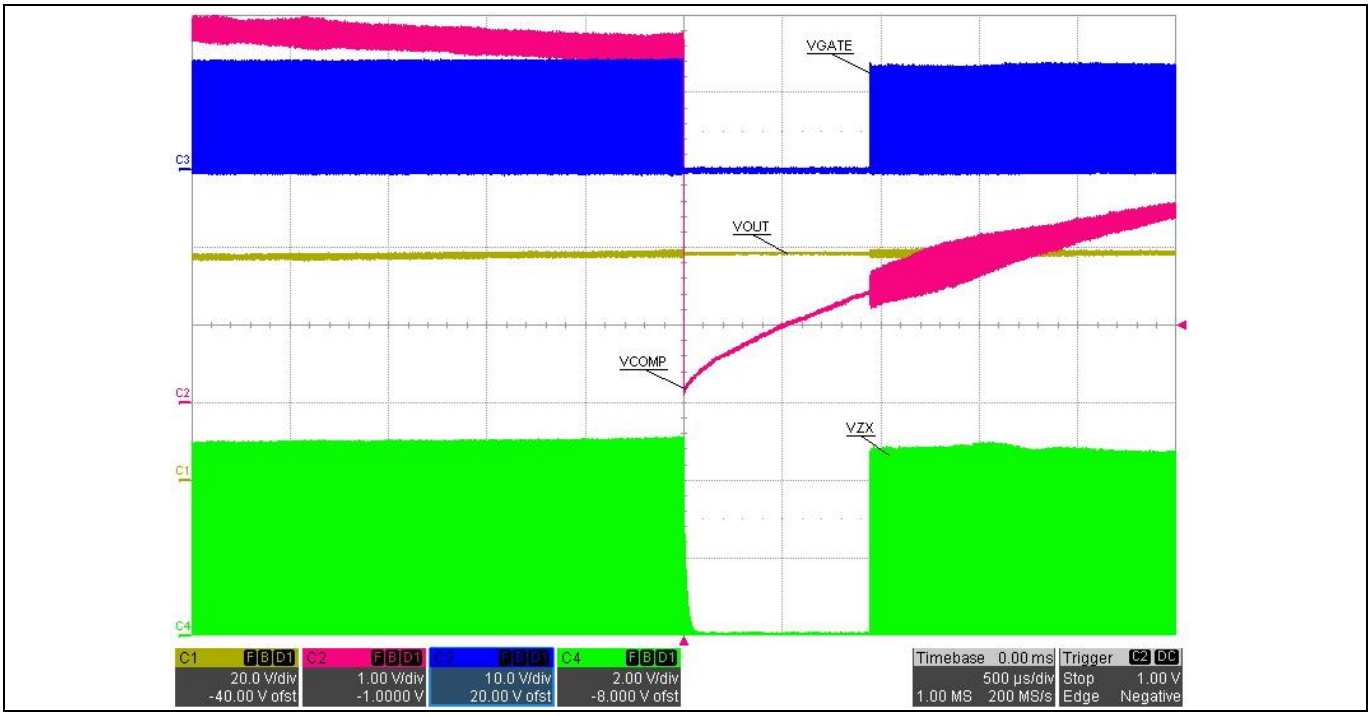


Figure 28 265 VAC load step from 100% to 0%
VOUT (yellow), Gate drive (blue), VCOMP (red), VZX (green)

10.9 High voltage start-up operation

The high voltage start-up (HV pin) input current is measured with a 10 k resistor (RHV) connected from HV to the bus so that the oscilloscope traces in the following figures display approximately 1 mA/div:

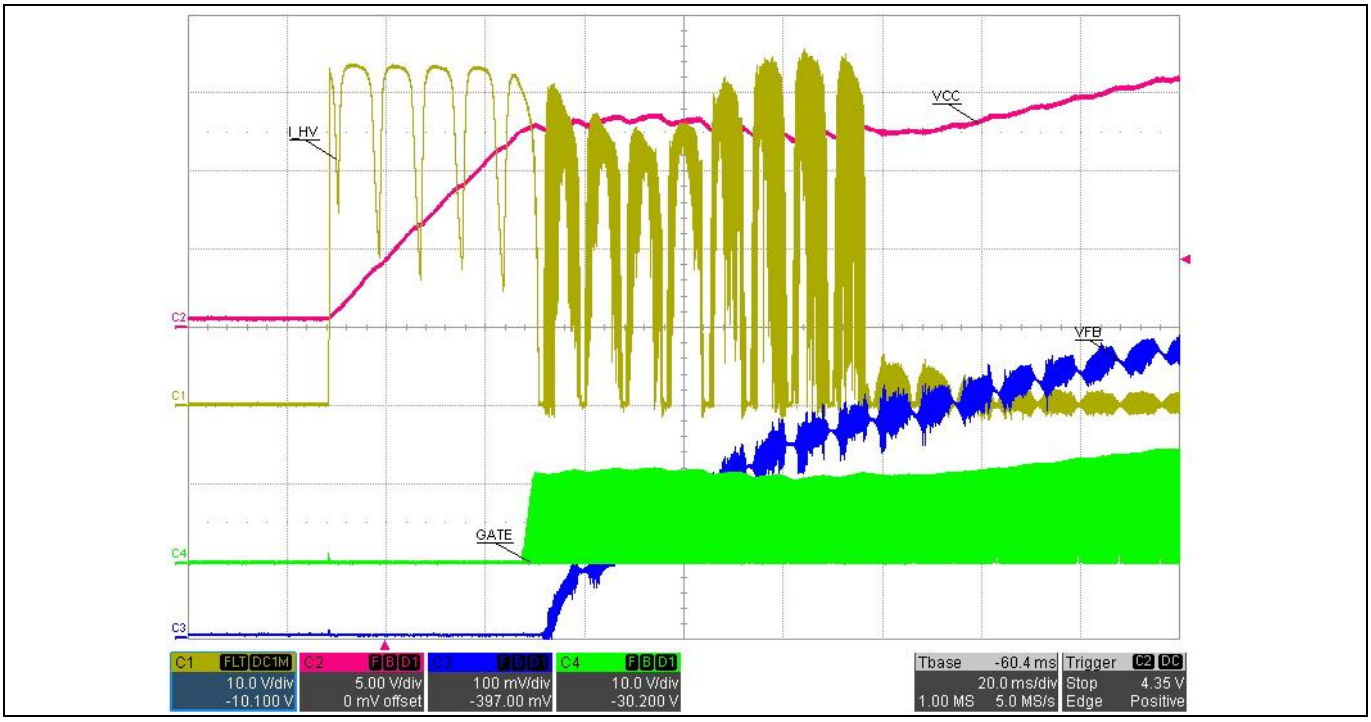


Figure 29 100 VAC start-up at 100% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

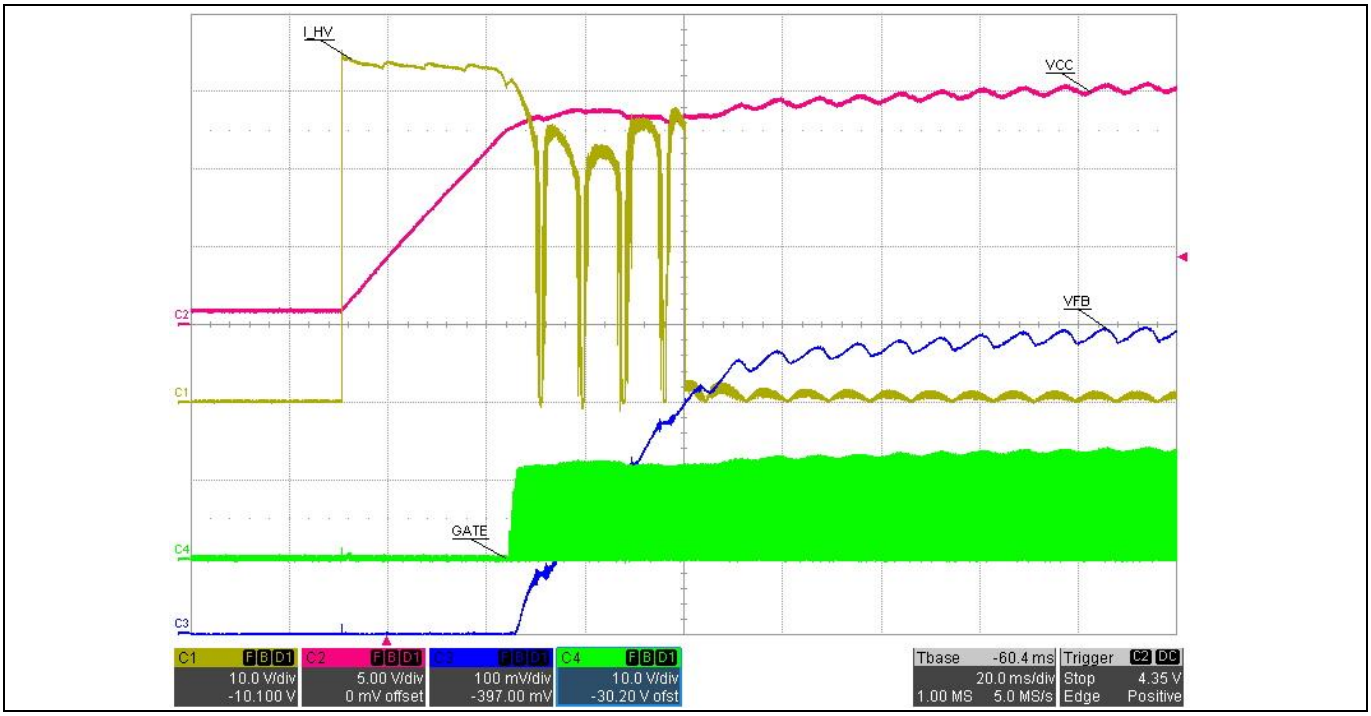


Figure 40 265 VAC start-up at 100% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

10.10 High voltage start-up cell operation during zero load burst mode

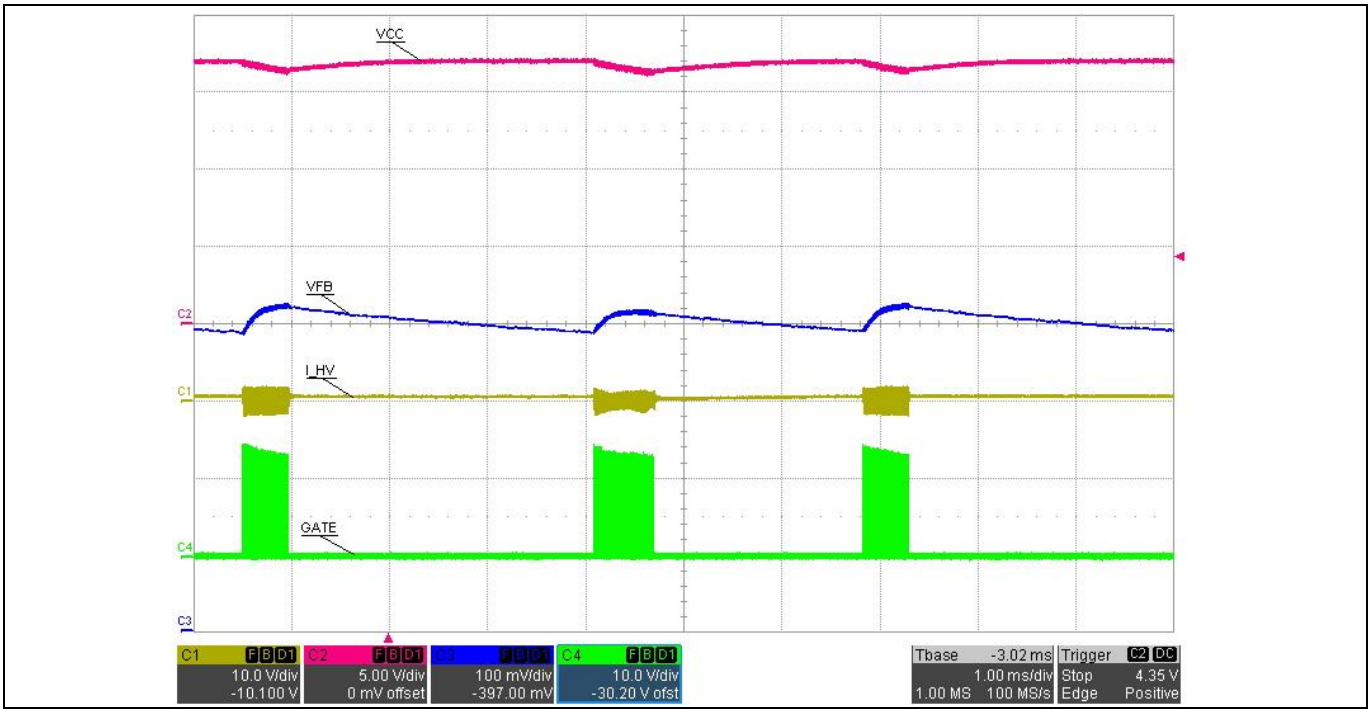


Figure 30 120 VAC start-up at 0% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

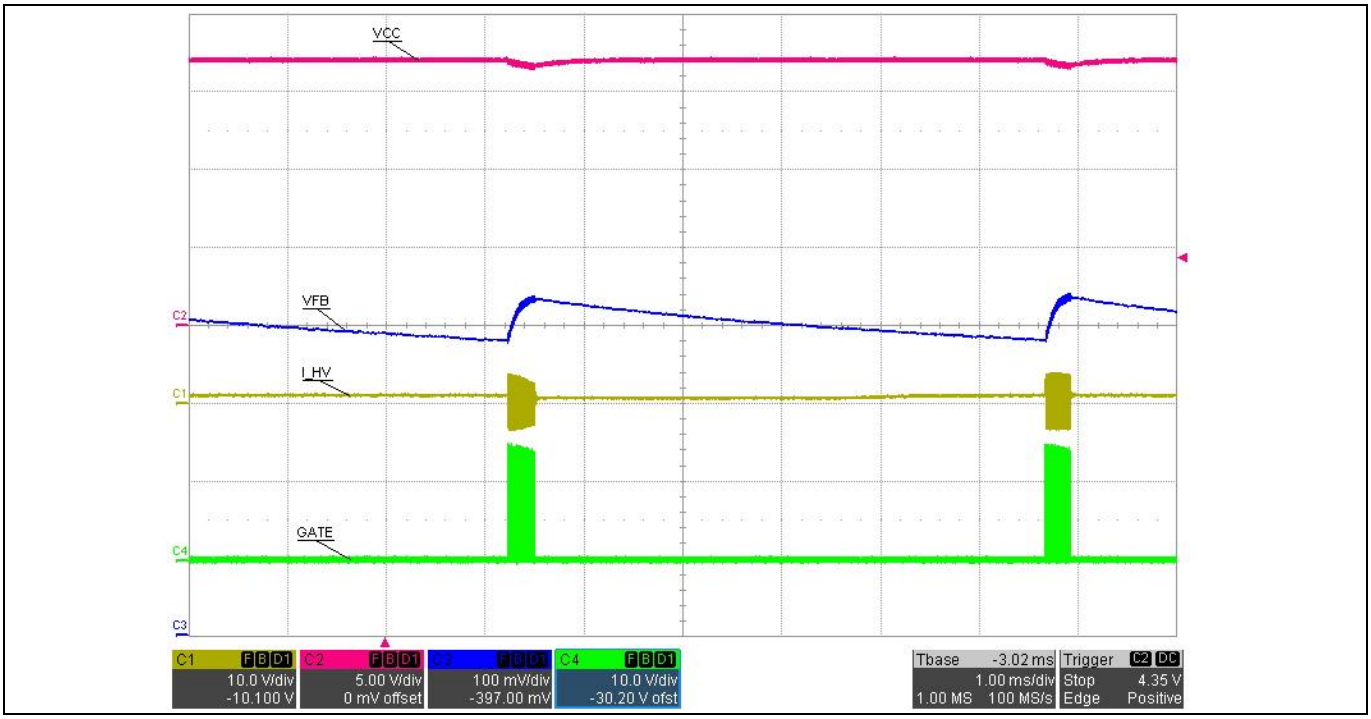


Figure 31 230 VAC start-up at 0% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

These waveforms show that in burst mode the auxiliary winding is able to supply VCC therefore the HV start-up cell support mode does not come into operation.

10.11 Thermal Performance under normal operating conditions

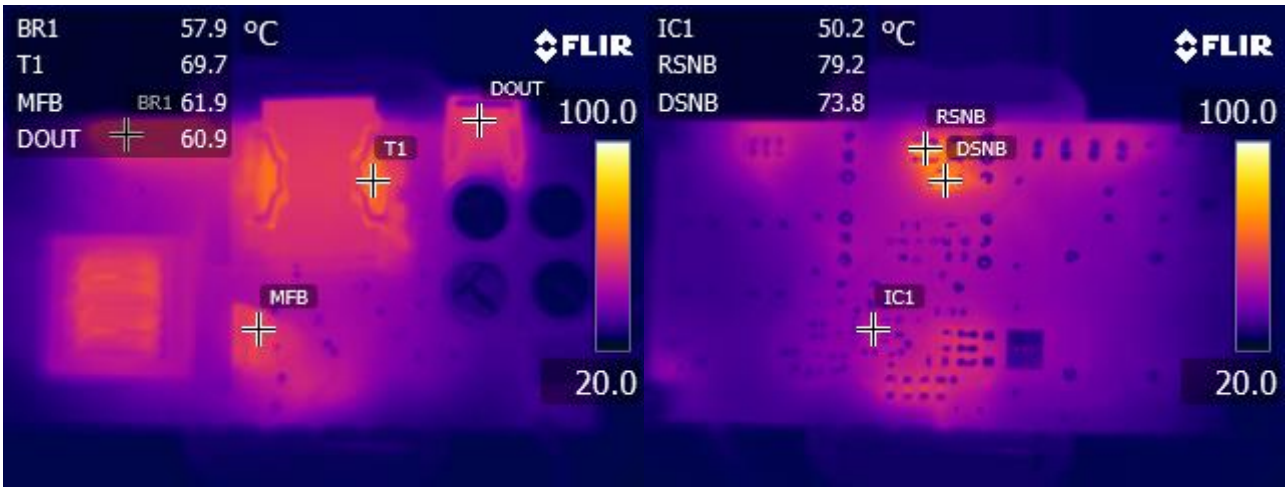


Figure 32 100 VAC at 100% load (board top and bottom sides)

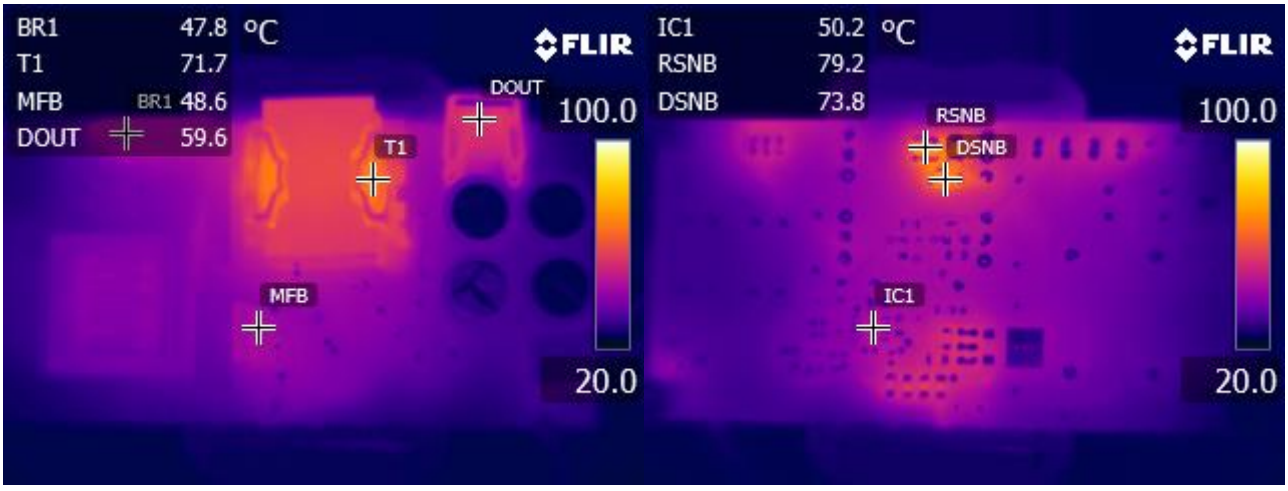


Figure 33 265 VAC at 100% load (board top and bottom sides)

10.12 Thermal Performance under abnormal operating conditions

10.12.1 Open feedback loop (RFB1 removed), VCC supply connected

The IRS2982S (IC1) reaches maximum case temperature at high line, 20% load. Temperature is measured in ambient of 25 °C.

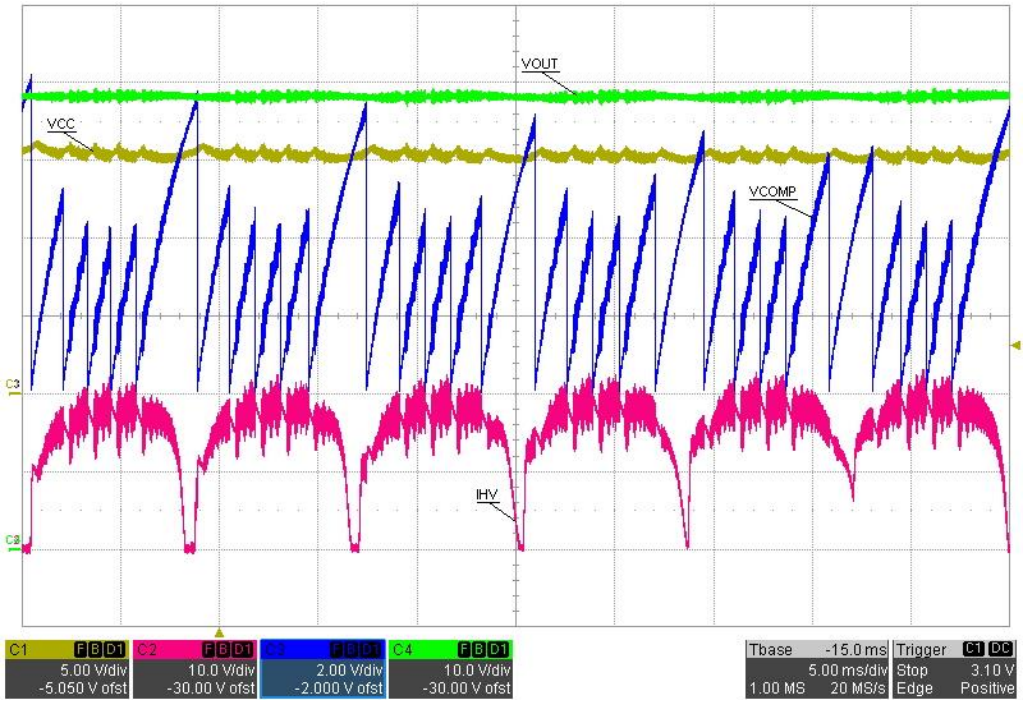


Figure 34 265 VAC at 20% load (IHV is 1mA/div)
VCC (yellow), VCOMP (blue), IHV (red), VOUT (green)

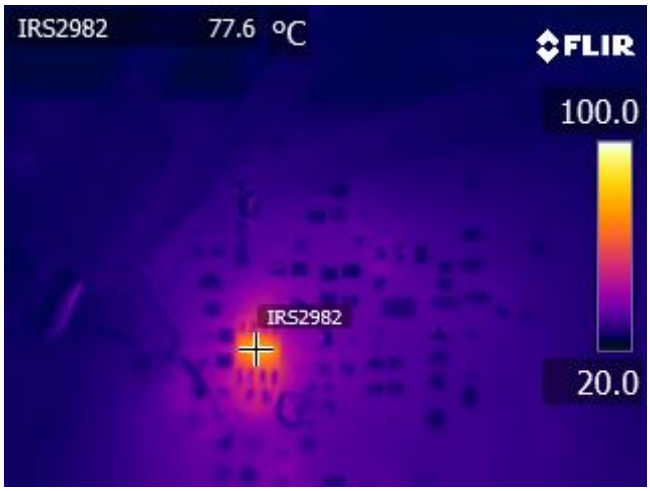


Figure 35 265 VAC at 20% load, IRS2982S case temperature

10.12.2 VCC supply removed (DVCC2 removed), feedback loop connected

The IRS2982S (IC1) reaches maximum case temperature at high line, 20% load. Temperature is measured in ambient of 25 °C.

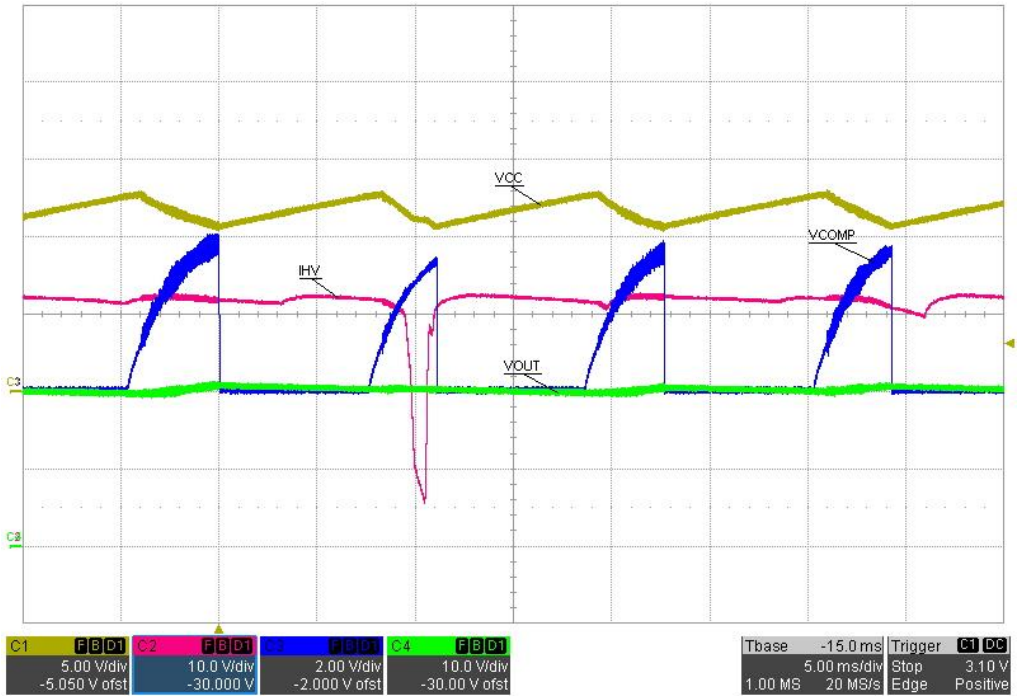


Figure 36 265 VAC at 20% load (IHV is 1mA/div)
VCC (yellow), VCOMP (blue), IHV (red), VOUT (green)

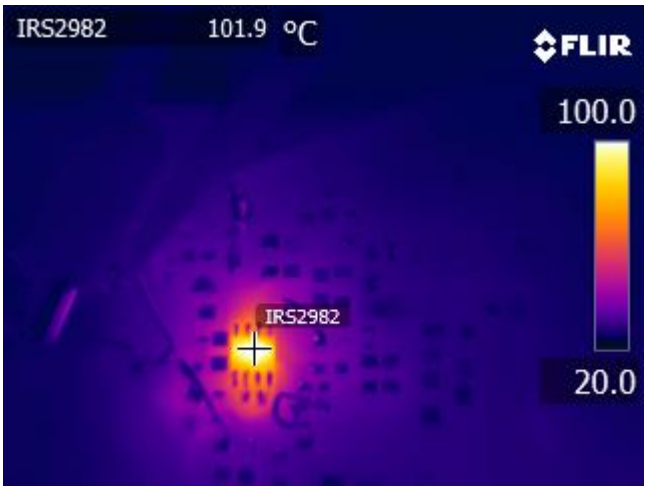


Figure 37 265 VAC at 20% load, IRS2982S case temperature

10.12.3 Reduced VCC supply (Support mode)

The IRS2982S (IC1) reaches maximum case temperature at high line, 20% load. Temperature is measured in ambient of 25 °C. VCC is supplied from an external supply maintained just above the UVLO threshold.

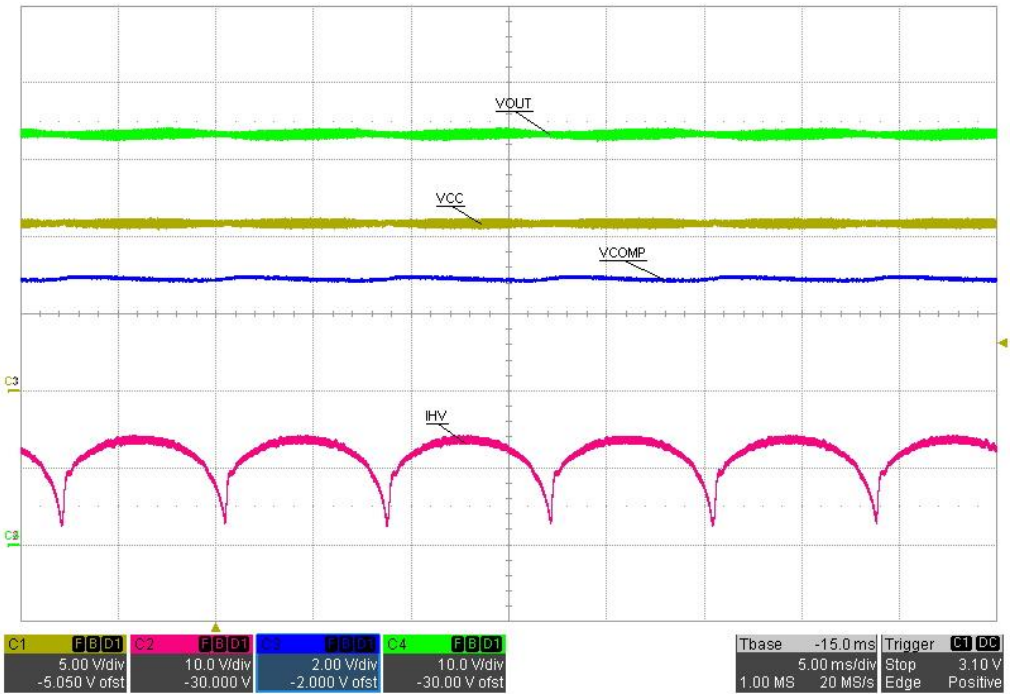


Figure 38 265VAC at 20% load (IHV is 1mA/div)
VCC (yellow), VCOMP (blue), IHV (red), VOUT (green)

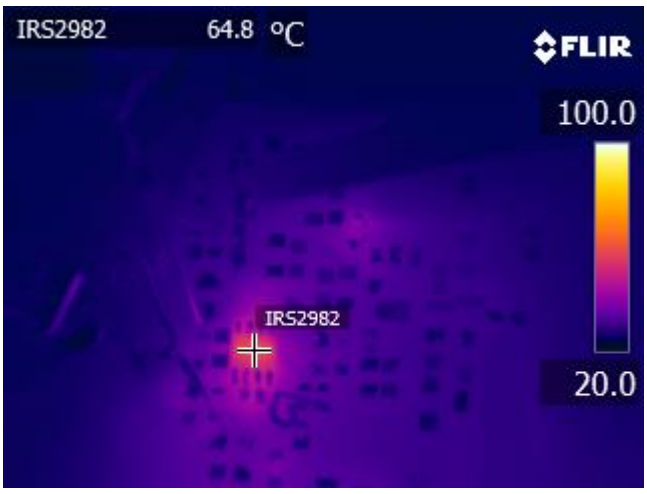


Figure 50 265 VAC at 100% load, IRS2982S case temperature

10.13 Line current harmonics according to EN61000-3-2

Requirements	Harmonics Limits Class C according EN 61000-3-2 for System Power > 25W	
	Harmonics order n	Maximum value expressed as a percentage of the fundamental input current
	2	<2%
	3	<30 λ %
	5	10%
	7	<7%
	9	<5%
	11 ≤ n ≤ 39	<3%
		λ = power factor

Table 6 EN61000-3-2 Class C limits for system power >25 W

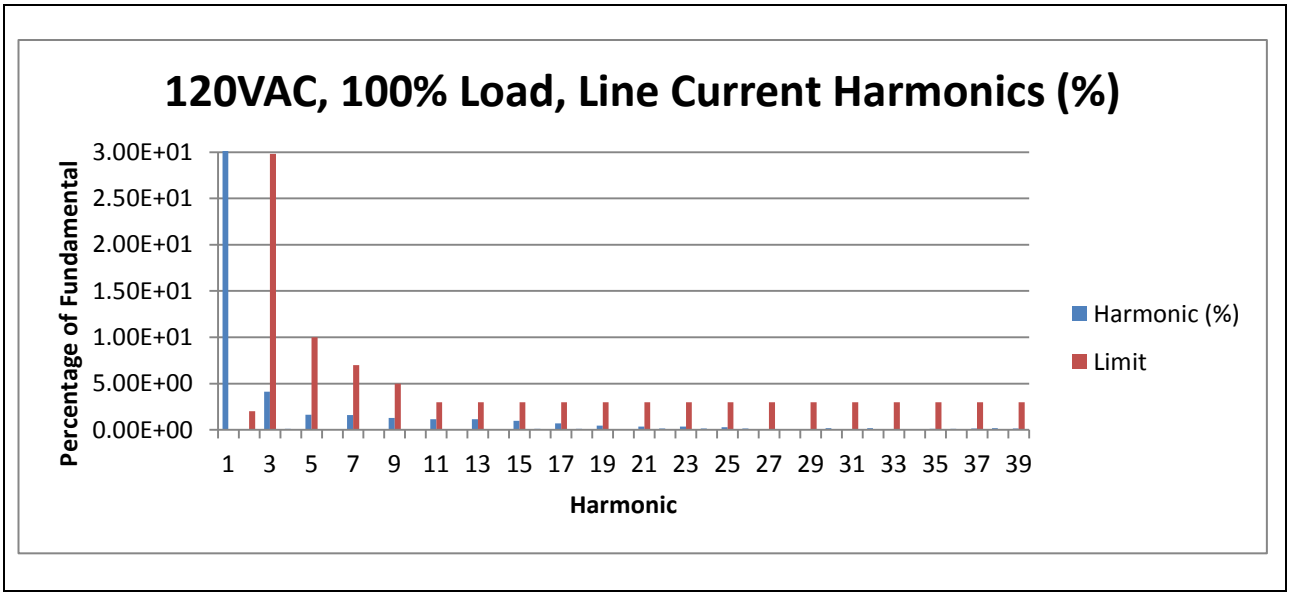


Figure 39 Harmonic test results at 120 VAC and 100% load

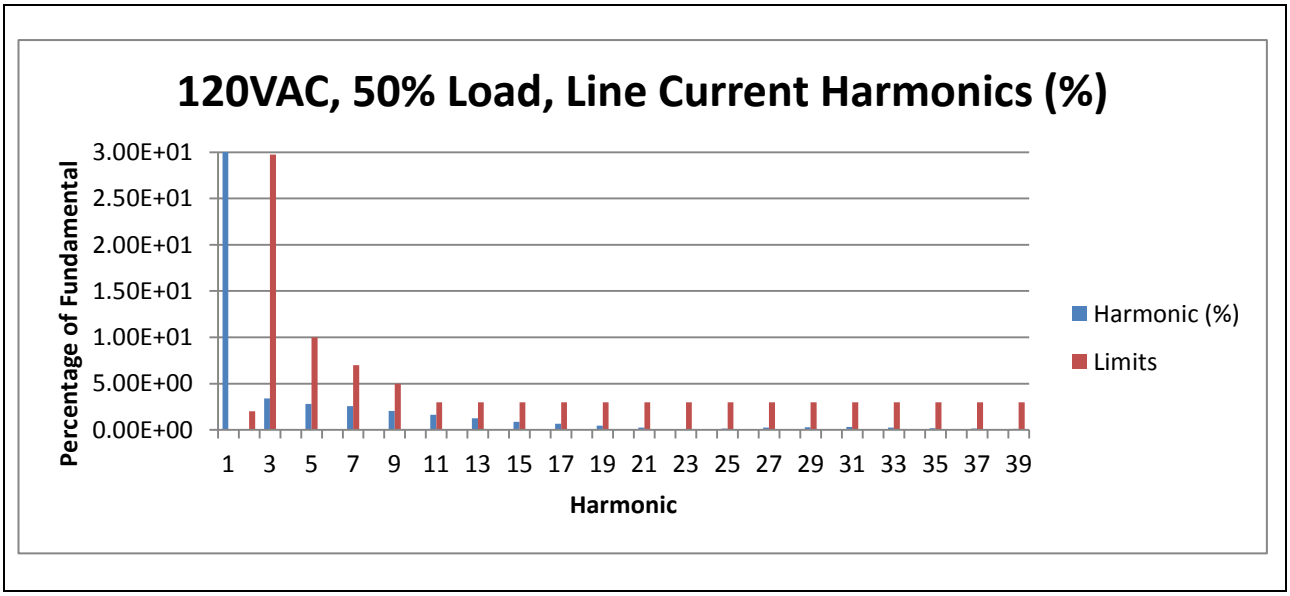


Figure 40 Harmonic test results at 120 VAC and 50% load

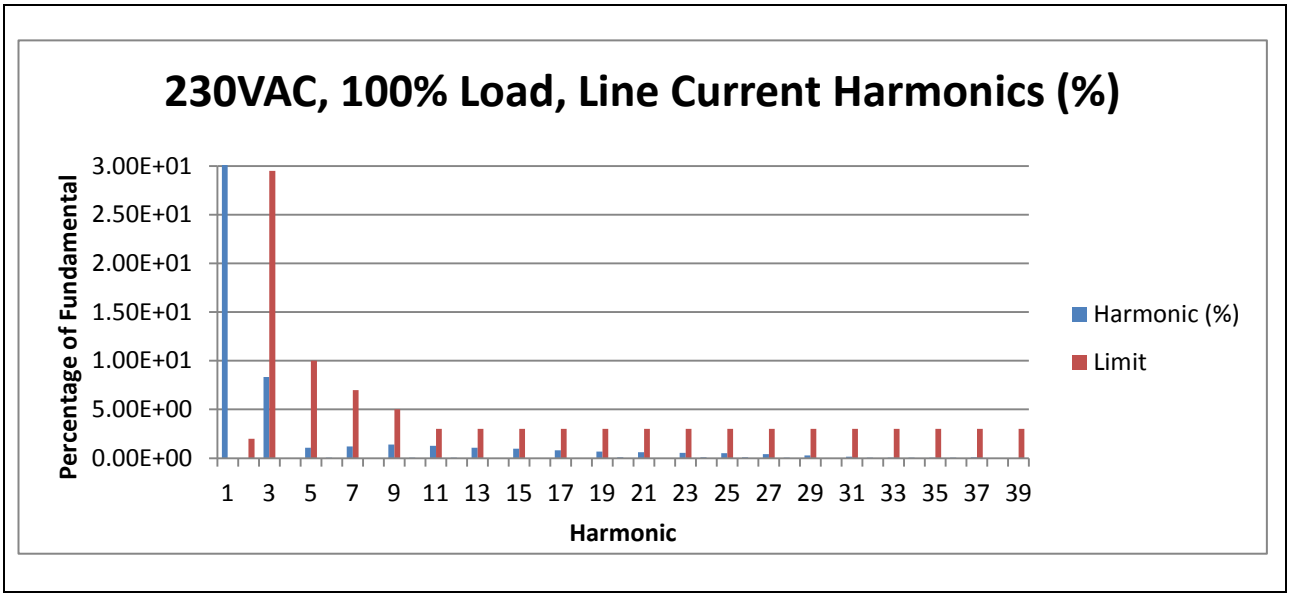


Figure 41 Harmonic test results at 230 VAC and 100% load

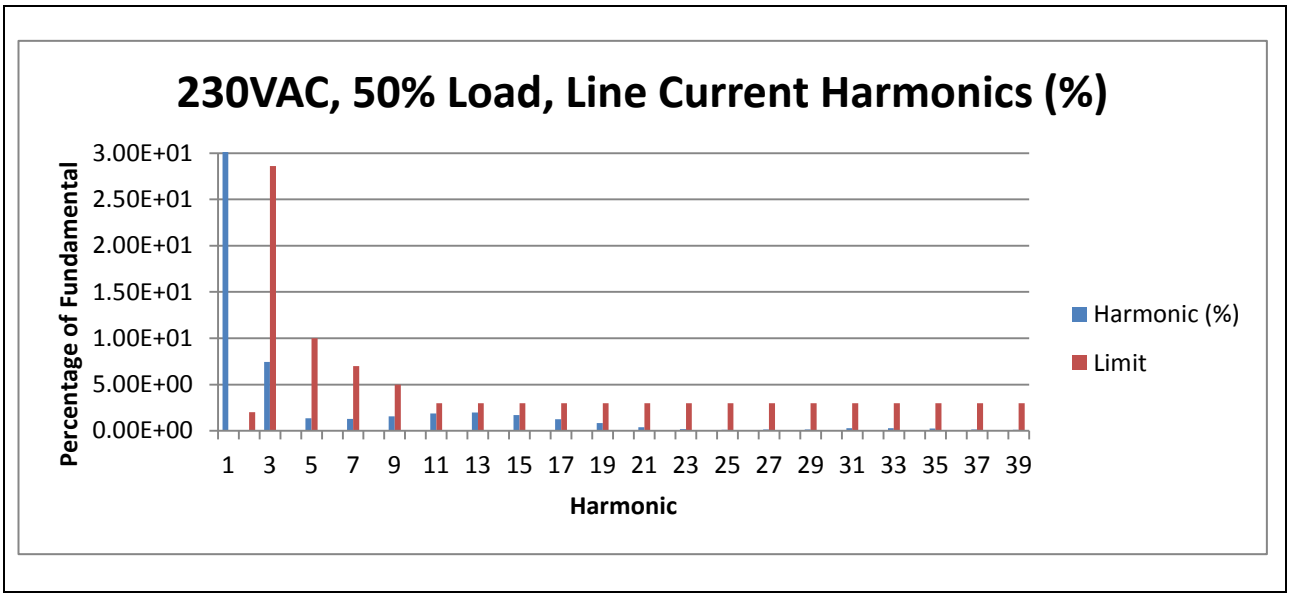


Figure 42 Harmonic test results at 230 VAC and 50% load

Class C limits are met at 50% and 100% loads at 120 VAC and 230 VAC.

10.13.1 EMI Conducted Emissions (tested to CISPR22 limits)

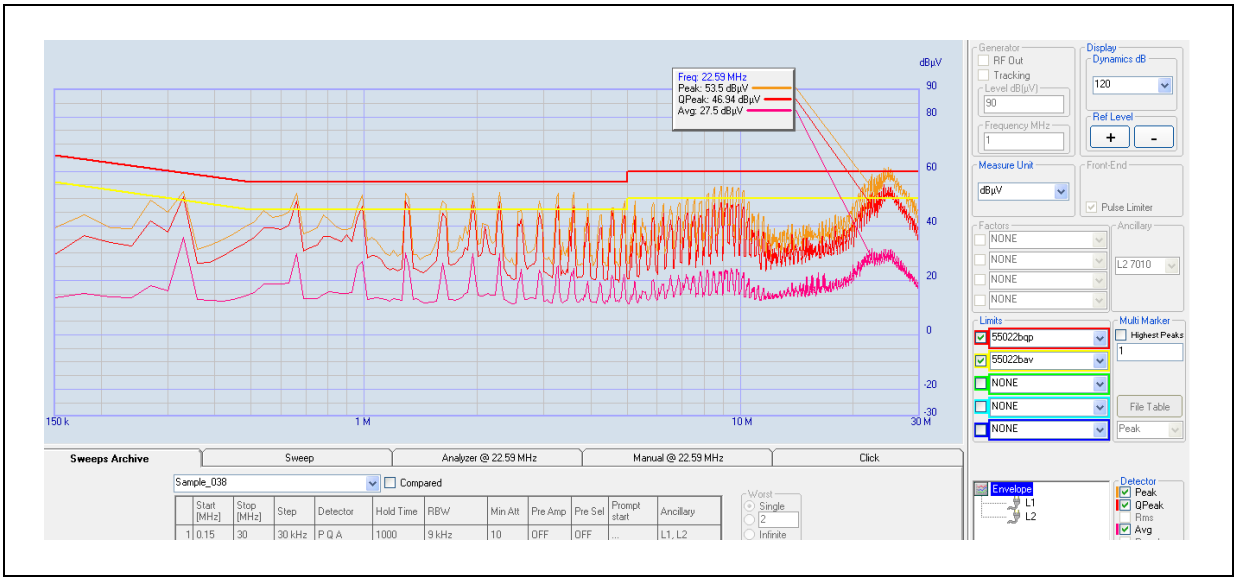


Figure 43 Conducted emissions at 120 VAC and 100% load

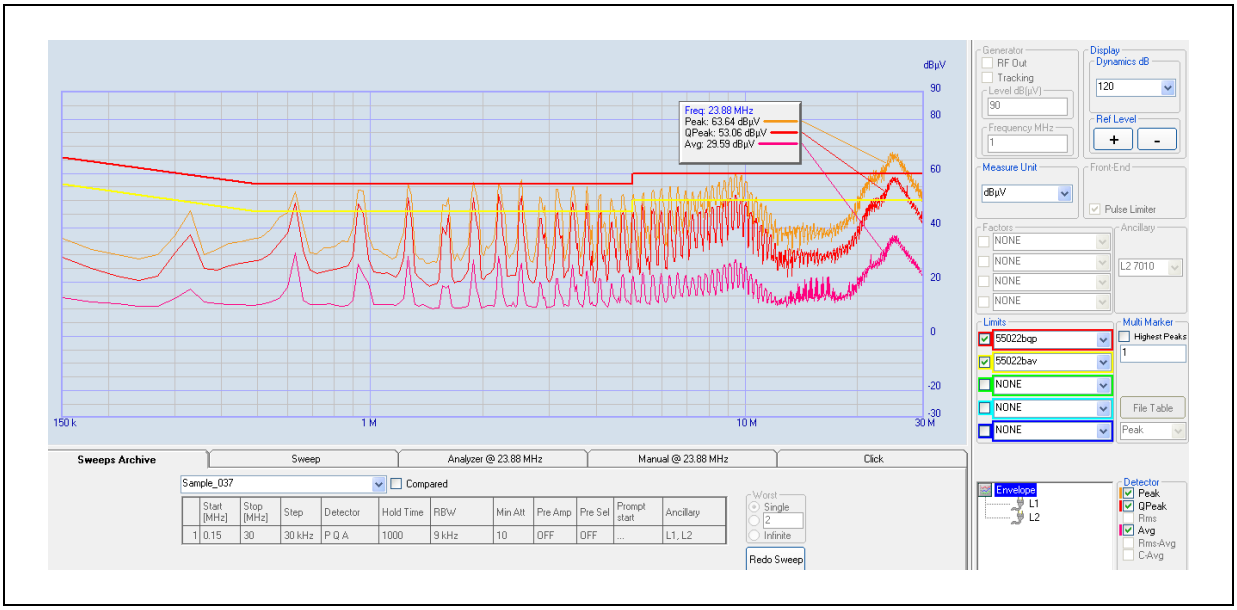


Figure 44 Conducted emissions at 230 VAC and 100% load

The red limit line shows the limit for the quasi-peak measurement, for which the frequency sweep trace is also shown in red. To pass the red trace must to remain below the red limit line and the pink average measurement trace must remain below the yellow average limit line. The orange peak trace may be disregarded.

EMI emissions are very dependent on the board layout, please refer to section 9.1.

Note

Infineon Technologies does not guarantee compliance with any EMI standard.

11 Conclusion

The specifications as listed in section 3.2 are met with efficiency exceeding 90% across the full line input voltage range from 50% to 100% load. Power factor remains above 0.95 at 120 VAC and 230 VAC nominal inputs from 50% load to 100%. The input current total harmonic distortion (iTHD) remains below 10% from 20% to 100% load over at 120 VAC input and from 70% to 100% load at 230 VAC, remaining below 20% down to 20% load from 100 to 265 VAC. At lighter loads power factor falls and iTHD increases, however output voltage regulation remains tight. Output voltage ripple at twice the AC line frequency remains 1.6 Vpp at full load at 60 Hz independent of the input voltage, which matches the calculated value from equation (10). Type 2 compensation of the operational trans-conductance error amplifier (OTA) provides tight load regulation from 10% to 100% load with a small increase below 10%. The output voltage rises to its operating level in less than 300 ms with no overshoot from 100 VAC to 265 VAC with only minimal overshoot at 100 VAC over the full load range. Performance indicates an over-damped control loop corresponding to the phase margin determined in section 6. The type 2 control loop compensation network successfully controls the startup and settling response while providing high power factor and low iTHD over a wide line/load range, which is able to meet EN61000-3-2 class C requirements for lighting apparatus. Over voltage protection as detected through the ZX input operates correctly to limit the output voltage under open and very light load conditions. Operation in DCM and burst mode are also seen to maintain output voltage regulation where necessary. Cycle by cycle primary over current protection operates correctly at start-up to limit inductor current and stress of the MOSFET. Operating waveforms confirm the calculated peak current value from section 5.

Thermal performance under normal operating conditions (measured in open air at 25 degrees C ambient) as shown in section 10.11, indicates a temperature rise of 45°C at the transformer windings, however the cores remain at a lower temperature. The input bridge (BR1) operates component at low line with a rise of 33°C with a greatly reduced temperature rise at high line of 23°C. The MOSFET (MFB) has a 37°C rise at low line and a 24°C rise at high line due to higher primary peak current at low line for the IPA80R650CE measured with no heatsink attached.

Under all normal conditions the high voltage start-up cell is deactivated as the feedback loop closes and it switches over from start-up mode to support mode. The HV cell allows the power supply to start up rapidly at any line input voltage, meeting the maximum specification of 300 ms from switch on to reaching nominal output voltage.

Standy power is composed of the power dissipated in the output resistor ROUT and the power consumed by the controller IC VCC supplying the MOSFET gate drive during burst mode operation as shown in figures 35 and 36. The power dissipated in ROUT is 240mW in this design, which can be reduced by increasing the resistor value athough this could cause the output to sightly exceed 60V under an open load condition. This would not be an issue in designs with lower output voltages. Figure 36 shows that the burst duration at 230VAC is much shorter than that at 120VAC as shown in figure 35, which explains why the standby power is higher at low line.

Conclusion

Under fault conditions as shown in section 10.12, the start-up cell continues to operate in support mode in the following cases:

1. The feedback loop is open because the IRS2982S never switches to support mode. In this case there is no output voltage regulation however the output voltage is limited by continuous operation of the over-voltage protection. The IRS2982S draws between 1 and 2 mA under this condition causing the case temperature to rise 50°C at maximum line input 265 VAC. The IC would therefore remain within its recommended operating range at an ambient temperature up to 75°C.
2. VCC is not supplied through the auxiliary transformer winding but the feedback loop is still connected. In this case the HV start-up cell operating in support mode supplies all of the current to VCC. At maximum line input with 20% load, which is the worst case, the IRS2982S case temperature rises nearly 80°C. At a high ambient temperature there is a risk that the IC could exceed its maximum recommended operating temperature of 125°C. This situation should be avoided by ensuring that VCC receives current from the auxiliary winding during initial testing of the board.
3. VCC is not sufficiently supplied through the auxiliary transformer winding so that the HV start-up cell continues to supply current in support mode. For this test the auxiliary VCC supply was adjusted to maintain VCC just above the under-voltage lock-out threshold where the HV start-up cell continues to supply a little over 1 mA during normal operation. In this case at maximum line input the IRS2982S case temperature rise measured was 40°C.

Quasi-peak and average conducted emission sweeps fall within limits over the frequency spectrum from 150 kHz to 30 MHz. It should be noted that these measurements were not made by a certified test lab and are intended only as an indication of performance.

In conclusion, the IRS2982S based Flyback converter design provides excellent performance and robustness with tight control and reliable protection. This design is well suited as a front end section in a two stage LED driver, where the back end section would typically be a constant current regulated Buck stage. Since there is no output over-load or short circuit protection the output current can reach several Amps, therefore the converter could become damaged under prolonged operation in these conditions.

References

[1] IRS2982SPBF SMPS control IC datasheet, Infineon Technologies.

Attention:

Revision History

Major changes since the last revision

Page or Reference	Description of change
	First Release
Rev 1.1	Added heat sinks and fasteners to the BOM
Rev 1.2	Correction to equation (5) and calculation. Added wiring diagram.

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