



# 170809119 Si53102 Datasheet Update

**PCN Issue Date:** 8/9/2017

**Effective Date:** 11/15/2017

**PCN Type:** Datasheet

## Description of Change

Silicon Labs is pleased to announce Revision 1.4 of the SI53102 Datasheet. The changes include:

- 1) Separated the output clock VOX spec into separate rows for 2.5V and 3.3V
- 2) Separated the output clock PCIe Gen3 jitter spec into separate rows for 2.5V and 3.3V and updated max numbers
- 3) Separated the output clock PCIe Gen4 spec into separate rows for 2.5V and 3.3V and updated max numbers.

From Revision 1.2

- 1) Crossing Point Voltage at 0.7V Swing (VDD = 2.5V - 3.3V) : 300mV (min); 500mV (max)
- 2) PCIe Gen 3 Additive Phase Jitter max (VDD = 2.5V - 3.3V) : 0.20ps
- 3) PCIe Gen 4 Additive Phase Jitter max (VDD = 2.5V - 3.3V) : 0.20ps

To Revision 1.4

- 1) Crossing Point Voltage at 0.7V Swing (VDD = 3.3V) : 300mV (min); 500mV (max)  
Crossing Point Voltage at 0.7V Swing (VDD = 2.5V) : 200mV (min); 500mV (max)
- 2) PCIe Gen 3 Additive Phase Jitter max (3.3V) : 0.22ps  
PCIe Gen 3 Additive Phase Jitter max (2.5V) : 0.25ps
- 3) PCIe Gen 4 Additive Phase Jitter max (VDD = 3.3V) : 0.22ps  
PCIe Gen 4 Additive Phase Jitter max (VDD = 2.5V) : 0.25ps

## Reason for Change

This datasheet change adds additional details of the Jitter specification for 2.5V and 3.3V respectively.

## Impact on Form, Fit, Function, Quality, Reliability

none

## Product Identification

Existing Part #  
Si53102-A1-GM  
Si53102-A1-GMR  
Si53102-A2-GM  
Si53102-A2-GMR  
Si53102-A3-GM  
Si53102-A3-GMR

**Last Date of Unchanged Product:** 11/15/2017

## Qualification Samples

n/a

Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at <http://www.silabs.com>.

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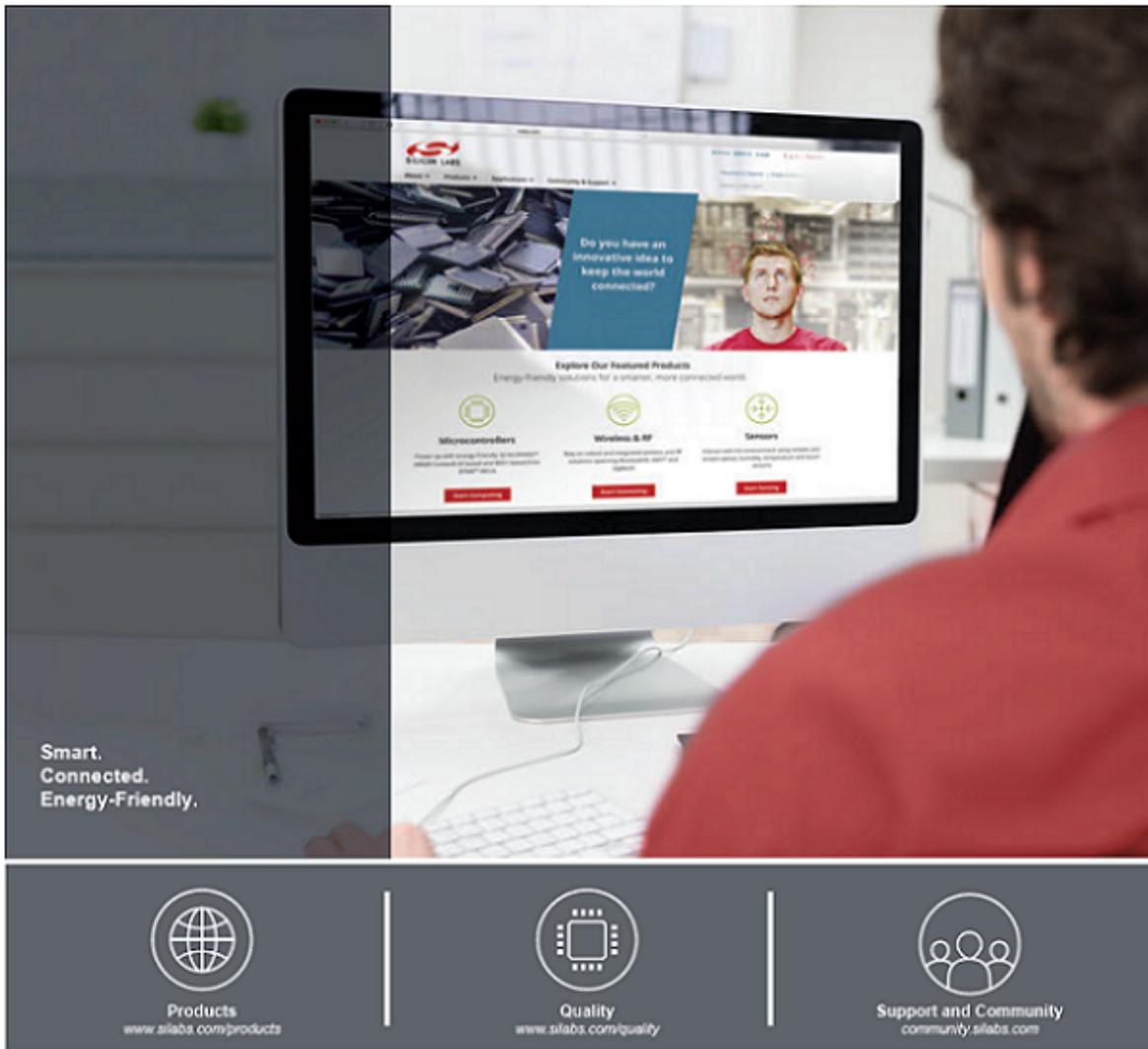
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### Qualification Data

n/a



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