MAX12900

Ultra-Low-Power Analog Front-End for 4mA–20mA Sensor Transmitter

General Description

The MAX12900 is an ultra-low-power, highly integrated Analog Front-End (AFE) for a 4mA–20mA sensor transmitter. The MAX12900 integrates ten building blocks in a small package: a wide input supply voltage LDO, two conditioner circuits for pulse-width-modulated (PWM) inputs, two low-power, low-drift, general-purpose operational amplifiers (op amp) one wide bandwidth, zero-offset drift operational amplifier; two diagnostic comparators, a power-up sequencer with power good output to allow for a smooth power-up, and a low-drift voltage reference.

The MAX12900 converts PWM data from a microcontroller into current over a 4mA–20mA loop with two, three, or four-wire configurations.

The equivalent to an ultra-low-power, high-resolution, digital-to-analog converter is realized with the combination of two-PWM signals received from a microcontroller, the two conditioner circuits, and an active filter built with the integrated low-power op amp. The outputs of the two conditioner circuits provide a stable PWM amplitude over voltage supply and temperature variation. The wide bandwidth amplifier, in combination with a discrete transistor, converts a voltage input into a current output and allows HART and Foundation Fieldbus H1 signal modulation. The zero-offset operational amplifier and the low-drift voltage reference provide negligible error over wide temperature. The low-power operational amplifier and comparators provide building blocks for enhanced diagnostic features. Supply rail monitoring, output current readback, open circuit and failure detection are a few examples of diagnostic features. All these features, as well as ultra-low-power and high accuracy make the MAX12900 ideal for loop-powered smart sensor transmitters for industrial application.

The MAX12900 is available in 5mm x 5mm 32-pin TQFN package and operates over a wide industrial temperature range of -40°C to +125°C.

Benefits and Features

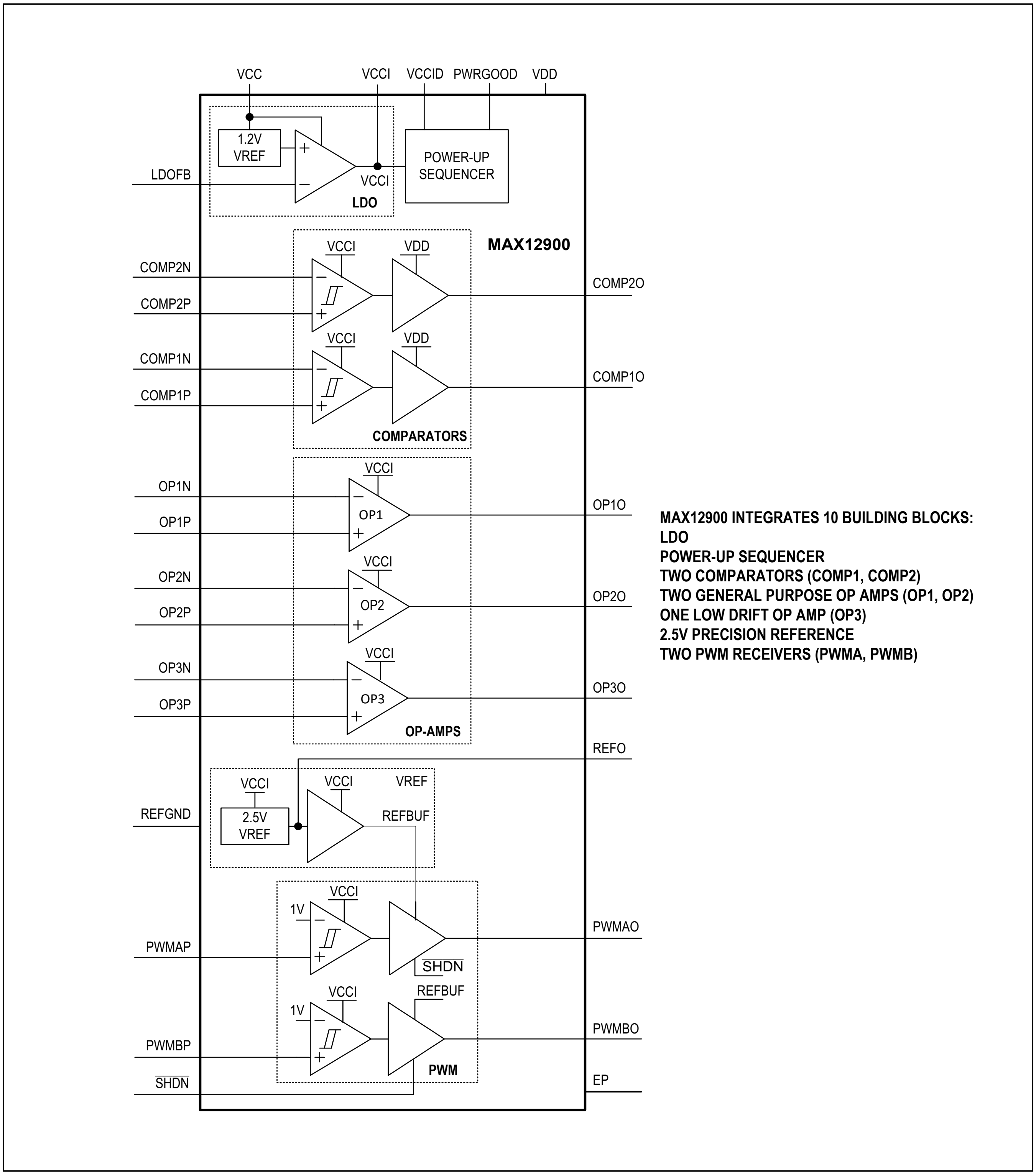
- Wide Input Supply Range: 4.0V to 36V
- Ultra-Low-Power Consumption: 170µA (typ)
- High Linearity: 0.01% (Max Error)
- High Resolution: Up to 16 Bit
- Low Drift Voltage Reference: 10ppm/°C max
- Wide Temperature Range: -40°C to +125°C
- Small Package: 5mm x 5mm x 0.8mm 32-pin TQFN

Applications

- Loop-Powered 4mA–20mA Current Transmitter
- Smart Sensors
- Remote Instrumentation
- Industrial Automation and Process Control

***Ordering Information* appears at end of data sheet.**

Functional Block Diagram



Absolute Maximum Ratings

VCC to GND ....-0.3V to +40V
VCC to VCCI ....-0.3V to +40V
VCCI and VCCID to GND ....-0.3V to +6V
VCCI to VCCID..-0.3V to +0.3V
VDD to GND ....-0.3V to +6V
PWRGOOD to GND.................................-0.3V to VCCI + 0.3V
LDOFB to GND ....-0.3V to VCCI + 0.3V
I/C and REFGND to GND ....-0.3V to + 0.3V
$\overline{\text{SHDN}}$ to GND ....-0.3V to VCCI + 0.3V
REFO to GND ....-0.3V to VCCI + 0.3V

Op Amps

OP1O, OP2O, OP3O to GND ....-0.3V to VCCI + 0.3V
OP1P, OP1N, OP2P, OP2N, OP3P,
OP3N to GND......................-0.3V to min [4.5V, VCCI + 0.3V]
Current into OP1P, OP1N, OP2P, OP2N,
OP3P, OP3N...±20mA
Current into OP3O...±30mA
Output Short-Circuit Duration for OP1 and
OP2 to VCCI or GND ....Continuous

Comparators

COMP1P, COMP1N, COMP2P, COMP2N
to GND..-0.3V to VCCI + 0.3V
COMP1O, COMP2O to GND ....-0.3V to VDD + 0.3V
Current into COMP1P, COMP1N,
COMP2P, COMP2N ....±20mA
Output Short-Circuit Duration to
VDD or GND...Continuous

PWM Conditioners

PWMAP, PWMBP to GND.........................-0.3V to VCCI + 0.3V
PWMAO, PWMBO to GND ....-0.3V to VCCI + 0.3V
Current into PWMAP, PWMBP.......................................±20mA
Output Short-Circuit Duration to VCCI or GND.........Continuous

Continuous Power Dissipation (T_A = +70°C,
derate 35.7mW/°C above +70°C)...........................2857.1mW
Operating Temperature Range......................... -40°C to +125°C
Functional Temperature Range
(Startup condition) .... -55°C to +125°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Soldering Temperature (reflow).....................................+260°C
Lead Temperature ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

PACKAGE CODE	T3255
Outline Number	21-0140
Land Pattern Number	90-0015
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	40.2°C/W
Junction to Case (θ_{JC})	2.0°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

Voltage Reference

V_{CCI} = +3.0V to +5.5V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE 2.5V						
STATIC						
Supply Voltage	V_{CCI}	Guaranteed by line regulation test	3.0		5.5	V
V_{CCI} Line Regulation	$\Delta V_{REF}/\Delta V_{CCI}$	3.0V ≤ V_{CCI} ≤ 5.5V		20	140	µV/V
V_{CC} Line Regulation	$\Delta V_{REF}/\Delta V_{CC}$	4.3V ≤ V_{CC} ≤ 36V, V_{CCI} = 3.3V		1.2		nV/V
Output Voltage	V_{OUT}	T_A = +25°C	2.495	2.500	2.505	V
Output Voltage Temperature Coefficient	TCV_{OUT}	C_{REF} = 2nF (Note 2)		2	10	ppm/°C
Temperature Hysteresis	ΔV_{REF}/Cycle	C_{REF} = 2nF		-140		ppm
Load Regulation	$\Delta V_{REF}/\Delta I_{OUT}$	Sourcing 0V ≤ I_{OUT} ≤ 500 µA		0.14	0.6	µV/µA
Short-Circuit Current	I_{SC}	Short to GND		3		mA
Maximum Capacitive Load	C_{REF}			2		nF
DYNAMIC						
V_{CCI} Ripple Rejection	V_{REF}/V_{CCI}	V_{CCI} = 3.3V, f = 120Hz		90		dB
V_{CC} Ripple Rejection	V_{REF}/V_{CC}	V_{CC} = 12V, V_{CC}I = 3.3V, f = 120Hz		160		dB
Turn-On Settling Time	t_R	From 90% of V_{CCI} to within 0.1% of V_{REF}, C_{REF} = 2nF		85		µs
Noise Voltage	e_{REF}	0.1Hz to 10Hz		40		$µV_{p-p}$
		10Hz to 10kHz		125		$µV_{RMS}$

Electrical Characteristics (continued)

PWM Conditioners

V_{CCI} = +3.0V to +5.5V, V_{GND} = 0V, outputs connected to 100kΩ in parallel with 10pF terminated to V_{REF}/2, input pulses have 10ns rise and fall times, PWM period = 100µs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWMA, PWMB						
STATIC						
Supply Voltage	V_{CCI}	Guaranteed by $PSRR_{VOH}$ test	3.0		5.5	V
V_{CCI} Supply Rejection Ratio of Input Threshold Voltage	$PSRR_{VTH}$	3.0V ≤ V_{CCI} ≤ 5.5V		65		dB
V_{CC} Supply Rejection Ratio of Input Threshold Voltage		4.3V ≤ V_{CC} ≤ 36V, V_{CCI} = 3.3V		150		dB
V_{CCI} Supply Rejection Ratio of Output Voltage High	$PSRR_{VOH}$	3.0V ≤ V_{CCI} ≤ 5.5V, no load	59	75		dB
V_{CC} Supply Rejection Ratio of Output Voltage High		4.3V ≤ V_{CC} ≤ 36V, V_{CCI} = 3.3V, no load		160		dB
Input Voltage Range			0		V_{CCI}	V
Input Voltage High	V_{IH}	PWMAP, PWMBP, $\overline{SHDN}$	1.4			V
Input Voltage Low	V_{IL}	PWMAP, PWMBP, $\overline{SHDN}$			0.6	V
PWMAP, PWMBP Input Threshold	V_{TH}			1.0		V
PWMAP, PWMBP Input Threshold Accuracy				1		mV
PWMAP, PWMBP Hysteresis	PWM_{HYS}			5		mV
SHDN Hysteresis	$SHDN_{HYS}$			50		mV
Input Bias Current	I_B	V_{PWMAP} = V_{PWMBP} = 0V		-1		nA
Input Capacitance	C_{IN}			2		pF
Output Voltage High	V_{OH}	V_{REF} - V_{OUT}, I_{SOURCE} = 100 µA			0.1	V
Output Voltage Low	V_{OL}	V_{OUT} – V_{GND}, I_{SINK} = 100 µA			0.1	V
Short Circuit Current	I_{SC}	PWMAO or PWMBO short to V_{REF}		-12		mA
		PWMAO or PWMBO short to GND		6		mA
Output High Level Voltage Matching		Difference between the voltage of the two PWM outputs	-2		+2	mV
Output Low Level Voltage Matching		Difference between the voltage of the two PWM outputs	-2		+2	mV
PWMAO, PWMBO Output Voltage High Drift				7		µV/°C
Linearity		From code 10 to code 245 (Note 2), Figure 1			0.01	%FSR

Electrical Characteristics (continued)

PWM Conditioners (continued)

V_{CCI} = +3.0V to +5.5V, V_{GND} = 0V, outputs connected to 100kΩ in parallel with 10pF terminated to V_{REF}/2, input pulses have 10ns rise and fall times, PWM period = 100μs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Propagation Delay Active to Shut down	t_{SHDN}	From 50% of $\overline{SHDN}$ to when PWM outputs are Hi-Z		10		μs
Propagation Delay Shut down to Active	t_{ACT}	From 50% of $\overline{SHDN}$ to when PWM outputs are active		10		μs
Minimum Input Pulse Width	I_{PW}	Single high state, guaranteed by PWM timing tests	390			ns
Driver Rise Time for PWMAO and PWMBO	R_{TA}, R_{TB}	Single 390ns pulse, 10% to 90%			7	ns
Driver Fall Time for PWMAO and PWMBO	F_{TA}, F_{TB}				6	ns
PWMAO to PWMBO Rise Time Matching		Single 390ns pulse	-4		+4	ns
PWMAO to PWMBO Fall Time Matching		Single 390ns pulse	-2		+2	ns
PWMAO to PWMBO Delay Matching		Single 390ns pulse, measured at 50% FSR of rising edges	-30		+30	ns
PWMAO and PWMBO Pulse Width Accuracy		Single 390ns pulse, pulse width difference between input and output waveforms (measured at 50% points)	-30		+30	ns
PWMAO and PWMBO Pulse Width Variation vs. Temperature		Single 390ns pulse		25		ps/°C
PWMAO and PWMBO Pulse Width Matching		Single 390ns pulse, difference between PWMAO and PWMBO pulse widths	-30		+30	ns

Electrical Characteristics (continued)

Op Amps

V_{CCI} = +3.0V to +5.5V, V_{GND} = 0V, V_{CM} = V_{OUT} = V_{CCI}/2, no resistive load, C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OP1, OP2						
STATIC						
Supply Voltage	V_{CCI}	Guaranteed by $PSRR_{VCCI}$ test	3.0		5.5	V
V_{CCI} Supply Rejection Ratio	$PSRR_{VCCI}$	3.0V ≤ V_{CCI} ≤ 5.5V	62	80		dB
V_{CC} Supply Rejection Ratio	$PSRR_{VCC}$	4.3V ≤ V_{CC} ≤ 36V, V_{CCI} = 3.3V		165		dB
Common Mode Input Voltage	V_{CMR}	Guaranteed by CMRR test V_{CCI} ≤ 4.5V	-0.1		V_{CCI} - 0.5	V
		Guaranteed by CMRR test 4.5V ≤ V_{CCI} ≤ 5.5V	-0.1		+4.0	V
Common Mode Rejection Ratio	CMRR	-0.1V ≤ V_{CM} ≤ min (4.0V, V_{CCI} - 0.5V)	56			dB
Input Offset Voltage	V_{OS}			1		mV
Input Offset Voltage Drift	ΔV_{OS}	(Note 2)			15	µV/°C
Input Bias Current	I_B	-40°C ≤ T_A ≤ +85°C (Note 2)	-15		+15	pA
		-40°C ≤ T_A ≤ +125°C (Note 2)	-125		+125	pA
Input Offset Current	I_{OS}	-40°C ≤ T_A ≤ +85°C (Note 2)	-15		+15	pA
		-40°C ≤ T_A ≤ +125°C (Note 2)	-80		+80	pA
Open-Loop Gain	AVOL	150mV ≤ V_{OUT} ≤ V_{CCI} - 150mV, R_L = 100kΩ connected to V_{CCI} / 2, -40°C ≤ T_A ≤ +85°C	78			dB
		-40°C ≤ T_A ≤ +125°C	72			
Output Voltage High	V_{OH}	V_{CCI} – V_{OUT}, R_L = 100kΩ connected to V_{CCI} / 2			25	mV
Output Voltage Low	V_{OL}	V_{OUT} - V_{GND}, R_L = 100kΩ connected to V_{CCI} / 2			25	mV
Output Short-Circuit Current	$I_{OUT(SC)}$			±3		mA

Electrical Characteristics (continued)

Op Amps (continued)

V_{CCI} = +3.0V to +5.5V, V_{GND} = 0V, V_{CM} = V_{OUT} = V_{CCI}/2, no resistive load, C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Input Voltage Noise Density	eN	f = 1kHz		150		nV/√Hz
Input Current Noise Density	iN	f = 1kHz		40		fA/√Hz
Gain Bandwith Product	GBWP			200		kHz
Slew Rate	SR			0.1		V/ µs
Settling Time		To 0.1%, V_{OUT} = 2V step, A_V = -1V/V		25		µs
Maximum Capacitive Load	C_L	No sustained oscillations, A_V = 1V/V		100		pF
OP3 (R_L = 100kΩ CONNECTED to V_{CCI}/2, C_L = 20pF)						
STATIC						
Supply Voltage	V_{CCI}	Guaranteed by $PSRR_{VCCI}$ test	3.0		5.5	V
V_{CCI} Supply Rejection Ratio	$PSRR_{VCCI}$	3.0V ≤ V_{CCI} ≤ 5.5V	107			dB
V_{CC} Supply Rejection Ratio	$PSRR_{VCC}$	4.3V ≤ V_{CC} ≤ 36V, V_{CCI} = 3.3V		195		dB
Common Mode Input Voltage	V_{CMR}	Guaranteed by CMRR test V_{CCI} ≤ 4.3V	-0.1		V_{CCI} - 0.3	V
		Guaranteed by CMRR test 4.3V □ V_{CCI} ≤ 5.5V	-0.1		+4.0	V
Common Mode Rejection Ratio	CMRR	-0.1V ≤ V_{CM} ≤ min(4.0V, V_{CCI} - 0.3V)	105			dB
Input Offset Voltage	V_{OS}	T_A = 25°C, V_{CCI} = 3.3V (Note 2)	-10		+10	µV
Input Offset Voltage Drift	ΔV_{OS}	(Note 2)		5	70	nV/°C
Input Bias Current	I_B	-40°C ≤ T_A ≤ +85°C (Note 2)	-15		+15	pA
		-40°C ≤ T_A ≤ +125°C (Note 2)	-125		+125	pA
Input Offset Current	I_{OS}			-40		pA
Input Capacitance	C_{IN}			2		pF
Open-Loop Gain	AVOL	150mV ≤ V_{OUT} ≤ VCCI-150mV, R_L = 5kΩ connected to V_{CCI} / 2	123	150		dB
Output Voltage High	V_{OH}	V_{CCI} – V_{OUT}, R_L = 100kΩ connected to V_{CCI} / 2			12	mV
Output Voltage Low	V_{OL}	V_{OUT} - V_{GND}, R_L = 100kΩ connected to V_{CCI} / 2			12	mV

Electrical Characteristics (continued)

Op Amps (continued)

V_{CCI} = +3.0V to +5.5V, V_{GND} = 0V, V_{CM} = V_{OUT} = V_{CCI}/2, no resistive load, C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Input Voltage Noise Density	eN	f = 1kHz		35		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz		0.7		µVp-p
Input Current Noise Density	iN	f = 1kHz		80		fA/√Hz
Gain Bandwidth Product	GBWP			2.2		MHz
Slew Rate	SR			0.7		V/µs
Phase Margin				57		°
Maximum Capacitive Load	C_L	No sustained oscillations, A_V = 1V/V		300		pF

Electrical Characteristics (continued)

Comparators

V_{CCI} = +3.0V to +5.5V, V_{DD} = +1.8V to +3.6V, V_{GND} = 0V, V_{CM} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{DD} = V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMP1, COMP2						
STATIC						
Supply Voltage	V_{CCI}	Guaranteed by $PSRR_{VCCI}$ test	3.0		5.5	V
Supply Voltage Output Stage	V_{DD}		1.8		3.6	V
V_{CCI} Supply Rejection Ratio	$PSRR_{VCCI}$	3.0V ≤ V_{CCI} ≤ 5.5V	54			dB
V_{CC} Supply Rejection Ratio	$PSRR_{VCC}$	4.3V ≤ V_{CC} ≤ 36V, V_{CCI} = 3.3V		160		dB
Common Mode Input Voltage	V_{CMR}	Guaranteed by CMRR test	0		V_{CCI} - 1.3	V
Common Mode Rejection Ratio	CMRR	0V ≤ V_{CM} ≤ V_{CCI} – 1.3V	56	75		dB
Input Offset Voltage	V_{OS}		-10		+10	mV
Hysteresis	V_{HYS}			15		mV
Input Bias Current	I_B	V_{CM} = 0V	-10	-1		nA
Input Offset Current	I_{OS}			1		nA
Input Capacitance	C_{IN}			2		pF
Output Voltage High	V_{OH}	V_{DD} - V_{OUT}, I_{SOURCE} = 100 µA			0.4	V

Electrical Characteristics (continued)

Comparators (continued)

V_{CCI} = +3.0V to +5.5V, V_{DD} = +1.8V to +3.6V, V_{GND} = 0V, V_{CM} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{DD} = V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Low	V_{OL}	V_{OUT} – V_{GND}, I_{SINK} = 100 µA			0.4	V
Short Circuit Current	I_{SC}	Short to GND		2		mA
		Short to V_{DD}		-2		mA
DYNAMIC						
Propagation Delay Low to High	t_{PD+}	C_{LOAD} = 10pF, threshold set to V_{CCI} -1.4V, input swings from 0V to V_{CCI} -1.3V		2		µs
Propagation Delay High to Low	t_{PD-}	C_{LOAD} = 10pF, threshold set to 0.1V, input swings from V_{CCI} -1.3V to 0V		0.5		µs
Rise Time	T_R	C_{LOAD}= 10pF		50		ns
Fall Time	T_F	C_{LOAD}= 10pF		50		ns

LDO

V_{CC} = +4.0V to +36V, V_{GND} = 0V, C_{LOAD} = 0.32µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = +24V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO						
STATIC						
Supply Voltage	V_{CC}	Guaranteed by line regulation test	4.0	24	36	V
Dropout Voltage		Guaranteed by line and load regulation tests	1			V
V_{CC} Line Regulation		V_{CC} from V_{CCI}+1V to 36V, I_{LDO} = 4mA, V_{CCI} = 3.0V to 5.5V		2	25	mV
Output Voltage	V_{CCI}	Guaranteed by block $PSRR_{VCCI}$ tests	3.0		5.5	V
Output Voltage Accuracy		V_{CC} = 24V, no load except for LDOFB resistor divider, V_{CCI} = 3.3V	-3.5		+3.5	%
Output Current Range	I_{LDO}	Guaranteed by load regulation test	0		4	mA
V_{CCI} Current Limit	I_{CCI_Limit}	V_{CCI} short to GND		12		mA
Load Regulation		V_{CC} = V_{CCI}+1V, I_{LDO} from 0mA to 4mA, V_{CCI} = 3.0V to 5.5V		1	10	mV
Maximum Capacitive Load	C_{LOAD}	No resistive load except for LDOFB resistor divider		5		µF
DYNAMIC						
V_{CC} Supply Rejection Ratio	PSRR	V_{CC} = 12V, DC to 120Hz		70		dB

Electrical Characteristics (continued)

Chip-Level Specifications

V_{CC} = +4.0V to +36V, V_{CCI} = +3.0V to +5.5V, V_{DD} = +1.8V to +3.6V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = +24V, V_{DD} = V_{CCI} = +3.3V. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC						
V_{CC} Supply Current	I_{CC}	V_{CC} = 24V, V_{CCI} = 3.3V, $\overline{SHDN}$ = 3.3V, no load, -40°C ≤ T_A ≤ +85°C		170	250	μA
		-40°C ≤ T_A ≤ +125°C			265	μA
V_{CC} Supply Current with PWM Conditioners Shutdown	I_{CC_SHDN}	V_{CC} = 24V, V_{CCI} = 3.3V, $\overline{SHDN}$ = 0V, no load		142		μA
V_{DD} Supply Current	I_{DD}				1	μA
PWRGOOD Turn-on Threshold				90		% of V_{CCI}
PWRGOOD Turn-off Threshold				80		% of V_{CCI}
PWRGOOD Voltage High	V_{OH}	V_{CCI} – V_{OUT}, I_{SOURCE} = 100 μA			0.4	V
PWRGOOD Voltage Low	V_{OL}	V_{OUT} – V_{GND}, I_{SINK} = 100 μA			0.4	V
PWRGOOD Short Circuit Current	I_{SC}	Short to GND		2		mA
		Short to V_{CCI}		-2		mA
DYNAMIC						
PWRGOOD Turn-on Delay		From V_{CCI} crossing turn-on threshold to PWRGOOD high		0.7		ms

Note 1: Specifications are 100% tested at T_A = +25°C (exceptions noted). All temperature limits are guaranteed by design.
Note 2: Guaranteed by design, not production tested.

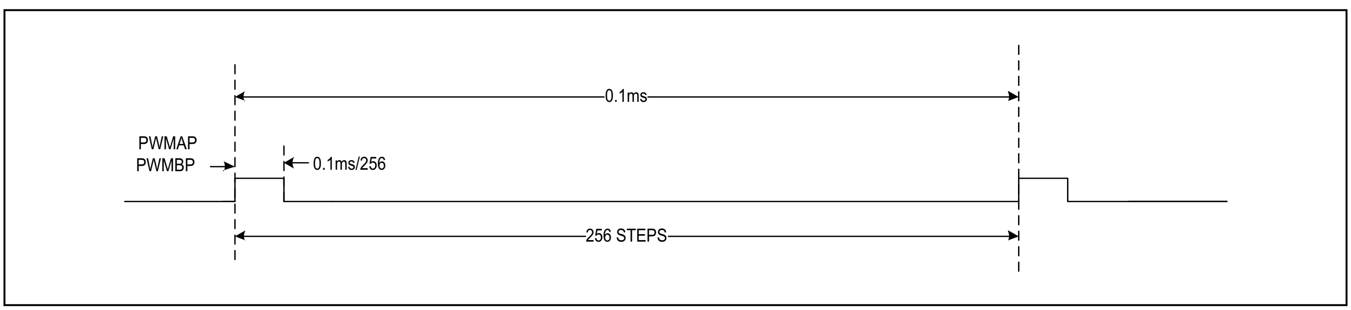
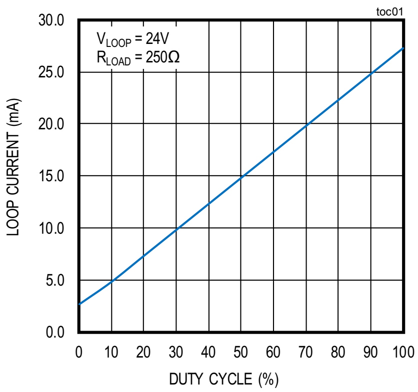


Figure 1. Typical PWM Timing Diagram

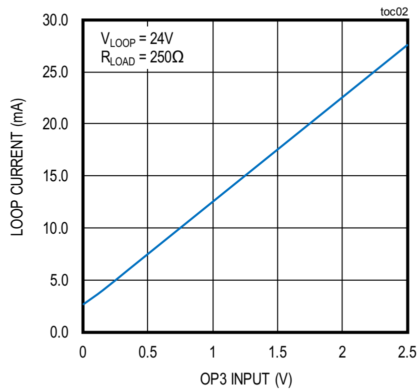
Typical Operating Characteristics

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = $V_{CCI}/2$, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

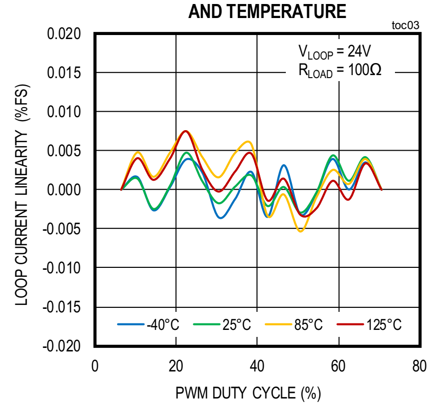
TRANSFER CHARACTERISTICS
LOOP CURRENT vs. PWM DUTY CYCLE



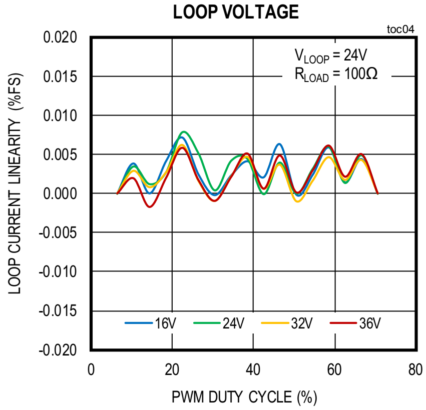
TRANSFER CHARACTERISTICS
LOOP CURRENT vs. OP3 INPUT



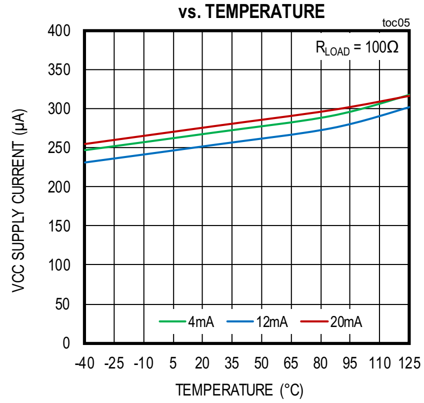
4mA–20mA LINEARITY vs.
PWM DUTY CYCLE
AND TEMPERATURE



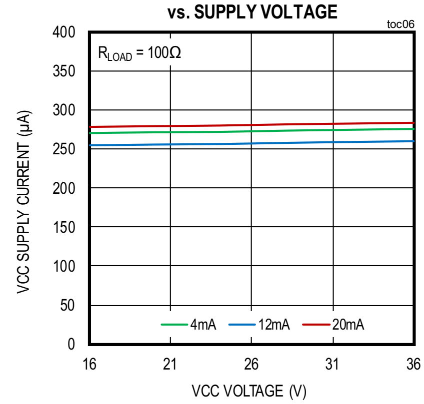
4-20mA LINEARITY vs.
PWM DUTY CYCLE AND
LOOP VOLTAGE



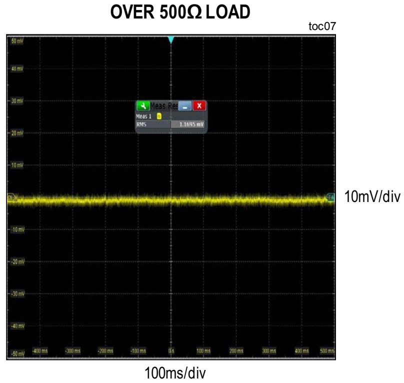
VCC SUPPLY CURRENT
(SYSTEM LEVEL)
vs. TEMPERATURE



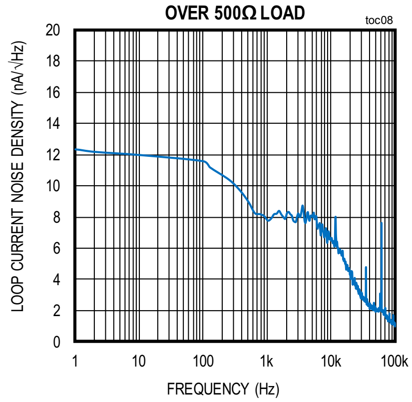
VCC SUPPLY CURRENT
vs. SUPPLY VOLTAGE



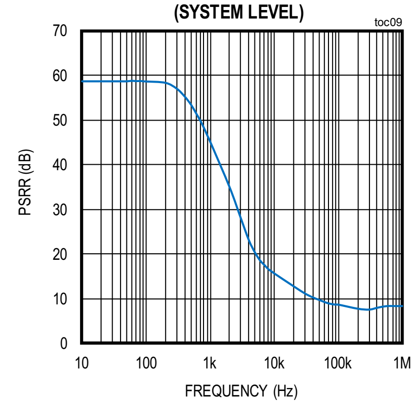
4mA LOOP CURRENT NOISE
DURING SILENCE
OVER 500Ω LOAD



4mA LOOP CURRENT NOISE
DENSITY vs. FREQUENCY
OVER 500Ω LOAD



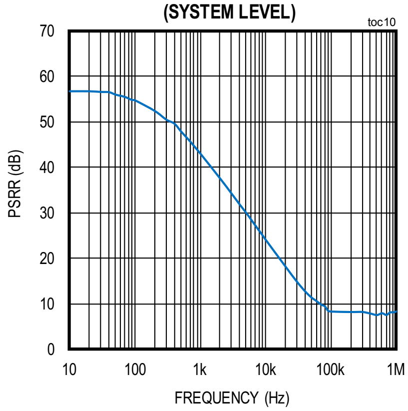
VCC SUPPLY REJECTION
RATIO vs. FREQUENCY
(SYSTEM LEVEL)



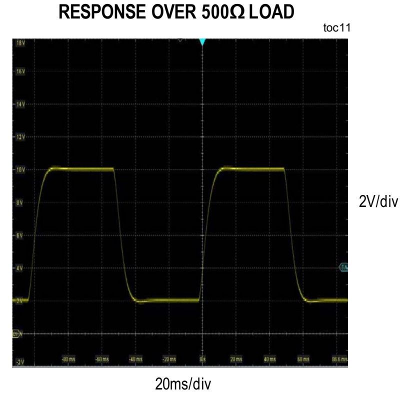
Typical Operating Characteristics (continued)

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = V_{CCI}/2, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

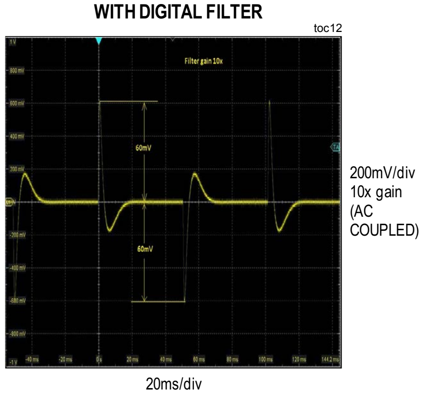
LOOP SUPPLY REJECTION RATIO vs. FREQUENCY (SYSTEM LEVEL)



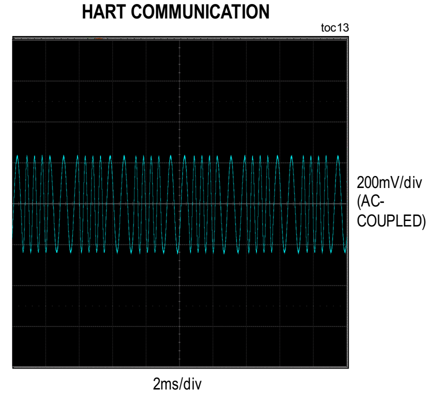
4mA–20mA STEP TRANSIENT RESPONSE OVER 500Ω LOAD



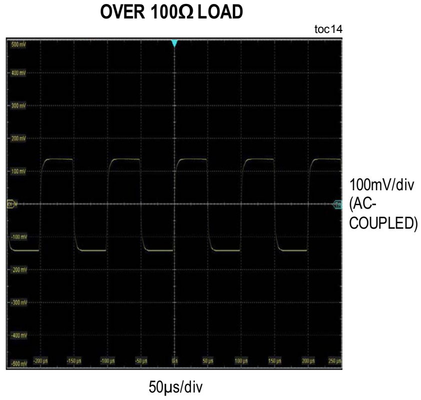
ANALOG RATE OF CHANGE OVER 500Ω LOAD WITH DIGITAL FILTER



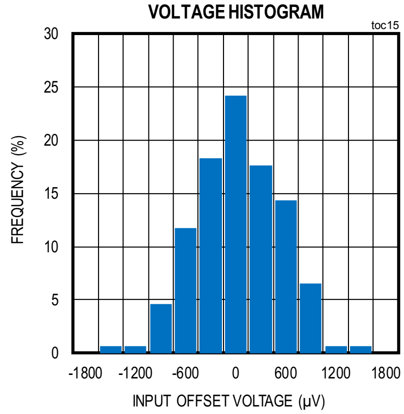
HART COMMUNICATION



10kHZ SQUARE WAVE OVER 100Ω LOAD



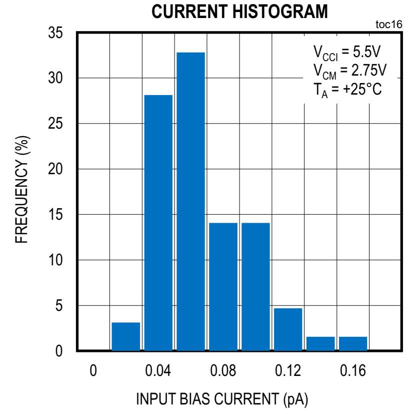
OP1/OP2 INPUT OFFSET VOLTAGE HISTOGRAM



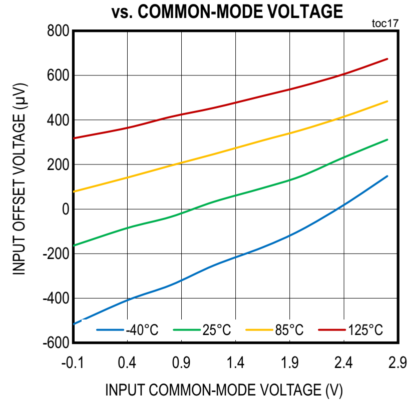
Typical Operating Characteristics (continued)

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = V_{CCI}/2, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

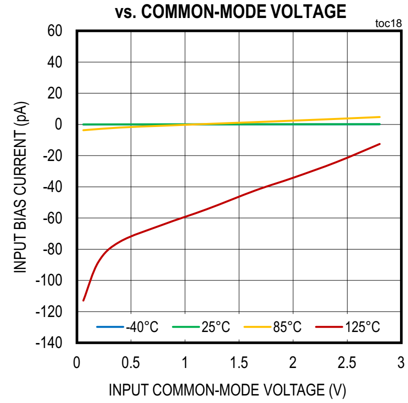
OP1/OP2 INPUT BIAS CURRENT HISTOGRAM



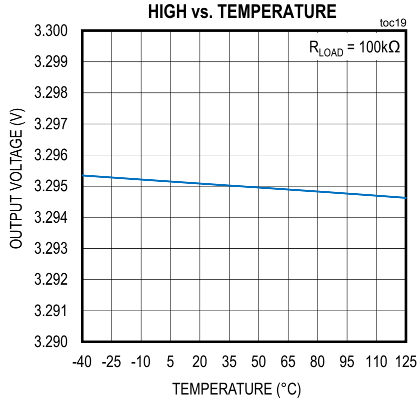
OP1/OP2 INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



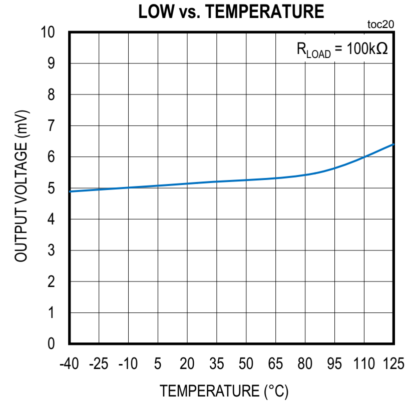
OP1/OP2 INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



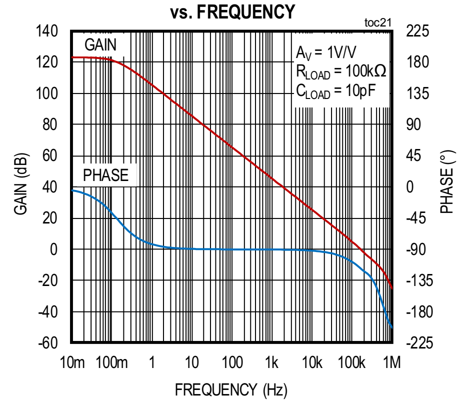
OP1/OP2 OUTPUT VOLTAGE HIGH vs. TEMPERATURE



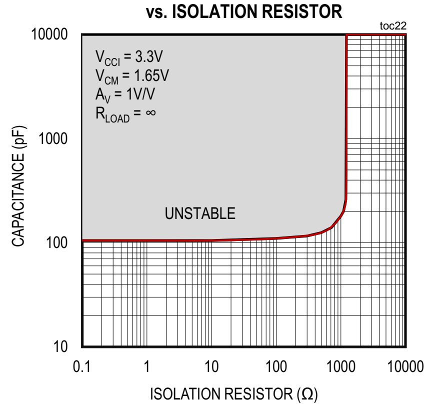
OP1/OP2 OUTPUT VOLTAGE LOW vs. TEMPERATURE



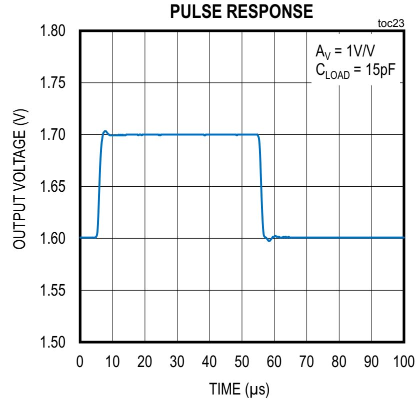
OP1/OP2 GAIN AND PHASE vs. FREQUENCY



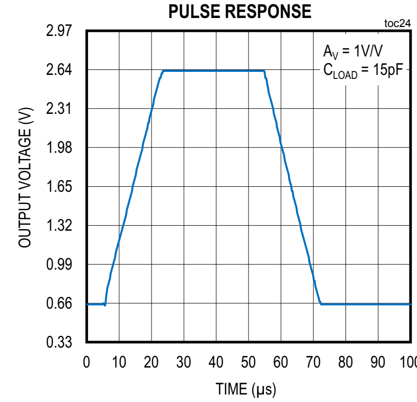
OP1/OP2 CAPACITIVE LOAD vs. ISOLATION RESISTOR



OP1/OP2 SMALL-SIGNAL PULSE RESPONSE



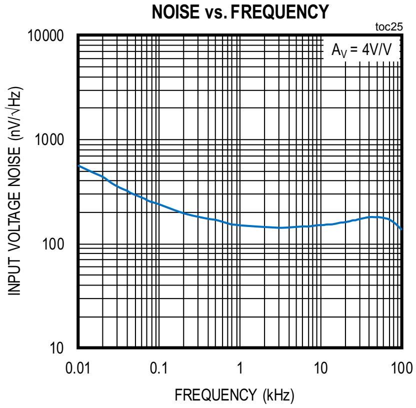
OP1/OP2 LARGE-SIGNAL PULSE RESPONSE



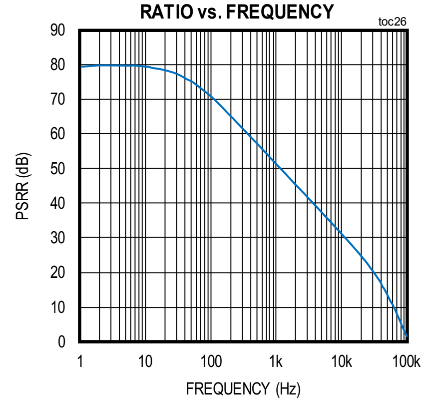
Typical Operating Characteristics (continued)

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = $V_{CCI}/2$, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

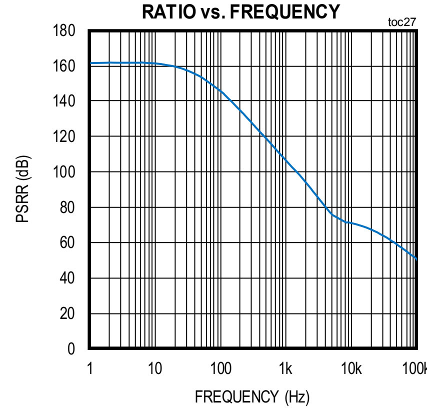
OP1/OP2 INPUT VOLTAGE NOISE vs. FREQUENCY



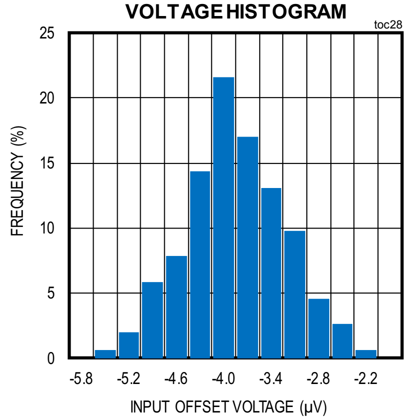
OP1/OP2 VCCI SUPPLY REJECTION RATIO vs. FREQUENCY



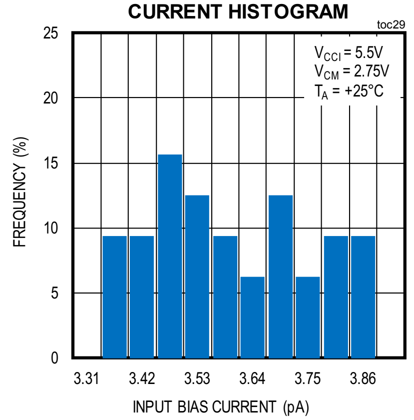
OP1/OP2 VCC SUPPLY REJECTION RATIO vs. FREQUENCY



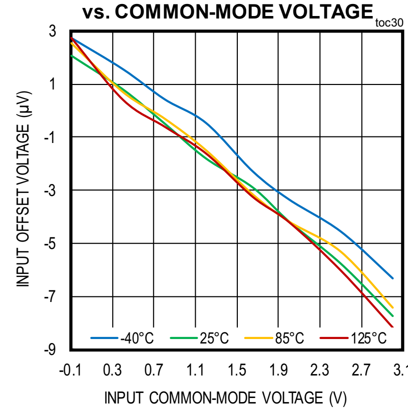
OP3 INPUT OFFSET VOLTAGE HISTOGRAM



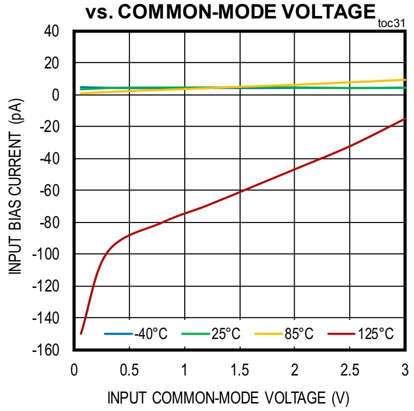
OP3 INPUT BIAS CURRENT HISTOGRAM



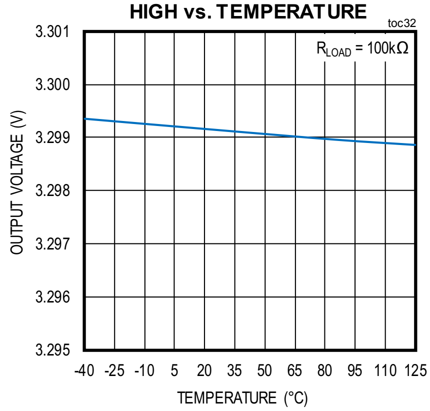
OP3 INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



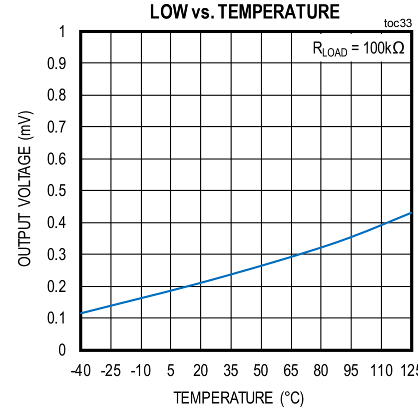
OP3 INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



OP3 OUTPUT VOLTAGE HIGH vs. TEMPERATURE



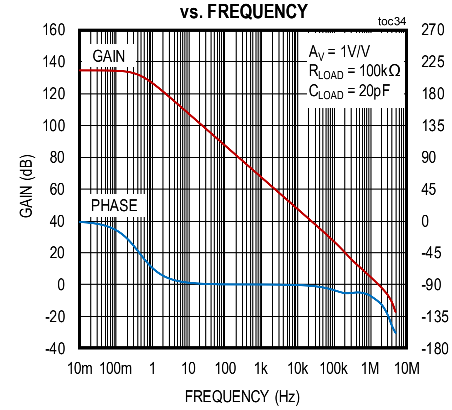
OP1/OP2 OUTPUT VOLTAGE LOW vs. TEMPERATURE



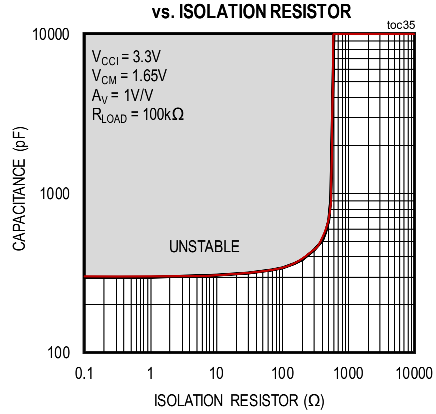
Typical Operating Characteristics (continued)

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = V_{CCI}/2, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

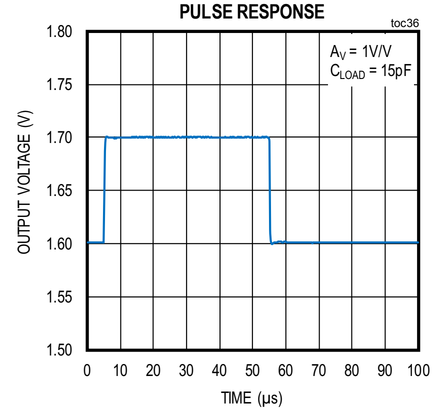
OP3 GAIN AND PHASE
vs. FREQUENCY



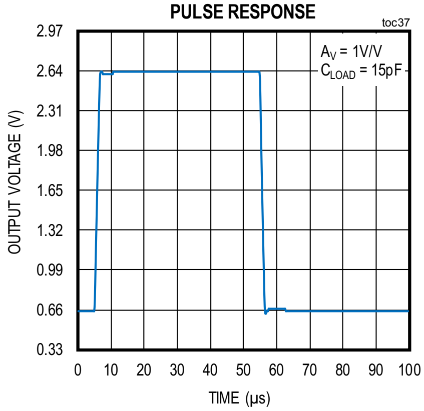
OP3 CAPACITIVE LOAD
vs. ISOLATION RESISTOR



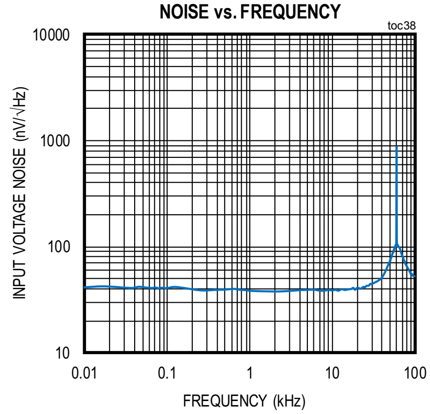
OP3 SMALL-SIGNAL
PULSE RESPONSE



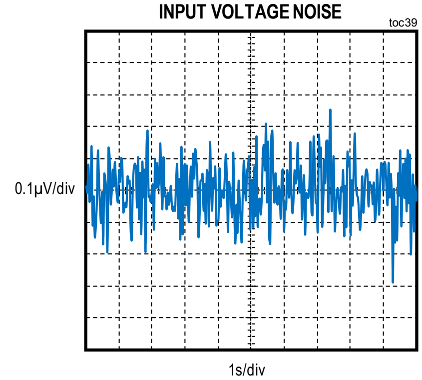
OP3 LARGE-SIGNAL
PULSE RESPONSE



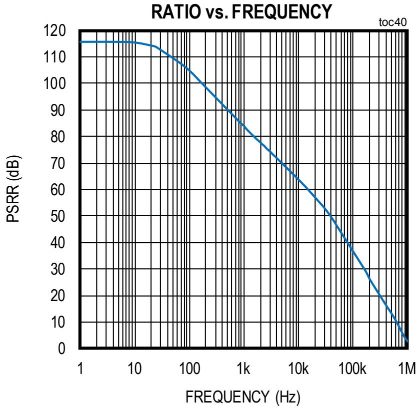
OP3 INPUT VOLTAGE
NOISE vs. FREQUENCY



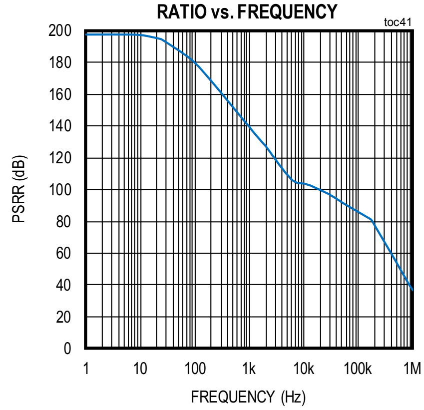
OP3 0.1Hz TO 10Hz
INPUT VOLTAGE NOISE



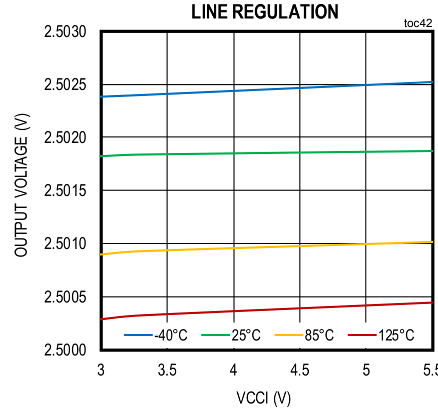
OP3 VCCI SUPPLY REJECTION
RATIO vs. FREQUENCY



OP3 VCC SUPPLY REJECTION
RATIO vs. FREQUENCY



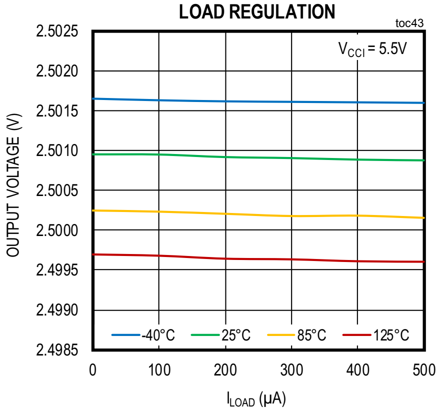
VOLTAGE REFERENCE
LINE REGULATION



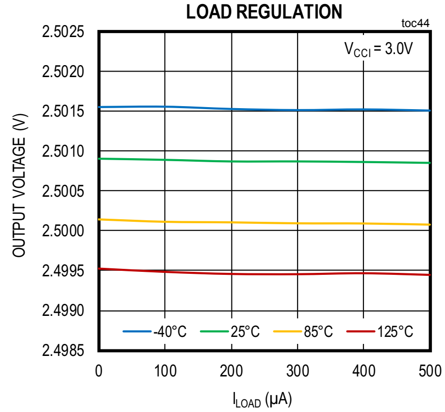
Typical Operating Characteristics (continued)

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = V_{CCI}/2, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

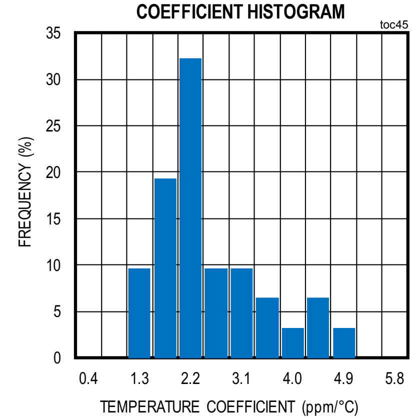
VOLTAGE REFERENCE LOAD REGULATION



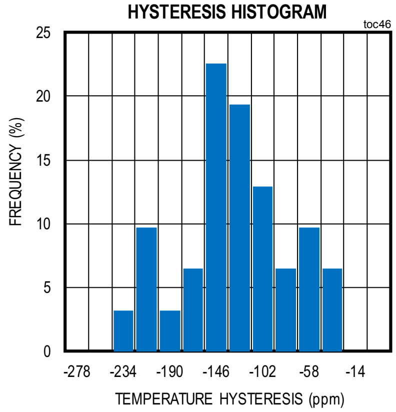
VOLTAGE REFERENCE LOAD REGULATION



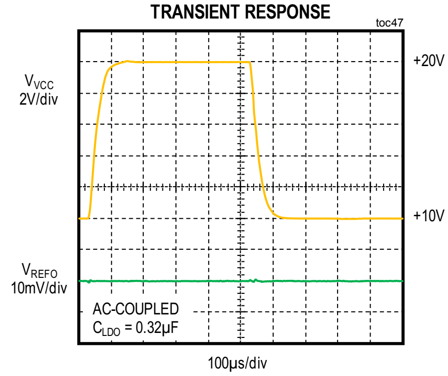
VOLTAGE REFERENCE TEMPERATURE COEFFICIENT HISTOGRAM



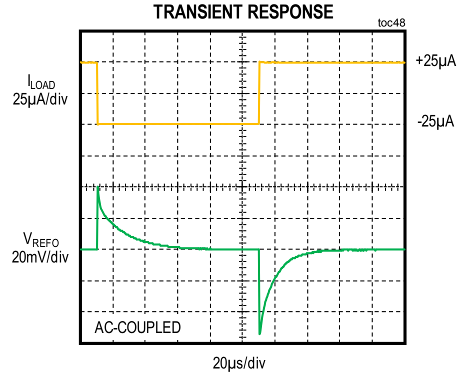
VOLTAGE REFERENCE TEMPERATURE HYSTERESIS HISTOGRAM



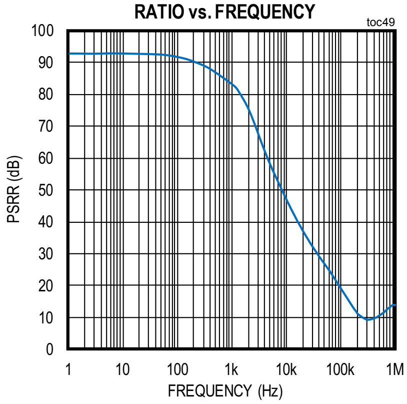
VOLTAGE REFERENCE LINE TRANSIENT RESPONSE



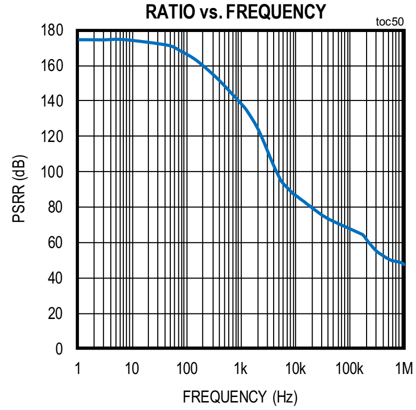
VOLTAGE REFERENCE LOAD TRANSIENT RESPONSE



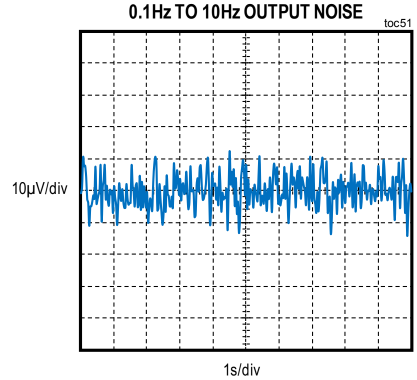
VOLTAGE REFERENCE VCCI REJECTION RATIO vs. FREQUENCY



VOLTAGE REFERENCE VCC REJECTION RATIO vs. FREQUENCY

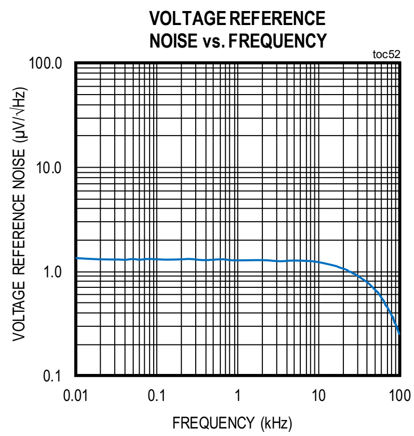


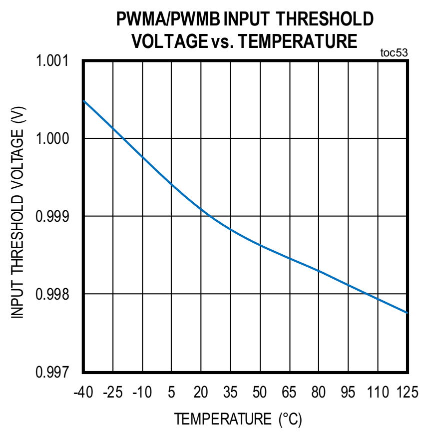
VOLTAGE REFERENCE 0.1Hz TO 10Hz OUTPUT NOISE

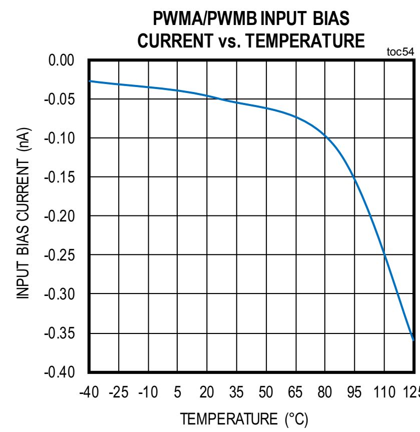


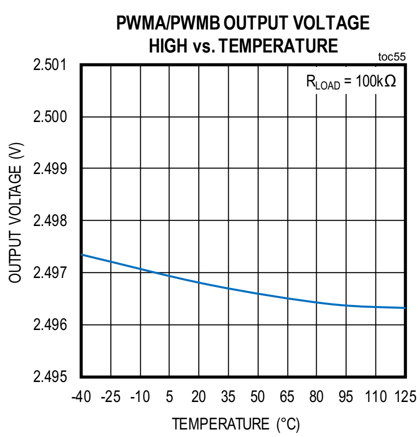
Typical Operating Characteristics (continued)

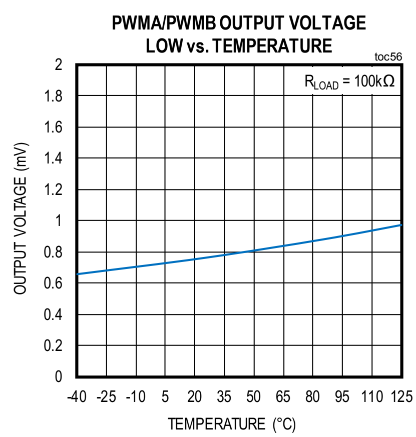
V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = $V_{CCI}/2$, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

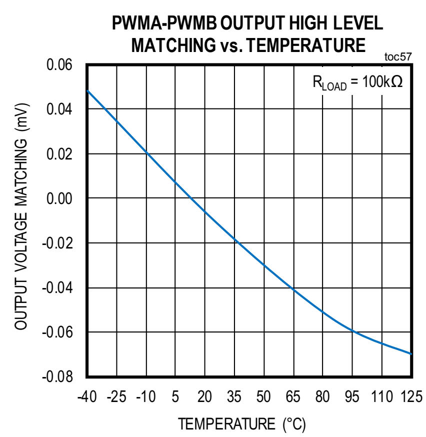


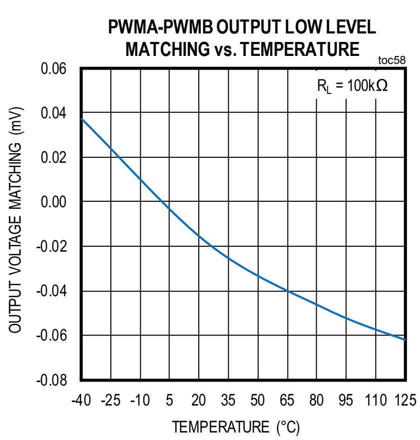


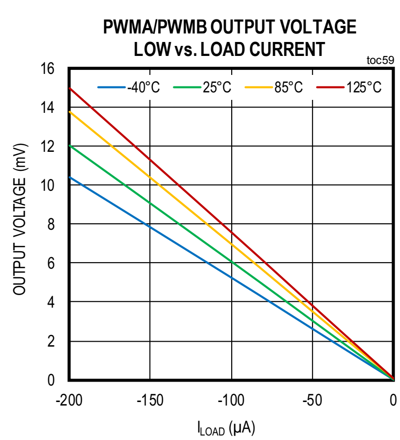


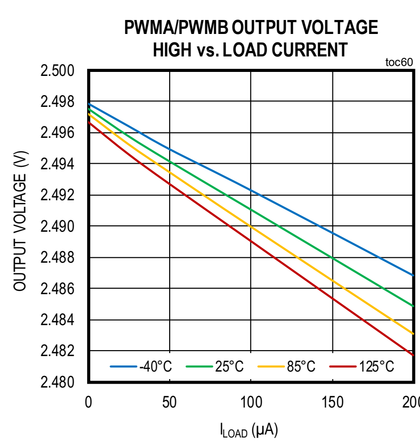








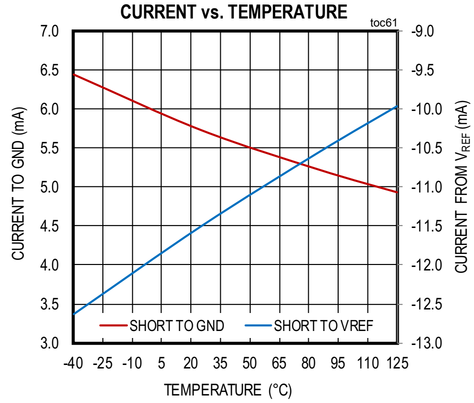




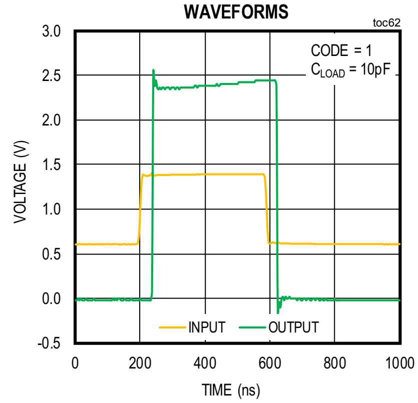
Typical Operating Characteristics (continued)

V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = $V_{CCI}/2$, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

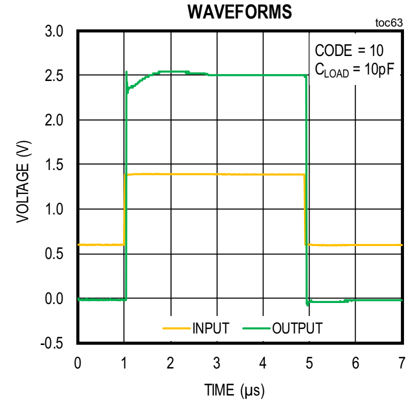
PWMA/PWMB SHORT-CIRCUIT CURRENT vs. TEMPERATURE



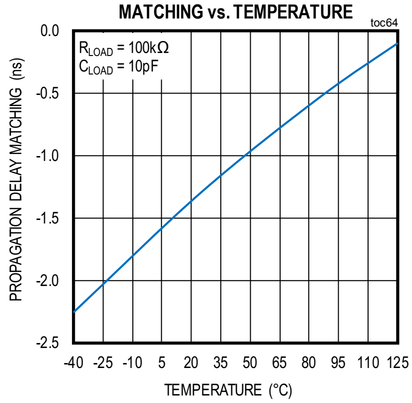
PWMA/PWMB INPUT/OUTPUT WAVEFORMS



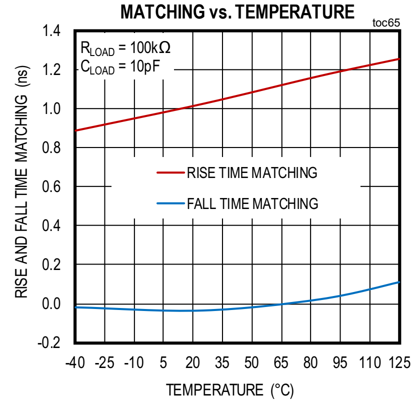
PWMA/PWMB INPUT/OUTPUT WAVEFORMS



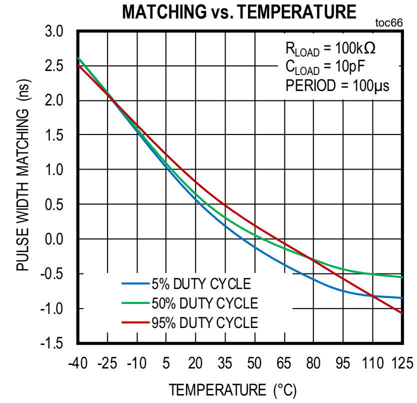
PWMA-PWMB PROPAGATION DELAY MATCHING vs. TEMPERATURE



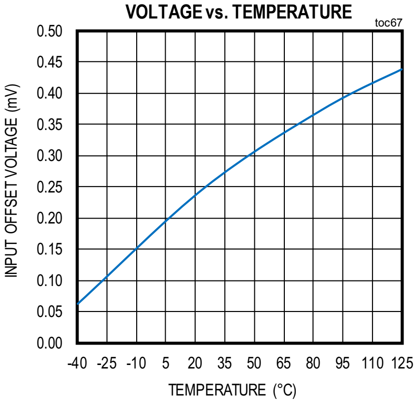
PWMA-PWMB RISE AND FALL TIME MATCHING vs. TEMPERATURE



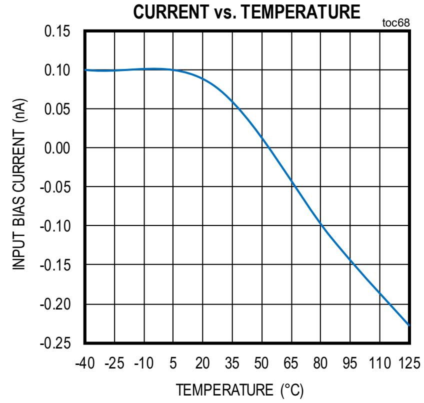
PWMA-PWMB PULSE WIDTH MATCHING vs. TEMPERATURE



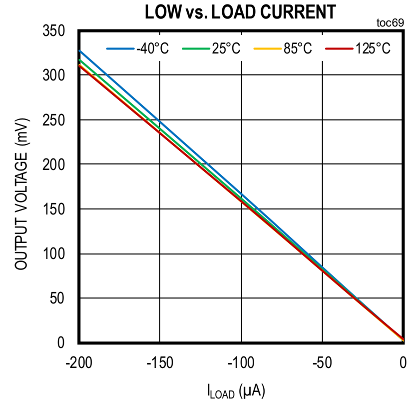
COMP1/COMP2 INPUT OFFSET VOLTAGE vs. TEMPERATURE



COMP1/COMP2 INPUT BIAS CURRENT vs. TEMPERATURE

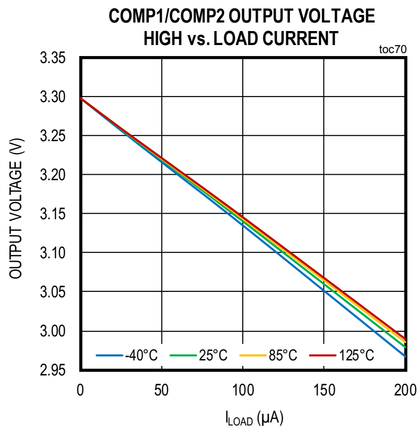


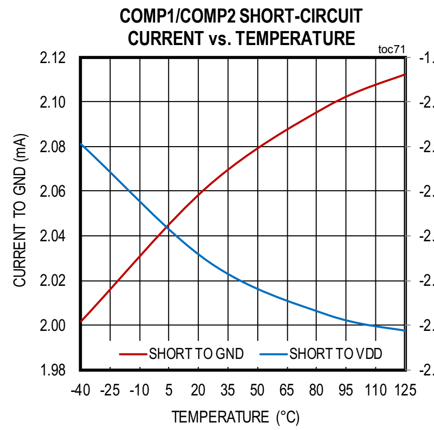
COMP1/COMP2 OUTPUT VOLTAGE LOW vs. LOAD CURRENT

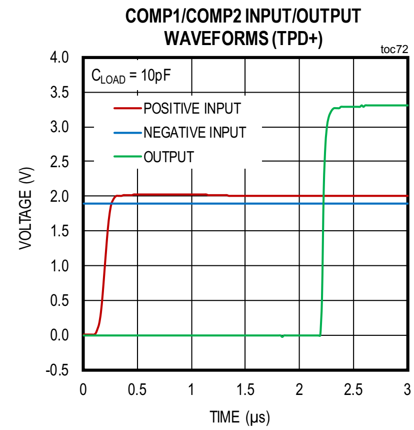


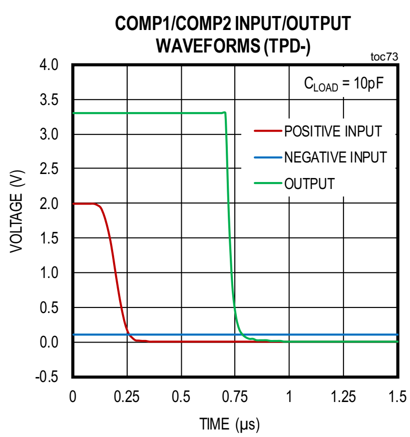
Typical Operating Characteristics (continued)

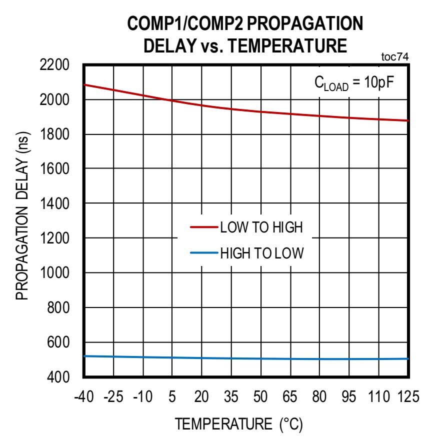
V_{CC} = +24V, V_{DD} = V_{CCID} = V_{CCI} = +3.3V, GND = 0V, op amp V_{CM} = V_{OUT} = V_{CCI}/2, op amp C_L = 15pF, comparator and PWM C_L = 10pF, LDO C_{LOAD} = 0.32µF, no resistive load on any output, T_A = +25°C, unless otherwise noted.

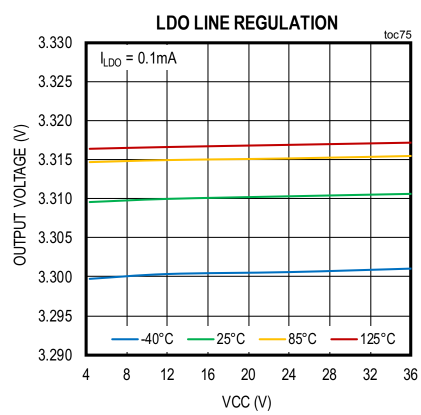


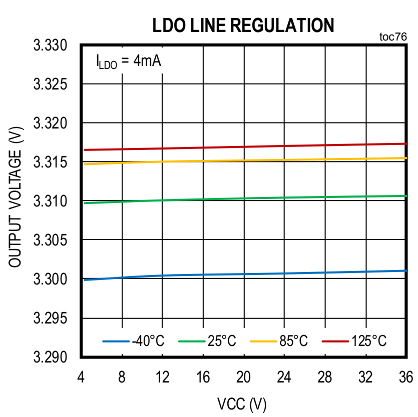


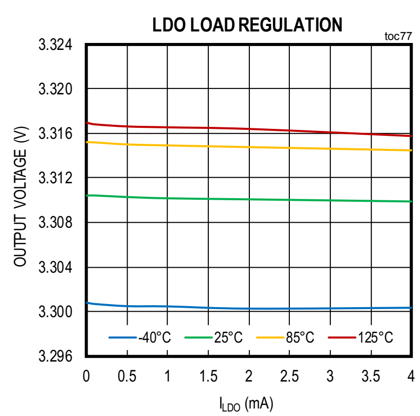


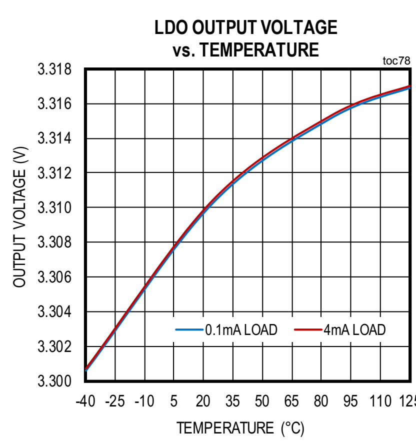












Typical Operating Characteristics (continued)

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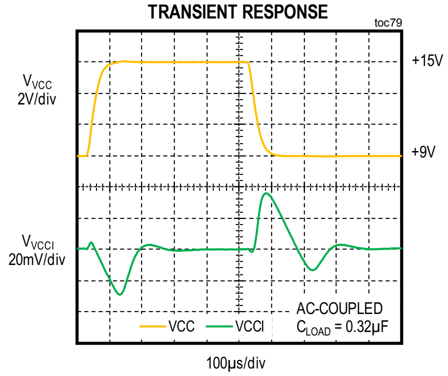
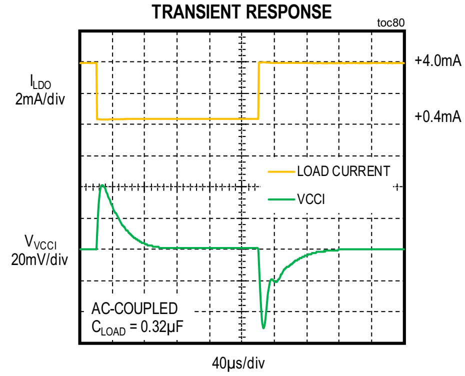
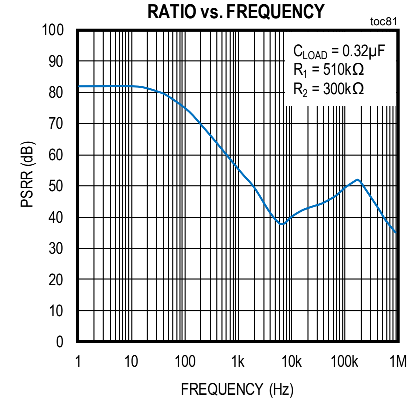
LDO LINE TRANSIENT RESPONSE



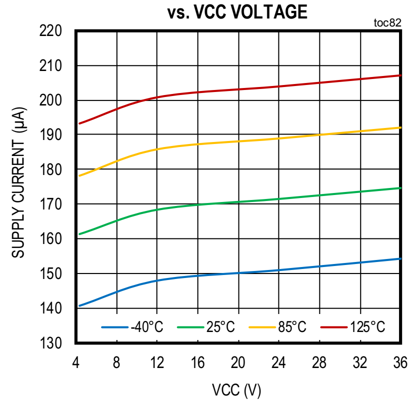
LDO LOAD TRANSIENT RESPONSE



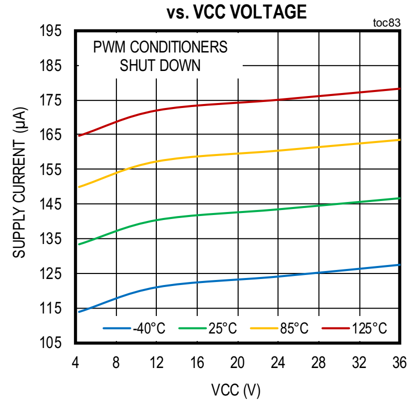
LDO VCC SUPPLY REJECTION RATIO vs. FREQUENCY



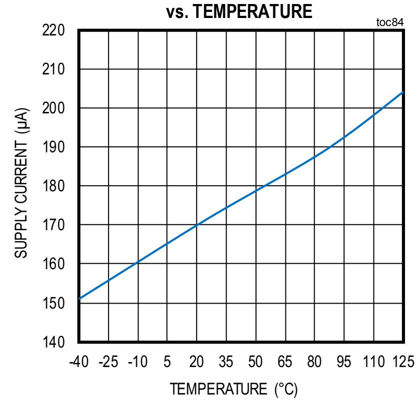
QUIESCENT CURRENT vs. VCC VOLTAGE



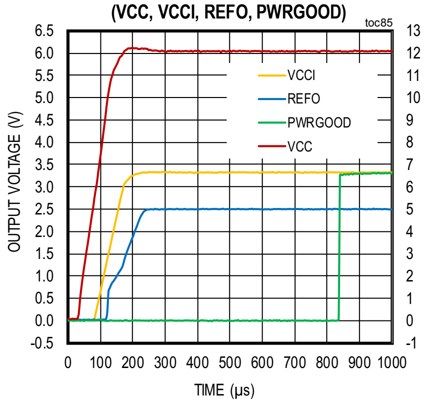
QUIESCENT CURRENT vs. VCC VOLTAGE



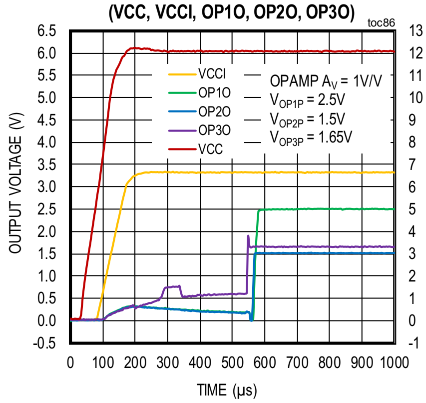
QUIESCENT CURRENT vs. TEMPERATURE



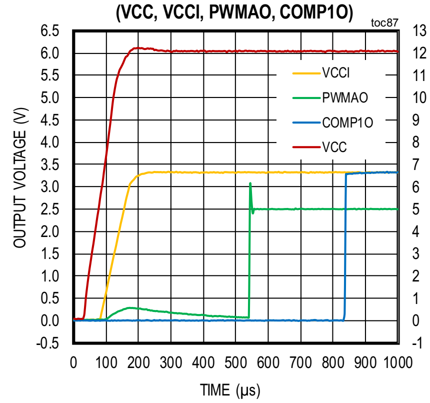
POWER-UP WAVEFORMS (VCC, VCCI, REFO, PWRGOOD)



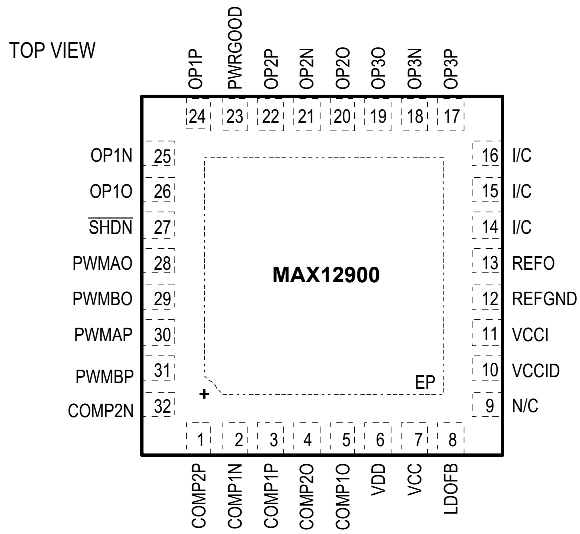
POWER-UP WAVEFORMS (VCC, VCCI, OP1O, OP2O, OP3O)



POWER-UP WAVEFORMS (VCC, VCCI, PWMAO, COMP1O)



Pin Configuration



Pin Description

PIN #	NAME	DESCRIPTION
1	COMP2P	Comparator 2 noninverting input
2	COMP1N	Comparator 1 inverting input
3	COMP1P	Comparator 1 noninverting input
4	COMP2O	Comparator 2 output
5	COMP1O	Comparator 1 output
6	VDD	Comparator Output Supply Voltage. Add a 0.1μF bypass cap from VDD to GND.
7	VCC	Positive Supply Voltage at Internal LDO Input. Add a 1μF bypass cap from VCC to GND.
8	LDOFB	LDO feedback voltage. Connect to resistor divider between VCCI and GND.
9	N/C	Not connected
10	VCCID	Digital power input. Connect this pin to VCCI.
11	VCCI	LDO output. Add a 0.22μF bypass cap from VCCI to GND.
12	REFGND	Internal reference ground. Connect to GND.
13	REFO	Internal reference output.
14	I/C	Internally connected pin. Connect this pin to GND.
15	I/C	Internally connected pin. Connect this pin to GND.
16	I/C	Internally connected pin. Connect this pin to GND.
17	OP3P	Op Amp 3 noninverting input
18	OP3N	Op Amp 3 inverting input
19	OP3O	Op Amp 3 output
20	OP2O	Op Amp 2 output

Pin Description (continued)

PIN #	NAME	DESCRIPTION
21	OP2N	Op Amp 2 inverting input
22	OP2P	Op Amp 2 noninverting input
23	PWRGOOD	Active-high output signal that indicates when the MAX12900 is ready.
24	OP1P	Op Amp 1 non-inverting input
25	OP1N	Op Amp 1 inverting input
26	OP1O	Op Amp1 output
27	$\overline{\text{SHDN}}$	Active-Low, Shutdown Input for PWM Conditioners. PWM circuitry powers down and outputs go to Hi-Z state when this pin is low.
28	PWMAO	PWM conditioner output A
29	PWMBO	PWM conditioner output B
30	PWMAP	PWM conditioner input A
31	PWMBP	PWM conditioner input B
32	COMP2N	Comparator 2 inverting input
EP	GND	Exposed pad, chip ground.

Detailed Description

The MAX12900 is an ultra-low-power, highly integrated AFE for a 4mA–20mA transmitter. The MAX12900 integrates ten building blocks in a small package: a wide supply voltage range LDO, two comparators for PWM conditioning (PWMA and PWMB), two low-drift, general purpose op amps (OP1 and OP2), one zero-drift, wide-bandwidth op amp (OP3), two diagnostic comparators (COMP1 and COMP2), a power-up sequencer with power good output, and a low-drift voltage reference. There are many ways that one can connect these building blocks to optimize overall functionality and performance of the MAX12900 for a specific application.

Power-Up Sequencer

The power-up sequencer keeps all op amp and PWM outputs at Hi-Z, and outputs of the comparators low during power-up until VCCI reaches 90% of its final value. After that, the PWRGOOD signal is asserted and all outputs become controlled by their inputs. The PWRGOOD signal is delayed by 0.7ms (typ) after VCCI reaches 90% of its final value, thus allowing for external loops controlled by the MAX12900 to stabilize before signaling that the part is ready.

Note that external components, such as a sensor or microcontroller, should not draw load current from VCCI until the PWRGOOD signal has been asserted.

PWM Conditioners

The PWM conditioners generate ground level when the input is below the threshold voltage, and generate V_{REF} when the input is above the threshold voltage. The PWM conditioners can be powered down by setting the $\overline{\text{SHDN}}$ pin low. The PWM outputs are Hi-Z during shutdown.

General Purpose Op Amps (OP1, OP2)

The general purpose op amps, OP1 and OP2, feature a low operating supply voltage, low input bias current, rail-to-rail outputs, and a maximized ratio of Gain Bandwidth Product (GBWP) to supply current. These CMOS devices feature ultra-low input bias current up to 15pA at 85°C. They are unity-gain stable with a 200 kHz GBWP, driving capacitive loads up to 100pF. The input common mode voltage range can extend 100mV below ground with excellent common-mode rejection. The OP1 and OP2 op amps can drive the output to within 25mV of both supply rails with a 100kΩ load. Op amp settling time depends primarily on the output voltage and is slew-rate limited.

The general-purpose op amps can be used as PWM filters, linear filters/amplifiers, or as linear or shunt regulator controllers, refer to the Application Information section.

Zero-Drift High Bandwidth Op Amp (OP3)

The zero-drift, wide bandwidth op amp OP3 uses an innovative auto-zero technique that allows precision and low noise with a minimum amount of power. The ultra-low input offset voltage, offset drift, and 1/f noise allow for building a highly accurate current transmitter. The high GBWP allows for noise suppression over a wider frequency band. The OP3 amplifier achieves rail-to-rail performance at the output.

Driving large capacitive loads can cause instability in many op amps. The OP3 amplifier is stable with capacitive loads up to 300pF. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op amp output.

Low-Drift 2.5V Voltage Reference

The precision bandgap reference uses a proprietary curvature-correction circuit and laser-trimmed thin-film resistors, resulting in a low temperature coefficient of <10ppm/°C, and initial accuracy of better than 0.2%. The reference can sink and source up to 500µA, making it attractive for use in low-voltage applications. It is stable for capacitive loads up to 2nF. In applications where the load can experience step changes, an output capacitor will reduce the amount of overshoot (or undershoot) and assist the circuit's transient response. The reference typically turns on and settles to within 0.1% of its final value in 220µs.

General-Purpose Comparators

The comparators COMP1 and COMP2 feature a 2µs propagation delay. Two independent rails supply each comparator. The input stage operates with V_{CCI} from 3.0V to 5.5V, and the output drivers operate with VDD from 1.8V to 3.6V. This allows for a direct connection to a microcontroller. The internal output driver allows for rail-to-rail output swings with up to 100µA load. Both comparators offer a push-pull output that sinks and sources current.

The input common-mode voltage range for these devices extends from 0V to V_{CCI} - 1.3V. The MAX12900's comparators can operate at any differential input voltage within these limits. Input bias current is typically less than 1nA.

These comparators can be used for VCC, VDD or VREF voltage monitoring or other diagnostic functions, providing status information to the microcontroller.

LDO

All components of the MAX12900 are powered from an integrated LDO that generates a 3.0V to 5.5V VCCI voltage from an input VCC voltage of 4.0V to 36V. The LDO provides a clean supply for sensitive analog circuitry. The output of the LDO is set by external resistors and can be selected using the following equation:

$$V_{OUT} = 1.212V \times (1 + R1/R2)$$

Where, 1.212V is an internal reference voltage, R1 and R2 form a resistor divider providing feedback voltage to close the LDO loop, refer to the typical application diagrams. It is recommended that R2 be less than or equal to 470kΩ. For example, for VCCI = 3.3V, R1 = 698k and R2 = 402k can be used from standard 1% E96 resistor series values.

Application Information

Loop-Powered 4mA–20mA Sensor Transmitter with PWM inputs

One of the possible implementations of a loop powered 4mA–20mA sensor transmitter is shown in Figure 2. In this application diagram, the PWM inputs from a microcontroller are re-shaped by the conditioners, filtered by the OP1 op amp and converted to an analog voltage. The voltage is then converted to a 4mA–20mA loop current by OP3, an external transistor Q1 and a current sense resistor R_{SENSE}.

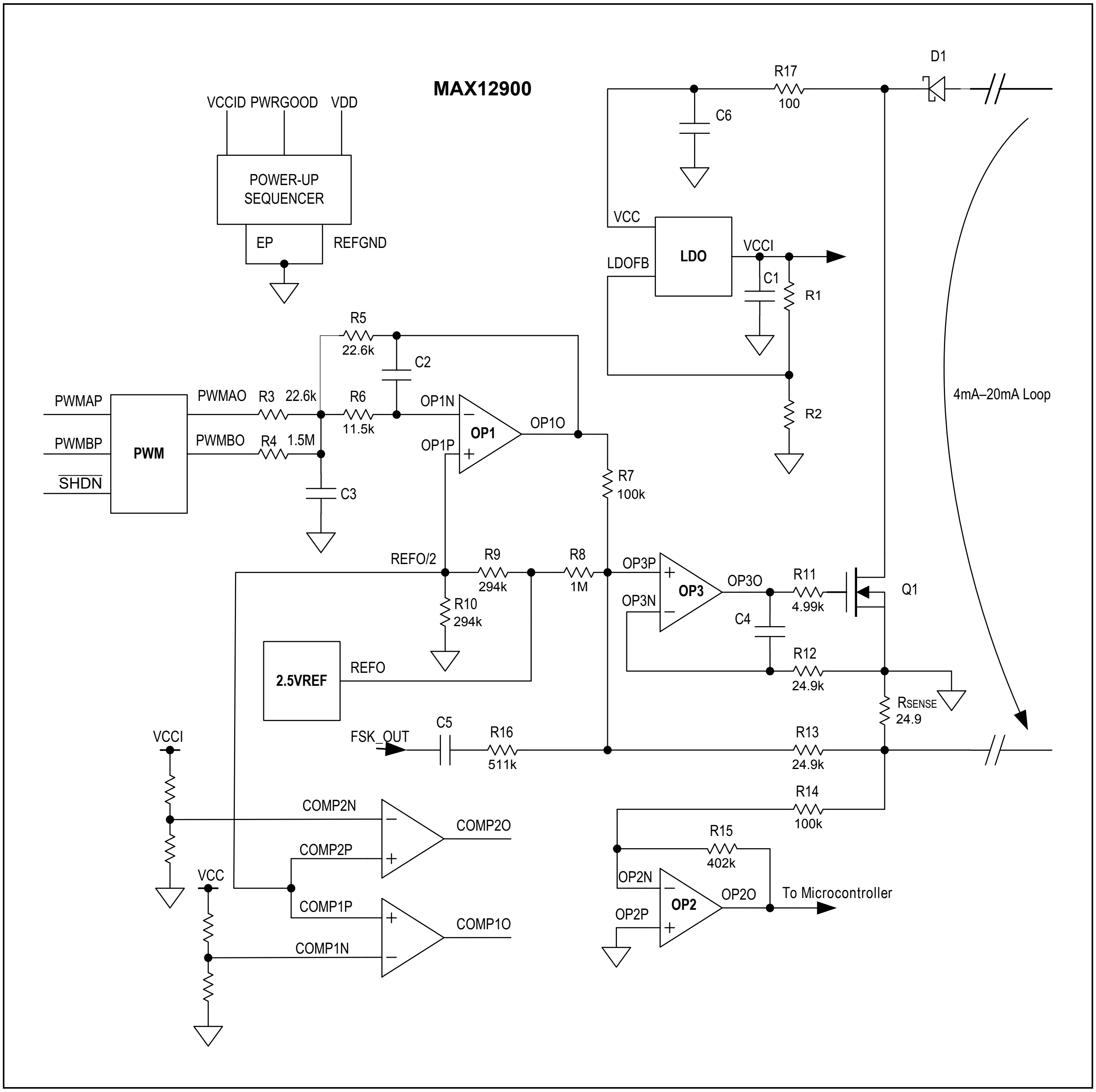


Figure 2. Loop-Powered 4mA-20mA Transmitter with Two PWM Inputs

The component selection of this circuit is as follows.

Let us assume the loop current range is 2.5mA to 27.5mA including NAMUR burnout detection. With the 24.9Ω R_{SENSE} resistor and the 2.5mA to 27.5mA loop current range, the non-inverting input of OP3 (OP3P) should be in the range 62.25mV (2.5mA x 24.9Ω = 62.25mV) to 684.75mV (27.5mA x 24.9Ω = 684.75mV).

The loop current (I_{loop}) has two components: offset current generated by the reference output (I_{offset}) and PWM signals converted to current (I_{PWMA}, I_{PWMB}).

$$I_{loop} = I_{offset} + I_{PWMA} + I_{PWMB}$$

After power-up, assuming the PWM signals do not contribute to the loop current, the initial 2.5mA offset current is generated by the reference voltage as follows:

$$Ioffset = \frac{REFO \times R13}{R8 \times R_{SENSE}}$$

The PWM currents are given by

$$I_{PWMA} = \frac{PWMADC \times REFO \times \left(\frac{R5}{R3}\right) \times R13}{R7 \times R_{SENSE}}$$

$$I_{PWMB} = \frac{PWMBDC \times REFO \times \left(\frac{R5}{R3}\right) \times R13}{R7 \times R_{SENSE}}$$

where, PWMADC and PWMBDC are the PWM duty cycles.

DAC Implementation with PWM and Low-Pass Filter

The sensor data received from the microcontroller can be arranged into a coarse and a fine PWM signal.

Both the coarse and fine signals can have up to 8 bits of resolution. The PWM signals are then converted to their voltage level representations via a LPF. The PWM outputs from the MAX12900 connect to the LPF through two gain setting resistors with ratios up to 1:256; the voltage levels at the output of the LPF are proportional to the PWM duty cycles.

The application diagram in Figure 2 shows an implementation of a 14-bit resolution signal path. The PWMAP input receives the coarse signal with 8-bits of resolution, and the PWMBP input receives the fine signal with 6-bits of resolution. A 1:66 ratio is used for the two gain setting resistors.

The coarse gain is set to 1 by using a 22.6kΩ gain resistor R3 and a 22.6kΩ feedback resistor R5, while the fine gain is set to 1/66 by using a 1.5MΩ gain resistor R4. The two PWM outputs are summed via the 22.6kΩ feedback resistor R5 of OP1.

The PWM frequency and filter parameters must satisfy the 4mA–20mA current loop noise requirements. In this example, the PWM frequency is 10kHz and the 4mA–20mA transmitter is designed to meet the HART specification. Consequently, the broadband noise of the current loop during silence must be below $138mV_{RMS}$, and the in-band noise (500Hz–10kHz) must be below $2.2mV_{RMS}$ across a 500Ω loop load. In order to reduce the noise level to $2.2mV_{RMS}$ in-band, the LPF should suppress the noise by more than 60dB (2.5V/2.2mV = 1136.4 or 61dB). Therefore, the cut-off frequency of the LPF should be less than 70Hz with a 40dB/decade roll-off slope. OP1 implements a second-order multi-feedback LPF.

Voltage-Controlled Current Source

The integrated OP3 op amp can be combined with an external current modulating transistor Q1 to implement a precision voltage controlled current source. Q1 can be either an N-MOSFET or a bipolar NPN transistor and needs to satisfy the peak voltage and power dissipation criteria of the current loop. OP3 and Q1, in combination with a few external components, provide an optimal point to compensate the current loop.

Loop Current Diagnostic

In the application example of Figure 2, the second general purpose amplifier (OP2) is used for current diagnostics and provides feedback to the microcontroller.

Connection with a Sensor

The MAX12900 can work with any kind of sensor transmitter, even though it is designed with smart sensors in mind. A smart sensor means that it has an integrated microcontroller and the ability to provide either linear analog or PWM output. If the total current consumption of the transmitter is less than 4mA, power to the sensor and the digital VDD supply can be provided directly from the VCCI pin. If the transmitter requires more than 4mA, an external dc-dc switching converter can be used. Such a scenario is shown in the application circuit in Figure 3, where OP2 is utilized as a linear voltage regulator and the dc-dc converter powers the microcontroller and drives the VDD supply pin.

Loop Powered 4mA–20mA Transmitter for Explosion-Proof Devices

If the sensor is to be deployed in hazardous or explosive areas, it must use additional protective components to limit the electrical energy from short circuit or failure conditions, and to prevent sparks that could cause an explosive atmosphere to ignite.

Figure 4 shows an application circuit with improved protection in hazardous environments. In order to limit the electrical energy that goes to the sensor transmitter, an additional Q2 transistor and Zener diodes are added. Typically, a Zener diode should have a clamping voltage from 5V to 12V. In this case, both Q1 and Q2 transistors are the current modulating elements of the circuit. The total 4mA–20mA loop current is the sum of the current flowing through the Zener diodes, the Q1 transistor and the sensor. Each current path is protected by limiting resistors. Most of the power dissipation is spread out through Q1, Q2 and the Zener diodes, which makes the system design more robust.

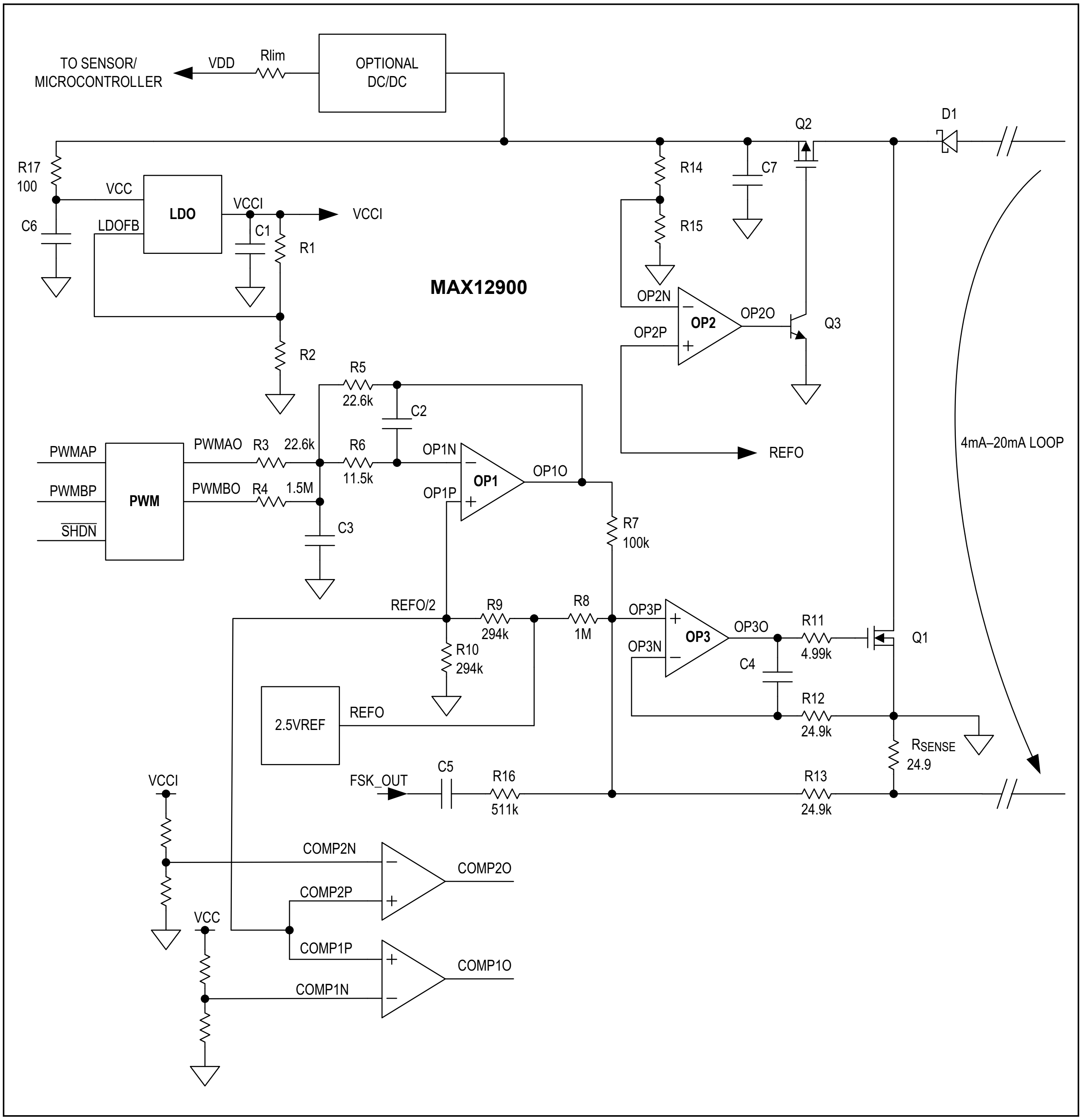


Figure 3. Loop-Powered 4mA-20mA Transmitter with an External Voltage Regulator

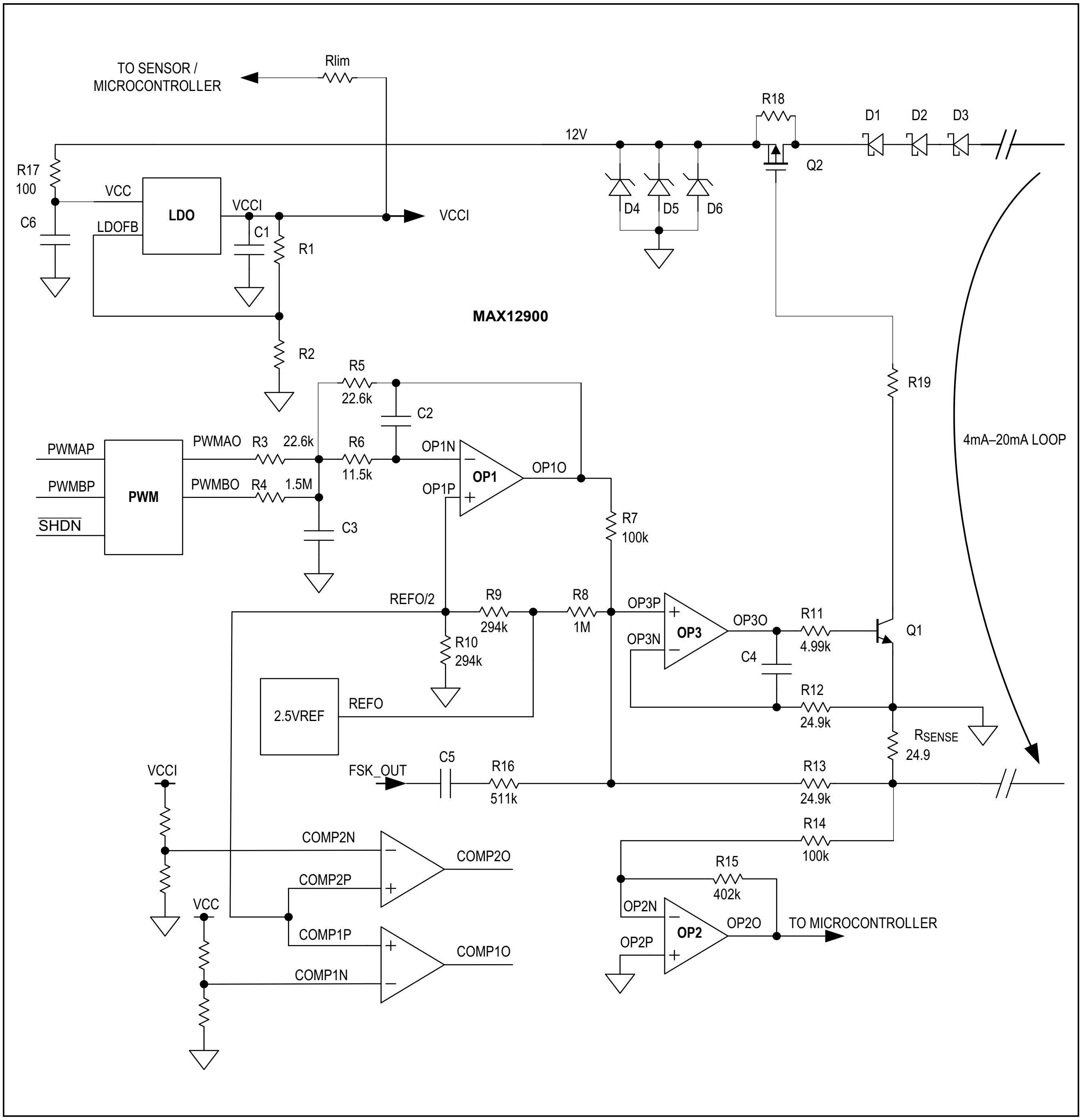


Figure 4. Loop-Powered 4mA–20mA Transmitter for Hazardous Environments

Ordering Information

PART	PACKAGE	BODY SIZE	PIN PITCH	TEMP RANGE (°C)
MAX12900AATJ+	TQFN32	5mm x 5mm	0.5mm	-40 to +125
MAX12900AATJ+T	TQFN32	5mm x 5mm	0.5mm	-40 to +125

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and Reel

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—

