Single-chip Type with Built-in FET Switching Regulator Series

Step-up / Inverted 2ch Switching Regulator

BD81870EFV-M

General Description

BD81870EFV is current mode step-up and inverted 2 channel switching regulator with built in FET.

Features

- AEC-Q100 Qualified(Note 1)
- Wide input voltage range 2.5V to 5.5V
- High Frequency 2.1MHz
- Built-in 300mΩ/22V Nch FET and 300mΩ/15.5V Pch FET.
- Built-in 150mΩ high-side switch for boost channel with soft-start function
- Independent ON/OFF signal, Built-in discharge switch
- Circuits protection : OCP, SCP, OVP, UVLO, TSD

(Note 1:Grade2)

Applications

- Car navigation panel, Car instrument panel

Special Characteristics

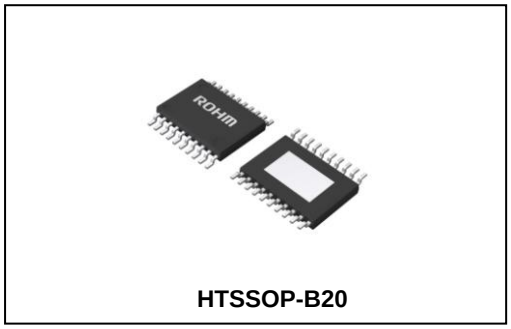
- Reference Accuracy : ±3%(Ta=-40 to 105°C)
- Switching Frequency : ±14.3%(Ta=-40 to 105°C)

Key Specification

- Input voltage range : 2.5V to 5.5V
- Step-up Output voltage range : VDD x 1.24 to 18.0V
- Inverted Output voltage range : VDD - 13.0V to -1.0V
- Switching Frequency : 2.1MHz(Typ.)
- Nch FET ON resistance : 300mΩ(Typ.)
- Pch FET ON resistance : 300mΩ(Typ.)
- Operating Temperature range : -40℃ to +105℃

Package

	W (Typ.) x D (Typ.) x H (Max.)
HTSSOP-B20	6.5mm x 6.4mm x 1.00mm



HTSSOP-B20

Typical Application Circuit

（TOP VIEW）

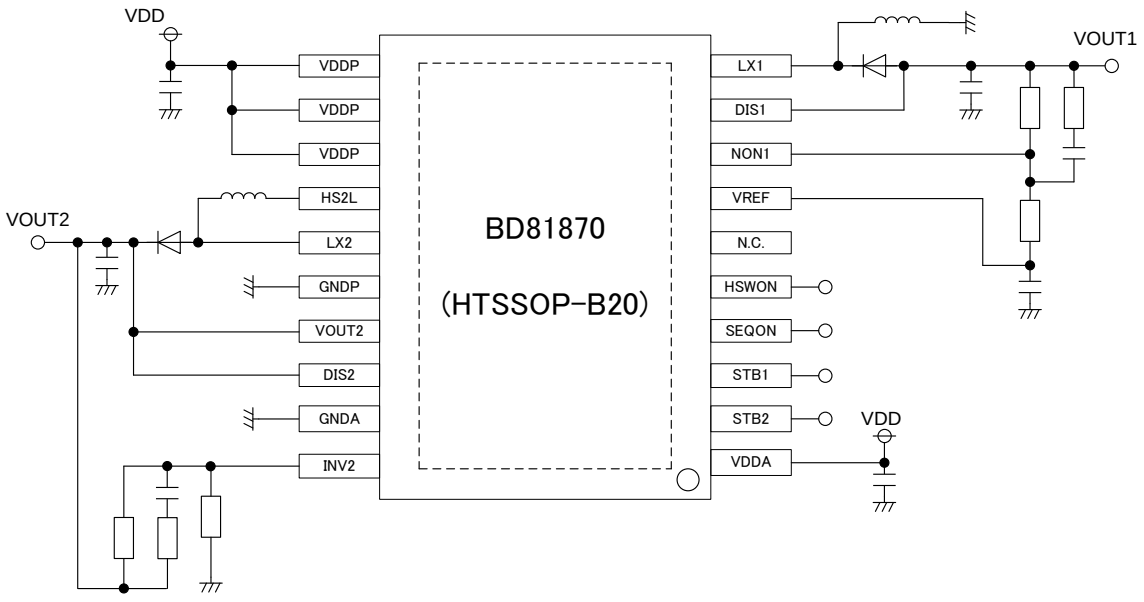


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration

(TOP View)

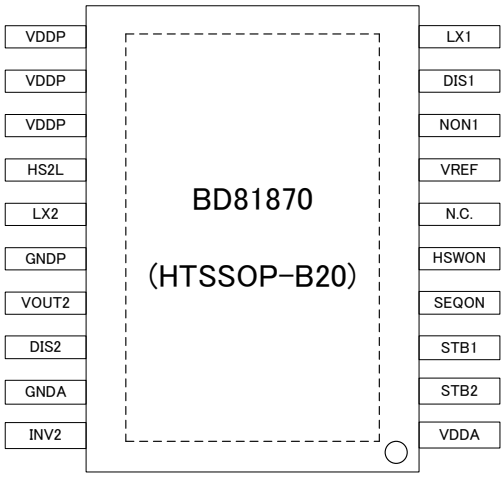


Figure 2. Pin Configuration

Pin Description

PIN No.	SYMBOL	FUNCTION	PIN No.	SYMBOL	FUNCTION
1	VDDA	Analog Power supply pin	11	VDDP	Power supply pin
2	STB2	Step-up DC/DC ON/OFF pin	12	VDDP	Power supply pin
3	STB1	Inverted DC/DC ON/OFF pin	13	VDDP	Power supply pin
4	SEQON	Sequence ON/OFF pin	14	HS2L	High-side switch output pin
5	HSWON	High-side switch ON/OFF pin	15	LX2	Step-up DC/DC switching pin
6	N.C.	—	16	GNDP	Step-up DC/DC GND pin
7	VREF	Inverted DC/DC reference output pin	17	VOUT2	Step-up DC/DC output sense pin
8	NON1	Inverted DC/DC feedback pin	18	DIS2	Step-up DC/DC discharge pin
9	DIS1	Inverted DC/DC discharge pin	19	GNDA	Analog GND pin
10	LX1	Inverted DC/DC switching pin	20	INV2	Step-up DC/DC feedback pin

Block Diagram

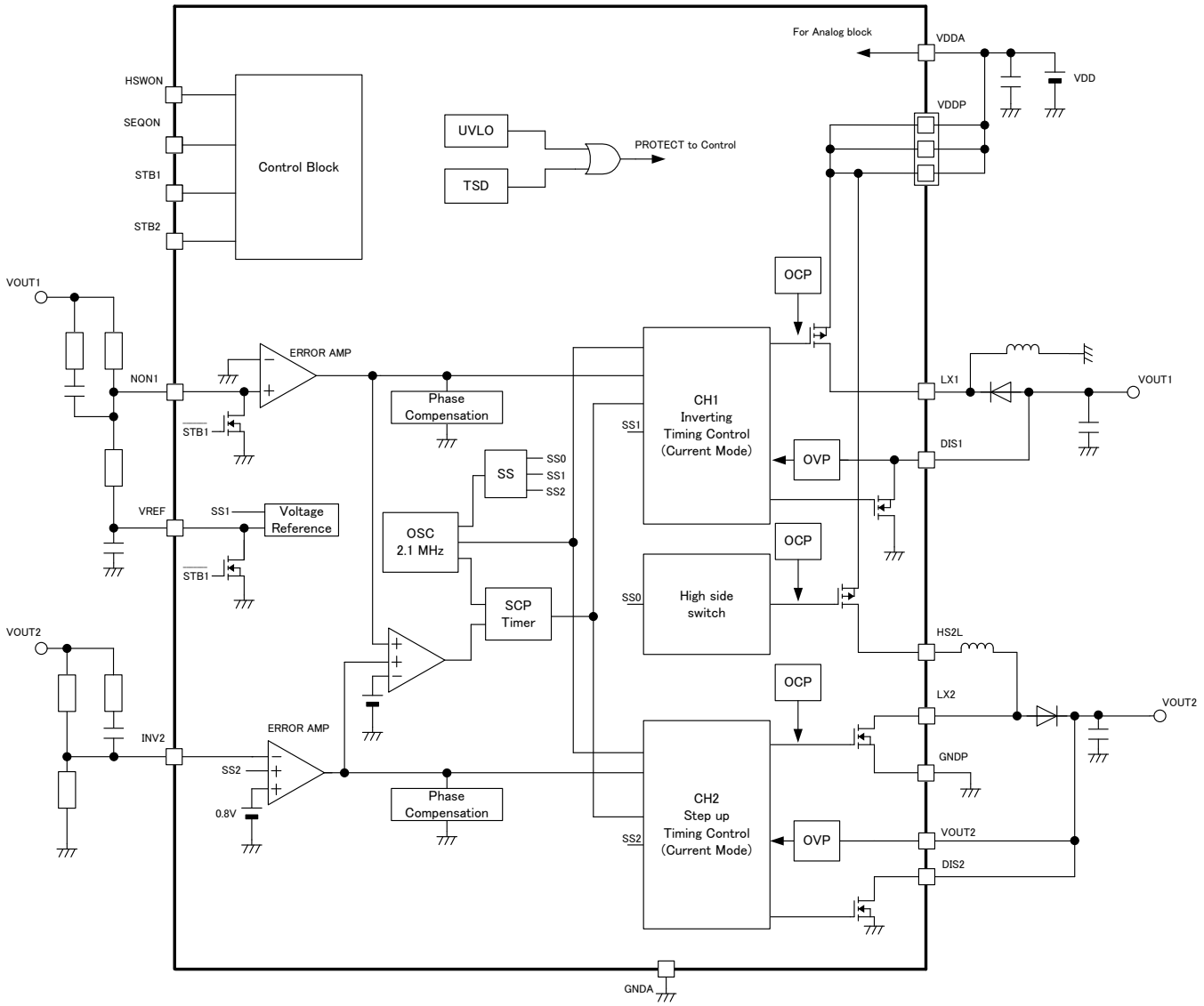


Figure 3. Block Diagram

Description of each Block

1. Control Block
   This block controls ON/OFF of each channels: Inverted DC/DC, step-up DC/DC and High-side switch channel.
   SEQON pin and HSWON pin set ON/OFF sequence.
   SEQON pin and HSWON pin must be short to VDD or GND.
   These pins are not fixed with internal pull-up or pull-down resistance.

Control Input					Output Channels		
UVLO/TSD internal signal	SEQON	HSWON	STB1	STB2	Inverted DC/DC	Step-up DC/DC	High-side switch
H	-	-	-	-	OFF	OFF	OFF
L	L	L	L/H	L/H	STB1	STB2	
L	L	H	L/H	L/H	STB1	STB2	ON
L	H	L	L/H	*(Note 1)*	Internal ON/OFF sequence		
L	H	H	L/H	*(Note 1)*	Internal ON/OFF sequence		ON

(Note 1) refer to the item of 12. Output discharge

2. Voltage Reference
   This block generates reference voltage for inverted and step-up channels.

3. UVLO
   This block is for under voltage lockout protection.

4. TSD
   This block is for protection for abnormal temperature.
   When the junction temperature exceeds 175℃(typ.), all output channels go shutdown. When the junction temperature falls below 150℃(typ.), the IC restarts.

5. OSC
   This block is the oscillator for internal clock.

6. Soft Start（SS）
   This block is the circuit for preventing in-rush current by increasing DC/DC converter output gradually.
   It generates internal soft-start reference for inverted DC/DC, step-up DC/DC and high-side switch.

7. SCP Timer
   This block is a timer-latch type short circuit protection.
   When inverted or step-up DC/DC is in operation, after 31msec (typ.) with SCP detected, all output channels go off-latch.
   When UVLO or TSD is detected, off-latch is released.
   In SEQON=L mode, when STB1 and STB2 are low, off-latch is released.
   In SEQON=H mode, when STB1 is low, off-latch is released.

   In inverted DC/DC, when NON1 pin is above error amp reference 0.0V, error amp output goes high and SCP is detected.
   In step-up DC/DC, when INV2 pin is below error amp reference 0.8V, error amp output goes high and SCP is detected.

8. High Side Switch
   This block prevents step-up channel output to become as high as VDD level by switching off the power supply of the step-up channel.
   At the start-up timing of step-up channel, soft-start function of high-side switch prevents in-rush current.
   When high-side OCP is detected, high-side switch is off-latch.
   When high-side switch channel in OFF conditions, off-latch is released.

9. ERROR AMP
   This block monitors feedback voltage. It provides voltage to control PWM.

10. Timing Control
    This block controls DUTY by monitoring ERROR AMP output voltage.

11. OCP
    This block prevent malfunction at over current by limiting internal FET current.
    When OCP is detected and duty is limited, Inverted DC/DC output increase or step-up DC/DC output decrease.
    So, SCP is detected and all output channels are OFF by off-latch function above.

12. Output discharge
Inverted DC/DC output capacitor is discharged through DIS1 pin when STB1 is low.
The discharge function can be disabled when STB2=H in SEQON=H mode.
The discharge function can NOT disabled in SEQON=L mode because STB2 controls ON/OFF of Step-up DC/DC.

Step-up DC/DC output capacitor is discharged through DIS2 pin when high-side switch is OFF.
In conditions where HSWON=H, when UVLO of VDD is released, high-side switch is ON.
So, discharge function of step-up DC/DC output capacitor is disabled, even if step-up DC/DC is OFF.
By cutting the route from DIS2 pin to the capacitor, discharge function can be disabled.
OVP function is not disabled because DIS2 pin is used to monitor the output voltage.
In this case, DIS2 pin should be shorted to GND.

13. OVP
By detecting high level of output voltage, this block stops switching and prevent malfunction by over voltage stress.

In inverted DC/DC, when DIS1 pin is -14.5V (typ.) from VDDA level, switching stops.
When DIS1 pin voltage rises, switching starts again. OVP of inverted DC/DC has hysteresis of 1.0V (typ.).

In step-up DC/DC, when VOUT2 in is 20.5V (typ.) from GND level, switching stops.
When VOUT2 pin voltage falls, switching starts again. OVP of step-up DC/DC has hysteresis of 1.5V (typ.).

Absolute Maximum Ratings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	VDDA, VDDP	-0.3	-	7	V
Input Voltage	STB1, STB2, SEQON, HSWON	-0.3	-	7	V
	NON1, INV2	-0.3	-	7	V
Output Voltage	VREF	-0.3	-	7	V
	LX1	VDDP -15.5	-	VDDP +0.3	V
	DIS1	VDDP -15.5	-	VDDP +0.3	V
	HS2L	-0.3	-	7	V
	LX2	-0.3	-	22	V
	VOUT2	-0.3	-	22	V
	DIS2	-0.3	-	22	V
Operating Ambient Temperature Range	Ta	-40	-	105	℃
Storage Temperature Range	Tstg	-55	-	150	℃
Maximum Continuous Junction Temperature	Tjmax	-	-	150	℃

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
HTSSOP-B20				
Junction to Ambient	θ_{JA}	143.0	26.8	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	8	4	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Ranges
(Ta=-40℃ to 105℃)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Power supply voltage	VDD	2.5	-	5.5	V
Inverted output voltage	VOUT1	VDD - 13	-	-1.0	V
Step up output voltage	VOUT2	VDD x 1.24	-	18	V

Electrical Characteristics

(Unless otherwise noted, Ta=25℃, VDD=3.6V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 Under Voltage Lockout Threshold 】						
UVLO disable voltage	UVL_DIS	2.1	2.3	2.5	V	VDD sweep up
UVLO detect voltage	UVL_DET	1.7	1.8	1.9	V	VDD sweep down
【 Oscillator 】						
Oscillating frequency	FOSC	1.8	2.1	2.4	MHz	-40<Ta<105°C
LX1 Max Duty	DMAX1	80	86	-	%	
LX2 Max Duty	DMAX2	80	86	-	%	
【 Error AMP, VREF 】						
VREF voltage	VREF	0.985	1.000	1.015	V	VREF- NON1 feedback resistance R1B 20kΩ
VREF voltage range	VREF_R	0.970	1.000	1.030	V	-40<Ta<105°C VDD=2.5 to 5.5V
INV2 voltage	VINV	0.788	0.800	0.812	V	
INV2 voltage range	VINV_R	0.776	0.800	0.824	V	-40<Ta<105°C VDD=2.5 to 5.5V
CH1 Soft start time	TSS1	2.5	3.2	3.9	ms	
CH2 Soft start time	TSS2	2.5	3.2	3.9	ms	
【 Internal FET 】						
LX1 PMOS ON resistance	RLX1	-	300	480	mΩ	
DIS1 discharge resistance	RDIS1	-	100	160	Ω	VSTB1=0V, IDIS1=-1mA
NON1 discharge resistance	RNON1	-	150	240	Ω	VSTB1=0V, INON1=1mA
VREF discharge resistance	RVREF	-	150	240	Ω	VSTB1=0V, IVREF=1mA
High-side SW ON resistance	RHSW	-	150	240	mΩ	
LX2 NMOS ON resistance	RLX2	-	300	480	mΩ	
DIS2 discharge resistance	RDIS2	-	100	160	Ω	VSTB2=0V, IDIS2=-1mA
LX1 OCP threshold *(Note 1)*	IOCP1	1.2	2.4	3.6	A	
LX2 OCP threshold *(Note 1)*	IOCP2	1.2	2.4	3.6	A	
HS2L leak current	ILX_HSW	-1	0	1	μA	
LX1 leak current	ILK_LX1	-1	0	1	μA	
LX2 leak current	ILK_LX2	-1	0	1	μA	
【 OVP 】						
CH1 Over voltage protection	OVP1	VDD -15.5	VDD -14.5	VDD -13.5	V	Monitoring DIS1
CH2 Over voltage protection	OVP2	19	20.5	22	V	Monitoring VOUT2
【 TSD 】						
TSD Detect Temperature *(Note 1)*	TSD_DET	150	175	200	℃	
TSD Hysteresis *(Note 1)*	TSD_HYS	-	25	-	℃	

(Note 1) These items are not production tested, guaranteed by design and evaluation.

Electrical Characteristics – continued

(Unless otherwise noted, Ta=25℃, VDD=3.6V)

Parameter		Symbol	Limits			Unit	Condition
			MIN	TYP	MAX		
【 Control Block 】							
Control voltage	Active	VH	VDD x0.7	-	-	V	
	Non-active	VL	-	-	VDD x0.3	V	
STB pull down resistance		RCTRL	560	800	1040	kΩ	STB1, STB2
【 Circuit current 】							
Standby current		ISTB	-	-	1	μA	STB1=STB2=0V SEQON=HSWON=0V LX1=0V, HS2L=0V
Standby current range		ISTB_R	-	-	20	μA	-40<Ta<105°C
Circuit current of operation VDD		IDD	-	500	700	μA	STB1=STB2=3.6V NON1=-0.2V, INV2=1.2V

Typical Performance Curves

(Unless otherwise noted, Ta=25℃, VDD=3.6V, VOUT1=-6.2V, VOUT2=6.2V)

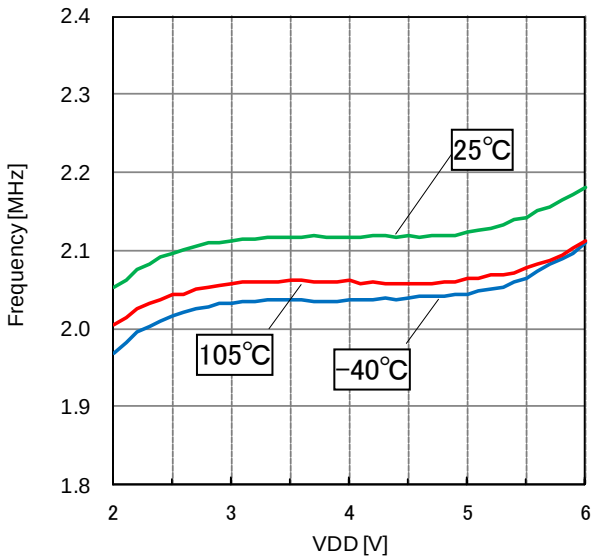


Figure 4. Frequency vs. VDD

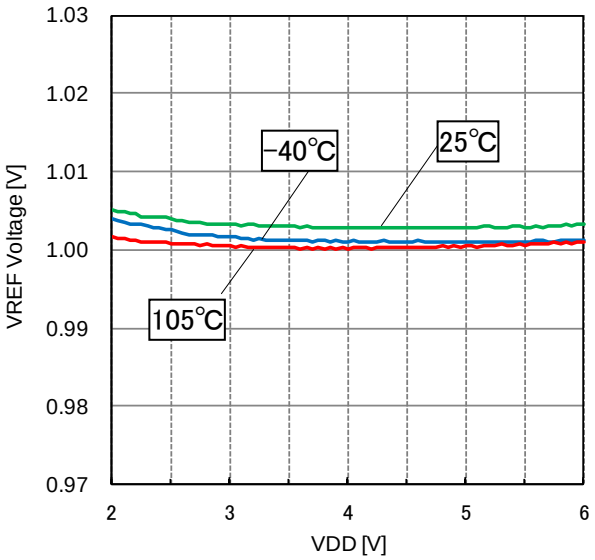


Figure 5. VREF Voltage vs. VDD

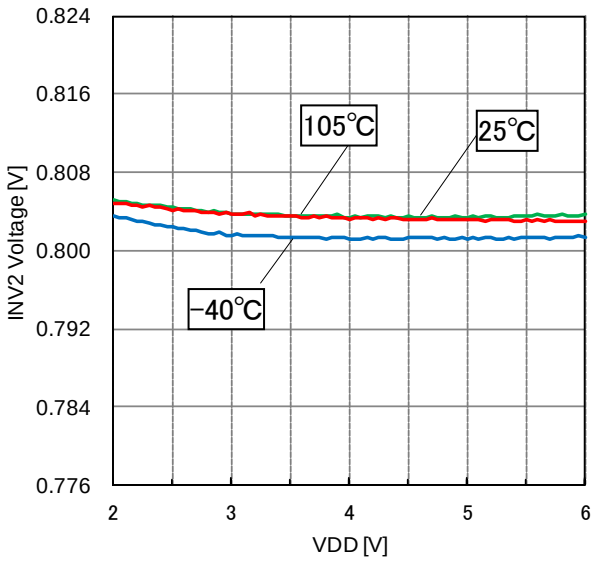


Figure 6. INV2 Voltage vs.VDD

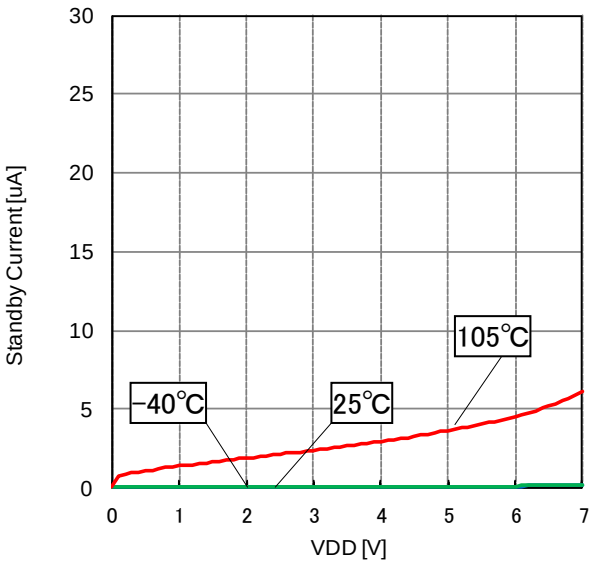


Figure 7. Standby Current vs. VDD

Typical Performance Curves

(Unless otherwise noted, Ta=25℃, VDD=3.6V, VOUT1=-6.2V, VOUT2=6.2V)

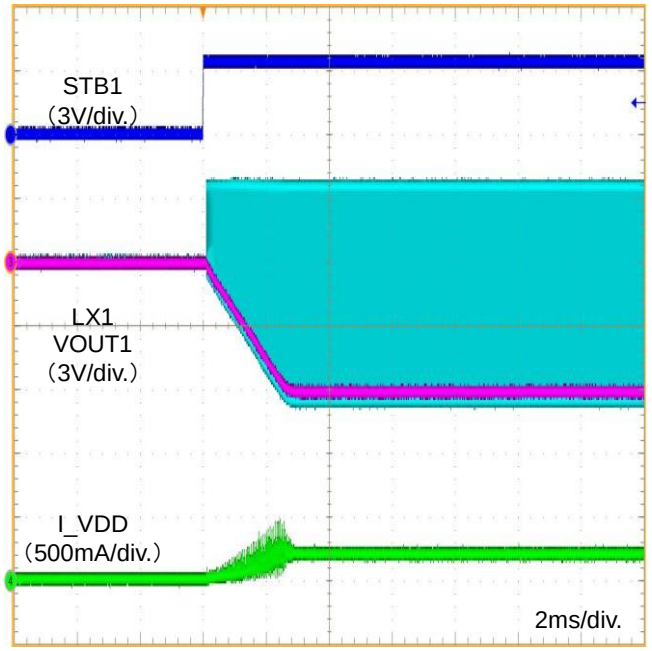


Figure 8. VOUT1 STB ON Waveform (Load 100mA)

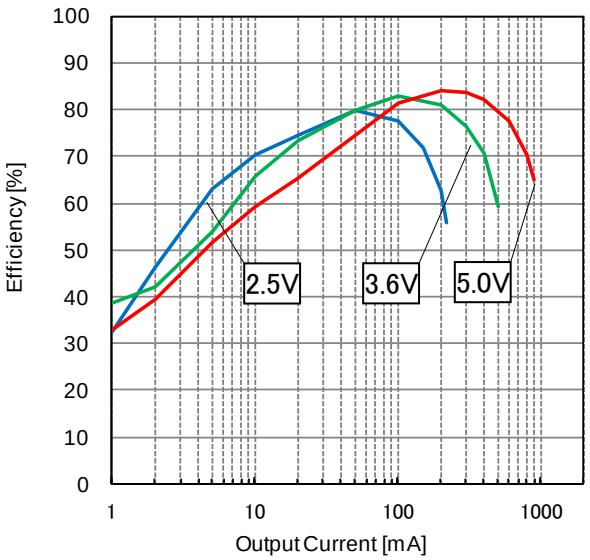


Figure 9. VOUT1 Efficiency vs. Output Current (VDD)

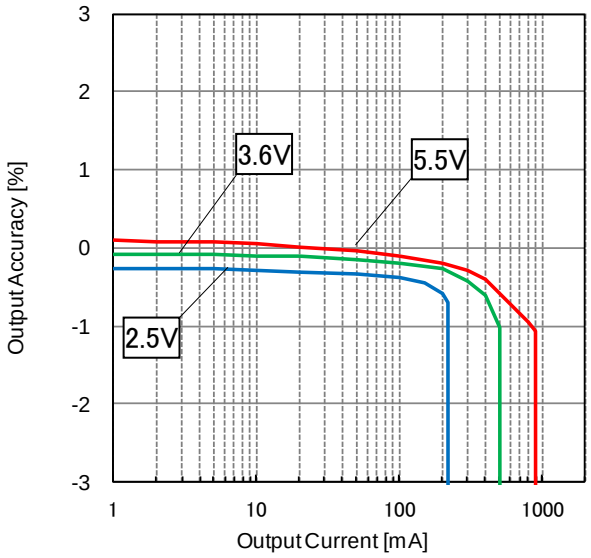


Figure 10. VOUT1 Output Accuracy vs. Output Current (VDD)

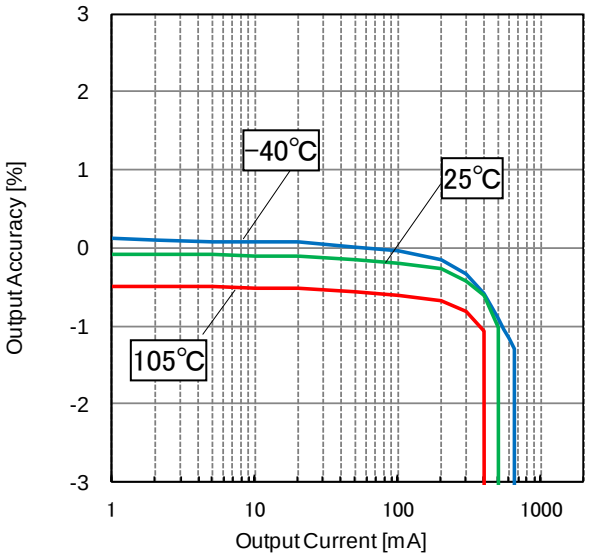


Figure 11. VOUT1 Output Accuracy vs. Output Current (Temp)

Typical Performance Curves

(Unless otherwise noted, Ta=25℃, VDD=3.6V, VOUT1=-6.2V, VOUT2=6.2V)

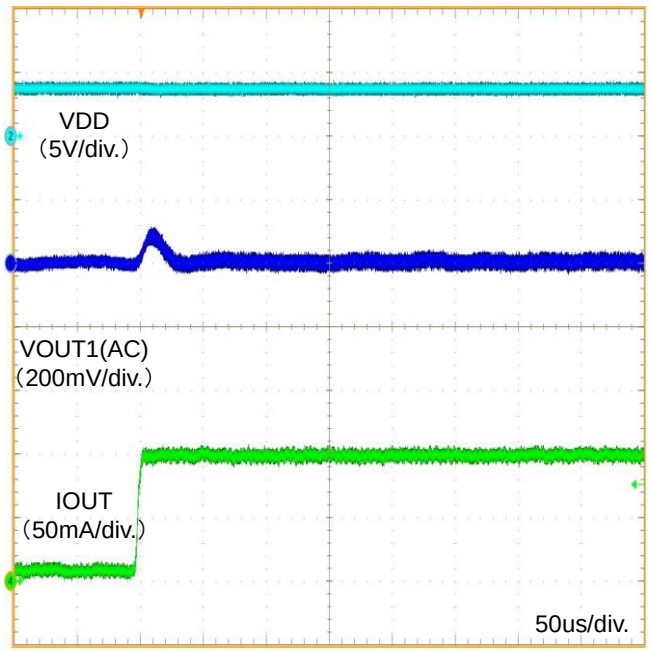


Figure 12. VOUT1 Load Transient Response Rising

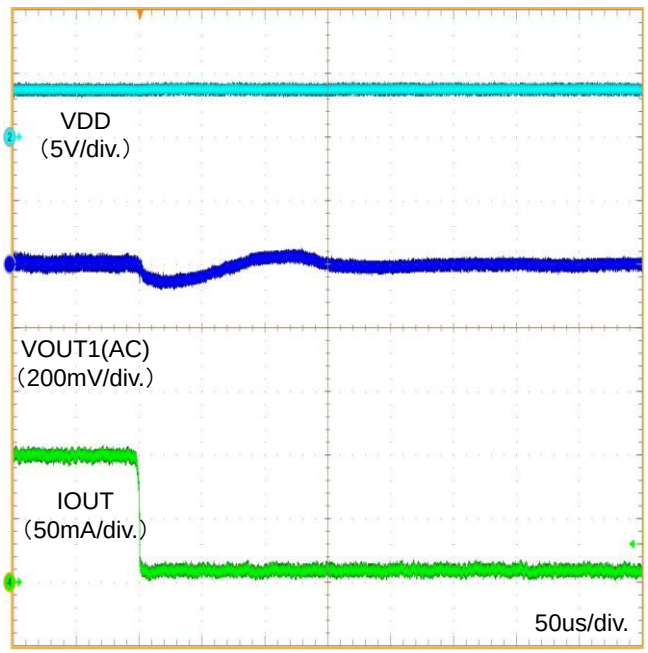


Figure 13. VOUT1 Load Transient Response Falling

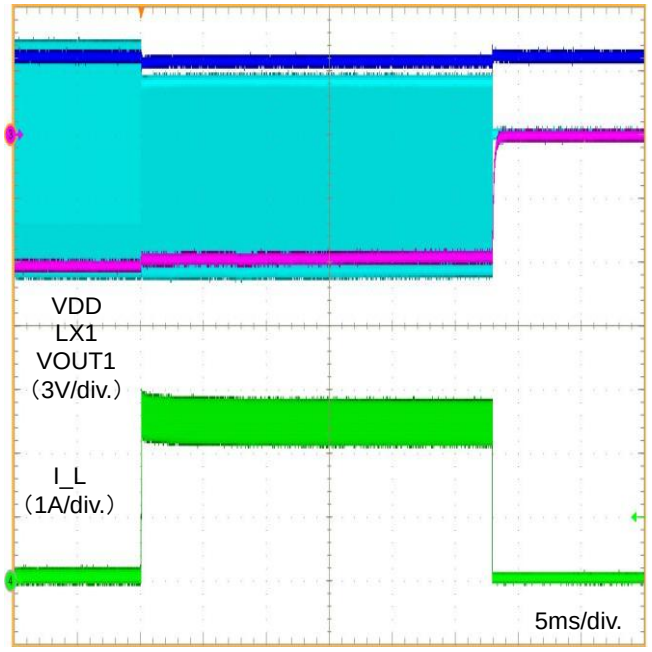


Figure 14. VOUT1 Over Current Protection

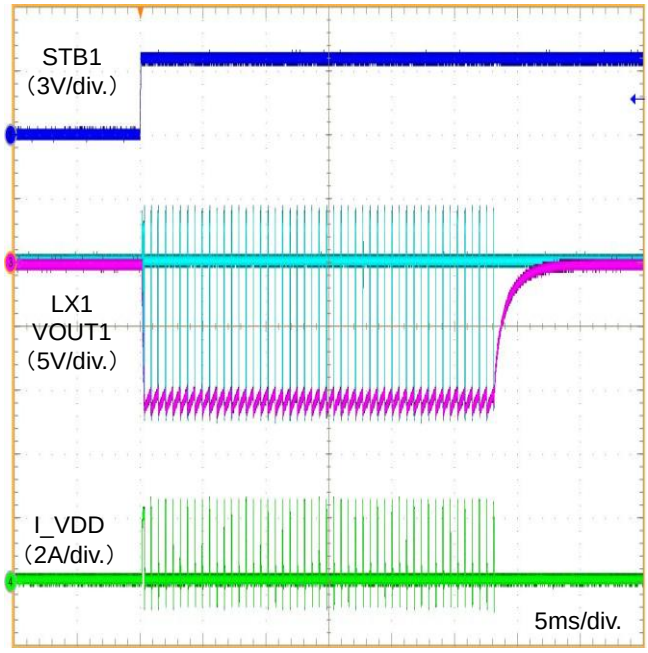


Figure 15. VOUT1 Over Voltage Protection

Typical Performance Curves

(Unless otherwise noted, Ta=25℃, VDD=3.6V, VOUT1=-6.2V, VOUT2=6.2V)

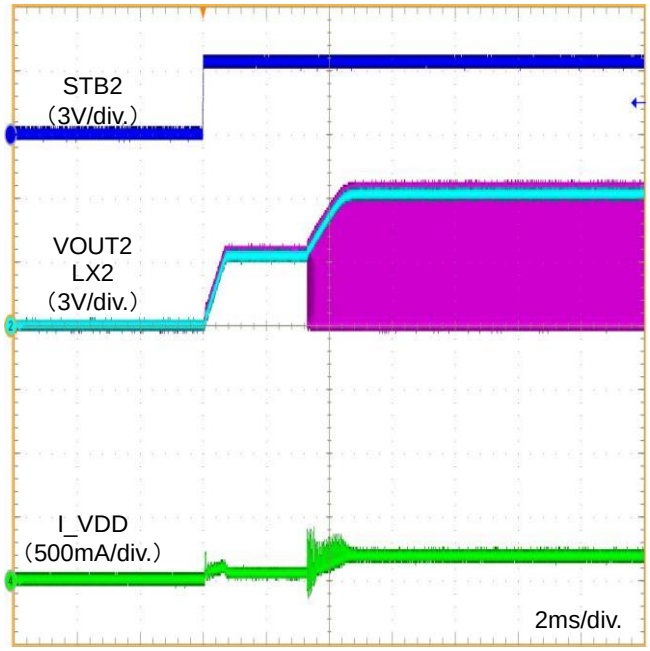


Figure 16. VOUT2 STB ON Waveform (Load 100mA)

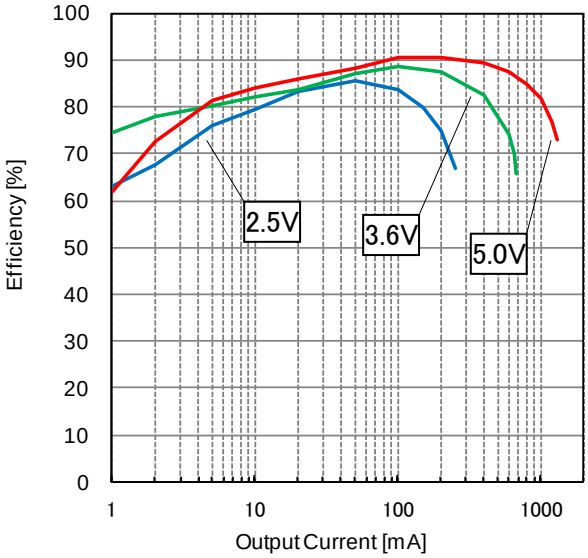


Figure 17. VOUT2 Efficiency vs. Output Current (VDD)

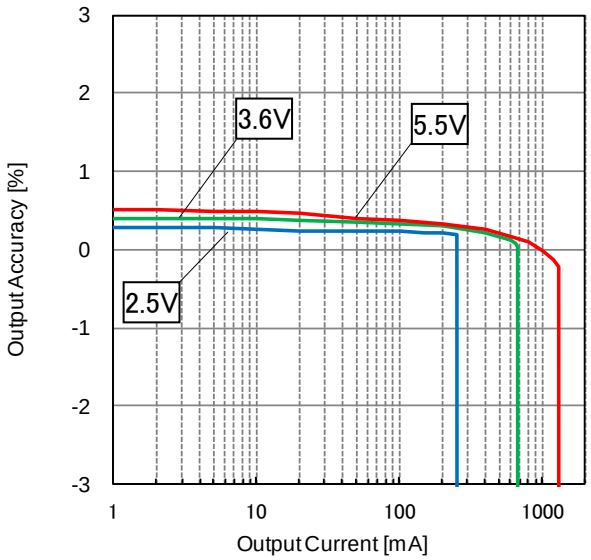


Figure 18. VOUT2 Output Accuracy vs. Output Current (VDD)

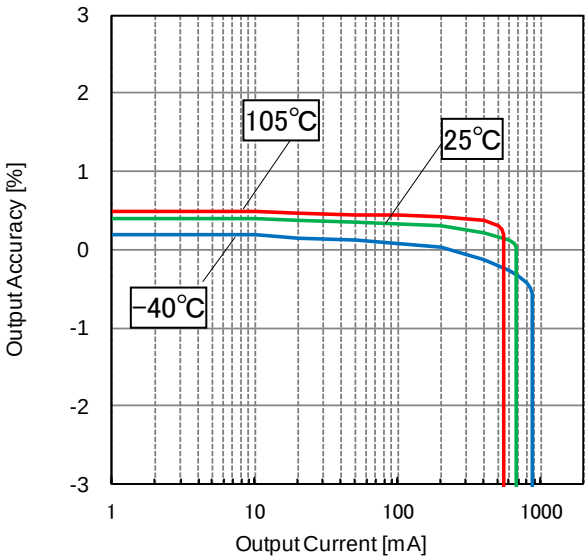


Figure 19. VOUT2 Output Accuracy vs. Output Current (Temp)

Typical Performance Curves

(Unless otherwise noted, Ta=25℃, VDD=3.6V, VOUT1=-6.2V, VOUT2=6.2V)

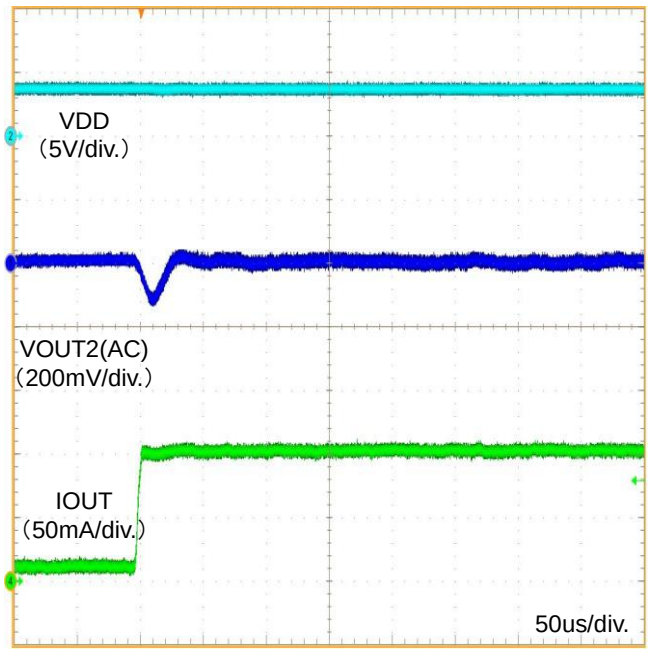


Figure 20. VOUT2 Load Transient Response Rising

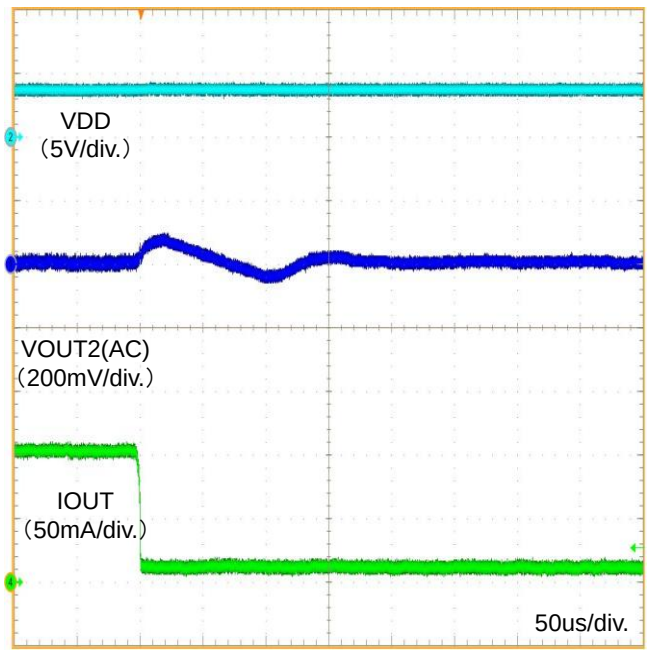


Figure 21. VOUT2 Load Transient Response Falling

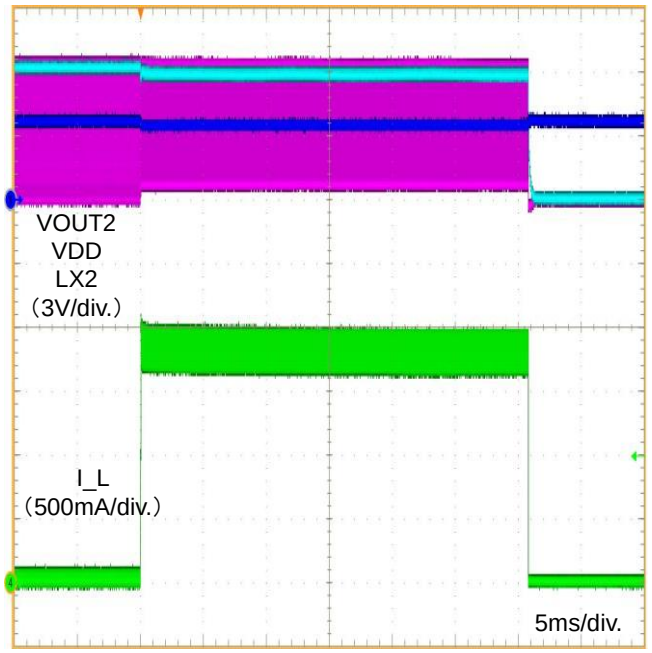


Figure 22. VOUT2 Over Current Protection

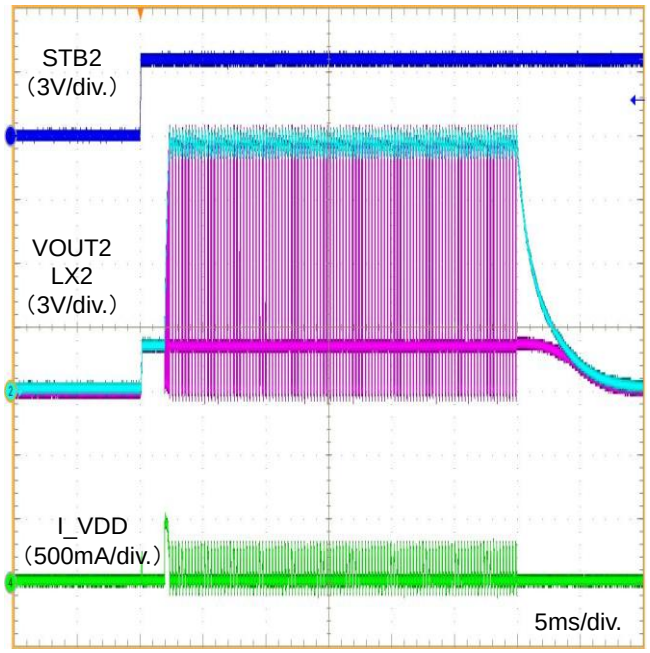


Figure 23. VOUT2 Over Voltage Protection

Typical Performance Curves

(Unless otherwise noted, Ta=25℃, VDD=3.6V, VOUT1=-6.2V, VOUT2=6.2V)

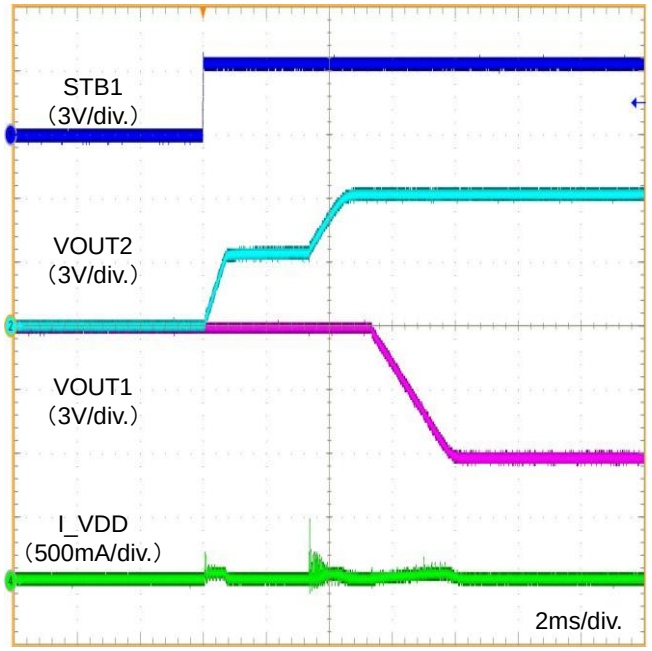


Figure 24. STB ON Waveform (SEQON=H, no load)

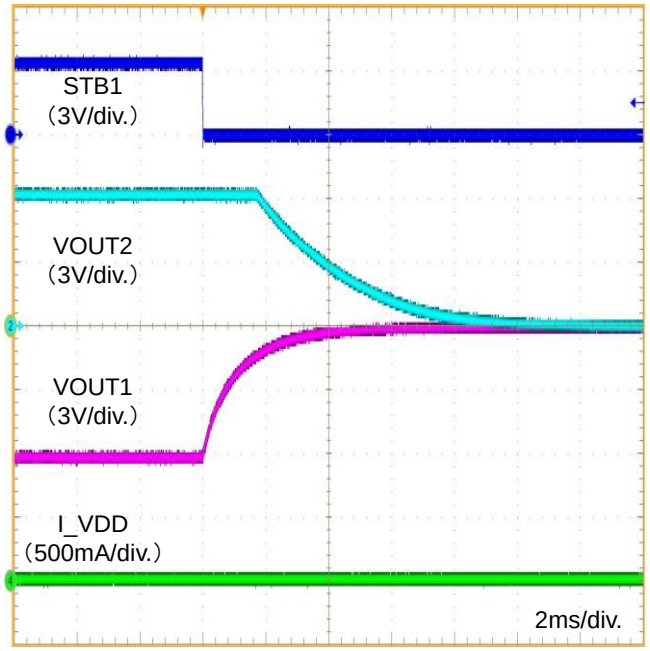


Figure 25. STB OFF Waveform (SEQON=H, no load)

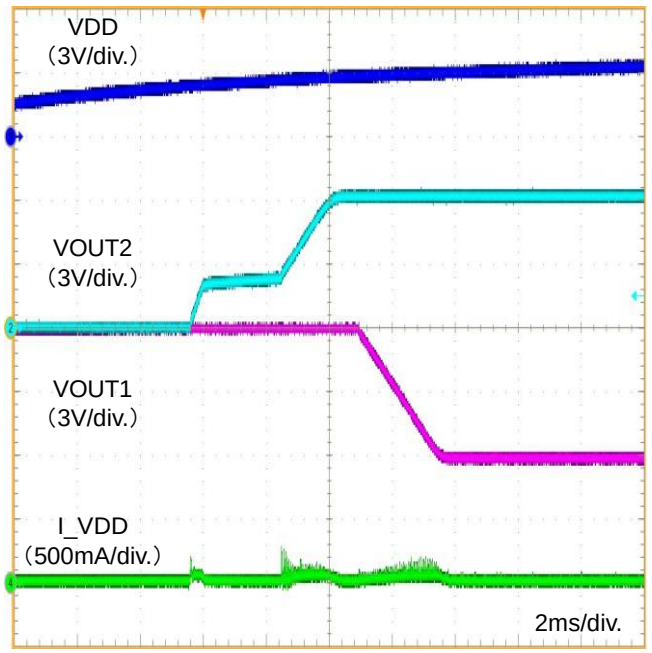


Figure 26. VDD ON Waveform (SEQON=H, no load)

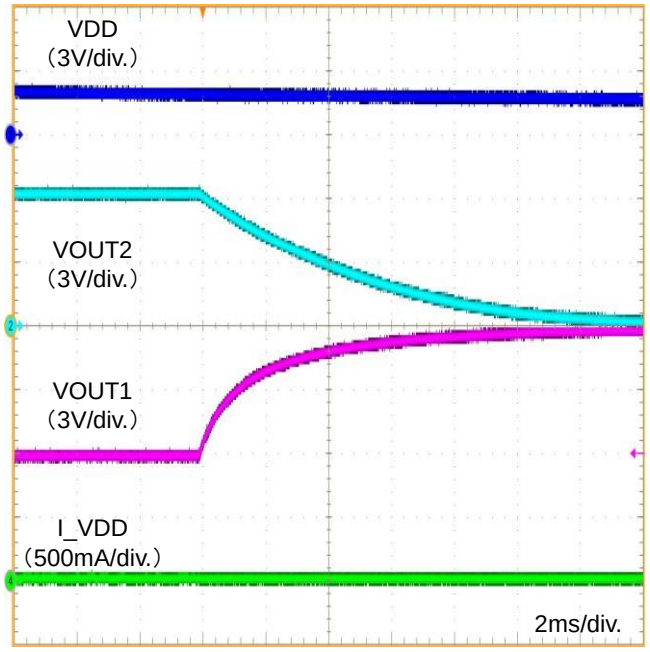


Figure 27. VDD OFF Waveform (SEQON=H, no load)

Timing Chart 1

ON/OFF sequence with STB control is as follows. STB1, STB2 and VDD are controlled independently.

When SEQON pin is L, inverted DC/DC and step-up DC/DC can be controlled independently.
When STB1 pin is H, inverted DC/DC soft-start begins.
When STB2 pin is H, step-up DC/DC soft-start begins.
Step-up DC/DC soft-start can begin after 2msec (typ.) from high-side switch soft-start.
High-side switch soft-start begins when STB2 pin is H and HSWON=L or when UVLO of VDD is released in condition where HSWON=H.
In condition where HSWON=H, ON/OFF sequence is shown in red-dotted line below.

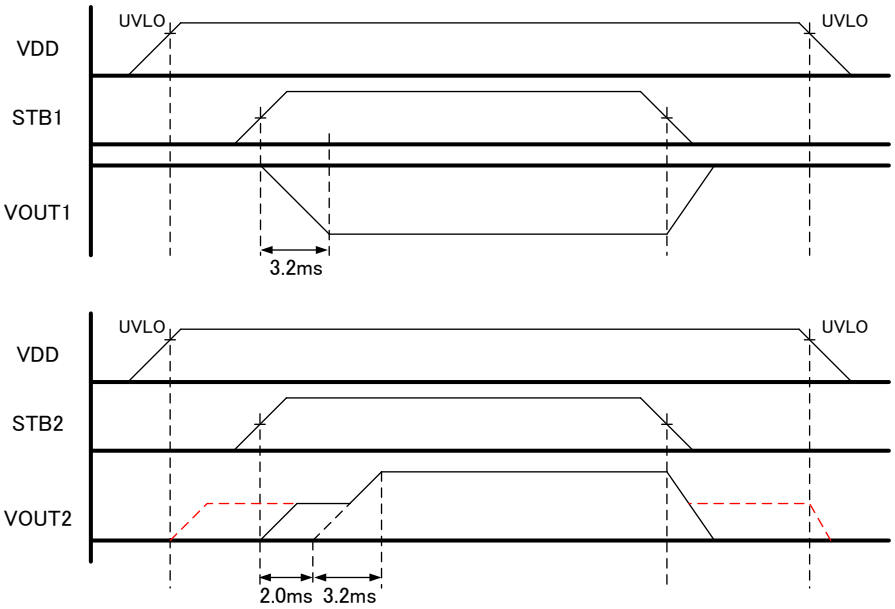


Figure 28. VDD≠STB, SEQON = GND

When SEQON pin is H, inverted DC/DC and step-up DC/DC is controlled by internal sequence.
When STB1 pin is H, inverted DC/DC soft-start begins, after step-up DC/DC soft-starts ends.
When STB1 pin is L, step-up DC/DC is OFF, 2msec after inverted DC/DC is OFF,
In condition where HSWON=H, ON/OFF sequence is shown in red-dotted line below.

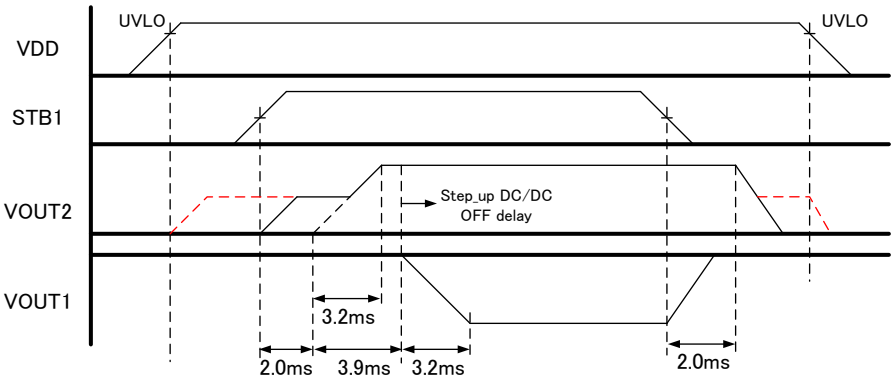


Figure 29. VDD≠STB, SEQON = VDD

Timing Chart 2

ON/OFF sequence with UVLO control is as follows. STB1 or STB2 are short to VDD.

When SEQON pin is L, inverted DC/DC and step-up DC/DC can be controlled independently.
When UVLO is released in condition where STB1 = VDD, inverted DC/DC soft-start begins.
When UVLO is released in condition where STB2 = VDD, step-up DC/DC soft-start begins.
Step-up DC/DC soft-start can begin after 2msec (typ.) from high-side switch soft-start.
High-side switch soft-start begins when UVLO of VDD is released.

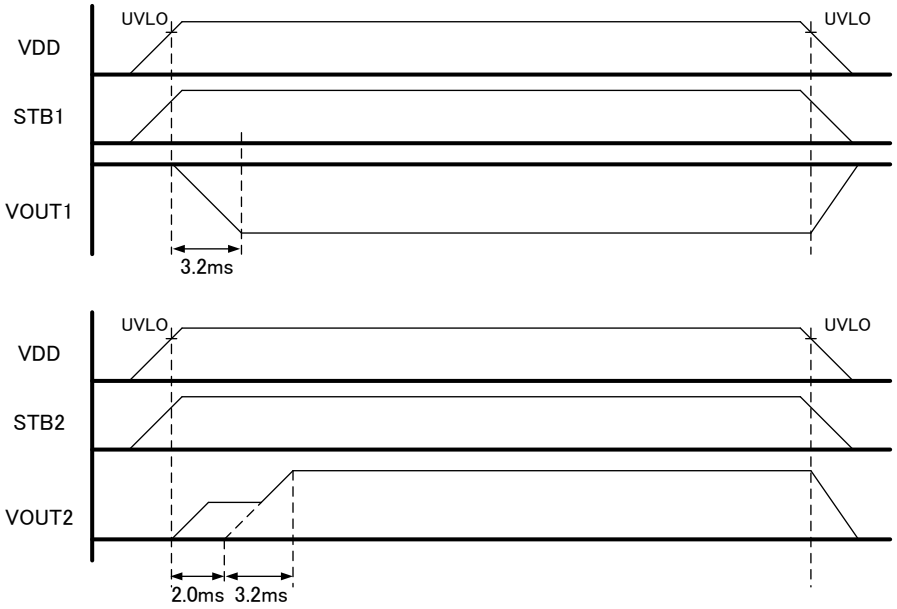


Figure 30. VDD=STB1=STB2, SEQON = GND

When SEQON pin is H, inverted DC/DC and step-up DC/DC is controlled by internal sequence.
When UVLO is released in condition where STB1 = VDD, inverted DC/DC soft-start begins, after step-up DC/DC soft-starts ends.
When UVLO is detected in condition where STB1 = VDD, inverted DC/DC and step-up DC/DC are OFF at the same timing.

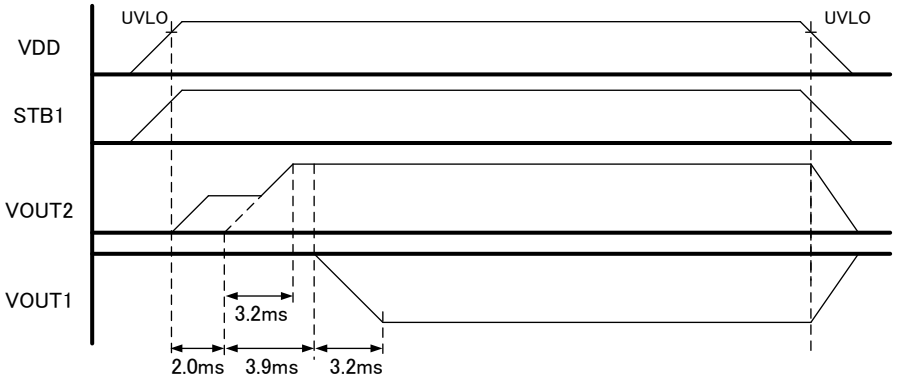


Figure 31. VDD=STB1=STB2, SEQON = VDD

Example Application

（TOP VIEW）

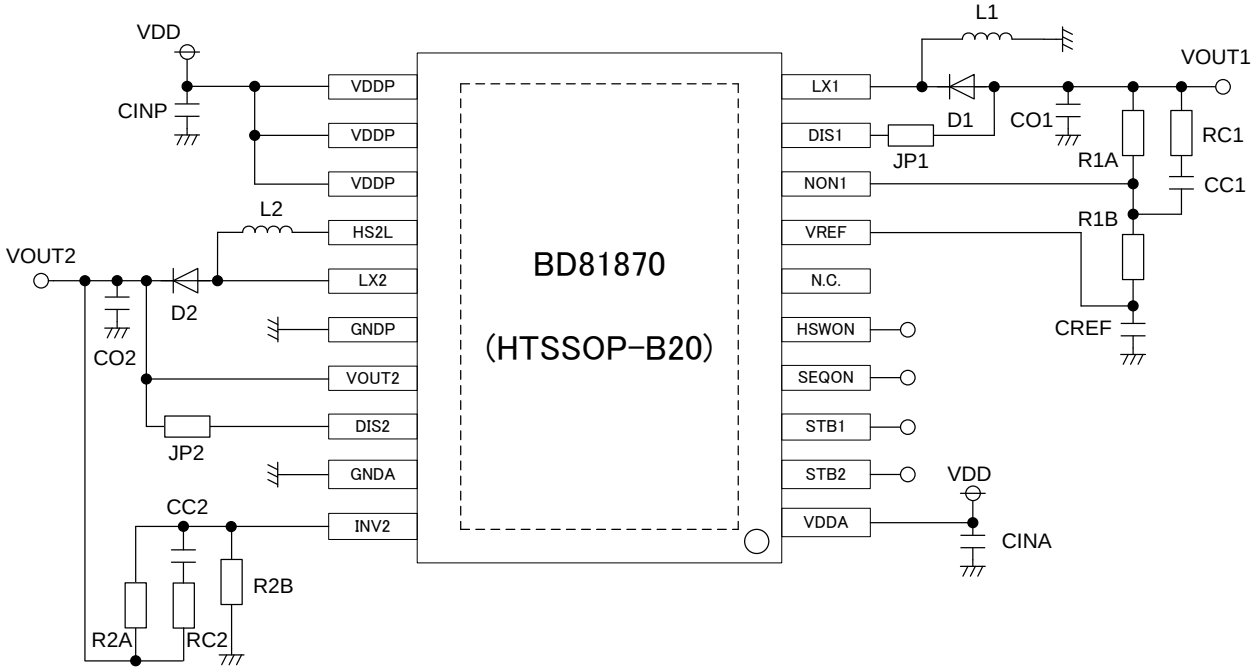


Figure 32. Application Example

Application Circuit components list

・VDD 3.6V, VOUT1 -6.2V/200mA, VOUT2 6.2V/200mA

Parts name	Value	Company	Parts Number
CINA	1uF/16V	Murata	GCM188R71C105KA64
CINP	10uF/16V	Murata	GCM31CR71C106KA64
L1	4.7uH/1.2A	Yuden	NRS4012T4R7MDGJV
D1	30V/1A	ROHM	RB550VAM-30TR
CO1	22uF/10V x2 series	Yuden	LMK316ABJ226KLHT
R1A	24kΩ, 100kΩ series	ROHM	MCR03
R1B	20kΩ	ROHM	MCR03
CC1	22pF/50V	Murata	GCM1885C1H220JA16
RC1	10kΩ	ROHM	MCR03
CREF	0.1uF/10V	Yuden	LMK105BJ104KVHF
L2	4.7uH/1.2A	Yuden	NRS4012T4R7MDGJV
D2	30V/1A	ROHM	RB550VAM-30TR
CO2	22uF/10V x2 series	Yuden	LMK316ABJ226KLHT
R2A	270kΩ x2 parallel	ROHM	MCR03
R2B	20kΩ	ROHM	MCR03
CC2	15pF/50V	Murata	GCM1885C1H150JA16
RC2	5.1kΩ	ROHM	MCR03

・VDD 3.6V, VOUT1 -9.0V/30mA, VOUT2 18V/30mA

Parts name	Value	Company	Parts Number
CINA	1uF/16V	Murata	GCM188R71C105KA64
CINP	10uF/16V	Murata	GCM31CR71C106KA64
L1	4.7uH/1.2A	Yuden	NRS4012T4R7MDGJV
D1	30V/1A	ROHM	RB550VAM-30TR
CO1	22uF/10V x2 series	Yuden	LMK316ABJ226KLHT
R1A	180kΩ	ROHM	MCR03
R1B	20kΩ	ROHM	MCR03
CC1	33pF/50V	Murata	GCM1885C1H330JA16
RC1	2.2kΩ	ROHM	MCR03
CREF	0.1uF/10V	Yuden	LMK105BJ104KVHF
L2	4.7uH/1.2A	Yuden	NRS4012T4R7MDGJV
D2	30V/1A	ROHM	RB550VAM-30TR
CO2	22uF/16V x2 series	Yuden	EMK325BJ226KMHP
R2A	430kΩ x2 parallel	ROHM	MCR03
R2B	10kΩ	ROHM	MCR03
CC2	68pF/50V	Murata	GCM1885C1H680JA16
RC2	5.1kΩ	ROHM	MCR03

Usable Component Range

Parts name	Limits			Unit	Conditions
	MIN	TYP	MAX		
CINA	0.6 *(Note 1)*	1	–	uF	VDD=2.5V to 5.5V
CINP	6 *(Note 1)*	10	–	uF	VDD=2.5V to 5.5V
CO1 *(Note 2)*	6.6 *(Note 1)*	11	*(Note 3)*	uF	VOUT1= -6.2V
CO1 *(Note 2)*	4.4 *(Note 1)*	11	*(Note 3)*	uF	VOUT1= -9V
CO2 *(Note 2)*	6.6 *(Note 1)*	11	*(Note 3)*	uF	VOUT2=6.2V
CO2 *(Note 2)*	4.4 *(Note 1)*	11	*(Note 3)*	uF	VOUT2=18V
L1 *(Note 2)*	2.2	4.7	10	uH	–
L2 *(Note 2)*	2.2	4.7	10	uH	–
R1	–	–	250	kΩ	R1 = R1A + R1B
R2	–	–	250	kΩ	R2 = R2A + R2B

(Note 1) Select capacitor more than MIN limits, considering temperature characteristic, DC bias characteristics and etc.
(Note 2) Select the parts considering gain and phase characteristics.
(Note 3) Select the parts considering in-rush current at soft-start timing.

Selecting Application Components

1. Output Inductor
   A shielded inductor that satisfies the current rating (current value, Ipeak as shown in the drawing below) and has a low DCR (direct current resistance component) is recommended.
   Inductor values affect output ripple current greatly.

$$Ipeak = \frac{Vin - Vout}{Vin \times \eta} \times Iout + \frac{1}{2} \times \frac{Vin \times (-Vout)}{L \times f \times (Vin - Vout)} \quad \text{(inverted DC/DC)}$$

$$Ipeak = \frac{Vout}{Vin \times \eta} \times Iout + \frac{1}{2} \times \frac{Vin \times (Vout - Vin)}{L \times f \times Vout} \quad \text{(step-up DC/DC)}$$

   η: Efficiency(<0.92), f: Switching frequency, L: inductance

   The second terms of the equations above are ripple current of the inductor which should be set at about 20 to 50% of the maximum output current.

   (Note) Applying a current more than the current rating of the inductor brings the inductor into magnetic saturation, which may lead to lower efficiency or undesired output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the inductor.

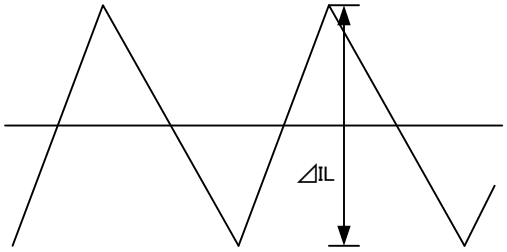


Figure 33. Ripple Current

2. Output capacitor
   A ceramic capacitor with low ESR is recommended for output in order to reduce output ripple.
   There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration.
   When ceramic capacitor is used, the output ripple voltage is obtained by the following equation.

$$\Delta VPP = Ipeak \times R_{ESR} + \frac{Iout}{Cout} \times \frac{-Vout}{Vin - Vout} \times \frac{1}{f} \quad \text{(inverted DC/DC)}$$

$$\Delta VPP = Ipeak \times R_{ESR} + \frac{Iout}{Cout} \times \frac{Vout - Vin}{Vout} \times \frac{1}{f} \quad \text{(step-up DC/DC)}$$

   Setting must be performed so that output ripple is within the allowable ripple voltage.

3. Output voltage

CH1

The reference voltage of CH1 is 1.0V and the internal reference voltage of the ERROR AMP is 0V.
Output voltage should be obtained by following equation.

$$VOUT1 = -\frac{R1A}{R1B} \times 1.0V$$

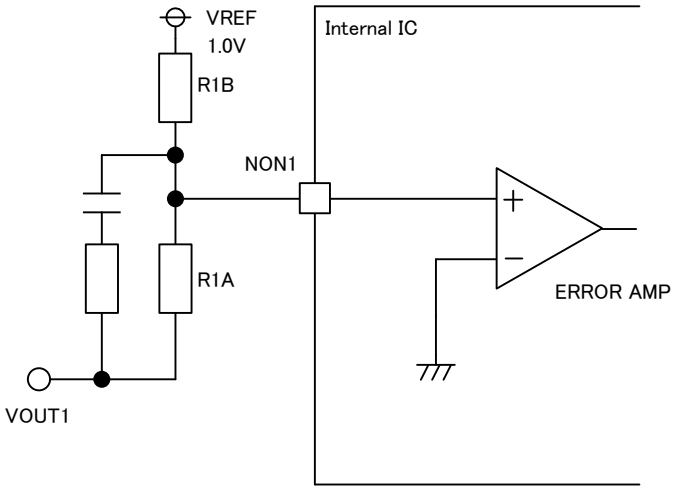


Figure 34. CH1 setting of feedback resistance

CH2

The internal reference voltage of the ERROR AMP is 0.8V.
Output voltage should be obtained by following equation.

$$VOUT2 = \frac{R2A + R2B}{R2B} \times 0.8V$$

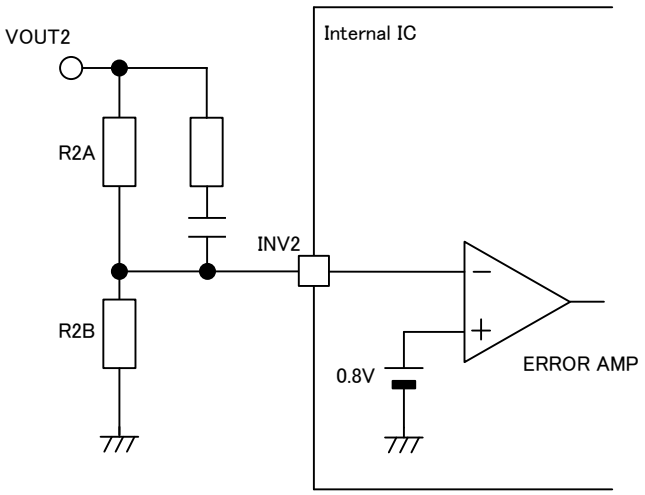


Figure 35. CH2 setting of feedback resistance

Notice for application

1. Soft-start function of inverted DC/DC

Soft-start function of inverted DC/DC is due to the soft-start function of VREF, voltage reference for inverted channel.
When inverted channel is OFF, VREF voltage is discharged by internal MOS (typ. 150Ω).

When inverted channel is turned ON immediately after turning OFF, in case VREF voltage is not fully discharged, there will be no soft-start of inverted output and it may cause in-rush current at the time of start-up.

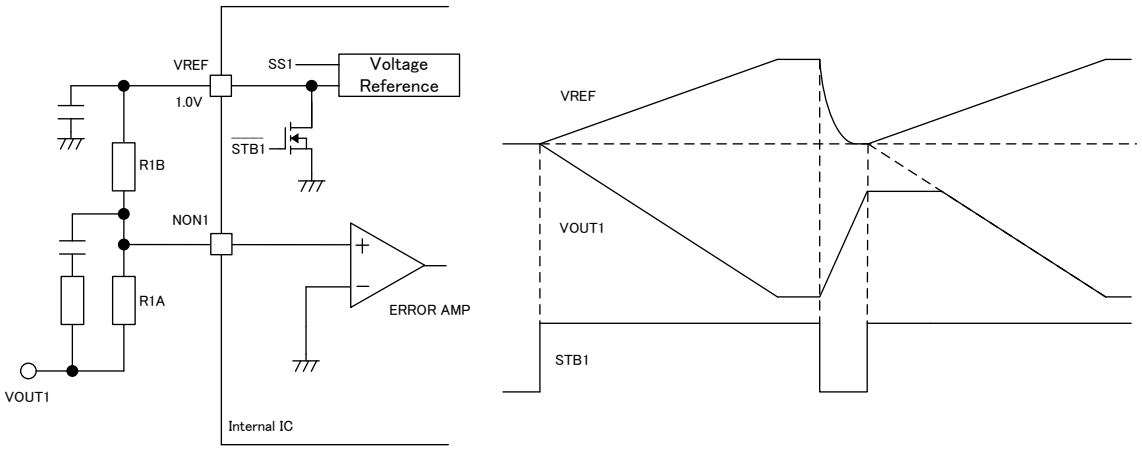


Figure 36. CH1 soft-start function

2. Soft-start time of high-side switch

Soft-start time of high-side switch is determined by input voltage and output voltage setting.
Soft-start time T_{HSWSS} is determined by following equation.

$$T_{HSWSS} = 1.6\text{msec} \times \frac{VDD - Vf}{Vout}$$

At high-side switch soft-start time, the current to output capacitor is determined by the following.

$$I_{HSWSS} = \frac{Cout \times Vout}{1.6\text{msec}}$$

As example, I_{HSWSS} = 53mA, when Cout=4.7uF and Vout=18V,

3. Capable output current

Capable output current of inverted DC/DC and step-up DC/DC is determined by input voltage and output voltage setting, because Duty or operating range of FET is limited. The table below shows the capable output current in input and output voltage conditions.
Table below shows the typical output current when an IC is off-latch. Not production tested.

Iout[mA]		VOUT1[V]	
		−6	−9
VDD[V]	2.5	220	123
	3	350	243
	3.5	480	343
	4	602	436
	4.5	722	
	5	844	
	5.5	952	

Iout [mA]		VOUT2[V]				
		6	9	12	15	18
VDD[V]	2.5	252	150	76		
	3	406	252	177	97	
	3.5	584	364	268	200	120
	4	777	481	352	273	215
	4.5	1000	608	440	340	276
	5		738	534	414	334
	5.5		876	644	487	383

Figure 37. Output Current Ability

4. Termination of not-in-use channel

When only inverted DC/DC is used, terminals should be set as below.

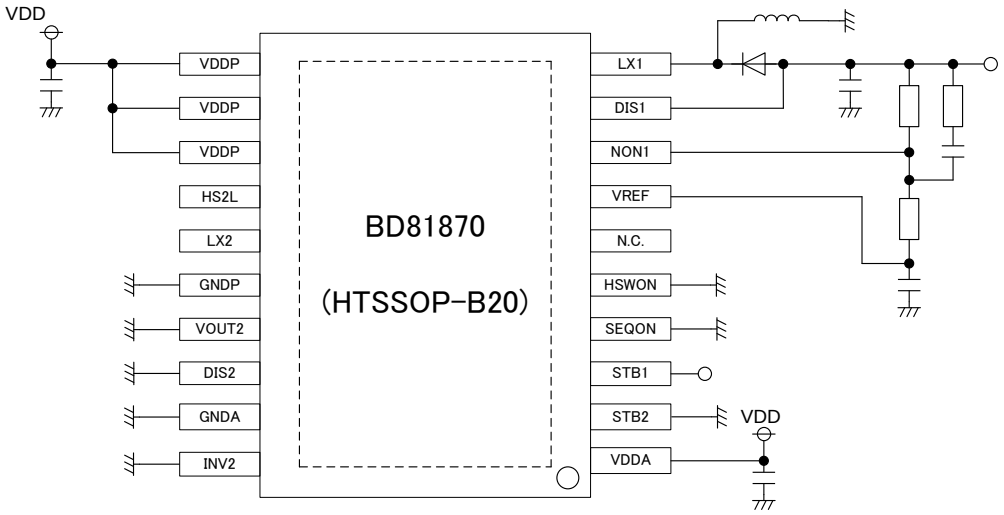


Figure 38. Disable CH2 boost DC/DC channel

When only step-up DC/DC is used, terminals should be set as below.

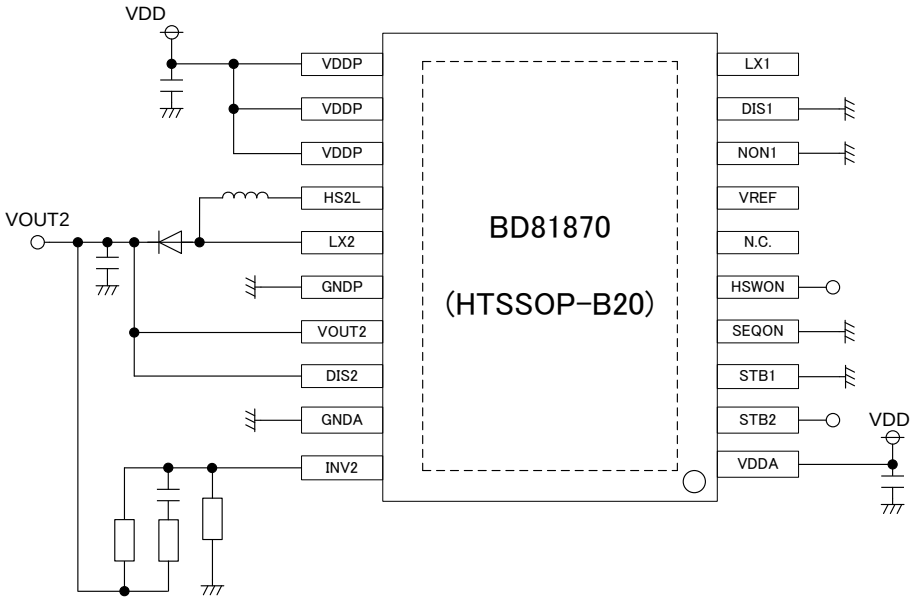


Figure 39. Disable CH1 inverted DC/DC channel

Layout Guideline

DC/DC converter switching line must be as short and thick as possible to reduce line impedance. If the wiring is long, ringing caused by switching would increase and this may exceed the absolute maximum voltage ratings. If the parts are located far apart, consider inserting a snubber circuit.

The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective. When there is unused area on PCB, please arrange the copper foil plain of DC nodes, such as GND, VIN and VOUT for helping heat dissipation of IC or circumference parts.

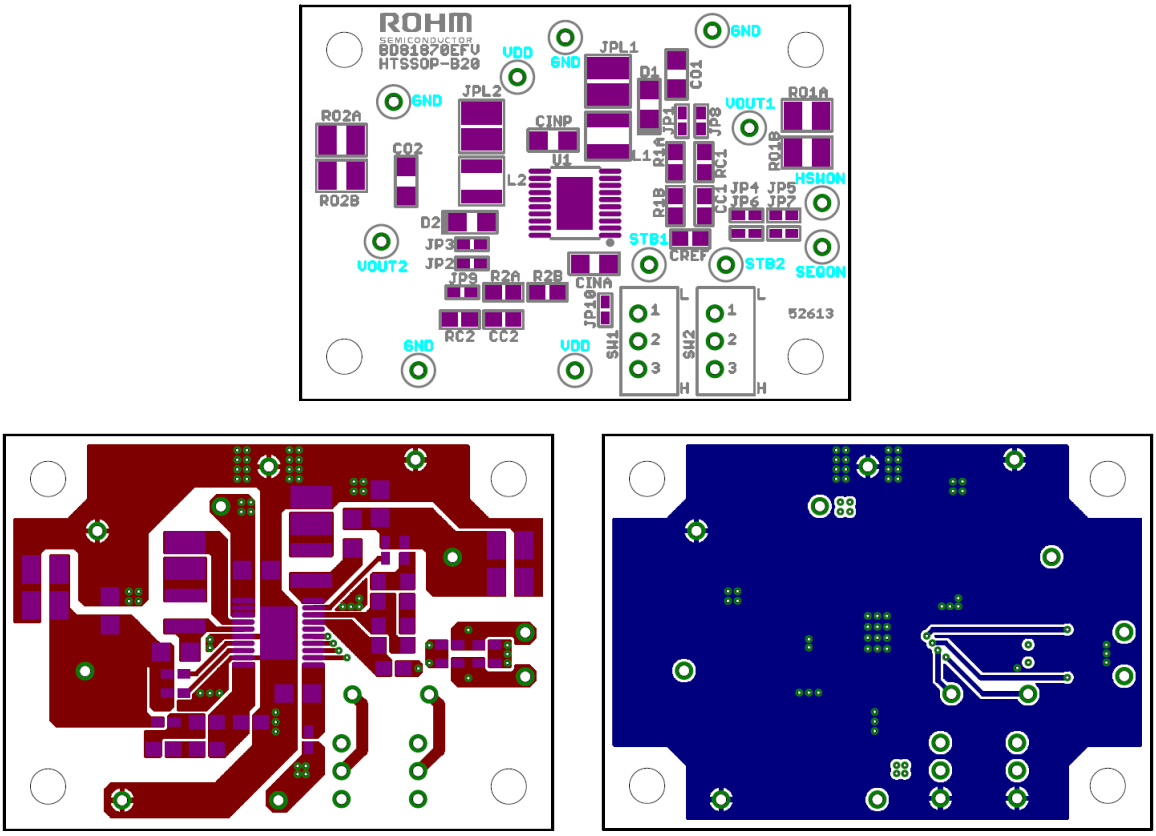
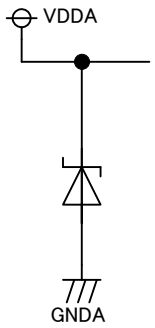
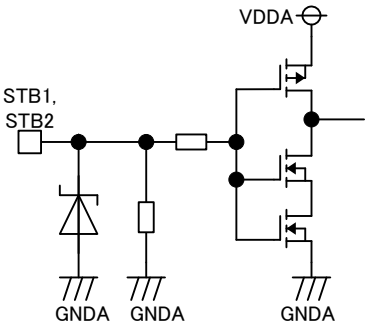
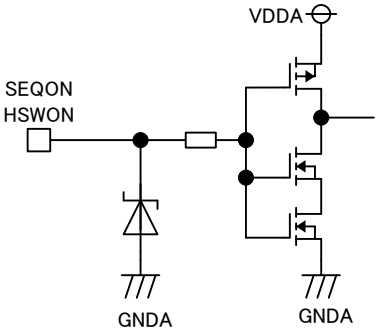
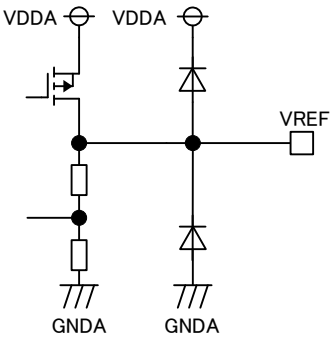
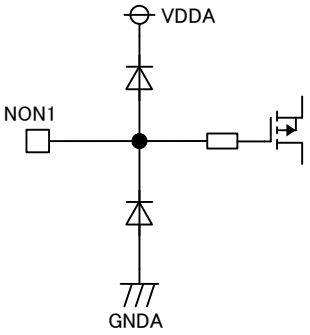
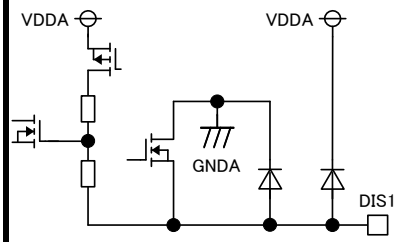
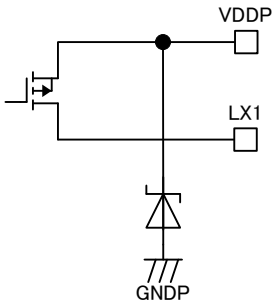
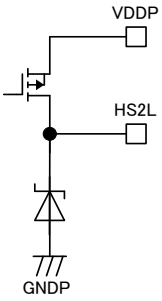
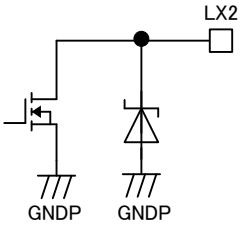
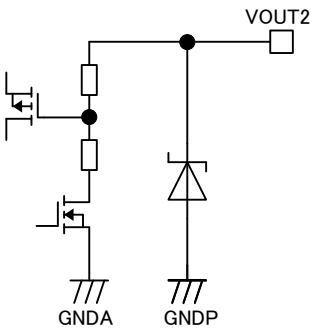
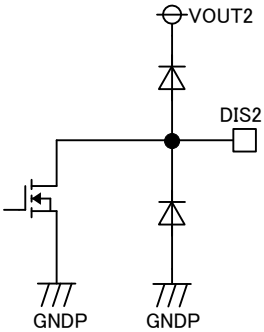
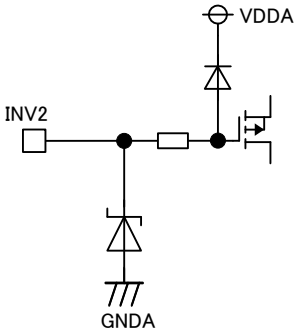


Figure 40. PCB Pattern Reference

I/O Equivalent Circuit

VDDA	STB2, STB1	SEQON, HSWON
		
VREF	**NON1**	**DIS1**
		
LX1, VDDP	**HS2L**	**LX2**
		
VOUT2	**DIS2**	**INV2**
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

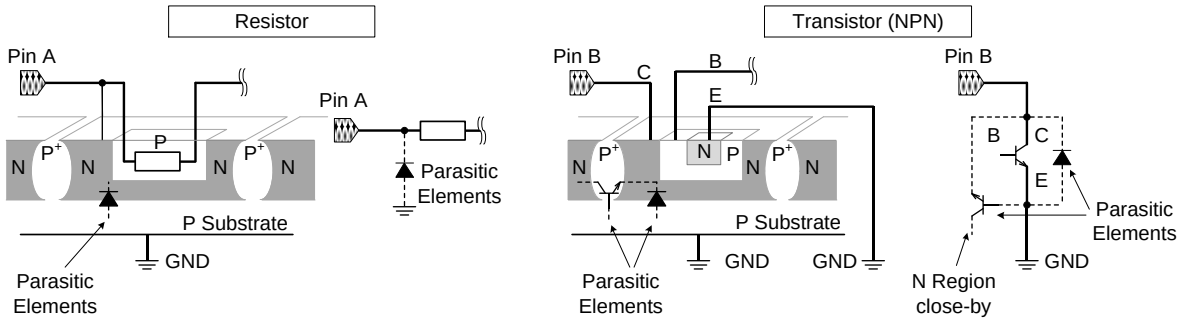


Figure 41. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

Operational Notes – continued

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

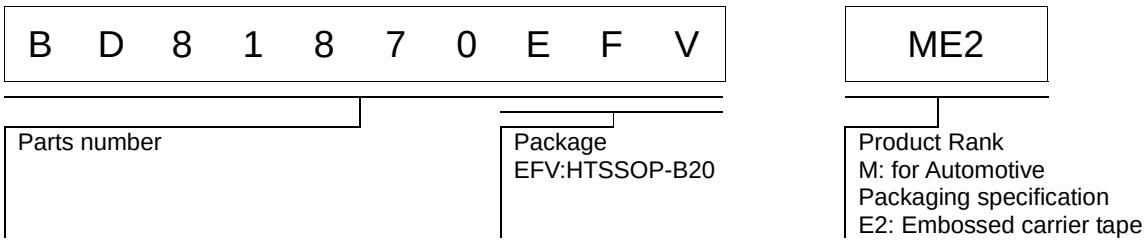
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

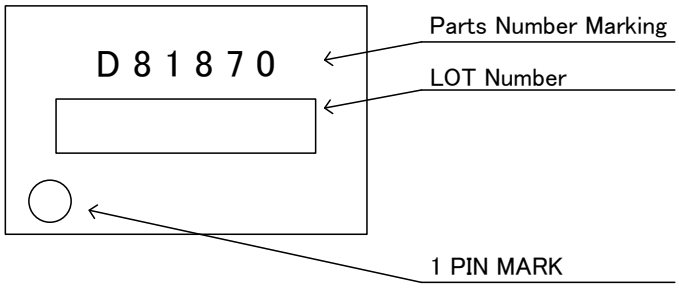
17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

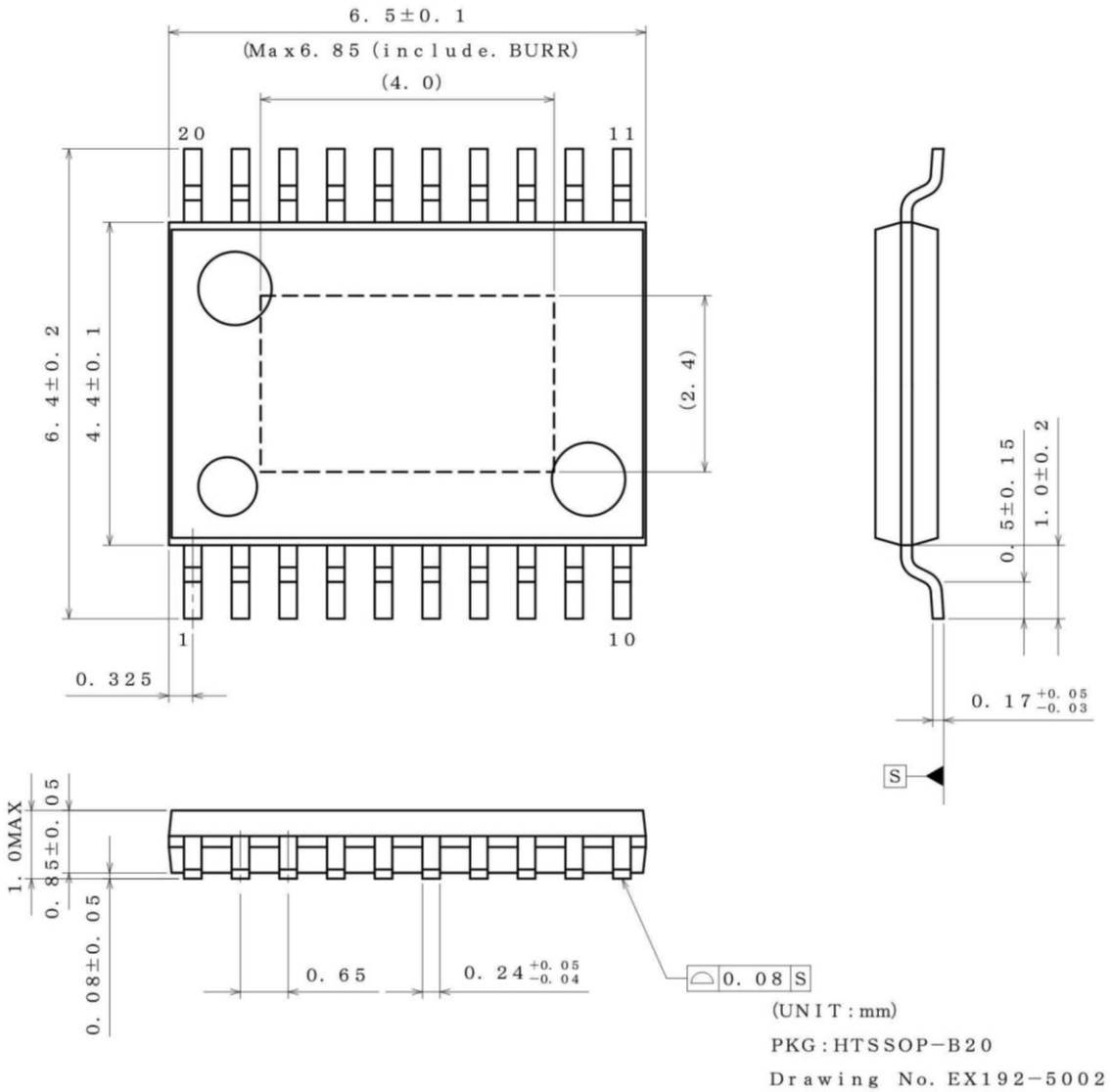


Marking Diagram



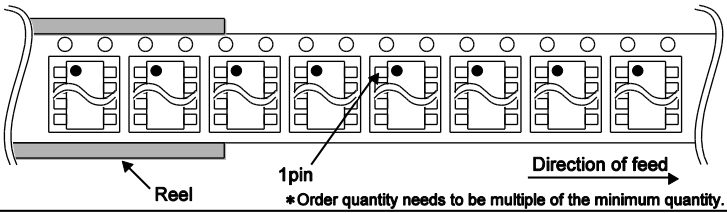
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

日付	Revision	変更内容
29.July.2016	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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Distribution Inventory

Part Number	BD81870EFV-M
Package	HTSSOP-B20
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes