Zynq UltraScale+ Device Packaging and Pinouts

Product Specification User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/10/2018	1.5	In Chapter 1: Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices. This includes updates to Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-5, Table 1-6, and Table 1-7. Added Figure 1-30 through Figure 1-41. In Chapter 3: Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR ASCII file links, see Table 3-2. In Chapter 4: Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices to Table 4-1. In Chapter 5: Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR mechanical drawings, see Table 5-2. In Chapter 7: Added the FFVD1156, FFVE1156, FSVE1156, FFVG1517, FSVG1517, FFVF1760, and FSVF1760 packages to Table 7-1. In Chapter 8: Revised the guidelines in Table 8-1 for Ramp-up rate, Peak temperature (lead/ball), and Peak temperature (body). Revised the same information in Figure 8-1. Added the FFVD1156, FFVE1156, FSVE1156, FFVG1517, FSVG1517, FFVF1760, and FSVF1760 packages to Table 8-2. In Chapter 10: Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices to Table 10-1 and added Note 1. In Chapter 11, Updated the System Level Heat Sink Solutions section and added the Heat Sink Removal and Measurement Debug sections.
12/21/2017	1.4	Added the XAZU2EG and XAZU3EG devices throughout the document. In Chapter 1, Revise the VCCINT_VCU description in Table 1-4. Updated the ZU11EG (Figure 1-16 through Figure 1-20) PCIE4 bank coordinates. In Chapter 2, Updated LPDDR4 Pin Swapping Restrictions and DDR4 Pin Swapping Restrictions and removed Figure 2-1: DDR Controller Implementation of DQ Mapping. In Table 2-2, updated the PS_DDR_ZQ connections. In Chapter 5, Revised Figure 5-4: Symbol A from (2.57/2.77/2.97) to (2.48/2.68/2.88) and Symbol A2 from (1.27/1.42/1.62) to (1.18/1.33/1.48). In Chapter 6, Revised the top mark diagram to show both older device versions and newer ones with a 2D bar code. In Chapter 8, added an Important note on page 176 about reflow rework. In Chapter 10, updated the SFVC784, FFVC900, FFVB1156, FFVC1156, FFVB1517, FFVF1517 data to account for the stamped lid in Table 10-1.

Date	Version	Revision
08/29/2017	1.3	In Chapter 1, updated Figure 1-3, Figure 1-13, Figure 1-14, Figure 1-15, Figure 1-21, Figure 1-22, Figure 1-23, Figure 1-24, Figure 1-25, Figure 1-26, Figure 1-27, and Figure 1-28. Revise the VCCINT_VCU description in Table 1-4. In Chapter 2, updated the DDR4 Pin Rules and the DDR4 Pin Swapping Restrictions. In Table 2-2, updated the configurations for PS_DDR_CK_N1 (DDR4 1Rank). In Chapter 3, updated the package specification designation of many of the packages listed in Table 3-1. In Chapter 4, updated Table 4-1 and added the following device diagrams: SFVC784 Package–XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG, SFVC784 Package–XCZU4EV and XCZU5EV, FBVB900 Package–XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG, FBVB900 Package–XCZU4EV and XCZU5EV, FFVF1517 Package–XCZU7CG and XCZU7EG, FFVC1156 Package–XCZU7EV, FFVC1156 Package–XCZU11EG, FFVB1517 Package–XCZU11EG, FFVF1517 Package–XCZU11EG, and FFVC1760 Package–XCZU11EG. In Chapter 5: Replace Figure 5-3, added Figure 5-4, Figure 5-5, Figure 5-11, and Figure 5-17. In Table 8-2, update the FFV packages to a mass reflow of 245°C.
01/13/2017	1.2	Added the following devices throughout: XCZU2CG, XCZU3CG, XCZU4CG, XCZU4EG, XCZU5CG, XCZU5EG, XCZU6CG, XCZU7CG, XCZU7EG, and XCZU9CG. In Table 1-3, revised the available PS I/O pin values for the SBVA484 and SFVA625 packages. In Table 1-4, updated the PS_MODE directions and the pin descriptions in the Power/Ground Pins section. In Table 1-6, revised the XCZU4 bank numbers and updated the FBVB900 mapping. Revised the mapping for the FBVB900 package in Table 1-7. Revised the Bank Locations of Dedicated and Multi-Function Pins section. Updated the HD I/O bank numbers in Figure 1-20. Added Chapter 2, PS Memory Interface Pin Guidelines. Added the Chapter 3, Package Specifications Designations section. In Table 3-1, updated links. Chapter 4, Device Diagrams and Chapter 5, Mechanical Drawings have updated tables and new diagrams. Revised the Bar Code section of Table 6-1 to include changes outlined in XCN16014: *Top Marking change for 7 Series, UltraScale, and UltraScale+ Products*. Updated the AUTOMOTIVE APPLICATIONS DISCLAIMER.
06/14/2016	1.1	In Table 1-3, updated Note 1 and the SBVA484 package total user HP I/Os. Clarified the I2C_SCLK and I2C_SDA descriptions and added SMBALERT and VCCINT_VCU to Table 1-4. Also updated the Multi-gigabit Serial Transceiver Pins (GTHE4, GTYE4, and PS-GTR) descriptions, Added further descriptions in the Die Level Bank Numbering Overview including adding an example device diagram (Figure 1-1). In Chapter 4, added new figures and updated all of the graphics because the PERSTN pins and SMBALERT pins have moved. Updated Figure 5-7 and added Figure 5-8. Added the bar code description in Chapter 6.
01/20/2016	1.0.2	Replaced the missing graphics in Chapter 1.
12/18/2015	1.0.1	Updated the package file links in Chapter 3.
11/24/2015	1.0	Initial Xilinx release.

Table of Contents

Packaging Overview

Introduction to the UltraScale Architecture

The Xilinx® UltraScale™ architecture is the first ASIC-class All Programmable architecture to enable multi-hundred gigabit-per-second levels of system performance with smart processing, while efficiently routing and processing data on-chip. UltraScale architecture-based devices address a vast spectrum of high-bandwidth, high-utilization system requirements by using industry-leading technical innovations, including next-generation routing, ASIC-like clocking, 3D-on-3D ICs, multiprocessor SoC (MPSoC) technologies, and new power reduction features. The devices share many building blocks, providing scalability across process nodes and product families to leverage system-level investment across platforms.

Virtex® UltraScale+™ devices provide the highest performance and integration capabilities in a FinFET node, including both the highest serial I/O and signal processing bandwidth, as well as the highest on-chip memory density. As the industry's most capable FPGA family, the Virtex UltraScale+ devices are ideal for applications including 1+Tb/s networking and data center and fully integrated radar/early-warning systems.

Virtex UltraScale devices provide the greatest performance and integration at 20 nm, including serial I/O bandwidth and logic capacity. As the industry's only high-end FPGA at the 20 nm process node, this family is ideal for applications including 400G networking, large scale ASIC prototyping, and emulation.

Kintex® UltraScale+ devices provide the best price/performance/watt balance in a FinFET node, delivering the most cost-effective solution for high-end capabilities, including transceiver and memory interface line rates as well as 100G connectivity cores. Our newest mid-range family is ideal for both packet processing and DSP-intensive functions and is well suited for applications including wireless MIMO technology, Nx100G networking, and data center.

Kintex UltraScale devices provide the best price/performance/watt at 20 nm and include the highest signal processing bandwidth in a mid-range device, next-generation transceivers, and low-cost packaging for an optimum blend of capability and cost-effectiveness. The family is ideal for packet processing in 100G networking and data centers applications as well as DSP-intensive processing needed in next-generation medical imaging, 8k4k video, and heterogeneous wireless infrastructure.

Zynq® UltraScale+ devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing. Integrating an ARM®-based system for advanced analytics and on-chip programmable logic for task acceleration creates unlimited possibilities for applications including 5G Wireless, next generation ADAS, and Industrial Internet-of-Things.

This user guide is part of the Zynq UltraScale+ MPSoC documentation suite.

Zynq UltraScale+ Device Packaging and Pinouts

This section describes the packages and pinouts for the in various organic flip-chip 0.8 mm and 1.0 mm pitch BGA packages.

IMPORTANT: *All standard packages are lead-free (signified by an additional V in the package name). All devices supported in a particular package are footprint compatible. Each device is split into I/O banks to allow for flexibility in the choice of I/O standards. See the UltraScale Architecture SelectIO Resources User Guide (UG571) [Ref 4].*

The flip-chip assembly materials for the Zynq UltraScale+ devices are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm^2 or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

Differences from Previous Generations

The packaging and pinout specifications for Zynq UltraScale+ devices differ from past generations, including the Zynq-7000 AP SoCs. These details are outlined in this section.

- All package and die components, including flip-chip solder bumps, are lead-free.
- Package names contain a single-character alphabetic designator followed by the exact number of pins found on the package.
- VCCAUX_IO pins are not divided into bank groups. VCCAUX_IO must be connected to VCCAUX at the board level.
- Internal logic is separated from I/O logic by the addition of the VCCINT_IO power pins. VCCINT_IO must be connected to VCCBRAM (depending on the device speed grade and voltage settings) at the board level.
- Groups of gigabit serial transceiver (GT) power pins are separated by column for each column of GT Quads.
- Standard HP I/O banks each have a total of 52 SelectIO™ pins, optionally configurable as (up to) 24 differential pairs.

- Standard HD I/O banks each have a total of 24 SelectIO pins, optionally configurable as (up to) 12 differential pairs.
- Each bank has one dedicated VREF pin. These pins cannot be used as user I/Os.
- Four differential clock pin pairs per bank consist of a single type of global clock (GC or HDGC) input.
- Four memory byte groups per HP I/O bank are each separated into an upper and a lower memory byte group.
- Multiple PL configuration pins are removed.
- A POR_OVERRIDE pin is used to override the default power-on-reset delay. See Table 1-4.

Device/Package Combinations

Table 1-1 shows the size and BGA pitch of the Zynq UltraScale+ device packages.

Table 1-1: **Package Specifications**

Packages	Description	Package Specifications		
		Package Type	**Pitch (mm)**	**Size (mm)**
SBVA484	Flip-chip, bare-die	BGA	0.8	19 x 19
SFVA625	Flip-chip			21 x 21
SFVC784	Flip-chip			23 x 23
FBVB900	Flip-chip, bare-die		1.0	31 x 31
FFVC900	Flip-chip			
FFVB1156				35 x 35
FFVC1156				
FFVD1156				
FFVE1156				
FFVB1517				40 x 40
FFVF1517				
FFVG1517				
FFVC1760				42.5 x 42.5
FFVD1760				
FFVF1760				42.5 x 42.5
FFVE1924				45 x 45
FSVE1156	Flip-chip, lidless with stiffener ring.			35 x 35
FSVG1517				40 x 40
FSVF1760				42.5 x 42.5

Gigabit Transceiver Channels by Device/Package

Table 1-2 lists the quantity of gigabit transceiver channels for the Zynq UltraScale+ devices. In all devices, a PS-GTR, GTH, or GTY channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-2: **Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package**

Device	Package	PS-GTR Channels	GTH Channels	GTY Channels
XCZU2CG	SBVA484	4	0	0
XCZU2EG		4	0	0
XCZU3CG		4	0	0
XCZU3EG		4	0	0
XAZU2EG		4	0	0
XAZU3EG		4	0	0
XCZU2CG	SFVA625	4	0	0
XCZU2EG		4	0	0
XCZU3CG		4	0	0
XCZU3EG		4	0	0
XAZU2EG		4	0	0
XAZU3EG		4	0	0
XCZU2CG	SFVC784	4	0	0
XCZU2EG		4	0	0
XCZU3CG		4	0	0
XCZU3EG		4	0	0
XCZU4CG		4	4	0
XCZU4EG		4	4	0
XCZU4EV		4	4	0
XCZU5CG		4	4	0
XCZU5EG		4	4	0
XCZU5EV		4	4	0
XAZU2EG		4	0	0
XAZU3EG		4	0	0

Table 1-2: **Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package *(Cont'd)***

Device	Package	PS-GTR Channels	GTH Channels	GTY Channels
XCZU4CG	FBVB900	4	16	0
XCZU4EG		4	16	0
XCZU4EV		4	16	0
XCZU5CG		4	16	0
XCZU5EG		4	16	0
XCZU5EV		4	16	0
XCZU7CG		4	16	0
XCZU7EG		4	16	0
XCZU7EV		4	16	0
XCZU6CG	FFVC900	4	16	0
XCZU6EG		4	16	0
XCZU9CG		4	16	0
XCZU9EG		4	16	0
XCZU15EG		4	16	0
XCZU6CG	FFVB1156	4	24	0
XCZU6EG		4	24	0
XCZU9CG		4	24	0
XCZU9EG		4	24	0
XCZU15EG		4	24	0
XCZU7CG	FFVC1156	4	20	0
XCZU7EG		4	20	0
XCZU7EV		4	20	0
XCZU11EG		4	20	0
XCZU21DR	FFVD1156	4	0	16
XCZU25DR	FFVE1156	4	0	8
XCZU27DR		4	0	8
XCZU28DR		4	0	8
XCZU25DR	FSVE1156	4	0	8
XCZU27DR		4	0	8
XCZU28DR		4	0	8
XCZU11EG	FFVB1517	4	16	0
XCZU17EG		4	16	0
XCZU19EG		4	16	0

Table 1-2: **Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package *(Cont'd)***

Device	Package	PS-GTR Channels	GTH Channels	GTY Channels
XCZU7CG	FFVF1517	4	24	0
XCZU7EG		4	24	0
XCZU7EV		4	24	0
XCZU11EG		4	32	0
XCZU25DR	FFVG1517	4	0	8
XCZU27DR		4	0	16
XCZU28DR		4	0	16
XCZU25DR	FSVG1517	4	0	8
XCZU27DR		4	0	16
XCZU28DR		4	0	16
XCZU11EG	FFVC1760	4	32	16
XCZU17EG		4	32	16
XCZU19EG		4	32	16
XCZU17EG	FFVD1760	4	44	28
XCZU19EG		4	44	28
XCZU29DR	FFVF1760	4	0	16
XCZU29DR	FSVF1760	4	0	16
XCZU17EG	FFVE1924	4	44	0
XCZU19EG		4	44	0

User I/O Pins by Device/Package

Table 1-3 lists the number of available PS I/Os, 3.3V-capable high-density (HD), and 1.8V-capable high-performance (HP) I/Os and the number of HD or HP differential I/O for each device/package combination.

Table 1-3: **Available I/O Pins by Device/Package**

Device	Package	PS I/Os	Total User I/O		Differential I/O	
			HD[(1)]	HP[(1)]	HD	HP
XCZU2CG	SBVA484	170	24	58	24	52
XCZU2EG		170	24	58	24	52
XCZU3CG		170	24	58	24	52
XCZU3EG		170	24	58	24	52
XAZU2EG		170	24	58	24	52
XAZU3EG		170	24	58	24	52
XCZU2CG	SFVA625	170	24	156	24	144
XCZU2EG		170	24	156	24	144
XCZU3CG		170	24	156	24	144
XCZU3EG		170	24	156	24	144
XAZU2EG		170	24	156	24	144
XAZU3EG		170	24	156	24	144
XCZU2CG	SFVC784	214	96	156	96	144
XCZU2EG		214	96	156	96	144
XCZU3CG		214	96	156	96	144
XCZU3EG		214	96	156	96	144
XCZU4CG		214	96	156	96	144
XCZU4EG		214	96	156	96	144
XCZU4EV		214	96	156	96	144
XCZU5CG		214	96	156	96	144
XCZU5EG		214	96	156	96	144
XCZU5EV		214	96	156	96	144
XAZU2EG		214	96	156	96	144
XAZU3EG		214	96	156	96	144

Table 1-3: **Available I/O Pins by Device/Package *(Cont'd)***

Device	Package	PS I/Os	Total User I/O		Differential I/O	
			HD[(1)]	HP[(1)]	HD	HP
XCZU4CG	FBVB900	214	48	156	48	144
XCZU4EG		214	48	156	48	144
XCZU4EV		214	48	156	48	144
XCZU5CG		214	48	156	48	144
XCZU5EG		214	48	156	48	144
XCZU5EV		214	48	156	48	144
XCZU7CG		214	48	156	48	144
XCZU7EG		214	48	156	48	144
XCZU7EV		214	48	156	48	144
XCZU6CG	FFVC900	214	48	156	48	144
XCZU6EG		214	48	156	48	144
XCZU9CG		214	48	156	48	144
XCZU9EG		214	48	156	48	144
XCZU15EG		214	48	156	48	144
XCZU6CG	FFVB1156	214	120	208	120	192
XCZU6EG		214	120	208	120	192
XCZU9CG		214	120	208	120	192
XCZU9EG		214	120	208	120	192
XCZU15EG		214	120	208	120	192
XCZU7CG	FFVC1156	214	48	312	48	288
XCZU7EG		214	48	312	48	288
XCZU7EV		214	48	312	48	288
XCZU11EG		214	48	312	48	288
XCZU21DR	FFVD1156	214	72	208	72	192
XCZU25DR	FFVE1156	214	48	104	48	96
XCZU27DR		214	48	104	48	96
XCZU28DR		214	48	104	48	96
XCZU25DR	FSVE1156	214	48	104	48	96
XCZU27DR		214	48	104	48	96
XCZU28DR		214	48	104	48	96
XCZU11EG	FFVB1517	214	72	416	72	384
XCZU17EG		214	72	572	72	528
XCZU19EG		214	72	572	72	528

Table 1-3: **Available I/O Pins by Device/Package *(Cont'd)***

Device	Package	PS I/Os	Total User I/O		Differential I/O	
			HD(1)	HP(1)	HD	HP
XCZU7CG	FFVF1517	214	48	416	48	384
XCZU7EG		214	48	416	48	384
XCZU7EV		214	48	416	48	384
XCZU11EG		214	48	416	48	384
XCZU25DR	FFVG1517	214	48	299	48	276
XCZU27DR		214	48	299	48	276
XCZU28DR		214	48	299	48	276
XCZU25DR	FSVG1517	214	48	299	48	276
XCZU27DR		214	48	299	48	276
XCZU28DR		214	48	299	48	276
XCZU11EG	FFVC1760	214	96	416	96	384
XCZU17EG		214	96	416	96	384
XCZU19EG		214	96	416	96	384
XCZU17EG	FFVD1760	214	48	260	48	240
XCZU19EG		214	48	260	48	240
XCZU29DR	FFVF1760	214	96	312	96	288
XCZU29DR	FSVF1760	214	96	312	96	288
XCZU17EG	FFVE1924	214	96	572	96	528
XCZU19EG		214	96	572	96	528

Notes:

1. The maximum user I/O numbers do not include the GT serial transceiver pins or the PUDC_B and POR_OVERRIDE pins used for configuration.

Pin Definitions

Table 1-4 lists the pin definitions.

Table 1-4: **Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_L[*1 to 24*][P or N]_T[*0 to 3*] [*U or L*]_N[*0 to 12*]_ [multi-function]_[bank number] or IO_T[*0 to 3*][*U or L*]_N[*0 to 12*]_[multi-function]_[bank number]			
	Dedicated	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. Each user I/O pin name consists of several indicator labels, where: • IO indicates a user I/O pin. • L[*1 to 24*] indicates a unique differential pair with P (positive) and N (negative) sides. User I/O pins without the L indicator are single-ended. • T[*0 to 3*][*U or L*] indicates the assigned byte group and nibble location (upper or lower portion) within that group for the pin. • N[*0 to 12*] the number of the I/O within its byte group. • [*multi-function*] indicates any other functions that the pin can provide. If not used for this function, the pin can be a user I/O. • [*bank number*] indicates the assigned bank for the user I/O pin.
User I/O Multi-Function Pins			
GC or HDGC	Multi-function	Input	Four global clock (GC or HDGC) pin pairs are in each bank. HDGC pins have direct access to the global clock buffers. GC pins have direct access to the global clock buffers and the MMCMs and PLLs that are in the clock management tile (CMT) adjacent to the same I/O bank. GC and HDGC inputs provide dedicated, high-speed access to the internal global and regional clock resources. GC and HDGC inputs use dedicated routing and must be used for clock inputs where the timing of various clocking features is imperative. Up-to-date information about designing with the GC (or HDGC) pin is available in the *UltraScale Architecture Clocking Resources User Guide* (UG572) [Ref 5]
VRP(1)	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with a reference resistor).

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
DBC QBC	Multi-function	Input	Byte lane clock (DBC and QBC) input pin pairs are clock inputs directly driving source synchronous clocks to the bit slices in the I/O banks. In memory applications, these are also known as DQS. For more information, consult the *UltraScale Architecture SelectIO Resources User Guide* (UG571) [Ref 4].
PERSTN[*0 to 1*]	Multi-function	Input	Default reset pin locations for the integrated block for PCI Express.
Configuration Pins			
For more information on configuration and recommended external pull-up/pull-down resistors, see the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 8] and the *UltraScale Architecture PCB and Pin Planning User Guide* (UG583) [Ref 12].			
PUDC_B	Dedicated	Input	Active-Low input enables internal pull-ups during configuration on all SelectIO pins: 0 = Weak preconfiguration I/O pull-up resistors enabled. 1 = Weak preconfiguration I/O pull-up resistors disabled. PUDC_B is powered by V_{CCAUX}.
POR_OVERRIDE	Dedicated	Input	Power-on reset delay override. 0 = Standard PL power-on delay time (recommended default). 1 = Faster PL power-on delay time. **CAUTION!** *Do not allow this pin to float before and during configuration. This pin must be tied to V_{CCINT} or GND.*
PS_DONE	Dedicated	Output	PS DONE signal. Requires an external pull-up resistor.
PS_ERROR_OUT	Dedicated	Output	PS error indication.
PS_ERROR_STATUS	Dedicated	Output	PS error status.
PS_INIT_B	Dedicated	Input/Output	Initialization completion indicator after POR. High voltage indicates completion of initialization (PL). Requires an external pull-up resistor.
PS_JTAG_TCK	Dedicated	Input	JTAG data clock.
PS_JTAG_TDI	Dedicated	Input	JTAG data input.
PS_JTAG_TDO	Dedicated	Output	JTAG data output.
PS_JTAG_TMS	Dedicated	Input	JTAG mode select.
PS_MODE	Dedicated	Input/Output	PS MIO mode selection pins.
PS_PADI	Dedicated	Input	Crystal pad input. Real-time clock (RTC).
PS_PADO	Dedicated	Output	Crystal pad output. Real-time clock (RTC).

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS_POR_B	Dedicated	Input	Power on reset. PS_POR_B must be held at 0 until all PS power supplies meet voltage requirements and the PS_CLK reference is within specification. When deasserted the PS begins the boot process.
PS_PROG_B	Dedicated	Input	PROG_B signal to reset configuration block. Requires an external pull-up resistor.
PS_REF_CLK	Dedicated	Input	System reference clock. PS_CLK must be between 27 MHz and 60 MHz.
PS_SRST_B	Dedicated	Input	System reset. For use when debugging. When 0, forces the PS to enter the system reset sequence.
Power/Ground Pins			
For more information on voltage specifications see the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* [Ref 6] or the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* [Ref 7].			
GND	Dedicated	N/A	Ground.
RSVDGND	Dedicated	N/A	Reserved pins that must be tied to GND. ***Note:*** These pins are labeled differently depending upon the device. They can serve a different purpose between footprint compatible devices. To migrate to a footprint compatible device, account for any variation in pin functionality.
RSVD	Dedicated	N/A	Reserved pin. Leave floating.
VCCINT	Dedicated	N/A	Power-supply pins for the PL internal logic.
VCCINT_IO	Dedicated	N/A	Power-supply pins for the I/O banks. VCCINT_IO must be connected to VCCBRAM on the board.
VCCINT_VCU	Dedicated	N/A	Power-supply pins for the video codec unit (EV devices only). ***Note:*** If the video codec unit is not used, then connect the VCCINT_VCU pins to GND to reduce power. In the CG and EG devices, the EV device VCCINT_VCU pins appear as RSVDGND pins. ***Note:*** When migrating from an EV device to a CG or EG device in the same package, Xilinx recommends connecting the VCCINT_VCU pins to GND to reduce power. Further VCCINT_VCU migration guidelines are available in *UltraScale Architecture PCB and Pin Planning User Guide* (UG583)[Ref 12]. **IMPORTANT:** *V_{CCINT_VCU} requires its own dedicated power supply. Do not combine with other power rails on the PCB.*
VCCAUX	Dedicated	N/A	Power-supply pins for auxiliary circuits.

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
VCCAUX_IO	Dedicated	N/A	Auxiliary power-supply pins for the I/O banks. VCCAUX_IO must be connected to VCCAUX on the board.
VCCBRAM	Dedicated	N/A	Power-supply pins for PL block RAM logic.
VCCO_[bank number](2)	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VREF_[bank number]	Dedicated	N/A	Voltage reference for input pins (per bank).
VCCADC	Dedicated	N/A	System Monitor analog supply voltage.
GNDADC	Dedicated	N/A	System Monitor analog ground.
VCC_PSADC	Dedicated	N/A	PS ADC supply voltage.
GND_PSADC	Dedicated	N/A	PS ADC analog ground.
VCC_PSAUX	Dedicated	N/A	PS auxiliary circuits supply voltage.
VCC_PSBATT	Dedicated	N/A	PS RTC battery supply voltage. When not used, tie to GND.
VCC_PSDDR_PLL	Dedicated	N/A	PS DDR PLL supply voltage.
VCC_PSPLL	Dedicated	N/A	PS PLL (DPLL, RPLL, APLL, VPLL, IOPLL) supply voltage.
VCC_PSINTFP	Dedicated	N/A	PS full-power domain supply voltage.
VCC_PSINTFP_DDR	Dedicated	N/A	PS DDR full-power domain supply voltage.
VCC_PSINTLP	Dedicated	N/A	PS low-power domain supply voltage.
VCCO_PSIO[0:3]_ [500:503]			PS I/O supply voltage.
VCCO_PSDDR_504			PS DDR controller I/O supply voltage.
PS MIO Pins			
PS_MIO	Multi-function	Input/Output	Multiplexed I/O can be configured to support multiple I/O interfaces. These interfaces include SPI and Quad-SPI flash, NAND, USB, Ethernet, SDIO, UART, SPI, and GPIO interfaces.
PS DDR Pins			
PS_DDR_DQ	Dedicated	Input/Output	DRAM data.
PS_DDR_DQS_P	Dedicated	Input/Output	DRAM differential data strobe positive.
PS_DDR_DQS_N	Dedicated	Input/Output	DRAM differential data strobe negative.
PS_DDR_ALERT_N	Dedicated	Input	DRAM alert signal.
PS_DDR_ACT_N	Dedicated	Output	DRAM activation command.
PS_DDR_A	Dedicated	Output	DRAM row and column address.
PS_DDR_BA	Dedicated	Output	DRAM bank address.
PS_DDR_BG	Dedicated	Output	DRAM bank group.
PS_DDR_CK_N	Dedicated	Output	DRAM differential clock negative.

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS_DDR_CK	Dedicated	Output	DRAM differential clock positive.
PS_DDR_CKE	Dedicated	Output	DRAM clock enable.
PS_DDR_CS	Dedicated	Output	DRAM chip select.
PS_DDR_DM	Dedicated	Output	DRAM data mask.
PS_DDR_ODT	Dedicated	Output	DRAM termination control.
PS_DDR_PARITY	Dedicated	Output	DRAM parity signal
PS_DDR_RAM_RST_N	Dedicated	Output	DRAM reset signal, active low.
PS_DDR_ZQ	Dedicated	Input/Output	ZQ calibration signal.
System Monitor Pins[(3)]			
AD[0 to 15][P or N]	Multi-function	Input	System Monitor differential auxiliary analog inputs 0–15.
VREFP	Dedicated	N/A	Voltage reference input.
VREFN	Dedicated	N/A	Voltage reference GND.
VP	Dedicated	Input	System Monitor dedicated differential analog input (positive side).
VN	Dedicated	Input	System Monitor dedicated differential analog input (negative side).
I2C_SCLK	Multi-function	Bidirectional	I2C serial clock. Directly connected to the System Monitor DRP interface for I2C operation configuration. **IMPORTANT:** *Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.*
I2C_SDA	Multi-function	Bidirectional	I2C serial data line. Directly connected to the System Monitor DRP interface for I2C operation configuration. **IMPORTANT:** *Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.*

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
SMBALERT	Multi-function	Bidirectional	Optional PMBus alert, interrupt signal. When Low, indicates a system fault that must be cleared using PMBus commands. Connect to SMBALERT_TS. For more information, see the *UltraScale Architecture System Monitor User Guide* [Ref 11]. **IMPORTANT:** *By default, the PMBus is active prior to configuration. Only use as a multi-functional I/O pin in designs that can tolerated this pin being driven prior to configuration.* This pin is present on Kintex UltraScale+ and Virtex UltraScale+ devices.
Multi-gigabit Serial Transceiver Pins (GTHE4, GTYE4, and PS-GTR)			
For more information on the GTH and GTY transceivers, see the *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 9] or *UltraScale Architecture GTY Transceivers User Guide* [Ref 10]. For more information on the PS-GTR transceivers, see the *Zynq UltraScale+ Device Technical Reference Manual* [Ref 8].			
MGTHRX[P or N][0 to 3] _[GT quad number]	Dedicated	Input	RXP and RXN are the differential input pairs for each of the receivers in the GTH Quad.
MGTHTX[P or N][0 to 3] _[GT quad number]	Dedicated	Output	TXP and TXN are the differential output pairs for each of the transmitters in the GTH Quad.
MGTYRX[P or N][0 to 3] _[GT quad number]	Dedicated	Input	RXP and RXN are the differential input pairs for each of the receivers in the GTY Quad.
MGTYTX[P or N][0 to 3] _[GT quad number]	Dedicated	Output	TXP and TXN are the differential output pairs for each of the transmitters in the GTY Quad.
PS_MGTRRX[P or N][0 to 3] _[GT quad number]	Dedicated	Input	RXP and RXN are the differential input pairs for each of the receivers in the PS-GTR Quad.
PS_MGTRTX[P or N][0 to 3] _[GT quad number]	Dedicated	Output	TXP and TXN are the differential output pairs for each of the transmitters in the PS-GTR Quad.
MGTAVCC_[L or R] [N or S][(4)]	Dedicated	Input	Analog power-supply pin for the receiver and transmitter internal circuits for the GTH or GTY transceivers.
PS_MGTRAVCC	Dedicated	N/A	Analog power-supply pin for the receiver and transmitter internal circuits for the PS-GTR transceivers.
MGTAVTT_[L or R] [N or S][(4)]	Dedicated	Input	Analog power-supply pin for the transmitter and receiver termination circuits for the GTH or GTY transceivers.
MGTVCCAUX_[L or R] [N or S][(4)]	Dedicated	Input	Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS_MGTRAVTT	Dedicated	N/A	Analog power-supply pin for the transmitter and receiver termination circuits for the PS-GTR transceivers.
MGTREFCLK[0 or 1] [P or N]	Dedicated	Input/Output	Configured as either reference clock input pins or as RX recovered clock output pins for the GTH or GTY transceivers.
PS_MGTREFCLK[0 to 3] [P or N]	Dedicated	Input	Differential reference clock for the PS-GTR transceivers.
MGTAVTTRCAL_[L or R] [N or S][4]	Dedicated	N/A	Bias current supply for the termination resistor calibration circuit.
MGTRREF_[L or R] [N or S][4]	Dedicated	Input	Calibration resistor pin for the termination resistor calibration circuit for the GTH or GTY transceivers.
PS_MGTRREF	Dedicated	Input	Calibration resistor pin for the termination resistor calibration circuit for the PS-GTR transceivers.
Zynq UltraScale+ RFSoC Dedicated Pins			
VCCSDFEC	Dedicated	N/A	Power supply for the FEC blocks.
VCCINT_AMS	Dedicated	N/A	Digital power supply for the DDC.
ADC_AVCC	Dedicated	N/A	Core ADC and PLL power supply.
ADC_AVCCAUX	Dedicated	N/A	Input buffer and PLL power supply.
ADC_GND	Dedicated	N/A	Analog ground for the ADC.
ADC_SUB_GND	Dedicated	N/A	Digital ground for the ADC.
ADC_CLK_[P or N]	Dedicated	Input	External reference clock for PLL or ADC direct sampling clock input.
VCM01/VCM23	Dedicated	N/A	ADC common mode voltage.
ADC_VIN_[0 to 3]_[P or N]	Dedicated	Input	Analog input signal to the ADC.
ADC_REXT	Dedicated	N/A	ADC external resistor.
DAC_AVCC	Dedicated	N/A	Core DAC and PLL power supply.
DAC_AVCCAUX	Dedicated	N/A	DAC and PLL power supply.
DAC_AVTT	Dedicated	N/A	Termination voltage for on-die 50Ω termination resistors.
DAC_GND	Dedicated	N/A	Analog ground for the DAC.
DAC_SUB_GND	Dedicated	N/A	Digital ground for the DAC.
DAC_CLK_[P or N]	Dedicated	Input	External reference clock for PLL or DAC direct sampling clock input.
SYSREF_[P or N]	Dedicated	Input	External reference clock/trigger for synchronizing timing of the data converters.
DAC_VOUT[0 to 3]_[P or N]	Dedicated	Output	Analog output signals from the DAC.
DAC_REXT	Dedicated	Input	DAC external resistor.

Table 1-4: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
Other Dedicated Pins			
DXN	Dedicated	N/A	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines.
DXP			

Notes:

1. See the DCI sections in *UltraScale Architecture SelectIO Resources User Guide* (UG571) [Ref 4] for more information on the VRP pins.
2. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank (for package migration). Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or GND).
3. See the *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 11] for the default connections required to support on-chip monitoring.
4. L (left), R (right), N (north), and S (south) signify the GT transceiver quad power supply groups.

Footprint Compatibility between Packages

Zynq UltraScale+ devices are footprint compatible only with other Zynq UltraScale+ devices with the same number of package pins and the same preceding alphabetic designator. For example, XCZU9EG-FFVB1156 is compatible with the XCZU15EG-FFVB1156, but not with the XCZU9EG-FFVC900. Pins that are available in one device but are not available in another device with a compatible package include the other device's name in the *No Connect* column of the package file. These pins are labeled as *No Connects* in the other device's package file.

IMPORTANT: *Footprint compatibility does not necessarily imply that all pins will function in the same manner for different devices in a package. For limitations and guidelines on designing for footprint compatible packages, refer to the Migration Between the Zynq UltraScale+ Devices and Packages section of UltraScale Architecture PCB and Pin Planning User Guide (UG583) [Ref 12].*

Table 1-5 shows the footprint compatible devices available for each package. See the *Zynq UltraScale+ MPSoC Overview* (DS891) [Ref 1] for specific package letter code options.

Table 1-5: **Footprint Compatibility**

Packages	Footprint Compatible Devices			
SBVA484	XCZU2CG, XCZU2EG, and XAZU2EG	XCZU3CG, XCZU3EG, and XAZU3EG		
SFVA625	XCZU2CG, XCZU2EG, and XAZU2EG	XCZU3CG, XCZU3EG, and XAZU3EG		
SFVC784	XCZU2CG, XCZU2EG, and XAZU2EG	XCZU3CG, XCZU3EG, and XAZU3EG	XCZU4CG, XCZU4EG, and XCZU4EV	XCZU5CG, XCZU5EG, and XCZU5EV
FBVB900	XCZU4CG, XCZU4EG, and XCZU4EV	XCZU5CG, XCZU5EG, and XCZU5EV	XCZU7CG, XCZU7EG, and XCZU7EV	
FFVC900	XCZU6CG and XCZU6EG	XCZU9CG and XCZU9EG	XCZU15EG	
FFVB1156	XCZU6CG and XCZU6EG	XCZU9CG and XCZU9EG	XCZU15EG	
FFVC1156	XCZU7CG, XCZU7EG, and XCZU7EV	XCZU11EG		
FFVD1156	XCZU21DR			
FFVE1156 FSVE1156	XCZU25DR	XCZU27DR	XCZU28DR	
FFVB1517	XCZU11EG	XCZU17EG	XCZU19EG	
FFVF1517	XCZU7CG, XCZU7EG, and XCZU7EV	XCZU11EG		
FFVG1517 FSVG1517	XCZU25DR	XCZU27DR	XCZU28DR	

Table 1-5: **Footprint Compatibility *(Cont'd)***

Packages	Footprint Compatible Devices			
FFVC1760	XCZU11EG	XCZU17EG	XCZU19EG	
FFVD1760	XCZU17EG	XCZU19EG		
FFVF1760 FSVF1760	XCZU29DR			
FFVE1924	XCZU17EG	XCZU19EG		

Many Zynq UltraScale+ devices that are footprint compatible in a package have different I/O bank and transceiver quad numbers connected to the same package pins. Due to these differences, when migrating between devices in a specific package, the type of bank (HD vs. HP) or quad (PS-GTR, GTH, or GTY), whether a bank is connected or NC at the package pins, and where the bank or quad is located on the die must be taken into consideration. Table 1-6 and Table 1-7 show how the banks and transceiver quads are numbered between devices in each package.

For all grouped-together footprint-compatible packages, the bank and quad numbers in the same column (indicated by the letters A through Z) for each device are connected to the same package pins. For example, in the FFVB1517 packages, bank 88 for the XCZU11 is connected to the same pins as bank 90 for the XCZU17 and XCZU19.

A limited number of HP I/O banks have fewer than 52 SelectIO pins. For a visual representation of all of this information, see the Die Level Bank Numbering Overview section.

Table 1-6: **I/O Bank Migration (HD Banks are Shaded)**

Package	Device	Package to Device I/O Mapping[1]																										Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	
SBVA484	XCZU2 XAZU2		26	65	66[2]																							25, 24, 44, 64
	XCZU3 XAZU3		26	65	66[2]																							25, 24, 44, 64
SFVA625	XCZU2 XAZU2		64	65	66	26																						25, 24, 44
	XCZU3 XAZU3		64	65	66	26																						25, 24, 44
SFVC784	XCZU2 XAZU2		64	65	66	25	26								24	44												
	XCZU3 XAZU3		64	65	66	25	26								24	44												
	XCZU4		64	65	66	45	46								44	43												63
	XCZU5		64	65	66	45	46								44	43												63
FBVB900	XCZU4		64	65	66										46	45												44, 43, 63
	XCZU5		64	65	66										46	45												44, 43, 63
	XCZU7		64	65	66										47	48												28, 27, 68, 67, 63, 88, 87
FFVC900	XCZU6		64	65	66										48	47												50, 49, 44, 67
	XCZU9		64	65	66										48	47												50, 49, 44, 67
	XCZU15		64	65	66										48	47												50, 49, 44, 67

Table 1-6: **I/O Bank Migration (HD Banks are Shaded)** ***(Cont'd)***

Package	Device	Package to Device I/O Mapping[(1)]																										Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	
FFVB1156	XCZU6	44	64	65	66	67									47	48	49	50										
	XCZU9	44	64	65	66	67									47	48	49	50										
	XCZU15	44	64	65	66	67									47	48	49	50										
FFVC1156	XCZU7		64	65	66										87	88	68	67	28									27, 48, 47, 63
	XCZU11		64	65	66										88	89	69	68	67									71, 70, 91, 90
FFVD1156	XCZU21DR			65	66	67	68								87	88	89											71, 70, 69, 64, 91, 90, 84
FFVE1156 FSVE1156	XCZU25DR			65	66										88	89												69, 68, 67, 64, 87, 84
	XCZU27DR			65	66										88	89												71, 70, 69, 68, 67, 64, 91, 90, 87, 84
	XCZU28DR			65	66										88	89												71, 70, 69, 68, 67, 64, 91, 90, 87, 84
FFVB1517	XCZU11			65	64	66									88	89	90				71	70	69	68	67			91
	XCZU17			65	64	66									90	91	93	74	73	72	71	70	69	68	67			94
	XCZU19			65	64	66									90	91	93	74	73	72	71	70	69	68	67			94
FFVF1517	XCZU7			65	66	64	63								87	88	67	68	28	27								48, 47
	XCZU11			65	66	67	64								88	89	70	71	69	68								91, 90
FFVG1517 FSVG1517	XCZU25DR	84	64	65	66										87			67	68	69								89, 88
	XCZU27DR	84	64	65	66										87			67	68	69								71, 70, 91, 90, 89, 88
	XCZU28DR	84	64	65	66										87			67	68	69								71, 70, 91, 90, 89, 88

Table 1-6: **I/O Bank Migration (HD Banks are Shaded) *(Cont'd)***

Package	Device	Package to Device I/O Mapping[(1)]																										Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	
FFVC1760	XCZU11			65	64	66	67								88	89	90	91	71	70	69	68						
	XCZU17			65	64	66	67								90	91	93	94	71	70	69	68						74, 73, 72
	XCZU19			65	64	66	67								90	91	93	94	71	70	69	68						74, 73, 72
FFVD1760	XCZU17			65	66										90	91	71	70	69									74, 73, 72, 68, 67, 64, 94, 93
	XCZU19			65	66										90	91	71	70	69									74, 73, 72, 68, 67, 64, 94, 93
FFVF1760 FSVF1760	XCZU29DR	84	64	65	66										87	88	89		67	68	69							71, 70, 91, 90
FFVE1924	XCZU17			65	64	66	67								90	91	93	94	74	73	72	71	70	69	68			
	XCZU19			65	64	66	67								90	91	93	94	74	73	72	71	70	69	68			

Notes:

1. An alphabetical designator, A through Z, is assigned to every bank in a package. I/Os from banks with the same designator are bonded out to the same pins in that package. For example, in the FFVF1517 package, the E designator is assigned to bank 67 for the XCZU11 and bank 64 for the XCZU7. These banks are bonded to the same pins, regardless of where they appear on the XCZU11 and XCZU7 device.
2. Bank 66 is partially bonded out in the SBVA484 package (see Figure 1-3).

For each grouped set of footprint compatible packages listed in Table 1-7, there is a row detailing the power supply group for each Quad. These groups are labeled according to the regions for the transceiver power supply pins, as listed in the ASCII Pinout Files linked from Chapter 3, Package Files. For a visual representation of all of this information, see the Die Level Bank Numbering Overview section.

Table 1-7: **Transceiver Quad Migration (GTY Quads are in Shaded)**

Package	Device	Package to Die Transceiver Mapping[(1)]																				Unbonded Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S-Z	AA-AF	
SBVA484	XCZU2 XAZU2																					
	XCZU3 XAZU3																					
SFVA625	XCZU2 XAZU2																					
	XCZU3 XAZU3																					
Power Supply Group		R																				
SFVC784	XCZU2 XAZU2																					
	XCZU3 XAZU3																					
	XCZU4	224																				226, 225, 223
	XCZU5	224																				226, 225, 223
Power Supply Group		R																				
FBVB900	XCZU4	223	224	225	226																	
	XCZU5	223	224	225	226																	
	XCZU7	224	225	226	227																	228, 223
Power Supply Group		R			L																	
FFVC900	XCZU6	228	229	230	128																	130, 129, 127
	XCZU9	228	229	230	128																	130, 129, 127
	XCZU15	228	229	230	128																	130, 129, 127

Table 1-7: **Transceiver Quad Migration (GTY Quads are in Shaded) *(Cont'd)***

Package	Device	Package to Die Transceiver Mapping[1]																				Unbonded Quads
		A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**	**M**	**N**	**O**	**P**	**Q**	**R**	**S-Z**	**AA-AF**	
Power Supply Group		R			L																	
FFVB1156	XCZU6	228	229	230	128	129	130															127
	XCZU9	228	229	230	128	129	130															127
	XCZU15	228	229	230	128	129	130															127
Power Supply Group		R																				
FFVC1156	XCZU7	223	224	225	226	227																228
	XCZU11	224	225	226	227	228																131, 130, 129, 128, 127, 229, 231, 230
Power Supply Group		L																				
FFVD1156	XCZU21DR	128	129	130	131																	127
Power Supply Group		L																				
FFVE1156 FSVE1156	XCZU25DR	128	129																			127
	XCZU27DR	128	129																			131, 130, 127
	XCZU28DR	128	129																			131, 130, 127
Power Supply Group		R																				
FFVB1517	XCZU11	224	225	226	227																	131, 130, 129, 128, 127, 231, 230, 229, 228
	XCZU17	224	225	226	227																	134, 133, 132, 131, 130, 129, 128, 127, 234, 233, 232, 231, 230, 229, 228
	XCZU19	224	225	226	227																	134, 133, 132, 131, 130, 129, 128, 127, 234, 233, 232, 231, 230, 229, 228
Power Supply Group		RS				RN																
FFVF1517	XCZU7	223	224	225	226	227	228															
	XCZU11	224	225	226	227	228	229	230	231													131, 130, 129, 128, 127
Power Supply Group		L																				
FFVG1517 FSVG1517	XCZU25DR	128	129																			127
	XCZU27DR	128	129	130	131																	127
	XCZU28DR	128	129	130	131																	127

Table 1-7: **Transceiver Quad Migration (GTY Quads are in Shaded) *(Cont'd)***

Package	Device	Package to Die Transceiver Mapping[(1)]																				Unbonded Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S-Z	AA-AF	
Power Supply Group		RS				RN					L											
FFVC1760	XCZU11	224	225	226	227	228	229	230	231		128	129	130	131								127
	XCZU17	224	225	226	227	228	229	230	231		128	129	130	131								127
	XCZU19	224	225	226	227	228	229	230	231		128	129	130	131								134, 133, 132, 127, 234, 233, 232
Power Supply Group		RS						RN					L									
FFVD1760	XCZU17	224	225	226	227	228	229	230	231	232	233	234	128	129	130	131	132	133	134			127
	XCZU19	224	225	226	227	228	229	230	231	232	233	234	128	129	130	131	132	133	134			127
Power Supply Group		L																				
FFVF1760 FSVF1760	XCZU29DR	128	129	130	131																	127
Power Supply Group		RS						RN														
FFVE1924	XCZU17	224	225	226	227	228	229	230	231	232	233	234										134, 133, 132, 131, 130, 129, 128, 127
	XCZU19	224	225	226	227	228	229	230	231	232	233	234										134, 133, 132, 131, 130, 129, 128, 127

Notes:

1. An alphabetical designator, A through Z, is assigned to every Quad in a package. Transceivers from Quads with the same designator are bonded out to the same pins in that package. For example, in the FFVF1517 package, the E designator is assigned to Quad 228 for the XCZU11 and Quad 227 for the XCZU7. These Quads are bonded to the same pins, regardless of where they appear on the XCZU11 and XCZU7 device.

Die Level Bank Numbering Overview

Banking and Clocking Summary

- For each device, not all banks are bonded out in every package.

GTH/GTY Columns

- One GT Quad = Four transceivers = Four GTHE4 or GTYE4 primitives.
- Not all GT Quads are bonded out in every package.
- Also shown are quads labeled with RCAL. This specifies the location of the RCAL masters for each device. With respect to the package, the RCAL masters are located on the same package pin for each package, regardless of the device.
- The XY coordinates shown in each quad correspond to the transceiver channel number found in the pin names for that quad, as shown in Figure 1-2.
- An alphabetic designator is shown in each quad. Each letter corresponds to the columns in Table 1-6 and Table 1-7.
- The power supply group is shown in brackets [ ] for each quad.

I/O Banks

- Each user HP I/O bank has a total of 52 I/Os where 48 can be used as differential (24 differential pairs) or single-ended I/Os. The remaining four function only as single-ended I/Os. All 52 pads of a bank are not always bonded out to pins.
- A limited number of HP I/O banks have fewer than 52 SelectIO pins. These banks are labeled as partial.
- Each user HD I/O bank has a total of 24 I/Os that can be used as differential (12 differential pairs) or single-ended I/Os.
- Adjacent to each bank is a physical layer (PHY) containing a CMT and other clock resources.
- Adjacent to each bank and PHY is a tile of logic resources that makes up a clock region.
- Banks are arranged in columns and separated into rows which are pitch-matched with adjacent PHY, clock regions, and GT blocks.
- An alphabetic designator is shown in each bank. Each letter corresponds to the columns in Table 1-6 and Table 1-7.

Clocking

- Each bank has four pairs of global clock (GC or HDGC) inputs for four differential or four single-ended clock inputs. Single-ended clock inputs should be connected to the P-side of the differential pair.
- Clock signals are distributed through global buffers driving routing and distribution networks to reach any clock region, I/O, or GT.
- Global clock inputs can connect to an MMCM and two PLLs within the horizontally adjacent CMT.

Bank Locations of Dedicated and Multi-Function Pins

- All dedicated configuration I/Os and HD I/Os are 3.3V capable.

Processor (PS) Blocks

- MIO pins are shared between banks 500, 501, and 502.
- Configuration pins are in bank 503.
- DDR memory pins are in bank 504.
- Transceiver pins are in the PS-GTR quad 505.

SYSMON, Configuration, PCIe, Interlaken, and 100GE Integrated Blocks

- Configuration: Configuration block.
- SYSMON/Configuration: Block shared between the SYSMONE4 and configuration.
- PCIe: Integrated block for PCIe.

  Note: PCIe blocks with an additional (Tandem) label support tandem configuration.
- ILKN: Interlaken block.
- CMAC: 100G Ethernet block.

Device Diagrams

Figure 1-1 shows an example diagram with a brief explanation for each component.

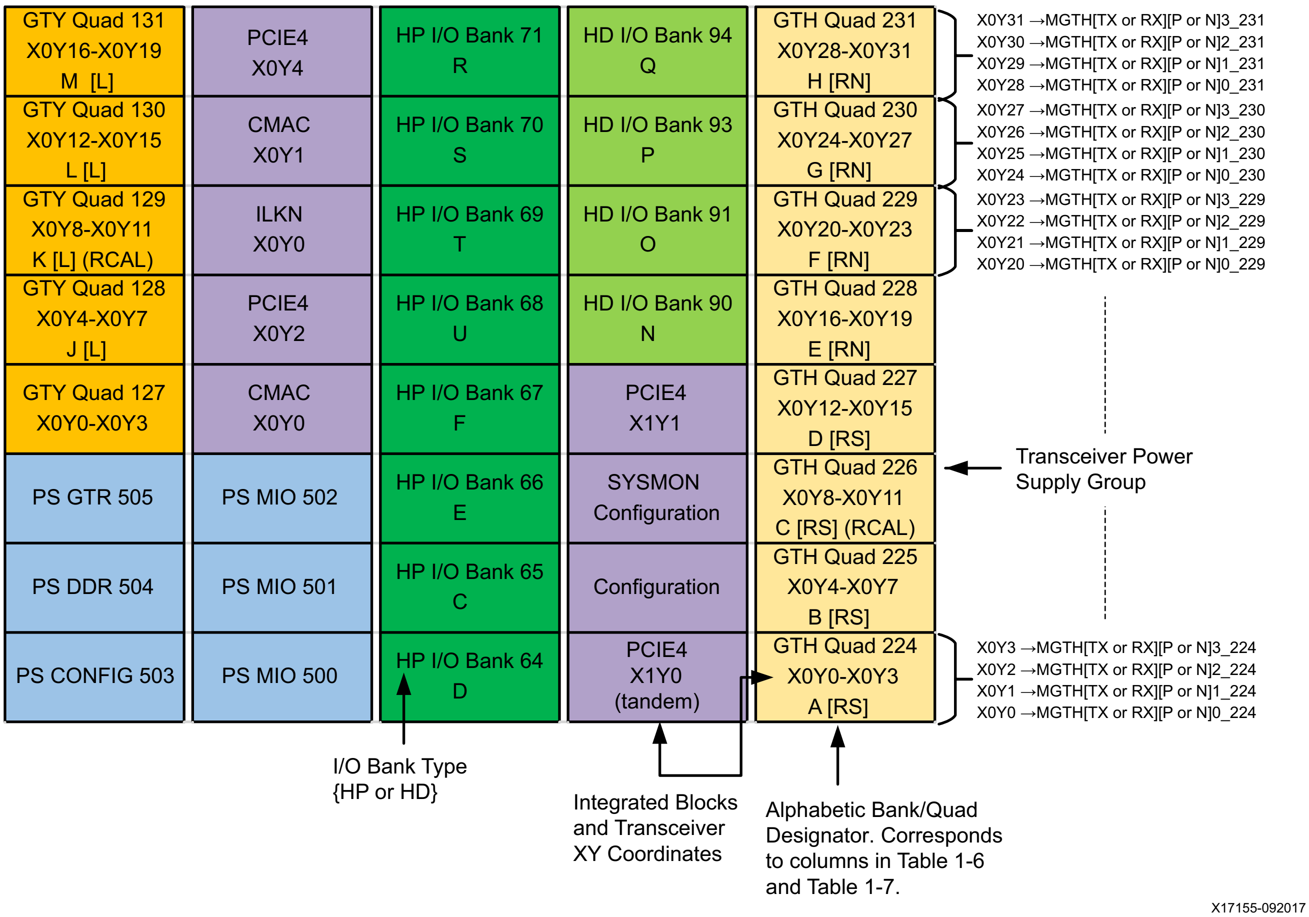

Figure 1-1: **Example Device Diagram**

Figure 1-2 through Figure 1-41 show a die view of each device followed by a view with respect to each available package. The available resources by device and package are detailed in the *Zynq UltraScale+ MPSoC Overview* (DS891) [Ref 1] or *Zynq UltraScale+ RFSoC Overview* (DS889) [Ref 2]

XCZU2, XAZU2, XCZU3, and XAZU3 Bank Diagram Overview

PS GTR 505	PS MIO 502	HD I/O Bank 26	SYSMON Configuration	HP I/O Bank 66
PS DDR 504	PS MIO 501	HD I/O Bank 25	Configuration	HP I/O Bank 65
PS CONFIG 503	PS MIO 500	HD I/O Bank 24	HD I/O Bank 44	HP I/O Bank 64

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Figure 1-2: **XCZU2, XAZU2, XCZU3, and XAZU3 Banks**

Bank Diagram by Package for XCZU2, XAZU2, XCZU3, and XAZU3

PS GTR 505	PS MIO 502	HD I/O Bank 26 B	SYSMON Configuration	HP I/O Bank 66 D (Partial)
PS DDR 504 (Partial)	PS MIO 501	HD I/O Bank 25	Configuration	HP I/O Bank 65 C
PS CONFIG 503	PS MIO 500	HD I/O Bank 24	HD I/O Bank 44	HP I/O Bank 64

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Figure 1-3: **XCZU2, XAZU2, XCZU3, and XAZU3 Banks in SBVA484 Package**

PS GTR 505	PS MIO 502	HD I/O Bank 26 E	SYSMON Configuration	HP I/O Bank 66 D
PS DDR 504 (Partial)	PS MIO 501	HD I/O Bank 25	Configuration	HP I/O Bank 65 C
PS CONFIG 503	PS MIO 500	HD I/O Bank 24	HD I/O Bank 44	HP I/O Bank 64 B

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Figure 1-4: **XCZU2, XAZU2, XCZU3, and XAZU3 Banks in SFVA625 Package**

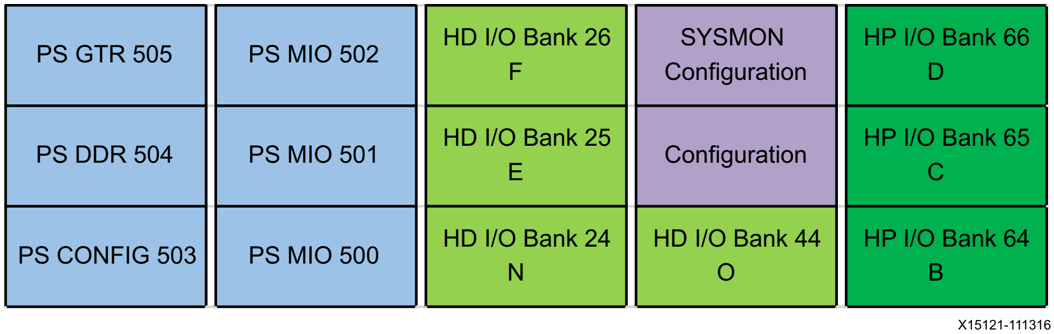

Figure 1-5: **XCZU2, XAZU2, XCZU3, and XAZU3 Banks in SFVC784 Package**

XCZU4 and XCZU5 Bank Diagram Overview

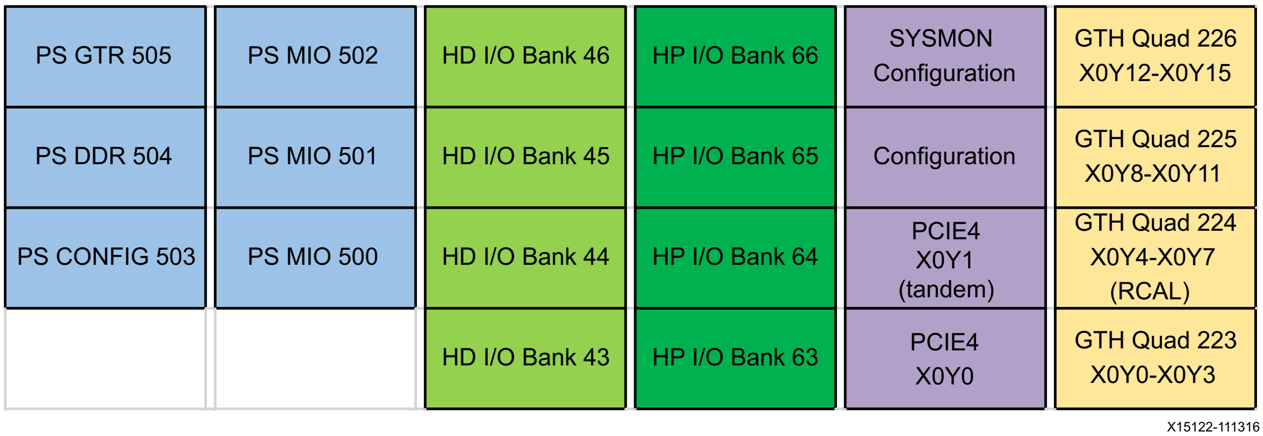

Figure 1-6: **XCZU4 and XCZU5 Banks**

Bank Diagram by Package for XCZU4 and XCZU5

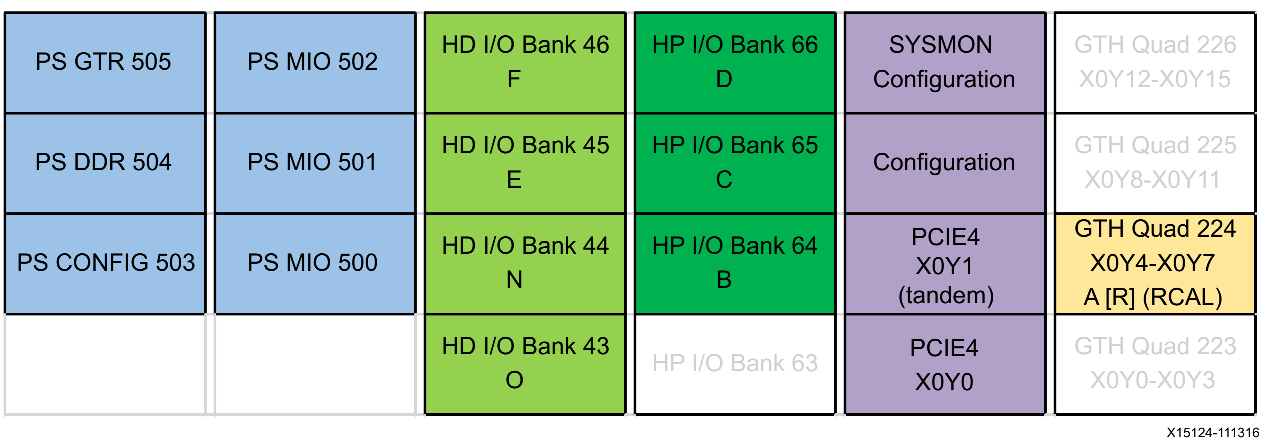

Figure 1-7: **XCZU4 and XCZU5 Banks in SFVC784 Package**

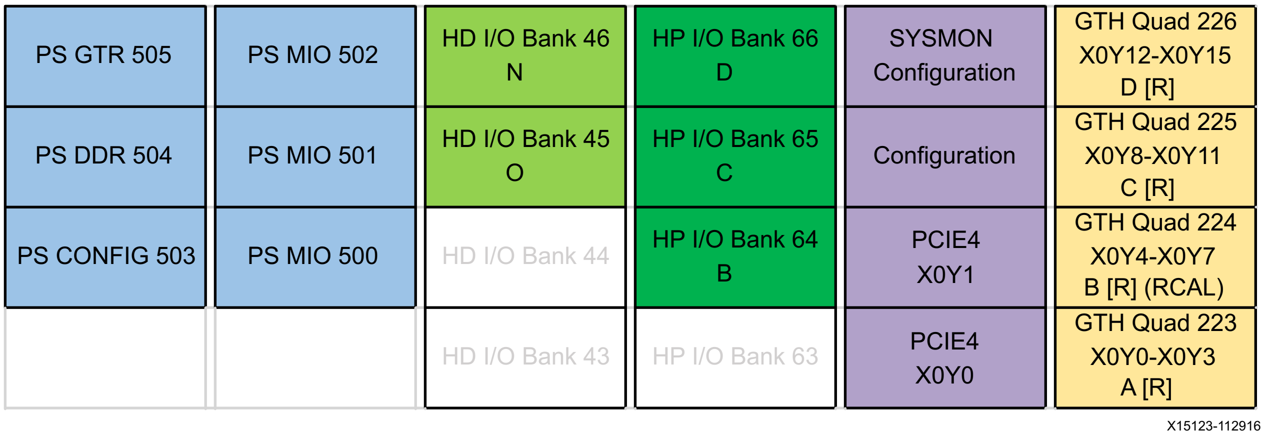

Figure 1-8: **XCZU4 and XCZU5 Banks in FBVB900 Package**

XCZU7 Bank Diagram Overview

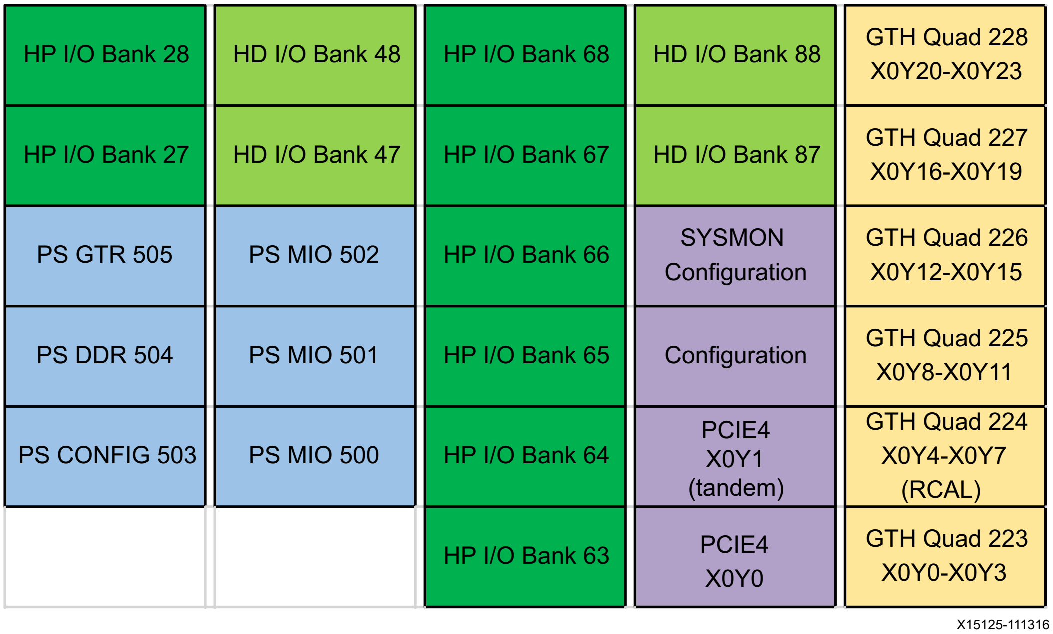

Figure 1-9: **XCZU7 Banks**

Bank Diagram by Package for XCZU7

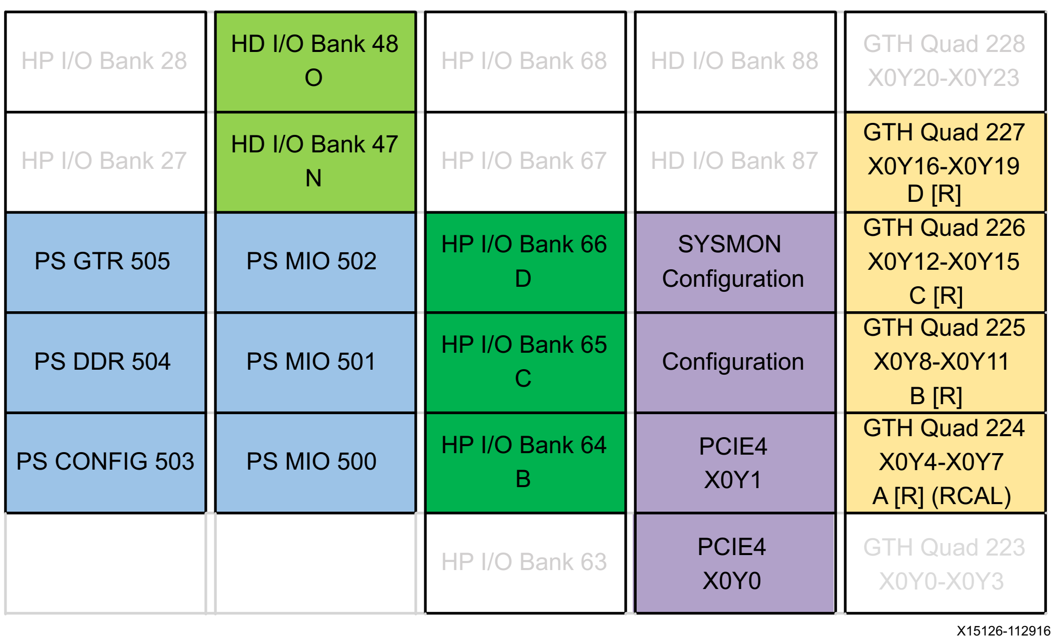

Figure 1-10: **XCZU7 Banks in FBVB900 Package**

HP I/O Bank 28 R	HD I/O Bank 48	HP I/O Bank 68 P	HD I/O Bank 88 O	GTH Quad 228 X0Y20-X0Y23
HP I/O Bank 27	HD I/O Bank 47	HP I/O Bank 67 Q	HD I/O Bank 87 N	GTH Quad 227 X0Y16-X0Y19 E [R]
PS GTR 505	PS MIO 502	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y12-X0Y15 D [R]
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y8-X0Y11 C [R]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 B	PCIE4 X0Y1 (tandem)	GTH Quad 224 X0Y4-X0Y7 B [R] (RCAL)
		HP I/O Bank 63	PCIE4 X0Y0	GTH Quad 223 X0Y0-X0Y3 A [R]

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Figure 1-11: **XCZU7 Banks in FFVC1156 Package**

HP I/O Bank 28 R	HD I/O Bank 48	HP I/O Bank 68 Q	HD I/O Bank 88 O	GTH Quad 228 X0Y20-X0Y23 F [RN]
HP I/O Bank 27 S	HD I/O Bank 47	HP I/O Bank 67 P	HD I/O Bank 87 N	GTH Quad 227 X0Y16-X0Y19 E [RN]
PS GTR 505	PS MIO 502	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y12-X0Y15 D [RS]
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y8-X0Y11 C [RS]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 E	PCIE4 X0Y1 (tandem)	GTH Quad 224 X0Y4-X0Y7 B [RS] (RCAL)
		HP I/O Bank 63 F	PCIE4 X0Y0	GTH Quad 223 X0Y0-X0Y3 A [RS]

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Figure 1-12: **XCZU7 Banks in FFVF1517 Package**

XCZU6 and XCZU9 Bank Diagram Overview

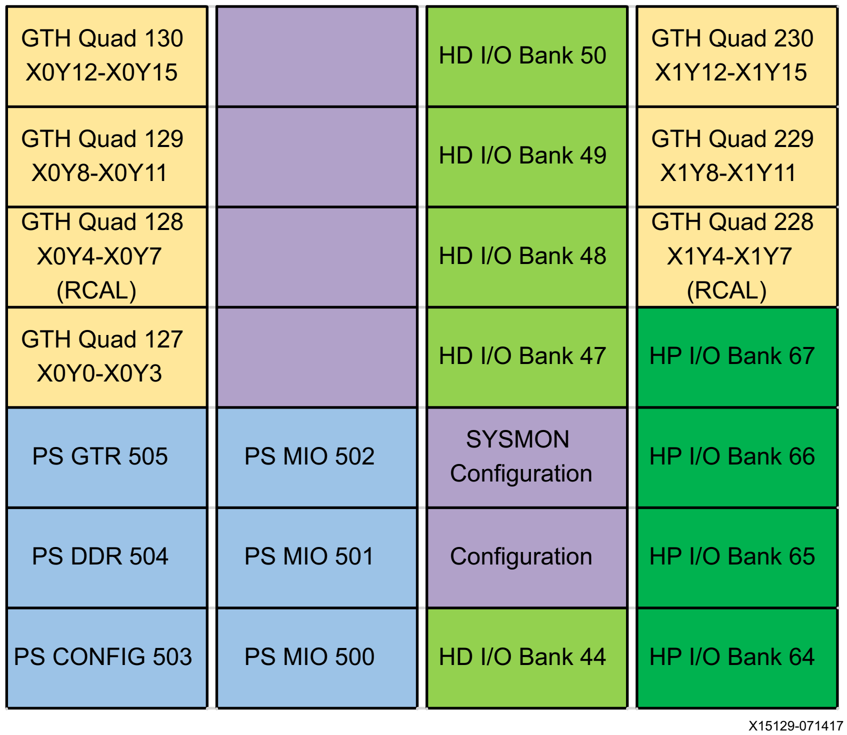

Figure 1-13: **XCZU6 and XCZU9 Banks**

Bank Diagram by Package for XCZU6 and XCZU9

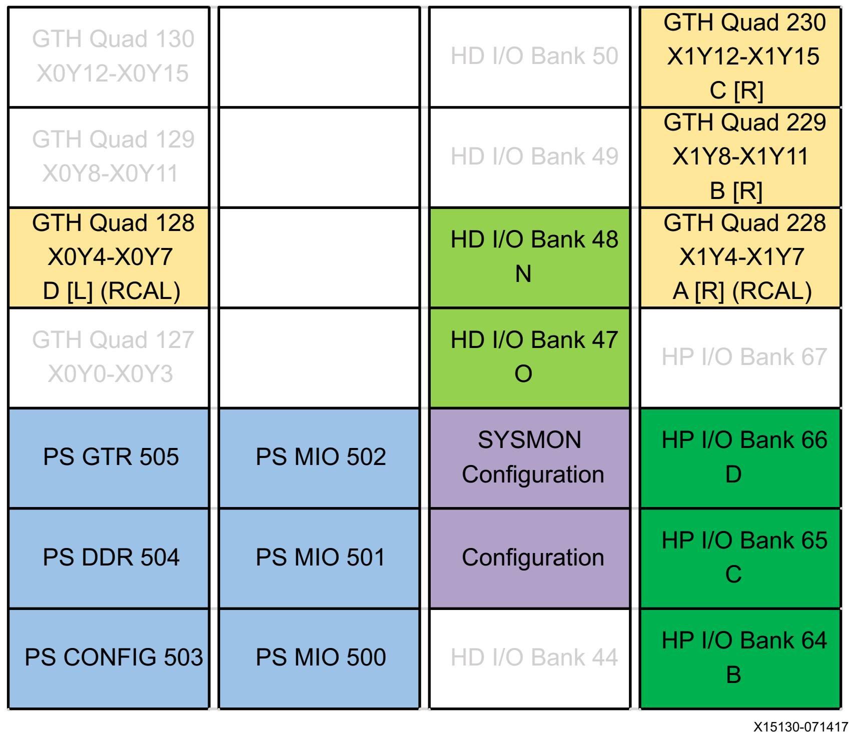

Figure 1-14: **XCZU6 and XCZU9 Banks in FFVC900 Package**

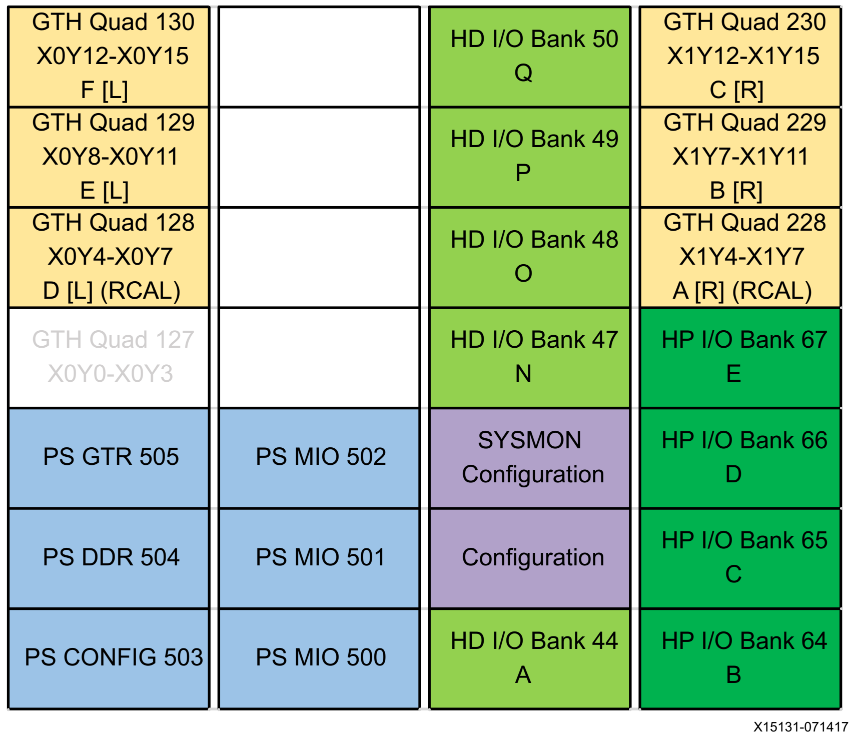

Figure 1-15: **XCZU6 and XCZU9 Banks in FFVB1156 Package**

XCZU11 Bank Diagram Overview

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y3	HP I/O Bank 71	HD I/O Bank 91	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 70	HD I/O Bank 90	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	HP I/O Bank 69	HD I/O Bank 89	GTH Quad 229 X0Y20-X0Y23
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y2	HP I/O Bank 68	HD I/O Bank 88	GTH Quad 228 X0Y16-X0Y19
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15
PS GTR 505	PS MIO 502	HP I/O Bank 66	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 (RCAL)
PS DDR 504	PS MIO 501	HP I/O Bank 65	Configuration	GTH Quad 225 X0Y4-X0Y7
PS CONFIG 503	PS MIO 500	HP I/O Bank 64	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3

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Figure 1-16: **XCZU11 Banks**

Bank Diagram by Package for XCZU11

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y3	HP I/O Bank 71	HD I/O Bank 91	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 70	HD I/O Bank 90	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	HP I/O Bank 69 P	HD I/O Bank 89 O	GTH Quad 229 X0Y20-X0Y23
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y2	HP I/O Bank 68 Q	HD I/O Bank 88 N	GTH Quad 228 X0Y16-X0Y19 E [R]
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67 R	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [R]
PS GTR 505	PS MIO 502	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R] (RCAL)
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 B	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

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Figure 1-17: **XCZU11 Banks in FFVC1156 Package**

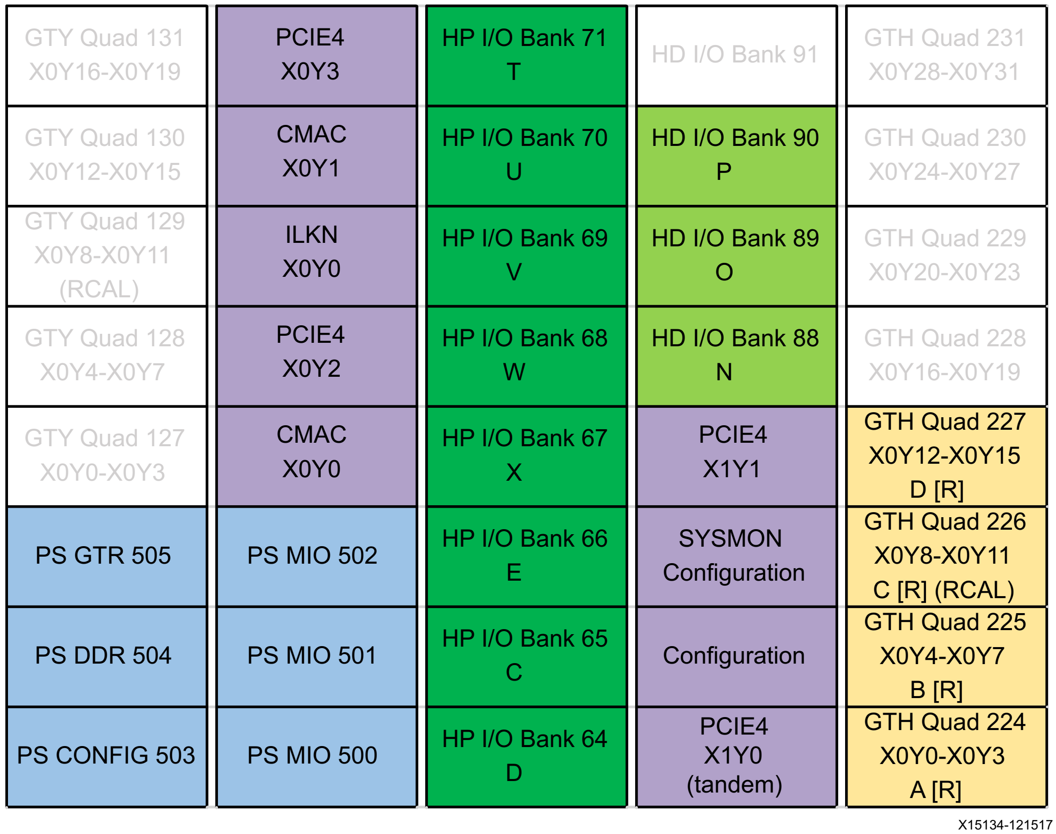

Figure 1-18: **XCZU11 Banks in FFVB1517 Package**

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y3	HP I/O Bank 71 Q	HD I/O Bank 91	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 70 P	HD I/O Bank 90	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	HP I/O Bank 69 R	HD I/O Bank 89 O	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y2	HP I/O Bank 68 S	HD I/O Bank 88 N	GTH Quad 228 X0Y16-X0Y19 E [RN]
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67 E	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [RS]
PS GTR 505	PS MIO 502	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 F	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-19: **XCZU11 Banks in FFVF1517 Package**

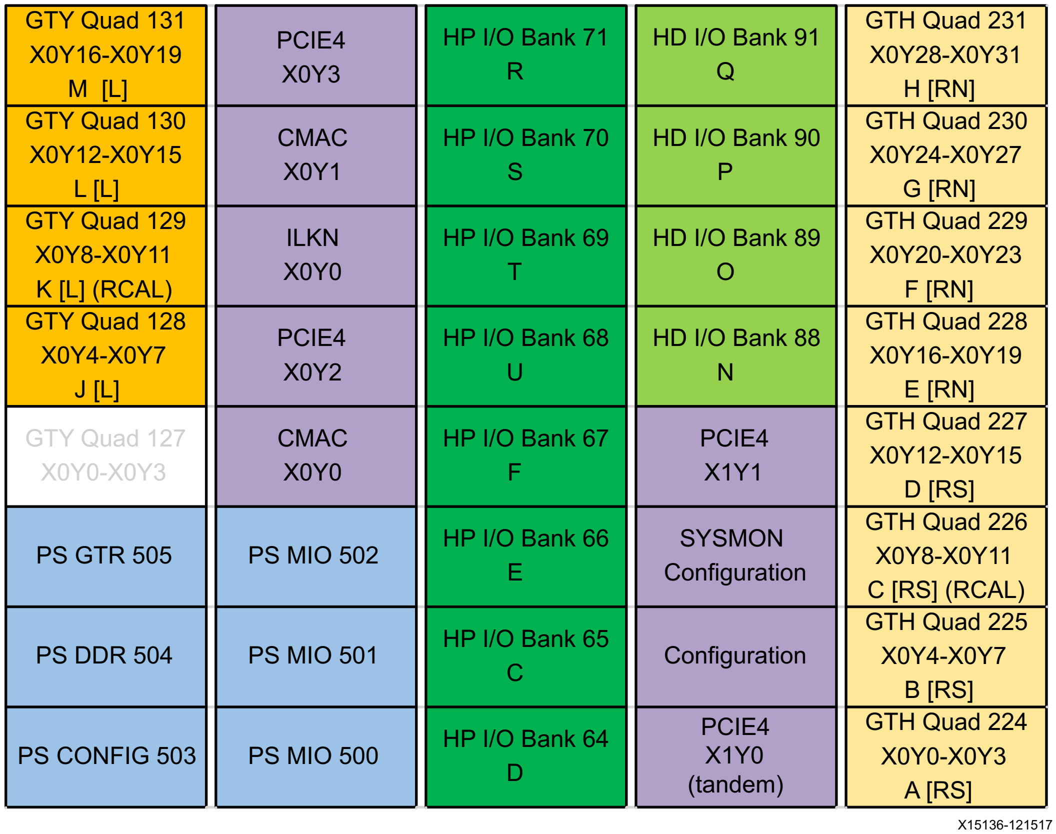

Figure 1-20: **XCZU11 Banks in FFVC1760 Package**

XCZU15 Bank Diagrams

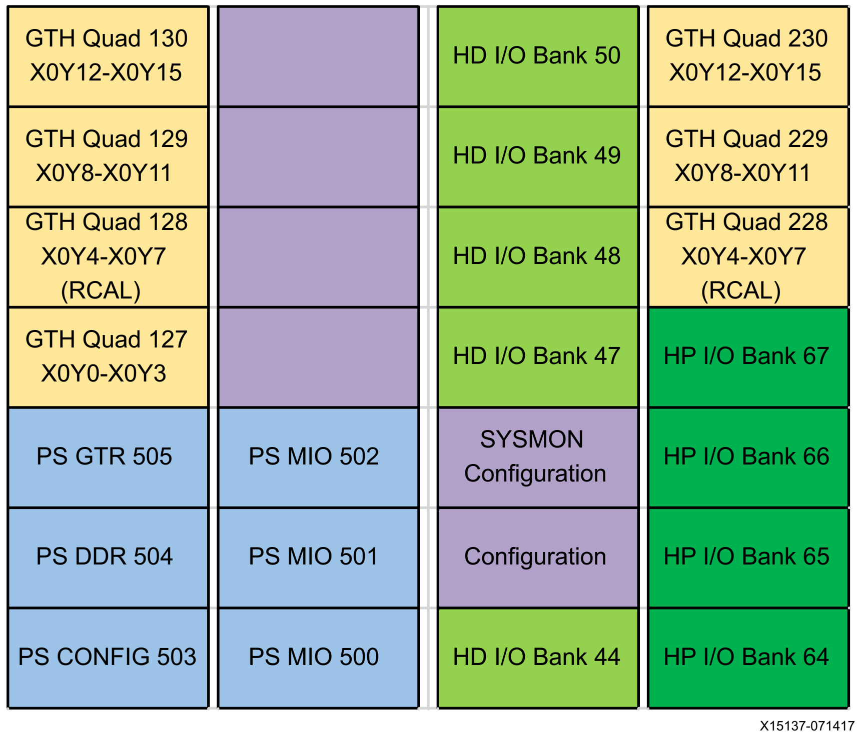

Figure 1-21: **XCZU15 Banks**

Bank Diagram by Package for XCZU15

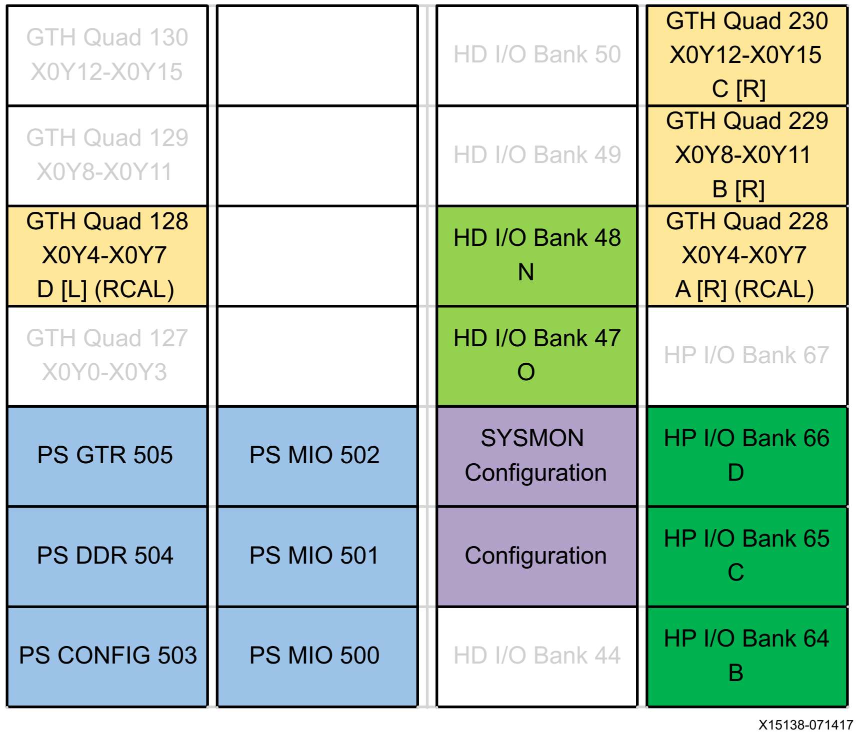

Figure 1-22: **XCZU15 Banks in FFVC900 Package**

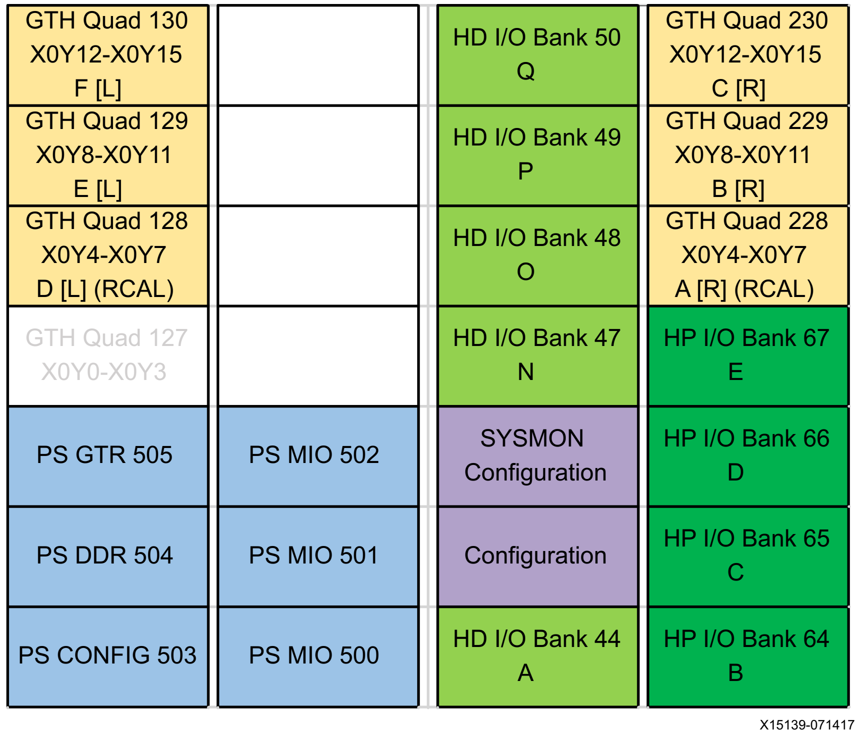

Figure 1-23: **XCZU15 Banks in FFVB1156 Package**

XCZU17 and XCZU19 Bank Diagram Overview

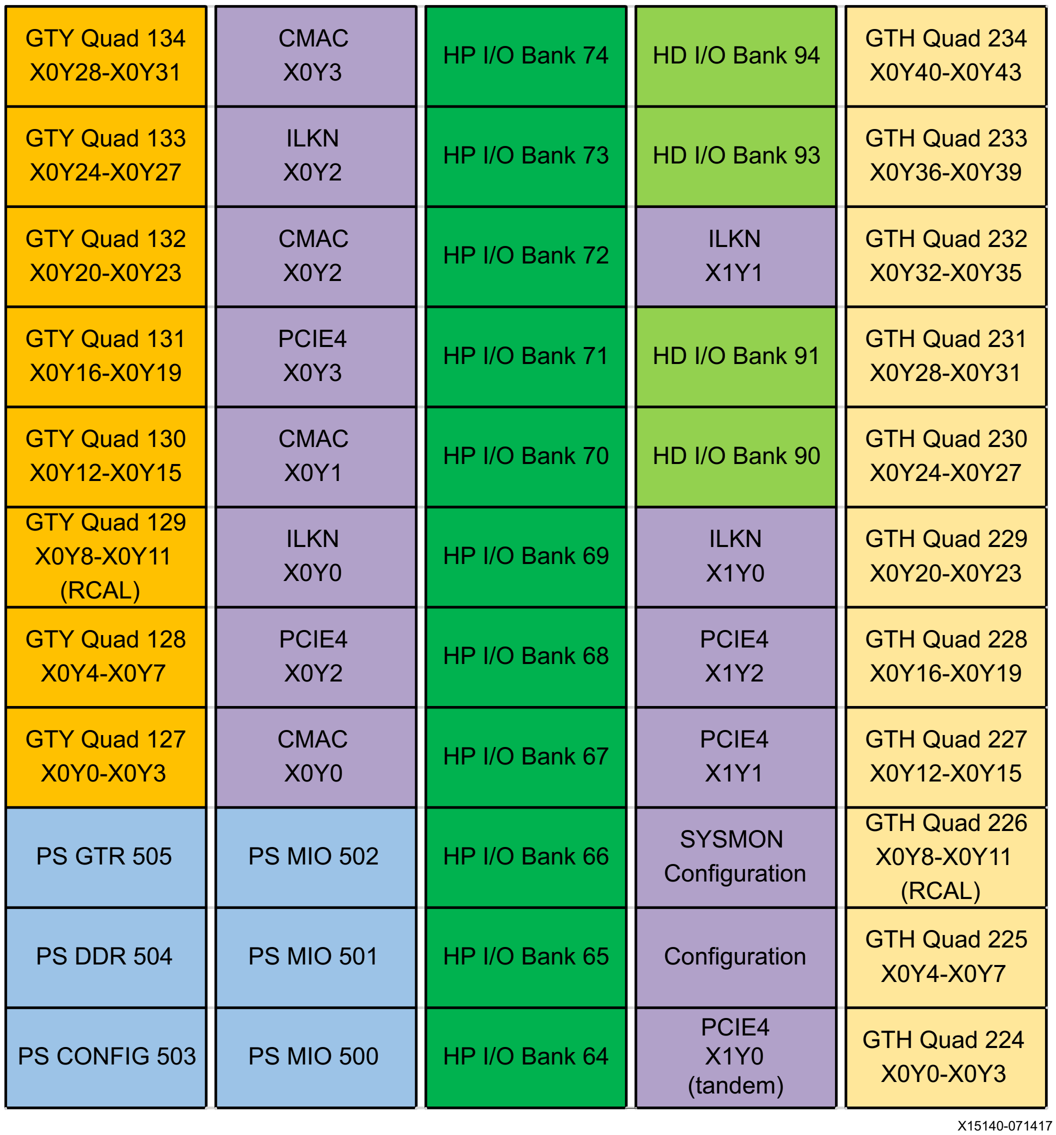

Figure 1-24: **XCZU17 and XCZU19 Banks**

Bank Diagram by Package for XCZU17 and XCZU19

GTY Quad 134 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 74 Q	HD I/O Bank 94	GTH Quad 234 X0Y40-X0Y43
GTY Quad 133 X0Y24-X0Y27	ILKN X0Y2	HP I/O Bank 73 R	HD I/O Bank 93 P	GTH Quad 233 X0Y36-X0Y39
GTY Quad 132 X0Y20-X0Y23	CMAC X0Y2	HP I/O Bank 72 S	ILKN X1Y1	GTH Quad 232 X0Y32-X0Y35
GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y3	HP I/O Bank 71 T	HD I/O Bank 91 O	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 70 U	HD I/O Bank 90 N	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	HP I/O Bank 69 V	ILKN X1Y0	GTH Quad 229 X0Y20-X0Y23
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y2	HP I/O Bank 68 W	PCIE4 X1Y2	GTH Quad 228 X0Y16-X0Y19
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67 X	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [R]
PS GTR 505	PS MIO 502	HP I/O Bank 66 E	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R] (RCAL)
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 D	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

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Figure 1-25: **XCZU17 and XCZU19 Banks in FFVB1517 Package**

GTY Quad 134 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 74	HD I/O Bank 94 Q	GTH Quad 234 X0Y40-X0Y43
GTY Quad 133 X0Y24-X0Y27	ILKN X0Y2	HP I/O Bank 73	HD I/O Bank 93 P	GTH Quad 233 X0Y36-X0Y39
GTY Quad 132 X0Y20-X0Y23	CMAC X0Y2	HP I/O Bank 72	ILKN X1Y1	GTH Quad 232 X0Y32-X0Y35
GTY Quad 131 X0Y16-X0Y19 M [L]	PCIE4 X0Y3	HP I/O Bank 71 R	HD I/O Bank 91 O	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y12-X0Y15 L [L]	CMAC X0Y1	HP I/O Bank 70 S	HD I/O Bank 90 N	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y8-X0Y11 K [L] (RCAL)	ILKN X0Y0	HP I/O Bank 69 T	ILKN X1Y0	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y4-X0Y7 J [L]	PCIE4 X0Y2	HP I/O Bank 68 U	PCIE4 X1Y2	GTH Quad 228 X0Y16-X0Y19 E [RN]
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67 F	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [RS]
PS GTR 505	PS MIO 502	HP I/O Bank 66 E	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 D	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-26: **XCZU17 and XCZU19 Banks in FFVC1760 Package**

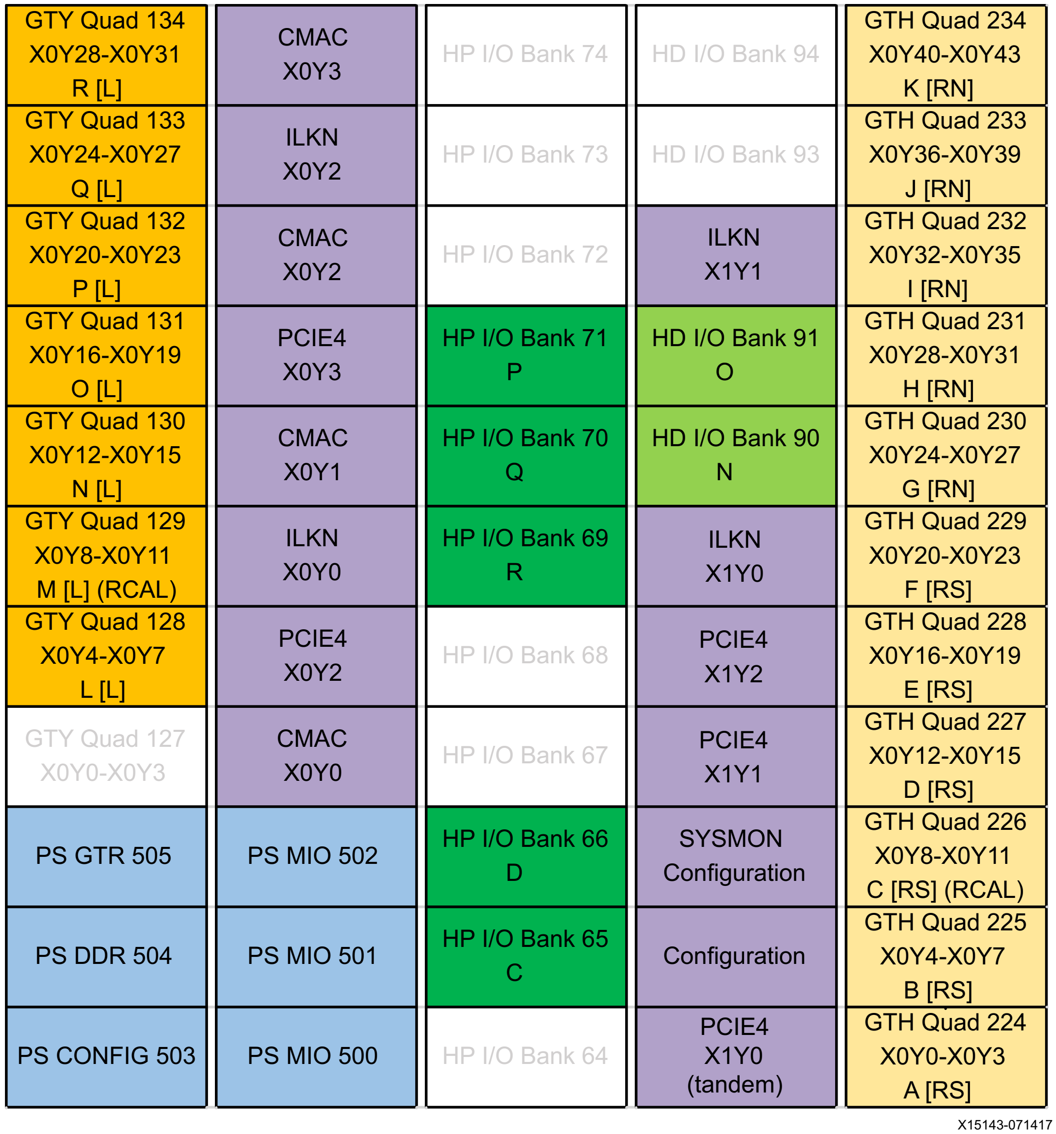

Figure 1-27: **XCZU17 and XCZU19 Banks in FFVD1760 Package**

GTY Quad 134 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 74 R	HD I/O Bank 94 Q	GTH Quad 234 X0Y40-X0Y43 K [RN]
GTY Quad 133 X0Y24-X0Y27	ILKN X0Y2	HP I/O Bank 73 S	HD I/O Bank 93 P	GTH Quad 233 X0Y36-X0Y39 J [RN]
GTY Quad 132 X0Y20-X0Y23	CMAC X0Y2	HP I/O Bank 72 T	ILKN X1Y1	GTH Quad 232 X0Y32-X0Y35 I [RN]
GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y3	HP I/O Bank 71 U	HD I/O Bank 91 O	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 70 V	HD I/O Bank 90 N	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	HP I/O Bank 69 W	ILKN X1Y0	GTH Quad 229 X0Y20-X0Y23 F [RS]
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y2	HP I/O Bank 68 X	PCIE4 X1Y2	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67 F	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [RS]
PS GTR 505	PS MIO 502	HP I/O Bank 66 E	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
PS CONFIG 503	PS MIO 500	HP I/O Bank 64 D	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-28: **XCZU17 and XCZU19 Banks in FFVE1924 Package**

XCZU21DR Bank Diagram Overview

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y1	FEC	HP I/O Bank 71	HD I/O Bank 91
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	FEC	HP I/O Bank 70	HD I/O Bank 90
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	FEC	HP I/O Bank 69	HD I/O Bank 89
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y0	FEC	HP I/O Bank 68	HD I/O Bank 88
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	FEC	HP I/O Bank 67	HD I/O Bank 87
PS GTR 505	PS MIO 502	FEC	HP I/O Bank 66	SYSMON Configuration
PS DDR 504	PS MIO 501	FEC	HP I/O Bank 65	Configuration
PS CONFIG 503	PS MIO 500	FEC	HP I/O Bank 64	HD I/O Bank 84

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Figure 1-29: **XCZU21DR Banks**

Bank Diagram by Package for XCZU21DR

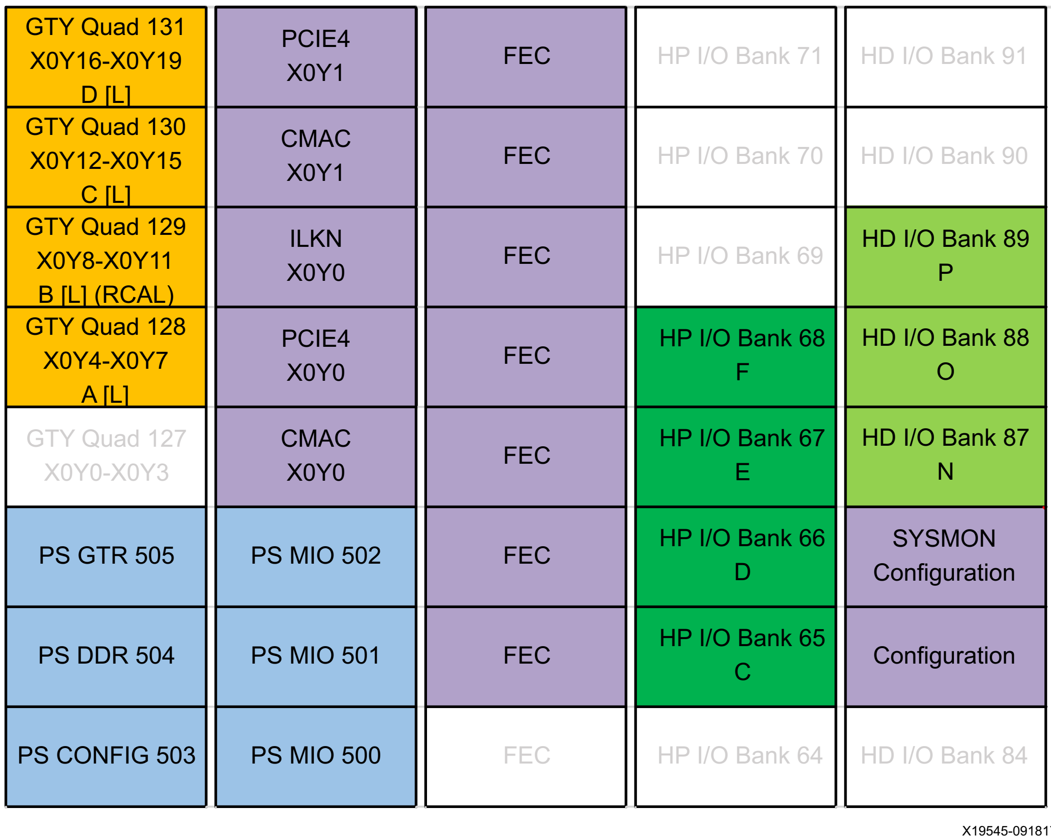

Figure 1-30: **XCZU21DR Banks in FFVD1156 Packages**

XCZU25DR Bank Diagram Overview

GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	HP I/O Bank 69	HD I/O Bank 89	DAC Bank 229
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y0	HP I/O Bank 68	HD I/O Bank 88	DAC Bank 228
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67	HD I/O Bank 87	ADC Bank 227
PS GTR 505	PS MIO 502	HP I/O Bank 66	SYSMON Configuration	ADC Bank 226
PS DDR 504	PS MIO 501	HP I/O Bank 65	Configuration	ADC Bank 225
PS CONFIG 503	PS MIO 500	HP I/O Bank 64	HD I/O Bank 84	ADC Bank 224

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Figure 1-31: **XCZU25DR Banks**

Bank Diagram by Package for XCZU25DR

GTY Quad 129 X0Y8-X0Y11 B [L] (RCAL)	ILKN X0Y0	HP I/O Bank 69	HD I/O Bank 89 O	DAC Bank 229
GTY Quad 128 X0Y4-X0Y7 A [L]	PCIE4 X0Y0	HP I/O Bank 68	HD I/O Bank 88 N	DAC Bank 228
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67	HD I/O Bank 87	ADC Bank 227
PS GTR 505	PS MIO 502	HP I/O Bank 66 D	SYSMON Configuration	ADC Bank 226
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	ADC Bank 225
PS CONFIG 503	PS MIO 500	HP I/O Bank 64	HD I/O Bank 84	ADC Bank 224

X19547-032218

Figure 1-32: **XCZU25DR Banks in FFVE1156 and FSVE1156 Packages**

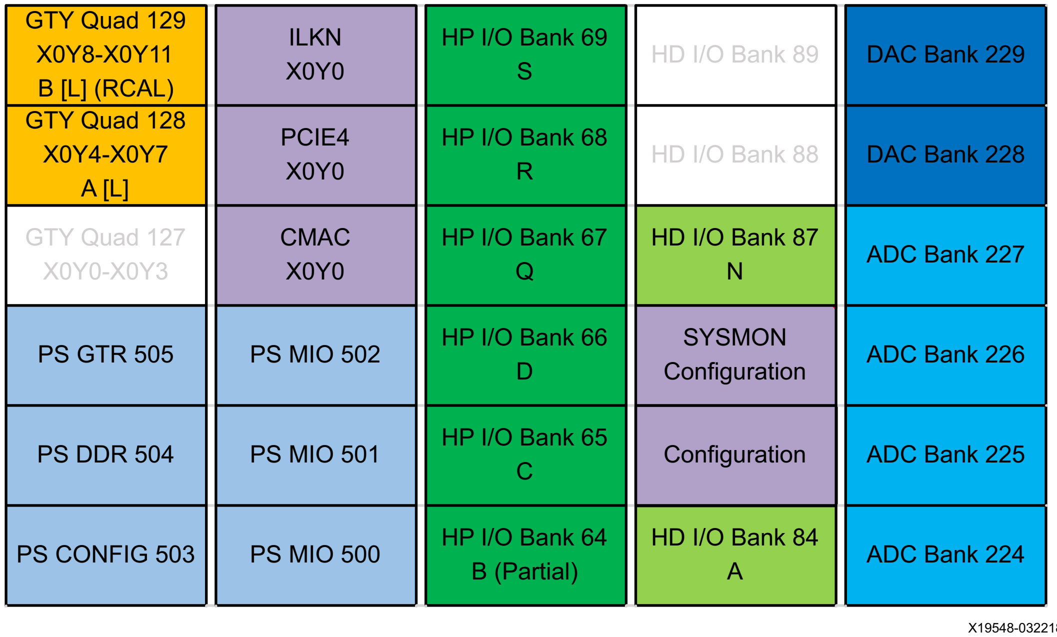

Figure 1-33: **XCZU25DR Banks in FFVG1517 and FSVG1517 Packages**

XCZU27DR Bank Diagram Overview

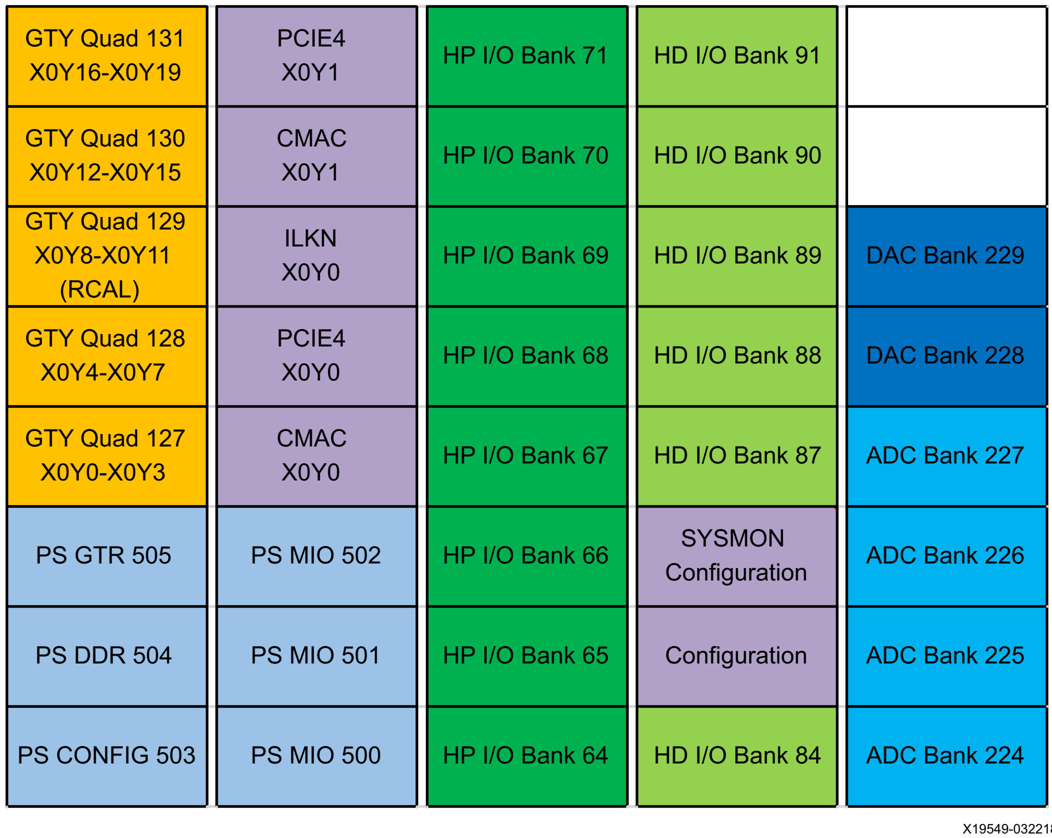

Figure 1-34: **XCZU27DR Banks**

Bank Diagram by Package for XCZU27DR

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y1	HP I/O Bank 71	HD I/O Bank 91	
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 70	HD I/O Bank 90	
GTY Quad 129 X0Y8-X0Y11 B [L] (RCAL)	ILKN X0Y0	HP I/O Bank 69	HD I/O Bank 89 O	DAC Bank 229
GTY Quad 128 X0Y4-X0Y7 A [L]	PCIE4 X0Y0	HP I/O Bank 68	HD I/O Bank 88 N	DAC Bank 228
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 67	HD I/O Bank 87	ADC Bank 227
PS GTR 505	PS MIO 502	HP I/O Bank 66 D	SYSMON Configuration	ADC Bank 226
PS DDR 504	PS MIO 501	HP I/O Bank 65 C	Configuration	ADC Bank 225
PS CONFIG 503	PS MIO 500	HP I/O Bank 64	HD I/O Bank 84	ADC Bank 224

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Figure 1-35: **XCZU27DR Banks in FFVE1156 and FSVE1156 Packages**

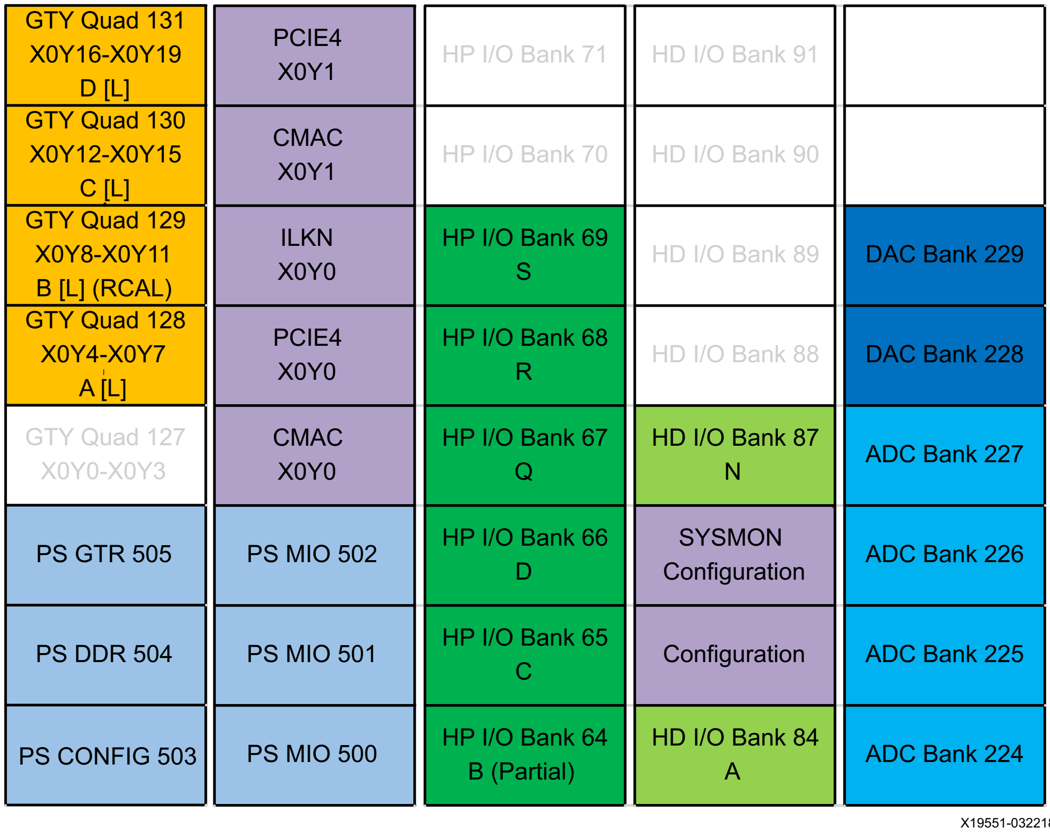

Figure 1-36: **XCZU27DR Banks in FFVG1517 and FSVG1517 Packages**

XCZU28DR Bank Diagram Overview

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y1	FEC	HP I/O Bank 71	HD I/O Bank 91	
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	FEC	HP I/O Bank 70	HD I/O Bank 90	
GTY Quad 129 X0Y8-X0Y11 (RCAL)	ILKN X0Y0	FEC	HP I/O Bank 69	HD I/O Bank 89	DAC Bank 229
GTY Quad 128 X0Y4-X0Y7	PCIE4 X0Y0	FEC	HP I/O Bank 68	HD I/O Bank 88	DAC Bank 228
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	FEC	HP I/O Bank 67	HD I/O Bank 87	ADC Bank 227
PS GTR 505	PS MIO 502	FEC	HP I/O Bank 66	SYSMON Configuration	ADC Bank 226
PS DDR 504	PS MIO 501	FEC	HP I/O Bank 65	Configuration	ADC Bank 225
PS CONFIG 503	PS MIO 500	FEC	HP I/O Bank 64	HD I/O Bank 84	ADC Bank 224

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Figure 1-37: **XCZU28DR Banks**

Bank Diagram by Package for XCZU28DR

GTY Quad 131 X0Y16-X0Y19	PCIE4 X0Y1	FEC	HP I/O Bank 71	HD I/O Bank 91	
GTY Quad 130 X0Y12-X0Y15	CMAC X0Y1	FEC	HP I/O Bank 70	HD I/O Bank 90	
GTY Quad 129 X0Y8-X0Y11 B [L] (RCAL)	ILKN X0Y0	FEC	HP I/O Bank 69	HD I/O Bank 89 O	DAC Bank 229
GTY Quad 128 X0Y4-X0Y7 A [L]	PCIE4 X0Y0	FEC	HP I/O Bank 68	HD I/O Bank 88 N	DAC Bank 228
GTY Quad 127 X0Y0-X0Y3	CMAC X0Y0	FEC	HP I/O Bank 67	HD I/O Bank 87	ADC Bank 227
PS GTR 505	PS MIO 502	FEC	HP I/O Bank 66 D	SYSMON Configuration	ADC Bank 226
PS DDR 504	PS MIO 501	FEC	HP I/O Bank 65 C	Configuration	ADC Bank 225
PS CONFIG 503	PS MIO 500	FEC	HP I/O Bank 64	HD I/O Bank 84	ADC Bank 224

X19553-032218

Figure 1-38: **XCZU28DR Banks in FFVE1156 and FSVE1156 Packages**

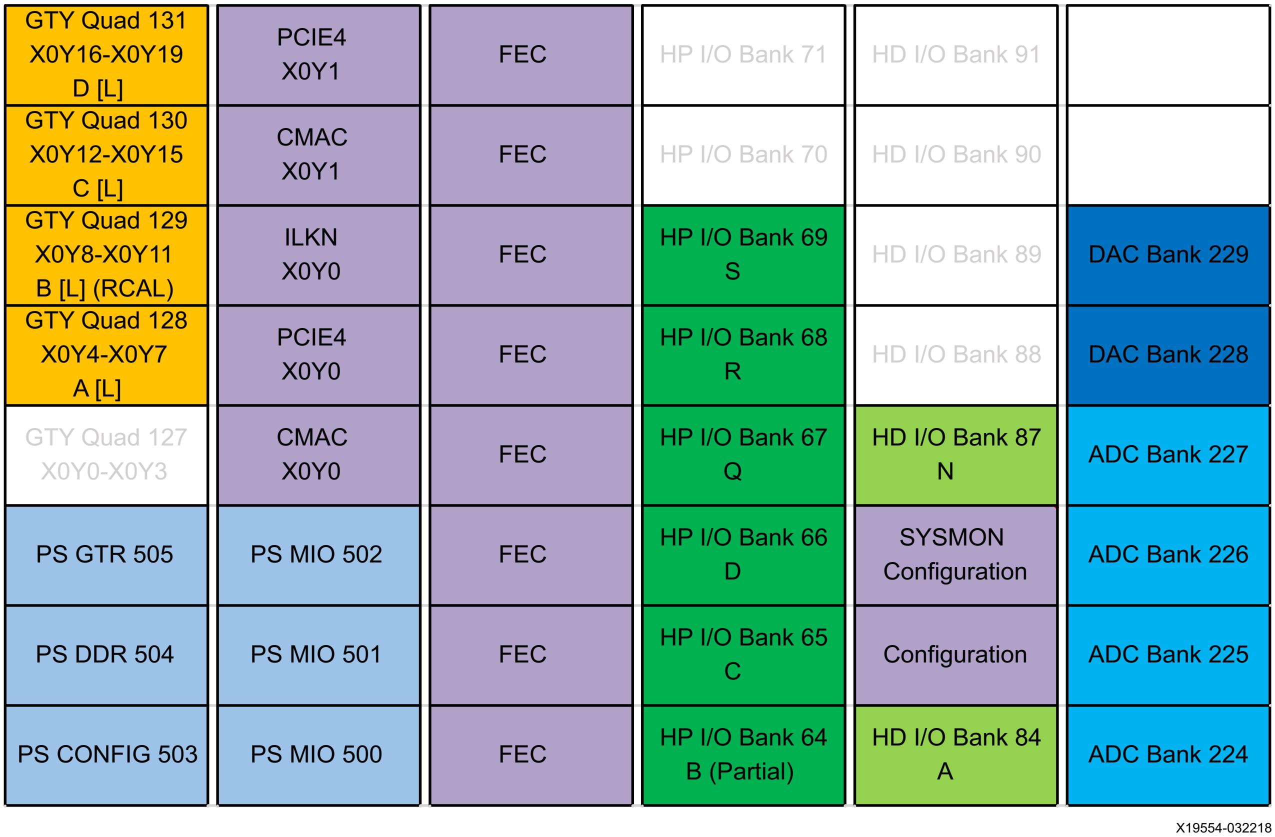


Figure 1-39: **XCZU28DR Banks in FFVG1517 and FSVG1517 Packages**

XCZU29DR Bank Diagram Overview

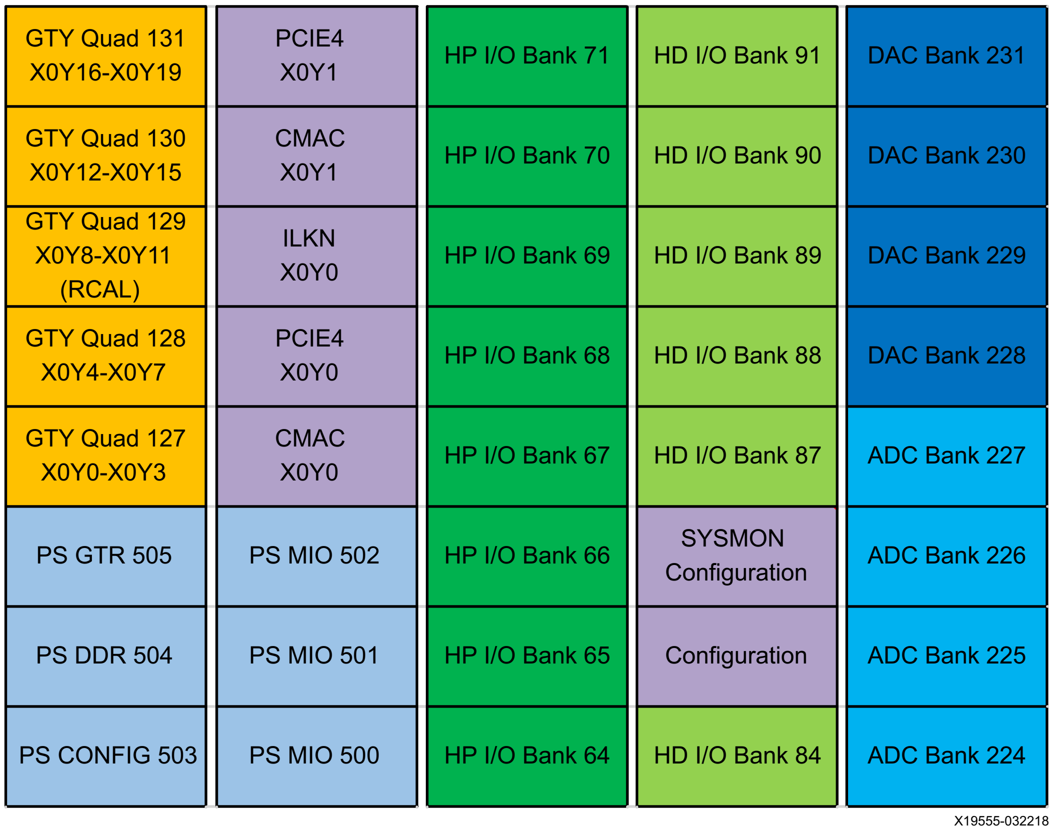


Figure 1-40: **XCZU29DR Banks**

Bank Diagram by Package for XCZU29DR

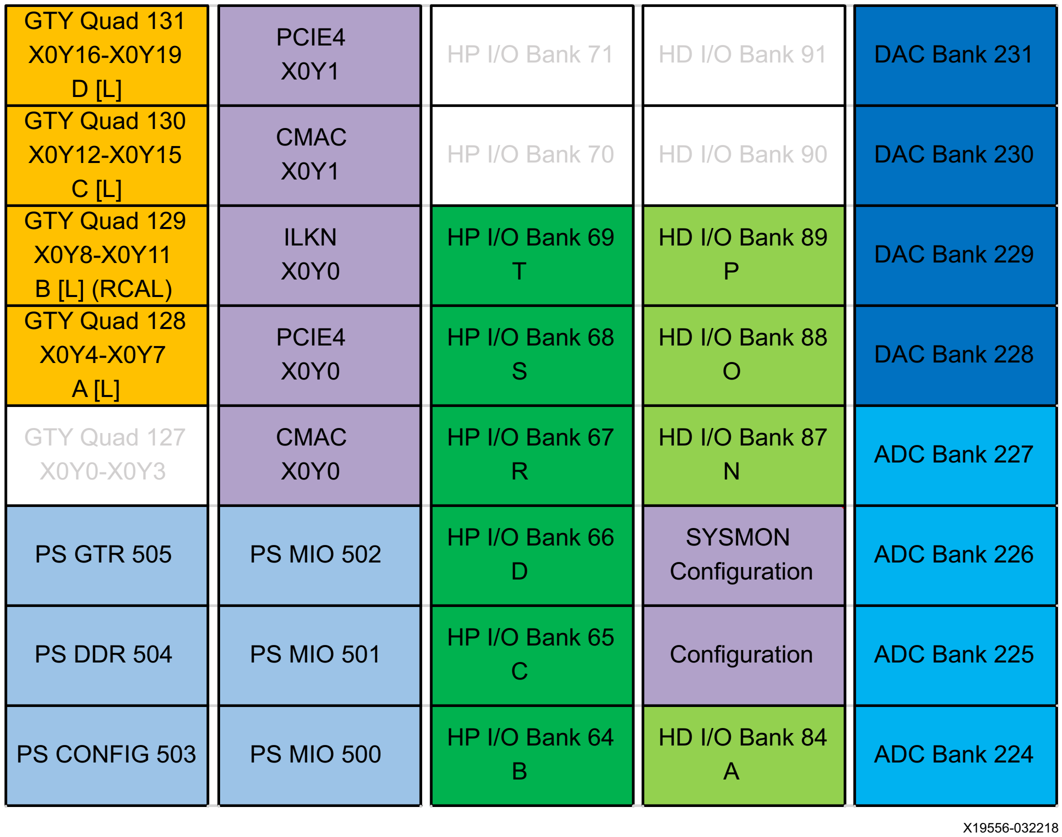


Figure 1-41: **XCZU29DR Banks in FFVF1760 and FSVF1760 Packages**

PS Memory Interface Pin Guidelines

Introduction to PS Memory Interface Pins

This chapter shows what is needed to support the broad requirements of various memory interfaces using the *UltraScale Architecture GTH Transceiver User Guide®* UltraScale+™ device processor system (PS) memory. It covers DDR3/3L, DDR4, LPDDR4, and LPDDR3.

DDR3/3L Guidelines

DDR3/3L Pin Rules

The DDR3/3L pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in a 64-bit interface without ECC, the PS_DDR_DQ64 to PS_DDR_DQ71, PS_DDR_DQS_P8/N8, and PS_DDR_DM8 pins can be left unconnected.
- Connect the PS_DDR_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the FPGA and at the DRAM.

DDR3/3L Pin Swapping Restrictions

- Address/command/control bits cannot be swapped.
- DQ byte lane swapping is allowed.
- DQ bits swapping within a byte lane is allowed.

DDR3/3L Pinout Example for Supported Configurations

Table 2-1 shows a pinout example for the DDR3/3L supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide* [Ref 12].

Table 2-1: **DDR3/3L Supported Pinout Configurations**

Pin Name	DDR3/3L 64-bit 1Rank	DDR3/3L 64-bit 2Rank	DDR3/3L 32-bit 1Rank	DDR3/3L 32-bit 2Rank
PS_DDR_A0 to PS_DDR_A15	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.
PS_DDR_A16	WE#.	WE#.	WE#.	WE#.
PS_DDR_A17	CAS#.	CAS#.	CAS#.	CAS#.
PS_DDR_ACT_N	RAS#.	RAS#.	RAS#.	RAS#.
PS_DDR_ALERT_N	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_BA0	BA[0].	BA[0].	BA[0].	BA[0].
PS_DDR_BA1	BA[1].	BA[1].	BA[1].	BA[1].
PS_DDR_BG0	BA[2].	BA[2].	BA[2].	BA[2].
PS_DDR_BG1	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_CK_N0	CK#.	CK#[0].	CK#.	CK#[0].
PS_DDR_CK_N1	Can be left unconnected.	CK#[1].	Can be left unconnected.	CK#[1].
PS_DDR_CK0	CK.	CK[0].	CK.	CK[0].
PS_DDR_CK1	Can be left unconnected.	CK[1].	Can be left unconnected.	CK[1].
PS_DDR_CKE0	CKE.	CKE[0].	CKE.	CKE[0].
PS_DDR_CKE1	Can be left unconnected.	CKE[1].	Can be left unconnected.	CKE[1].
PS_DDR_CS_N0	CS#.	CS#[0].	CS#.	CS#[0].
PS_DDR_CS_N1	Can be left unconnected.	CS#[1].	Can be left unconnected.	CS#[1].
PS_DDR_DM0 to PS_DDR_DM3	Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on.	Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on.	Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on.	Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on.
PS_DDR_DM4 to PS_DDR_DM7	Connect DM4 to PS_DDR_DM4, DM5 to PS_DDR_DM5, and so on.	Connect DM4 to PS_DDR_DM4, DM5 to PS_DDR_DM5, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DM8	DM8, can be left unconnected without ECC.	DM8, can be left unconnected without ECC.	DM4, can be left unconnected without ECC.	DM4, can be left unconnected without ECC.
PS_DDR_DQ0 to PS_DDR_DQ31	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.

Table 2-1: **DDR3/3L Supported Pinout Configurations *(Cont'd)***

Pin Name	DDR3/3L 64-bit 1Rank	DDR3/3L 64-bit 2Rank	DDR3/3L 32-bit 1Rank	DDR3/3L 32-bit 2Rank
PS_DDR_DQ32 to PS_DDR_DQ63	Connect DQ32 to PS_DDR_DQ32, DQ33 to PS_DDR_DQ33, and so on.	Connect DQ32 to PS_DDR_DQ32, DQ33 to PS_DDR_DQ33, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQ64	DQ64 (ECC_bit[0]), can be left unconnected without ECC.	DQ64 (ECC_bit[0]), can be left unconnected without ECC.	DQ32 (ECC_bit[0]), can be left unconnected without ECC.	DQ32 (ECC_bit[0]), can be left unconnected without ECC.
PS_DDR_DQ65	DQ65 (ECC_bit[1]), can be left unconnected without ECC.	DQ65 (ECC_bit[1]), can be left unconnected without ECC.	DQ33 (ECC_bit[1]), can be left unconnected without ECC.	DQ33 (ECC_bit[1]), can be left unconnected without ECC.
PS_DDR_DQ66	DQ66 (ECC_bit[2]), can be left unconnected without ECC.	DQ66 (ECC_bit[2]), can be left unconnected without ECC.	DQ34 (ECC_bit[2]), can be left unconnected without ECC.	DQ34 (ECC_bit[2]), can be left unconnected without ECC.
PS_DDR_DQ67	DQ67 (ECC_bit[3]), can be left unconnected without ECC.	DQ67 (ECC_bit[3]), can be left unconnected without ECC.	DQ35 (ECC_bit[3]), can be left unconnected without ECC.	DQ35 (ECC_bit[3]), can be left unconnected without ECC.
PS_DDR_DQ68	DQ68 (ECC_bit[4]), can be left unconnected without ECC.	DQ68 (ECC_bit[4]), can be left unconnected without ECC.	DQ36 (ECC_bit[4]), can be left unconnected without ECC.	DQ36 (ECC_bit[4]), can be left unconnected without ECC.
PS_DDR_DQ69	DQ69 (ECC_bit[5]), can be left unconnected without ECC.	DQ69 (ECC_bit[5]), can be left unconnected without ECC.	DQ37 (ECC_bit[5]), can be left unconnected without ECC.	DQ37 (ECC_bit[5]), can be left unconnected without ECC.
PS_DDR_DQ70	DQ70 (ECC_bit[6]), can be left unconnected without ECC.	DQ70 (ECC_bit[6]), can be left unconnected without ECC.	DQ38 (ECC_bit[6]), can be left unconnected without ECC.	DQ38 (ECC_bit[6]), can be left unconnected without ECC.
PS_DDR_DQ71	DQ71 (ECC_bit[7]), can be left unconnected without ECC.	DQ71 (ECC_bit[7]), can be left unconnected without ECC.	DQ39 (ECC_bit[7]), can be left unconnected without ECC.	DQ39 (ECC_bit[7]), can be left unconnected without ECC.
PS_DDR_DQS_N0 to PS_DDR_DQS_N3	Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.	Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.	Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.	Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.

Table 2-1: **DDR3/3L Supported Pinout Configurations *(Cont'd)***

Pin Name	DDR3/3L 64-bit 1Rank	DDR3/3L 64-bit 2Rank	DDR3/3L 32-bit 1Rank	DDR3/3L 32-bit 2Rank
PS_DDR_DQS_N4 to PS_DDR_DQS_N7	Connect DQS#4 to PS_DDR_DQS_N4, DQS#5 to PS_DDR_DQS_N5, and so on.	Connect DQS#4 to PS_DDR_DQS_N4, DQS#5 to PS_DDR_DQS_N5, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQS_N8	DQS#8, can be left unconnected without ECC.	DQS#8, can be left unconnected without ECC.	DQS#4, can be left unconnected without ECC.	DQS#4, can be left unconnected without ECC.
PS_DDR_DQS_P0 to PS_DDR_DQS_P3	Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.	Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.	Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.	Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.
PS_DDR_DQS_P4 to PS_DDR_DQS_P7	Connect DQS4 to PS_DDR_DQS_P4, DQS5 to PS_DDR_DQS_P5, and so on.	Connect DQS4 to PS_DDR_DQS_P4, DQS5 to PS_DDR_DQS_P5, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQS_P8	DQS8, can be left unconnected without ECC.	DQS8, can be left unconnected without ECC.	DQS4, can be left unconnected without ECC.	DQS4, can be left unconnected without ECC.
PS_DDR_ODT0	ODT.	ODT[0].	ODT.	ODT[0].
PS_DDR_ODT1	Can be left unconnected.	ODT[1].	Can be left unconnected.	ODT[1].
PS_DDR_PARITY	Par_In for RDIMMs. Can be left unconnected for components and UDIMMs.	Par_In for RDIMMs. Can be left unconnected for components and UDIMMs.	Par_In for RDIMMs. Can be left unconnected for components and UDIMMs.	Par_In for RDIMMs. Can be left unconnected for components and UDIMMs.
PS_DDR_RAM_RST_N	RESET#.	RESET#.	RESET#.	RESET#.
PS_DDR_ZQ	Connect a 240Ω resistor to GND.(1)	Connect a 240Ω resistor to GND.(1)	Connect a 240Ω resistor to GND.(1)	Connect a 240Ω resistor to GND.(1)

Notes:

1. There should be separate 240Ω resistors at the FPGA and at the DRAM.

DDR4 Guidelines

DDR4 Pin Rules

The DDR4 pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in a 64-bit interface without ECC, the PS_DDR_DQ64 to PS_DDR_DQ71, PS_DDR_DQS_P8/N8, and PS_DDR_DM8 pins can be left unconnected.
- For component interfaces, the PS_DDR_ALERT_N pin must be connected with fly-by routing to a 50Ω pull-up resistor to V_{CC} at the last DRAM component. If unused, the PS_DDR_ALERT_N for the FPGA and the DRAMs must be connected to a 4.7KΩ pull-up resistor to V_{DDQ}/V_{CCO_DDR}. The PS_DDR_ALERT_N can be left floating at the DRAM.
- Connect the PS_DDR_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the FPGA and at the DRAM.
- Component interfaces with the same component for all components in the interface. The x16 components have a different number of bank groups than the x8 components. For example, create a 72-bit wide component interface by using nine x8 components or five x16 components, where half of one component is not used. Creating four x16 components and one x8 component is not permissible.

DDR4 Pin Swapping Restrictions

- Address/command/control bits cannot be swapped.
- DQ byte lane swapping is allowed.
- DQ bits swapping within a byte lane is allowed.

DDR4 Pinout Example for Supported Configurations

Table 2-2 shows a pinout example for the DDR4 supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide* [Ref 12].

Table 2-2: **DDR4 Supported Pinout Configurations**

Pin Name	DDR4 64-bit 1Rank	DDR4 64-bit 2Rank	DDR4 32-bit 1Rank	DDR4 32-bit 2Rank
PS_DDR_A0 to PS_DDR_A17	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.	Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.
PS_DDR_ACT_N	ACT_n.	ACT_n.	ACT_n.	ACT_n.
PS_DDR_ALERT_N	ALERT_n.	ALERT_n.	ALERT_n.	ALERT_n.

Table 2-2: **DDR4 Supported Pinout Configurations *(Cont'd)***

Pin Name	DDR4 64-bit 1Rank	DDR4 64-bit 2Rank	DDR4 32-bit 1Rank	DDR4 32-bit 2Rank
PS_DDR_BA0	BA[0].	BA[0].	BA[0].	BA[0].
PS_DDR_BA1	BA[1].	BA[1].	BA[1].	BA[1].
PS_DDR_BG0	BG[0].	BG[0].	BG[0].	BG[0].
PS_DDR_BG1	BG[1].	BG[1].	BG[1].	BG[1].
PS_DDR_CK_N0	CK_c[0].	CK_c[0].	CK_c[0].	CK_c[0].
PS_DDR_CK_N1	Can be left unconnected.	CK_c[1].	Can be left unconnected.	CK_c[1].
PS_DDR_CK0	CK_t[0].	CK_t[0].	CK_t[0].	CK_t[0].
PS_DDR_CK1	Can be left unconnected.	CK_t[1].	Can be left unconnected.	CK_t[1].
PS_DDR_CKE0	CKE.	CKE[0].	CKE.	CKE[0].
PS_DDR_CKE1	Can be left unconnected.	CKE[1].	Can be left unconnected.	CKE[1].
PS_DDR_CS_N0	CS_n.	CS_n[0].	CS_n.	CS_n[0].
PS_DDR_CS_N1	Can be left unconnected.	CS_n[1].	Can be left unconnected.	CS_n[1].
PS_DDR_DM0 to PS_DDR_DM3	Connect DM_n[0]/DBI_n[0] to PS_DDR_DM0, DM_n[1]/DBI_n[1] to PS_DDR_DM1, and so on.	Connect DM_n[0]/DBI_n[0] to PS_DDR_DM0, DM_n[1]/DBI_n[1] to PS_DDR_DM1, and so on.	Connect DM_n[0]/DBI_n[0] to PS_DDR_DM0, DM_n[1]/DBI_n[1] to PS_DDR_DM1, and so on.	Connect DM_n[0]/DBI_n[0] to PS_DDR_DM0, DM_n[1]/DBI_n[1] to PS_DDR_DM1, and so on.
PS_DDR_DM4 to PS_DDR_DM7	Connect DM_n[4]/DBI_n[4] to PS_DDR_DM4, DM_n[5]/DBI_n[5] to PS_DDR_DM5, and so on.	Connect DM_n[4]/DBI_n[4] to PS_DDR_DM4, DM_n[5]/DBI_n[5] to PS_DDR_DM5, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DM8	DM_n[8]/DBI_n[8], can be left unconnected without ECC.	DM_n[8]/DBI_n[8], can be left unconnected without ECC.	DM_n[4]/DBI_n[4], can be left unconnected without ECC.	DM_n[4]/DBI_n[4], can be left unconnected without ECC.
PS_DDR_DQ0 to PS_DDR_DQ31	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.	Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.
PS_DDR_DQ32 to PS_DDR_DQ63	Connect DQ32 to PS_DDR_DQ32, DQ33 to PS_DDR_DQ33, and so on.	Connect DQ32 to PS_DDR_DQ32, DQ33 to PS_DDR_DQ33, and so on.	Can be left unconnected.	Can be left unconnected.

Table 2-2: **DDR4 Supported Pinout Configurations *(Cont'd)***

Pin Name	DDR4 64-bit 1Rank	DDR4 64-bit 2Rank	DDR4 32-bit 1Rank	DDR4 32-bit 2Rank
PS_DDR_DQ64	DQ64 (ECC_bit[0]), can be left unconnected without ECC.	DQ64 (ECC_bit[0]), can be left unconnected without ECC.	DQ32 (ECC_bit[0]), can be left unconnected without ECC.	DQ32 (ECC_bit[0]), can be left unconnected without ECC.
PS_DDR_DQ65	DQ65 (ECC_bit[1]), can be left unconnected without ECC.	DQ65 (ECC_bit[1]), can be left unconnected without ECC.	DQ33 (ECC_bit[1]), can be left unconnected without ECC.	DQ33 (ECC_bit[1]), can be left unconnected without ECC.
PS_DDR_DQ66	DQ66 (ECC_bit[2]), can be left unconnected without ECC.	DQ66 (ECC_bit[2]), can be left unconnected without ECC.	DQ34 (ECC_bit[2]), can be left unconnected without ECC.	DQ34 (ECC_bit[2]), can be left unconnected without ECC.
PS_DDR_DQ67	DQ67 (ECC_bit[3]), can be left unconnected without ECC.	DQ67 (ECC_bit[3]), can be left unconnected without ECC.	DQ35 (ECC_bit[3]), can be left unconnected without ECC.	DQ35 (ECC_bit[3]), can be left unconnected without ECC.
PS_DDR_DQ68	DQ68 (ECC_bit[4]), can be left unconnected without ECC.	DQ68 (ECC_bit[4]), can be left unconnected without ECC.	DQ36 (ECC_bit[4]), can be left unconnected without ECC.	DQ36 (ECC_bit[4]), can be left unconnected without ECC.
PS_DDR_DQ69	DQ69 (ECC_bit[5]), can be left unconnected without ECC.	DQ69 (ECC_bit[5]), can be left unconnected without ECC.	DQ37 (ECC_bit[5]), can be left unconnected without ECC.	DQ37 (ECC_bit[5]), can be left unconnected without ECC.
PS_DDR_DQ70	DQ70 (ECC_bit[6]), can be left unconnected without ECC.	DQ70 (ECC_bit[6]), can be left unconnected without ECC.	DQ38 (ECC_bit[6]), can be left unconnected without ECC.	DQ38 (ECC_bit[6]), can be left unconnected without ECC.
PS_DDR_DQ71	DQ71 (ECC_bit[7]), can be left unconnected without ECC.	DQ71 (ECC_bit[7]), can be left unconnected without ECC.	DQ39 (ECC_bit[7]), can be left unconnected without ECC.	DQ39 (ECC_bit[7]), can be left unconnected without ECC.
PS_DDR_DQS_N0 to PS_DDR_DQS_N3	Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on.	Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on.	Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on.	Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on.
PS_DDR_DQS_N4 to PS_DDR_DQS_N7	Connect DQS_c4 to PS_DDR_DQS_N4, DQS_c5 to PS_DDR_DQS_N5, and so on.	Connect DQS_c4 to PS_DDR_DQS_N4, DQS_c5 to PS_DDR_DQS_N5, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQS_N8	DQS_c8, can be left unconnected without ECC.	DQS_c8, can be left unconnected without ECC.	DQS_c4, can be left unconnected without ECC.	DQS_c4, can be left unconnected without ECC.

Table 2-2: **DDR4 Supported Pinout Configurations *(Cont'd)***

Pin Name	DDR4 64-bit 1Rank	DDR4 64-bit 2Rank	DDR4 32-bit 1Rank	DDR4 32-bit 2Rank
PS_DDR_DQS_P0 to PS_DDR_DQS_P3	Connect DQS_t0 to PS_DDR_DQS_P0, DQS_t1 to PS_DDR_DQS_P1, and so on.	Connect DQS_t0 to PS_DDR_DQS_P0, DQS_t1 to PS_DDR_DQS_P1, and so on.	Connect DQS_t0 to PS_DDR_DQS_P0, DQS_t1 to PS_DDR_DQS_P1, and so on.	Connect DQS_t0 to PS_DDR_DQS_P0, DQS_t1 to PS_DDR_DQS_P1, and so on.
PS_DDR_DQS_P4 to PS_DDR_DQS_P7	Connect DQS_t4 to PS_DDR_DQS_P4, DQS_t5 to PS_DDR_DQS_P5, and so on.	Connect DQS_t4 to PS_DDR_DQS_P4, DQS_t5 to PS_DDR_DQS_P5, and so on.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQS_P8	DQS_t8, can be left unconnected without ECC.	DQS_t8, can be left unconnected without ECC.	DQS_t4, can be left unconnected without ECC.	DQS_t4, can be left unconnected without ECC.
PS_DDR_ODT0	ODT.	ODT[0].	ODT.	ODT[0].
PS_DDR_ODT1	Can be left unconnected.	ODT[1].	Can be left unconnected.	ODT[1].
PS_DDR_PARITY	PAR.	PAR.	PAR.	PAR.
PS_DDR_RAM_RST_N	RESET_n.	RESET_n.	RESET_n.	RESET_n.
PS_DDR_ZQ	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor.	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor.	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor.	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor.

LPDDR4 Guidelines

LPDDR4 Pin Rules

The LPDDR4 pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in an 64-bit interface without ECC, the PS_DDR_DQ64 to PS_DDR_DQ71, PS_DDR_DQS_P8/N8, and PS_DDR_DM8 pins can be left unconnected.
- Connect the PS_DDR_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the FPGA and at the DRAM.
- To achieve maximum performance, address copy mode is suggested.

LPDDR4 Pin Swapping Restrictions

- Command/address bits cannot be swapped.
- To support command/address training, DQ byte lane swapping is not allowed.
- To support command/address training, DQ bits with bytes 0, 2, and 8 are not allowed to be swapped.
- Bits within bytes 1 and 3 can be swapped.

LPDDR4 Pinout Example for Supported Configurations

Table 2-3 shows a pinout example for the LPDDR4 supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide* [Ref 12].

Table 2-3: **LPDDR4 Supported Pinout Configurations**

Pin Name	LPDDR4 32-bit 1Rank	LPDDR4 32-bit 1Rank ECC	LPDDR4 32-bit 2Rank	LPDDR4 32-bit 2Rank ECC
PS_DDR_A0	CA0_A.	CA0_A.	CA0_A.	CA0_A.
PS_DDR_A1	CA1_A.	CA1_A.	CA1_A.	CA1_A.
PS_DDR_A2	CA2_A.	CA2_A.	CA2_A.	CA2_A.
PS_DDR_A3	CA3_A.	CA3_A.	CA3_A.	CA3_A.
PS_DDR_A4	CA4_A.	CA4_A.	CA4_A.	CA4_A.
PS_DDR_A5	CA5_A.	CA5_A.	CA5_A.	CA5_A.
PS_DDR_A6 to PS_DDR_A9	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_A10	CA0_B.	CA0_B.	CA0_B.	CA0_B.
PS_DDR_A11	CA1_B.	CA1_B.	CA1_B.	CA1_B.

Table 2-3: **LPDDR4 Supported Pinout Configurations *(Cont'd)***

Pin Name	LPDDR4 32-bit 1Rank	LPDDR4 32-bit 1Rank ECC	LPDDR4 32-bit 2Rank	LPDDR4 32-bit 2Rank ECC
PS_DDR_A12	CA2_B.	CA2_B.	CA2_B.	CA2_B.
PS_DDR_A13	CA3_B.	CA3_B.	CA3_B.	CA3_B.
PS_DDR_A14	CA4_B.	CA4_B.	CA4_B.	CA4_B.
PS_DDR_A15	CA5_B.	CA5_B.	CA5_B.	CA5_B.
PS_DDR_A16	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_A17	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_ACT_N	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_ALERT_N	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_BA0	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_BA1	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_BG0	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_BG1	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_CK_N0	CK_c_A.	CK_c_A.	CK_c_A.	CK_c_A.
PS_DDR_CK_N1	CK_c_B.	CK_c_B.	CK_c_B.	CK_c_B.
PS_DDR_CK0	CK_t_A.	CK_t_A.	CK_t_A.	CK_t_A.
PS_DDR_CK1	CK_t_B.	CK_t_B.	CK_t_B.	CK_t_B.
PS_DDR_CKE0	CKE_A and CKE_B.	CKE_A.	CKE0_A and CKE0_B.	CKE0_A.
PS_DDR_CKE1	Can be left unconnected.	Can be left unconnected.	CKE1_A and CKE1_B.	CKE1_A.
PS_DDR_CS_N0	CS_A and CS_B.	CS_A.	CS0_A and CS0_B.	CS0_A.
PS_DDR_CS_N1	Can be left unconnected.	Can be left unconnected.	CS1_A and CS1_B.	CS1_A.
PS_DDR_DM0	DMI0_A.	DMI0_A.	DMI0_A.	DMI0_A.
PS_DDR_DM1	DMI1_A.	DMI1_A.	DMI1_A.	DMI1_A.
PS_DDR_DM2	DMI0_B.	DMI0_B.	DMI0_B.	DMI0_B.
PS_DDR_DM3	DMI1_B.	DMI1_B.	DMI1_B.	DMI1_B.
PS_DDR_DM4 to PS_DDR_DM7	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DM8	Can be left unconnected.	DMI_ECC.	Can be left unconnected.	DMI_ECC.

Table 2-3: **LPDDR4 Supported Pinout Configurations *(Cont'd)***

Pin Name	LPDDR4 32-bit 1Rank	LPDDR4 32-bit 1Rank ECC	LPDDR4 32-bit 2Rank	LPDDR4 32-bit 2Rank ECC
PS_DDR_DQ0 to PS_DDR_DQ15	Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.	Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.	Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.	Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.
PS_DDR_DQ16 to PS_DDR_DQ31	Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on.	Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on.	Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on.	Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on.
PS_DDR_DQ32 to PS_DDR_DQ63	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQ64	Can be left unconnected.	DQ_ECC0 (ECC_bit[0]).	Can be left unconnected.	DQ_ECC0 (ECC_bit[0]).
PS_DDR_DQ65	Can be left unconnected.	DQ_ECC1 (ECC_bit[1]).	Can be left unconnected.	DQ_ECC1 (ECC_bit[1]).
PS_DDR_DQ66	Can be left unconnected.	DQ_ECC2 (ECC_bit[2]).	Can be left unconnected.	DQ_ECC2 (ECC_bit[2]).
PS_DDR_DQ67	Can be left unconnected.	DQ_ECC3 (ECC_bit[3]).	Can be left unconnected.	DQ_ECC3 (ECC_bit[3]).
PS_DDR_DQ68	Can be left unconnected.	DQ_ECC4 (ECC_bit[4]).	Can be left unconnected.	DQ_ECC4 (ECC_bit[4]).
PS_DDR_DQ69	Can be left unconnected.	DQ_ECC5 (ECC_bit[5]).	Can be left unconnected.	DQ_ECC5 (ECC_bit[5]).
PS_DDR_DQ70	Can be left unconnected.	DQ_ECC6 (ECC_bit[6]).	Can be left unconnected.	DQ_ECC6 (ECC_bit[6]).
PS_DDR_DQ71	Can be left unconnected.	DQ_ECC7 (ECC_bit[7]).	Can be left unconnected.	DQ_ECC7 (ECC_bit[7]).
PS_DDR_DQS_N0	DQS0_c_A.	DQS0_c_A.	DQS0_c_A.	DQS0_c_A.
PS_DDR_DQS_N1	DQS1_c_A.	DQS1_c_A.	DQS1_c_A.	DQS1_c_A.
PS_DDR_DQS_N2	DQS0_c_B.	DQS0_c_B.	DQS0_c_B.	DQS0_c_B.
PS_DDR_DQS_N3	DQS1_c_B.	DQS1_c_B.	DQS1_c_B.	DQS1_c_B.
PS_DDR_DQS_N4 to PS_DDR_DQS_N7	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQS_N8	Can be left unconnected.	DQS_c_ECC.	Can be left unconnected.	DQS_c_ECC.
PS_DDR_DQS_P0	DQS0_t_A.	DQS0_t_A.	DQS0_t_A.	DQS0_t_A.
PS_DDR_DQS_P1	DQS1_t_A.	DQS1_t_A.	DQS1_t_A.	DQS1_t_A.
PS_DDR_DQS_P2	DQS0_t_B.	DQS0_t_B.	DQS0_t_B.	DQS0_t_B.
PS_DDR_DQS_P3	DQS1_t_B.	DQS1_t_B.	DQS1_t_B.	DQS1_t_B.

Table 2-3: **LPDDR4 Supported Pinout Configurations *(Cont'd)***

Pin Name	LPDDR4 32-bit 1Rank	LPDDR4 32-bit 1Rank ECC	LPDDR4 32-bit 2Rank	LPDDR4 32-bit 2Rank ECC
PS_DDR_DQS_P4 to PS_DDR_DQS_P7	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_DQS_P8	Can be left unconnected.	DQS_t_ECC.	Can be left unconnected.	DQS_t_ECC.
PS_DDR_ODT0	Unconnected at FPGA.	Unconnected at FPGA.	Unconnected at FPGA.	Unconnected at FPGA.
PS_DDR_ODT1	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_PARITY	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_RAM_RST_N	RESET_n.	RESET_n.	RESET_n.	RESET_n.
PS_DDR_ZQ	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor.	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor.	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor.	Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor.

LPDDR3 Guidelines

LPDDR3 Pin Rules

The LPDDR3 pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in an 64-bit interface without ECC, the PS_DDR_DQ64 to PS_DDR_DQ71, PS_DDR_DQS_P8/N8, and PS_DDR_DM8 pins can be left unconnected.
- Connect the PS_DDR_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the FPGA and at the DRAM.
- To achieve maximum performance, address copy mode is suggested.

LPDDR3 Pin Swapping Restrictions

- Command/address bits cannot be swapped.
- To support command/address training, DQ byte lane swapping is not allowed.
- To support command/address training, DQ bits swapping within a byte lane is not allowed.

LPDDR3 Pinout Example for Supported Configurations

Table 2-4 shows a pinout example for the LPDDR3 supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide* [Ref 12].

Table 2-4: **LPDDR3 Supported Pinout Configurations)**

Pin Name	LPDDR3 64-bit (DDP—Single Component)	LPDDR3 64-bit (2 Component)	LPDDR3 32-bit (DDP—Single Component)
PS_DDR_A0	CA0_A.	CA0_A.	CA0.
PS_DDR_A1	CA1_A.	CA1_A.	CA1.
PS_DDR_A2	CA2_A.	CA2_A.	CA2.
PS_DDR_A3	CA3_A.	CA3_A.	CA3.
PS_DDR_A4	CA4_A.	CA4_A.	CA4.
PS_DDR_A5	CA5_A.	CA5_A.	CA5.
PS_DDR_A6	CA6_A.	CA6_A.	CA6.
PS_DDR_A7	CA7_A.	CA7_A.	CA7.
PS_DDR_A8	CA8_A.	CA8_A.	CA8.
PS_DDR_A9	CA9_A.	CA9_A.	CA9.
PS_DDR_A10	CA0_B.	CA0_B.	Can be left unconnected.

Table 2-4: **LPDDR3 Supported Pinout Configurations)** ***(Cont'd)***

Pin Name	LPDDR3 64-bit (DDP—Single Component)	LPDDR3 64-bit (2 Component)	LPDDR3 32-bit (DDP—Single Component)
PS_DDR_A11	CA1_B.	CA1_B.	Can be left unconnected.
PS_DDR_A12	CA2_B.	CA2_B.	Can be left unconnected.
PS_DDR_A13	CA3_B.	CA3_B.	Can be left unconnected.
PS_DDR_A14	CA4_B.	CA4_B.	Can be left unconnected.
PS_DDR_A15	CA5_B.	CA5_B.	Can be left unconnected.
PS_DDR_A16	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_A17	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_ACT_N	CA9_B.	CA9_B.	Can be left unconnected.
PS_DDR_ALERT_N	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_BA0	CA6_B.	CA6_B.	Can be left unconnected.
PS_DDR_BA1	CA7_B.	CA7_B.	Can be left unconnected.
PS_DDR_BG0	CA8_B.	CA8_B.	Can be left unconnected.
PS_DDR_BG1	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_CK_N0	CK_c_A.	CK_c_A.	CK_c.
PS_DDR_CK_N1	CK_c_B.	CK_c_B.	Can be left unconnected.
PS_DDR_CK0	CK_t_A.	CK_t_A.	CK_t.
PS_DDR_CK1	CK_t_B.	CK_t_B.	Can be left unconnected.
PS_DDR_CKE0	CKE_A.	CKE0_A and CKE0_B.	CKE0.
PS_DDR_CKE1	CKE_B.	CKE1_A and CKE1_B.	CKE1.
PS_DDR_CS_N0	CS_n_A.	CS0_n_A and CS0_n_B.	CS0_n.
PS_DDR_CS_N1	CS_n_B.	CS1_n_A and CS1_n_B.	CS1_n.
PS_DDR_DM0	DM0_A.	DM0_A.	DM0.
PS_DDR_DM1	DM1_A.	DM1_A.	DM1.
PS_DDR_DM2	DM2_A.	DM2_A.	DM2.
PS_DDR_DM3	DM3_A.	DM3_A.	DM3.
PS_DDR_DM4	DM0_B.	DM0_B.	Can be left unconnected.
PS_DDR_DM5	DM1_B.	DM1_B.	Can be left unconnected.
PS_DDR_DM6	DM2_B.	DM2_B.	Can be left unconnected.
PS_DDR_DM7	DM3_B.	DM3_B.	Can be left unconnected.
PS_DDR_DM8	DM_ECC, can be left unconnected without ECC.	DM_ECC, can be left unconnected without ECC.	DM_ECC, can be left unconnected without ECC.
PS_DDR_DQ0	DQ0_A.	DQ0_A.	DQ0.
PS_DDR_DQ1	DQ1_A.	DQ1_A.	DQ1.
PS_DDR_DQ2	DQ2_A.	DQ2_A.	DQ2.

Table 2-4: **LPDDR3 Supported Pinout Configurations)** ***(Cont'd)***

Pin Name	LPDDR3 64-bit (DDP—Single Component)	LPDDR3 64-bit (2 Component)	LPDDR3 32-bit (DDP—Single Component)
PS_DDR_DQ3	DQ3_A.	DQ3_A.	DQ3.
PS_DDR_DQ4	DQ4_A.	DQ4_A.	DQ4.
PS_DDR_DQ5	DQ5_A.	DQ5_A.	DQ5.
PS_DDR_DQ6	DQ6_A.	DQ6_A.	DQ6.
PS_DDR_DQ7	DQ7_A.	DQ7_A.	DQ7.
PS_DDR_DQ8	DQ8_A.	DQ8_A.	DQ8.
PS_DDR_DQ9	DQ9_A.	DQ9_A.	DQ9.
PS_DDR_DQ10	DQ10_A.	DQ10_A.	DQ10.
PS_DDR_DQ11	DQ11_A.	DQ11_A.	DQ11.
PS_DDR_DQ12	DQ12_A.	DQ12_A.	DQ12.
PS_DDR_DQ13	DQ13_A.	DQ13_A.	DQ13.
PS_DDR_DQ14	DQ14_A.	DQ14_A.	DQ14.
PS_DDR_DQ15	DQ15_A.	DQ15_A.	DQ15.
PS_DDR_DQ16	DQ16_A.	DQ16_A.	DQ16.
PS_DDR_DQ17	DQ17_A.	DQ17_A.	DQ17.
PS_DDR_DQ18	DQ18_A.	DQ18_A.	DQ18.
PS_DDR_DQ19	DQ19_A.	DQ19_A.	DQ19.
PS_DDR_DQ20	DQ20_A.	DQ20_A.	DQ20.
PS_DDR_DQ21	DQ21_A.	DQ21_A.	DQ21.
PS_DDR_DQ22	DQ22_A.	DQ22_A.	DQ22.
PS_DDR_DQ23	DQ23_A.	DQ23_A.	DQ23.
PS_DDR_DQ24	DQ24_A.	DQ24_A.	DQ24.
PS_DDR_DQ25	DQ25_A.	DQ25_A.	DQ25.
PS_DDR_DQ26	DQ26_A.	DQ26_A.	DQ26.
PS_DDR_DQ27	DQ27_A.	DQ27_A.	DQ27.
PS_DDR_DQ28	DQ28_A.	DQ28_A.	DQ28.
PS_DDR_DQ29	DQ29_A.	DQ29_A.	DQ29.
PS_DDR_DQ30	DQ30_A.	DQ30_A.	DQ30.
PS_DDR_DQ31	DQ31_A.	DQ31_A.	DQ31.
PS_DDR_DQ32	DQ0_B.	DQ0_B.	Can be left unconnected.
PS_DDR_DQ33	DQ1_B.	DQ1_B.	Can be left unconnected.
PS_DDR_DQ34	DQ2_B.	DQ2_B.	Can be left unconnected.
PS_DDR_DQ35	DQ3_B.	DQ3_B.	Can be left unconnected.
PS_DDR_DQ36	DQ4_B.	DQ4_B.	Can be left unconnected.

Table 2-4: **LPDDR3 Supported Pinout Configurations) *(Cont'd)***

Pin Name	LPDDR3 64-bit (DDP—Single Component)	LPDDR3 64-bit (2 Component)	LPDDR3 32-bit (DDP—Single Component)
PS_DDR_DQ37	DQ5_B.	DQ5_B.	Can be left unconnected.
PS_DDR_DQ38	DQ6_B.	DQ6_B.	Can be left unconnected.
PS_DDR_DQ39	DQ7_B.	DQ7_B.	Can be left unconnected.
PS_DDR_DQ40	DQ8_B.	DQ8_B.	Can be left unconnected.
PS_DDR_DQ41	DQ9_B.	DQ9_B.	Can be left unconnected.
PS_DDR_DQ42	DQ10_B.	DQ10_B.	Can be left unconnected.
PS_DDR_DQ43	DQ11_B.	DQ11_B.	Can be left unconnected.
PS_DDR_DQ44	DQ12_B.	DQ12_B.	Can be left unconnected.
PS_DDR_DQ45	DQ13_B.	DQ13_B.	Can be left unconnected.
PS_DDR_DQ46	DQ14_B.	DQ14_B.	Can be left unconnected.
PS_DDR_DQ47	DQ15_B.	DQ15_B.	Can be left unconnected.
PS_DDR_DQ48	DQ16_B.	DQ16_B.	Can be left unconnected.
PS_DDR_DQ49	DQ17_B.	DQ17_B.	Can be left unconnected.
PS_DDR_DQ50	DQ18_B.	DQ18_B.	Can be left unconnected.
PS_DDR_DQ51	DQ19_B.	DQ19_B.	Can be left unconnected.
PS_DDR_DQ52	DQ20_B.	DQ20_B.	Can be left unconnected.
PS_DDR_DQ53	DQ21_B.	DQ21_B.	Can be left unconnected.
PS_DDR_DQ54	DQ22_B.	DQ22_B.	Can be left unconnected.
PS_DDR_DQ55	DQ23_B.	DQ23_B.	Can be left unconnected.
PS_DDR_DQ56	DQ24_B.	DQ24_B.	Can be left unconnected.
PS_DDR_DQ57	DQ25_B.	DQ25_B.	Can be left unconnected.
PS_DDR_DQ58	DQ26_B.	DQ26_B.	Can be left unconnected.
PS_DDR_DQ59	DQ27_B.	DQ27_B.	Can be left unconnected.
PS_DDR_DQ60	DQ28_B.	DQ28_B.	Can be left unconnected.
PS_DDR_DQ61	DQ29_B.	DQ29_B.	Can be left unconnected.
PS_DDR_DQ62	DQ30_B.	DQ30_B.	Can be left unconnected.
PS_DDR_DQ63	DQ31_B.	DQ31_B.	Can be left unconnected.
PS_DDR_DQ64	DQ_ECC0 (ECC_bit[0]), can be left unconnected without ECC.	DQ_ECC0 (ECC_bit[0]), can be left unconnected without ECC.	DQ_ECC0 (ECC_bit[0]), can be left unconnected without ECC.
PS_DDR_DQ65	DQ_ECC1 (ECC_bit[1]), can be left unconnected without ECC.	DQ_ECC1 (ECC_bit[1]), can be left unconnected without ECC.	DQ_ECC1 (ECC_bit[1]), can be left unconnected without ECC.
PS_DDR_DQ66	DQ_ECC2 (ECC_bit[2]), can be left unconnected without ECC.	DQ_ECC2 (ECC_bit[2]), can be left unconnected without ECC.	DQ_ECC2 (ECC_bit[2]), can be left unconnected without ECC.

Table 2-4: **LPDDR3 Supported Pinout Configurations)** ***(Cont'd)***

Pin Name	LPDDR3 64-bit (DDP—Single Component)	LPDDR3 64-bit (2 Component)	LPDDR3 32-bit (DDP—Single Component)
PS_DDR_DQ67	DQ_ECC3 (ECC_bit[3]), can be left unconnected without ECC.	DQ_ECC3 (ECC_bit[3]), can be left unconnected without ECC.	DQ_ECC3 (ECC_bit[3]), can be left unconnected without ECC.
PS_DDR_DQ68	DQ_ECC4 (ECC_bit[4]), can be left unconnected without ECC.	DQ_ECC4 (ECC_bit[4]), can be left unconnected without ECC.	DQ_ECC4 (ECC_bit[4]), can be left unconnected without ECC.
PS_DDR_DQ69	DQ_ECC5 (ECC_bit[5]), can be left unconnected without ECC.	DQ_ECC5 (ECC_bit[5]), can be left unconnected without ECC.	DQ_ECC5 (ECC_bit[5]), can be left unconnected without ECC.
PS_DDR_DQ70	DQ_ECC6 (ECC_bit[6]), can be left unconnected without ECC.	DQ_ECC6 (ECC_bit[6]), can be left unconnected without ECC.	DQ_ECC6 (ECC_bit[6]), can be left unconnected without ECC.
PS_DDR_DQ71	DQ_ECC7 (ECC_bit[7]), can be left unconnected without ECC.	DQ_ECC7 (ECC_bit[7]), can be left unconnected without ECC.	DQ_ECC7 (ECC_bit[7]), can be left unconnected without ECC.
PS_DDR_DQS_N0	DQS0_c_A.	DQS0_c_A.	DQS0_c.
PS_DDR_DQS_N1	DQS1_c_A.	DQS1_c_A.	DQS1_c.
PS_DDR_DQS_N2	DQS2_c_A.	DQS2_c_A.	DQS2_c.
PS_DDR_DQS_N3	DQS3_c_A.	DQS3_c_A.	DQS3_c.
PS_DDR_DQS_N4	DQS0_c_B.	DQS0_c_B.	Can be left unconnected.
PS_DDR_DQS_N5	DQS1_c_B.	DQS1_c_B.	Can be left unconnected.
PS_DDR_DQS_N6	DQS2_c_B.	DQS2_c_B.	Can be left unconnected.
PS_DDR_DQS_N7	DQS3_c_B.	DQS3_c_B.	Can be left unconnected.
PS_DDR_DQS_N8	DQS_c_ECC, can be left unconnected without ECC.	DQS_c_ECC, can be left unconnected without ECC.	DQS_c_ECC, can be left unconnected without ECC.
PS_DDR_DQS_P0	DQS0_t_A.	DQS0_t_A.	DQS0_t.
PS_DDR_DQS_P1	DQS1_t_A.	DQS1_t_A.	DQS1_t.
PS_DDR_DQS_P2	DQS2_t_A.	DQS2_t_A.	DQS2_t.
PS_DDR_DQS_P3	DQS3_t_A.	DQS3_t_A.	DQS3_t.
PS_DDR_DQS_P4	DQS0_t_B.	DQS0_t_B.	Can be left unconnected.
PS_DDR_DQS_P5	DQS1_t_B.	DQS1_t_B.	Can be left unconnected.
PS_DDR_DQS_P6	DQS2_t_B.	DQS2_t_B.	Can be left unconnected.
PS_DDR_DQS_P7	DQS3_t_B.	DQS3_t_B.	Can be left unconnected.
PS_DDR_DQS_P8	DQS_t_ECC, can be left unconnected without ECC.	DQS_t_ECC, can be left unconnected without ECC.	DQS_t_ECC, can be left unconnected without ECC.
PS_DDR_ODT0	ODT_CA_A.	ODT_A and ODT_B.	ODT.
PS_DDR_ODT1	ODT_CA_B.	Can be left unconnected.	Can be left unconnected.
PS_DDR_PARITY	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.

Table 2-4: **LPDDR3 Supported Pinout Configurations)** ***(Cont'd)***

Pin Name	LPDDR3 64-bit (DDP—Single Component)	LPDDR3 64-bit (2 Component)	LPDDR3 32-bit (DDP—Single Component)
PS_DDR_RAM_RST_N	Can be left unconnected.	Can be left unconnected.	Can be left unconnected.
PS_DDR_ZQ	Connect a 240Ω resistor to GND.(1)	Connect a 240Ω resistor to GND.(1)	Connect a 240Ω resistor to GND.(1)

Notes:

1. There should be separate 240Ω resistors at the FPGA and at the DRAM.

Package Files

About ASCII Package Files

The ASCII package files for each Zynq® UltraScale+™ device include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor in fixed-width fonts. The information in each of the files includes:

- Device/Package name (*family-device-package*), with date and time of creation
- Seven columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3 split into upper (U) and lower (L) halves. For more information on the memory byte group, see the *UltraScale Architecture-Based Memory Interface Solutions Product Guide* (PG150) [Ref 13].
  - Bank—Bank number.
  - I/O Type—CONFIG, HD, HP, GTH, GTY, PS-GTR, PSMIO, PSDDR, or PSCONFIG depends on the I/O type. For more information on the I/O type, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571) [Ref 4].
  - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.

Package Specifications Designations

Package specifications are designated as evaluation only, engineering sample, or production. Each designation is defined as follows.

Evaluation Only

These package specifications are based on initial device specifications, package routability analysis and mechanical package construction. Package specifications with this designation are not stable and package pinouts are likely to change and these specifications should only be used for initial system level design feasibility.

Engineering Sample

These package specifications are based on a released package design and validated with ES engineering sample (ES) devices. Package specifications with this designation are considered stable, however some pinout and mechanical specifications might change prior to the production release of the particular device. Package pinouts with this designation are to be used for PCB and Vivado® designs using ES devices.

Production

These package specifications are released coincident with production release of a particular device. Customers receive formal notification of any subsequent changes.

ASCII Pinout Files

Links to the ASCII pinout information device/package combinations are listed in Table 3-1.

Download all available package/device/pinout files at:

www.xilinx.com/support/package-pinout-files/zynq-ultrascale-plus-pkgs.html

Note: All package files are ASCII files in TXT and CSV file format. Only the available files listed in Table 3-1 are linked and consolidated in this ZIP file:

www.xilinx.com/support/packagefiles/zuppackages/zupall.zip

Table 3-1: **Package/Device Pinout Files for CG, EG, and EV devices**

Packages	Footprint Compatible Devices			
SBVA484	XCZU2CG XCZU2EG XAZU2EG Production	XCZU3CG XCZU3EG XAZU3EG Production		
SFVA625	XCZU2CG XCZU2EG XAZU2EG Production	XCZU3CG XCZU3EG XAZU3EG Production		
SFVC784	XCZU2CG XCZU2EG XAZU2EG Production	XCZU3CG XCZU3EG XAZU3EG Production	XCZU4CG XCZU4EG XCZU4EV Production	XCZU5CG XCZU5EG XCZU5EV Production
FBVB900	XCZU4CG XCZU4EG XCZU4EV Production	XCZU5CG XCZU5EG XCZU5EV Production	XCZU7CG XCZU7EG XCZU7EV Production	
FFVC900	XCZU6CG XCZU6EG Production	XCZU9CG XCZU9EG Production	XCZU15EG Production	
FFVB1156	XCZU6CG XCZU6EG Production	XCZU9CG XCZU9EG Production	XCZU15EG Production	
FFVC1156	XCZU7CG XCZU7EG XCZU7EV Production	XCZU11EG Production		

Table 3-1: **Package/Device Pinout Files for CG, EG, and EV devices *(Cont'd)***

Packages	Footprint Compatible Devices			
FFVB1517	XCZU11EG Production	XCZU17EG Production	XCZU19EG Production	
FFVF1517	XCZU7CG XCZU7EG XCZU7EV Production	XCZU11EG Production		
FFVC1760	XCZU11EG Production	XCZU17EG Production	XCZU19EG Production	
FFVD1760	XCZU17EG Production	XCZU19EG Production		
FFVE1924	XCZU17EG Production	XCZU19EG Production		

Table 3-2: **Package/Device Pinout Files for Zynq UltraScale+ RFSoCs**

Package	Footprint Compatible Devices		
FFVD1156	XCZU21DR Engineering Sample		
FFVE1156	XCZU25DR Engineering Sample	XCZU27DR Engineering Sample	XCZU28DR Engineering Sample
FSVE1156	XCZU25DR Engineering Sample	XCZU27DR Engineering Sample	XCZU28DR Engineering Sample
FFVG1517	XCZU25DR Engineering Sample	XCZU27DR Engineering Sample	XCZU28DR Engineering Sample
FSVG1517	XCZU25DR Engineering Sample	XCZU27DR Engineering Sample	XCZU28DR Engineering Sample
FFVF1760	XCZU29DR Engineering Sample		
FSVF1760	XCZU29DR Engineering Sample		

Device Diagrams

Summary

The diagrams in this chapter show top-view perspective of the package pinout of each Zynq® UltraScale+™ device/package combination. Table 4-1 is a cross reference to the device/package diagrams. The I/O-bank diagram shows the location of each user I/O, PSMIO, PSDDR, PSCONFIG, and PS-GTR, GTH, and GTY transceiver and the respective bank or GT quad. The configuration-power diagram shows the location of every power pin and dedicated as well as multi-function configuration pin in the package. See Package Specifications Designations in Chapter 3 for definitions of Evaluation Only, Engineering Sample, and Production device diagrams.

Table 4-1: **Cross-Reference to Zynq UltraScale+ Device Diagrams by Package**

Packages	Footprint Compatible Devices			
SBVA484	XCZU2CG, XCZU2EG, XAZU2EG Production page 95	XCZU3CG, XCZU3EG, XAZU3EG Production page 95		
SFVA625	XCZU2CG, XCZU2EG, XAZU2EG Production page 97	XCZU3CG, XCZU3EG, XAZU3EG Production page 97		
SFVC784	XCZU2CG, XCZU2EG, XAZU2EG Production page 99	XCZU3CG, XCZU3EG, XAZU3EG Production page 99	XCZU4CG, XCZU4EG, XCZU5CG, XCZU5EG Production page 101	XCZU4EV, XCZU5EV Production page 103
FBVB900	XCZU4CG, XCZU4EG, XCZU5CG, XCZU5EG Production page 105	XCZU4EVand XCZU5EV Production page 107	XCZU7CG, XCZU7EG Production page 109	XCZU7EV Production page 111
FFVC900	XCZU6CG, XCZU6EG Production page 113	XCZU9CG, XCZU9EG Production page 113	XCZU15EG Production page 113	

Table 4-1: **Cross-Reference to Zynq UltraScale+ Device Diagrams by Package *(Cont'd)***

Packages	Footprint Compatible Devices			
FFVB1156	XCZU6CG, XCZU6EG Production page 115	XCZU9CG, XCZU9EG Production page 115	XCZU15EG Production page 115	
FFVC1156	XCZU7CG, XCZU7EG Production page 117	XCZU7EV Production page 119	XCZU11EG Production page 121	
FFVD1156	XCZU21DR Engineering Sample page 123			
FFVE1156 FSVE1156	XCZU25DR Engineering Sample page 125	XCZU27DR Engineering Sample page 127	XCZU28DR Engineering Sample page 127	
FFVB1517	XCZU11EG Production page 129	XCZU17EG Production page 131	XCZU19EG Production page 131	
FFVF1517	XCZU7CG, XCZU7EG Production page 133	XCZU7EV Production page 135	XCZU11EG Production page 137	
FFVG1517 FSVG1517	XCZU25DR Engineering Sample page 139	XCZU27DR Engineering Sample page 141	XCZU28DR Engineering Sample page 141	
FFVC1760	XCZU11EG Production page 143	XCZU17EG Production page 145	XCZU19EG Production page 145	
FFVD1760	XCZU17EG Production page 147	XCZU19EG Production page 147		
FFVF1760 FSVF1760	XCZU29DR Engineering Sample page 149			
FFVE1924	XCZU17EG Production page 151	XCZU19EG Production page 151		

SBVA484 Package–XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG

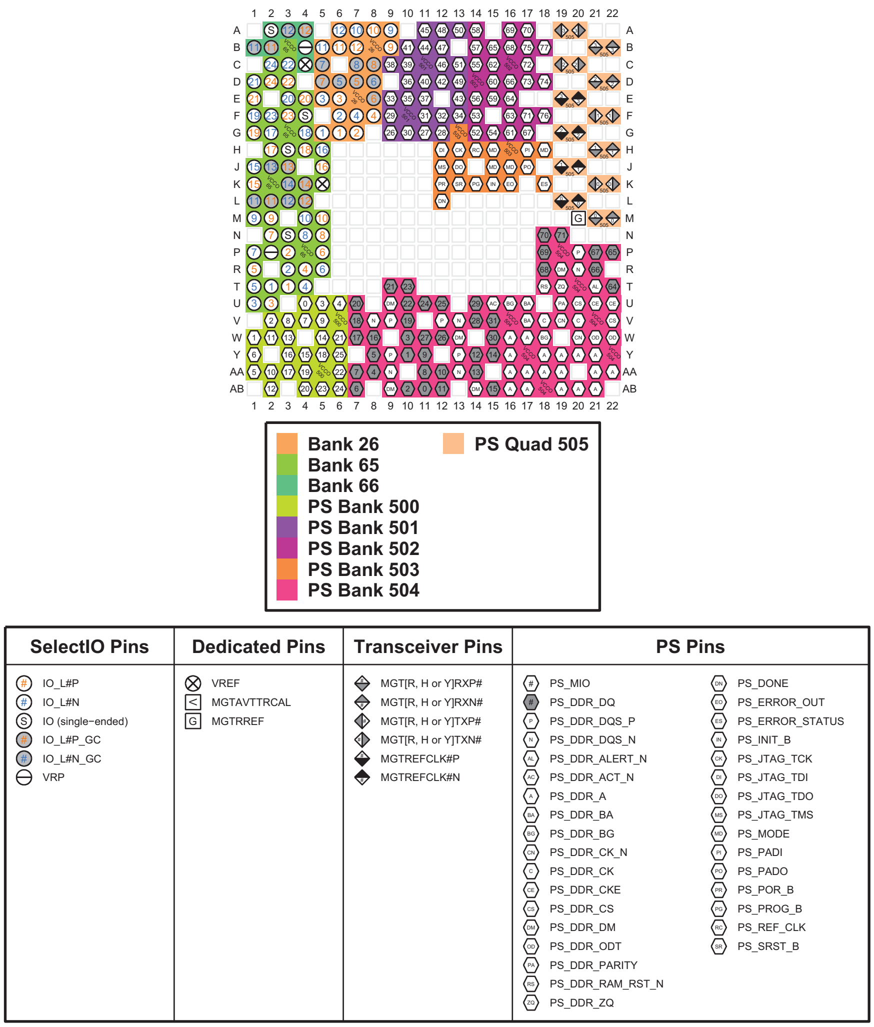
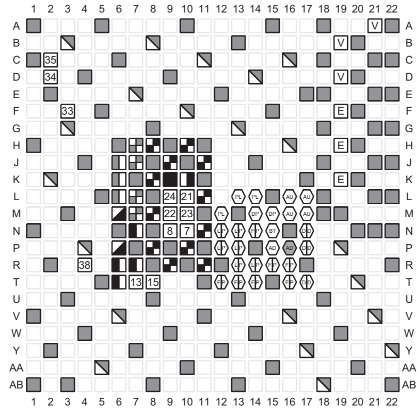


Figure 4-1: **SBVA484 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-2: **SBVA484 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG Power, Dedicated, and Multi-function Pin Diagram**

SFVA625 Package–XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG

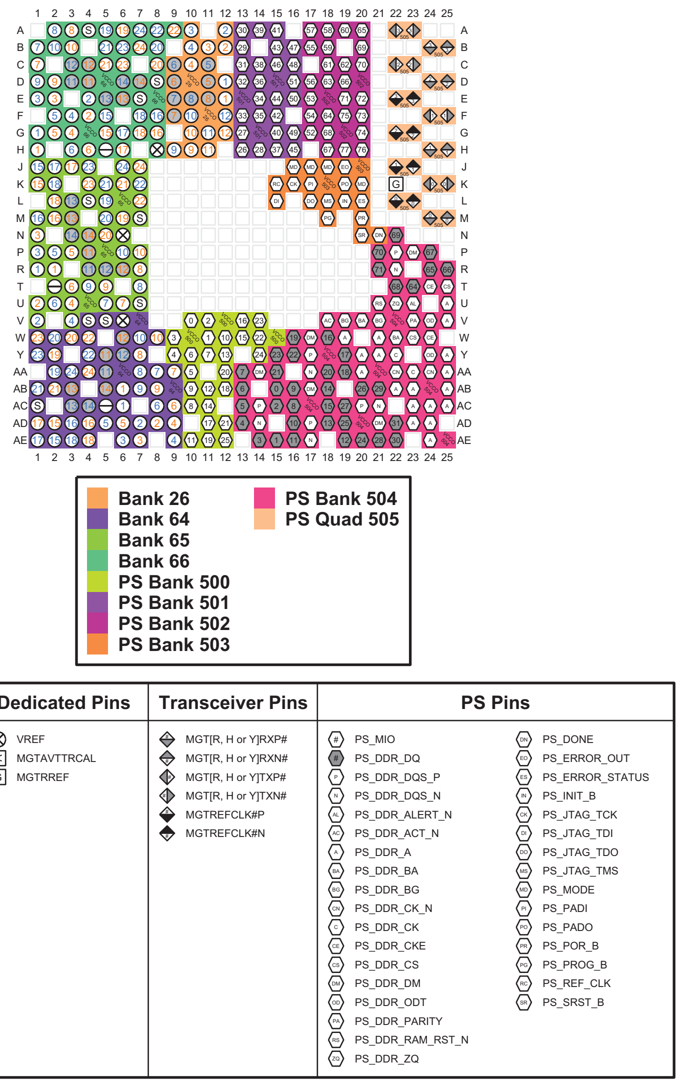


Figure 4-3: **SFVA625 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG I/O Bank Diagram**

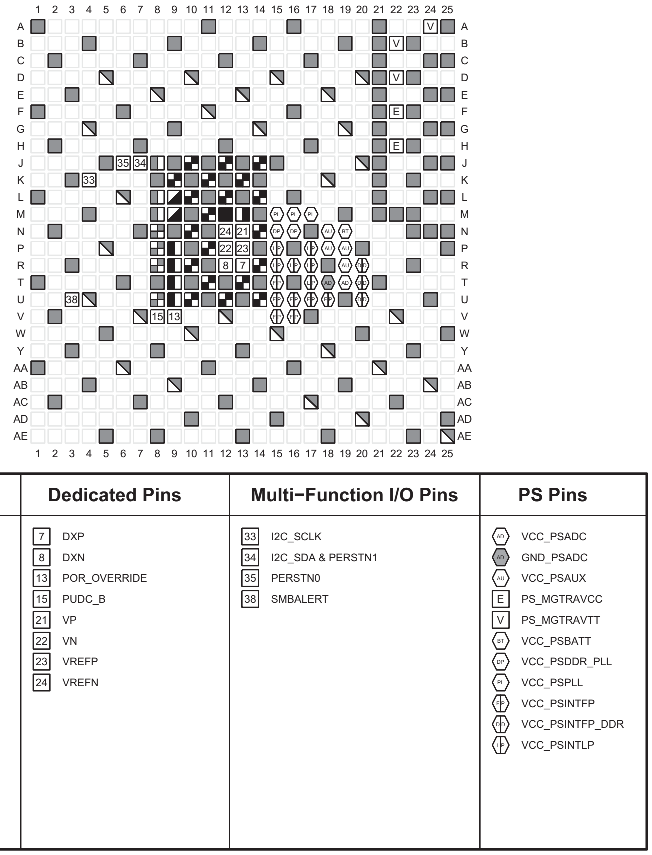


Figure 4-4: **SFVA625 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG Power, Dedicated, and Multi-function Pin Diagram**

SFVC784 Package–XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG

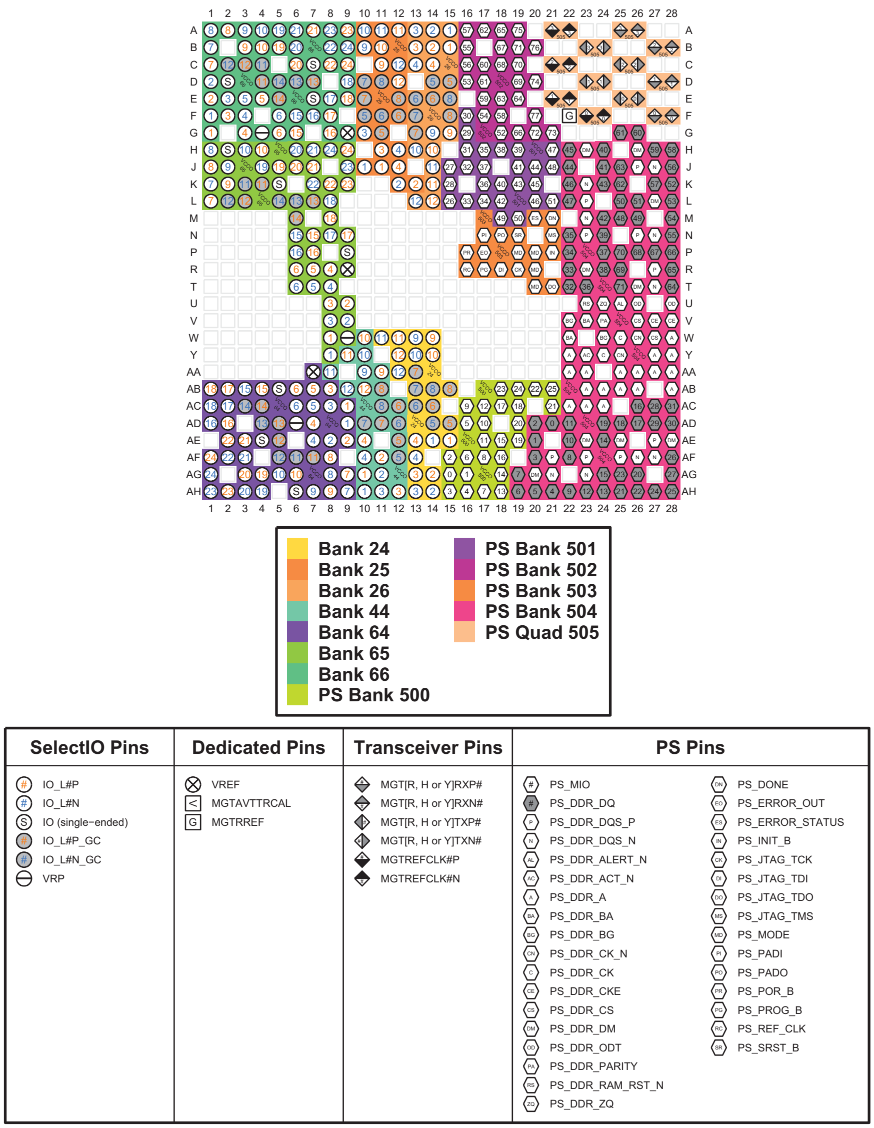
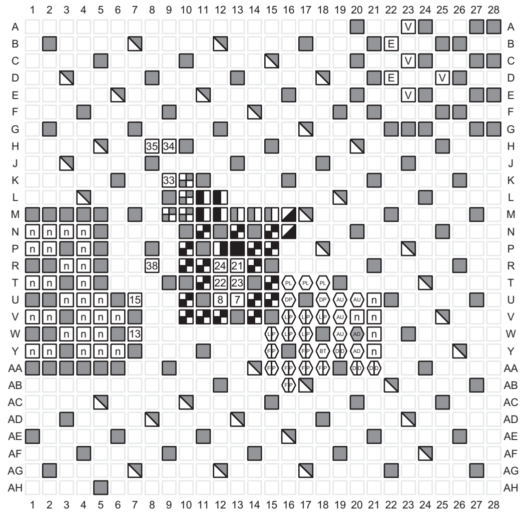


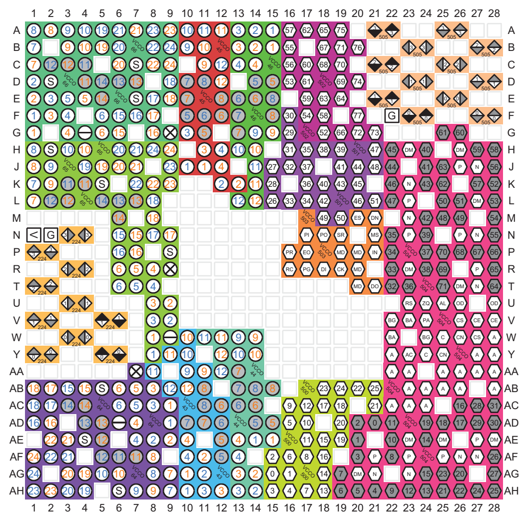
Figure 4-5: **SFVC784 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi−Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-6: **SFVC784 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG Power, Dedicated, and Multi-function Pin Diagram**

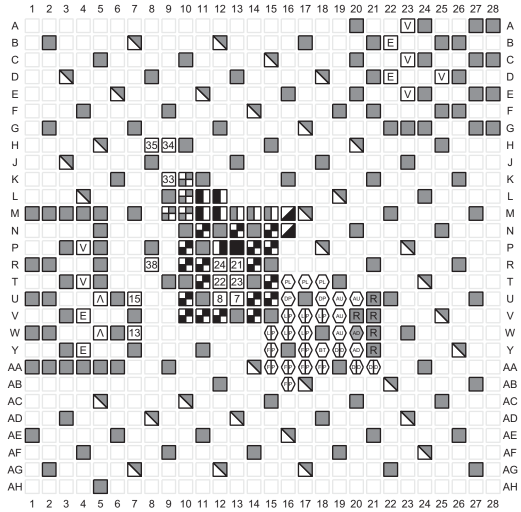
SFVC784 Package–XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG



- Bank 43
- Bank 44
- Bank 45
- Bank 46
- Bank 64
- Bank 65
- Bank 66
- Quad 224
- PS Bank 500
- PS Bank 501
- PS Bank 502
- PS Bank 503
- PS Bank 504
- PS Quad 505

SelectIO Pins	Dedicated Pins	Transceiver Pins	PS Pins	
IO_L#P	VREF	MGT[R, H or Y]RXP#	PS_MIO	PS_DONE
IO_L#N	MGTAVTTRCAL	MGT[R, H or Y]RXN#	PS_DDR_DQ	PS_ERROR_OUT
IO (single-ended)	MGTRREF	MGT[R, H or Y]TXP#	PS_DDR_DQS_P	PS_ERROR_STATUS
IO_L#P_GC		MGT[R, H or Y]TXN#	PS_DDR_DQS_N	PS_INIT_B
IO_L#N_GC		MGTREFCLK#P	PS_DDR_ALERT_N	PS_JTAG_TCK
VRP		MGTREFCLK#N	PS_DDR_ACT_N	PS_JTAG_TDI
			PS_DDR_A	PS_JTAG_TDO
			PS_DDR_BA	PS_JTAG_TMS
			PS_DDR_BG	PS_MODE
			PS_DDR_CK_N	PS_PADI
			PS_DDR_CK	PS_PADO
			PS_DDR_CKE	PS_POR_B
			PS_DDR_CS	PS_PROG_B
			PS_DDR_DM	PS_REF_CLK
			PS_DDR_ODT	PS_SRST_B
			PS_DDR_PARITY	
			PS_DDR_RAM_RST_N	
			PS_DDR_ZQ	

Figure 4-7: **SFVC784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi−Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-8: **SFVC784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG Power, Dedicated, and Multi-function Pin Diagram**

SFVC784 Package–XCZU4EV and XCZU5EV

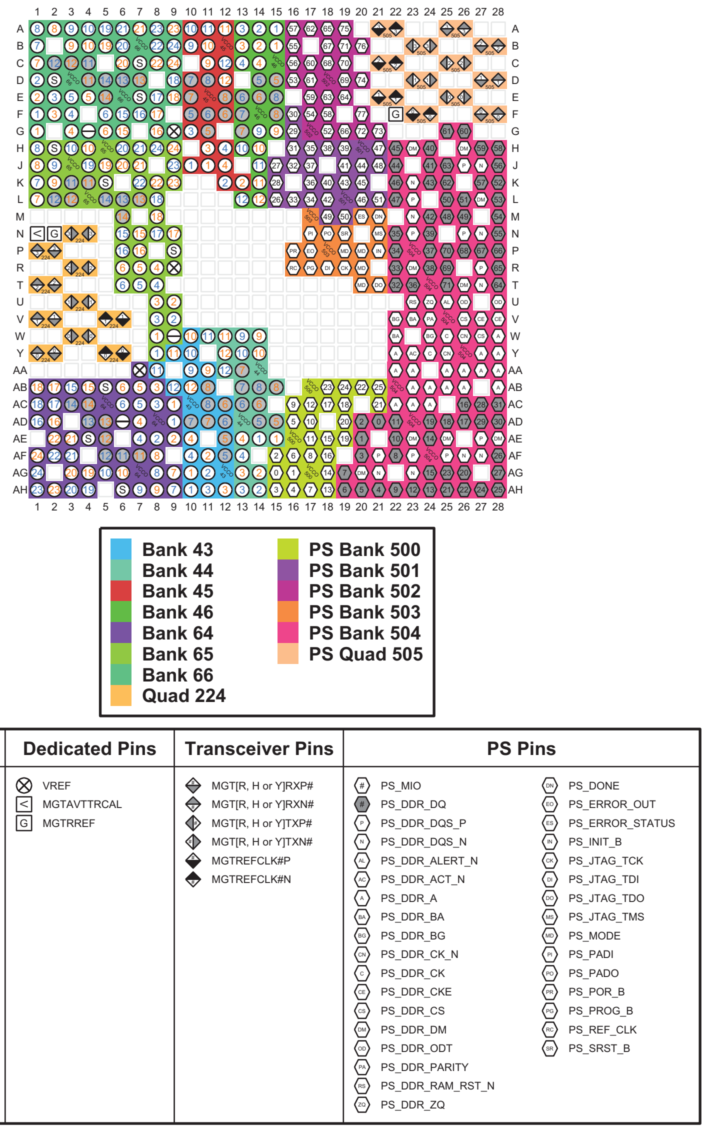
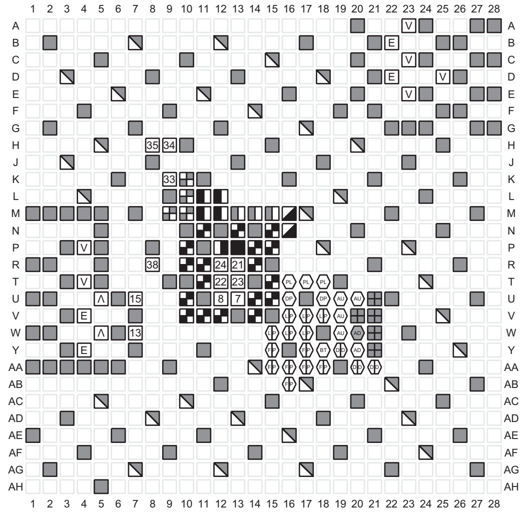


Figure 4-9: **SFVC784 Package—XCZU4EV and XCZU5EV I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-10: **SFVC784 Package—XCZU4EV and XCZU5EV Power, Dedicated, and Multi-function Pin Diagram**

FBVB900 Package–XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG

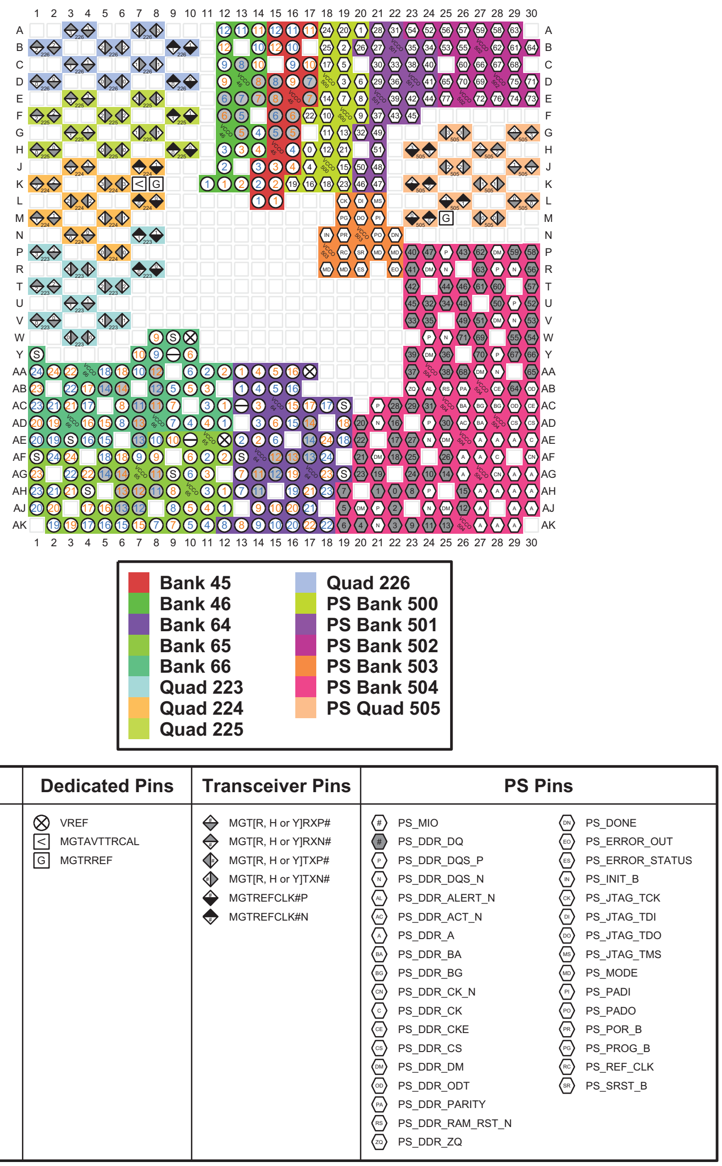
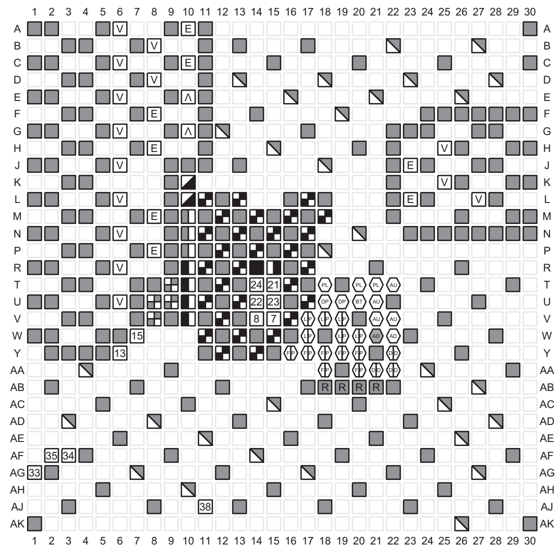


Figure 4-11: **FBVB900 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-12: **FBVB900 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG Power, Dedicated, and Multi-function Pin Diagram**

FBVB900 Package–XCZU4EV and XCZU5EV

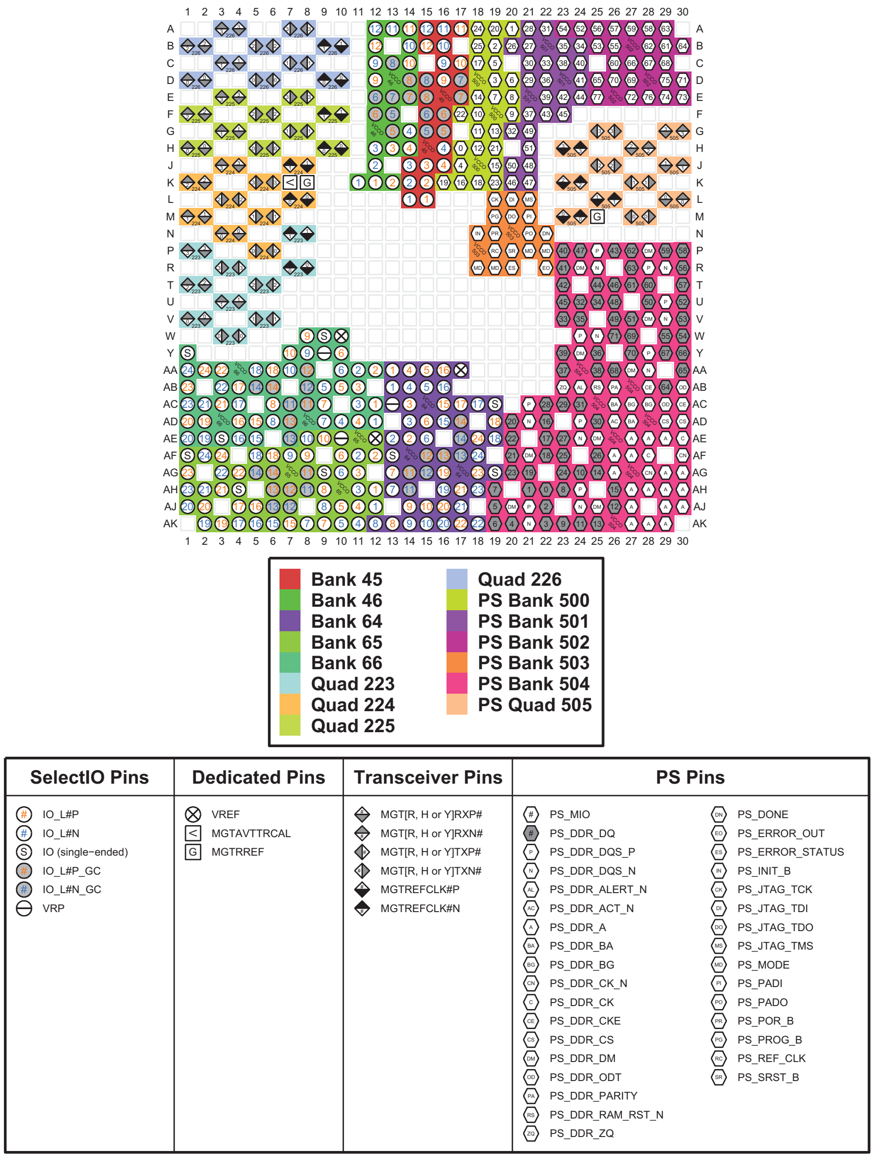
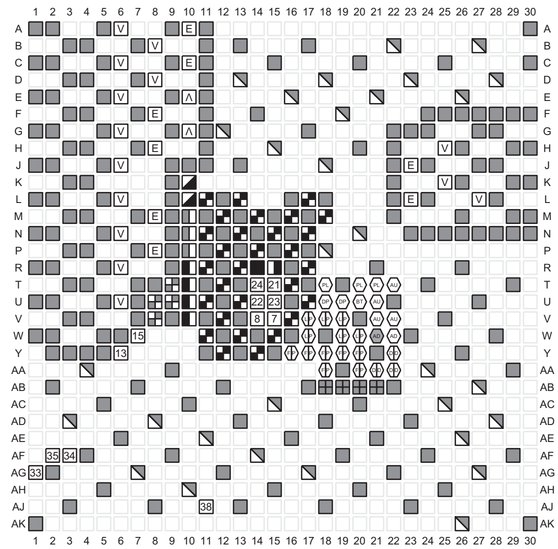


Figure 4-13: **FBVB900 Package—XCZU4EV and XCZU5EV I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi–Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-14: **FBVB900 Package—XCZU4EV and XCZU5EV Power, Dedicated, and Multi-function Pin Diagram**

FBVB900 Package–XCZU7CG and XCZU7EG

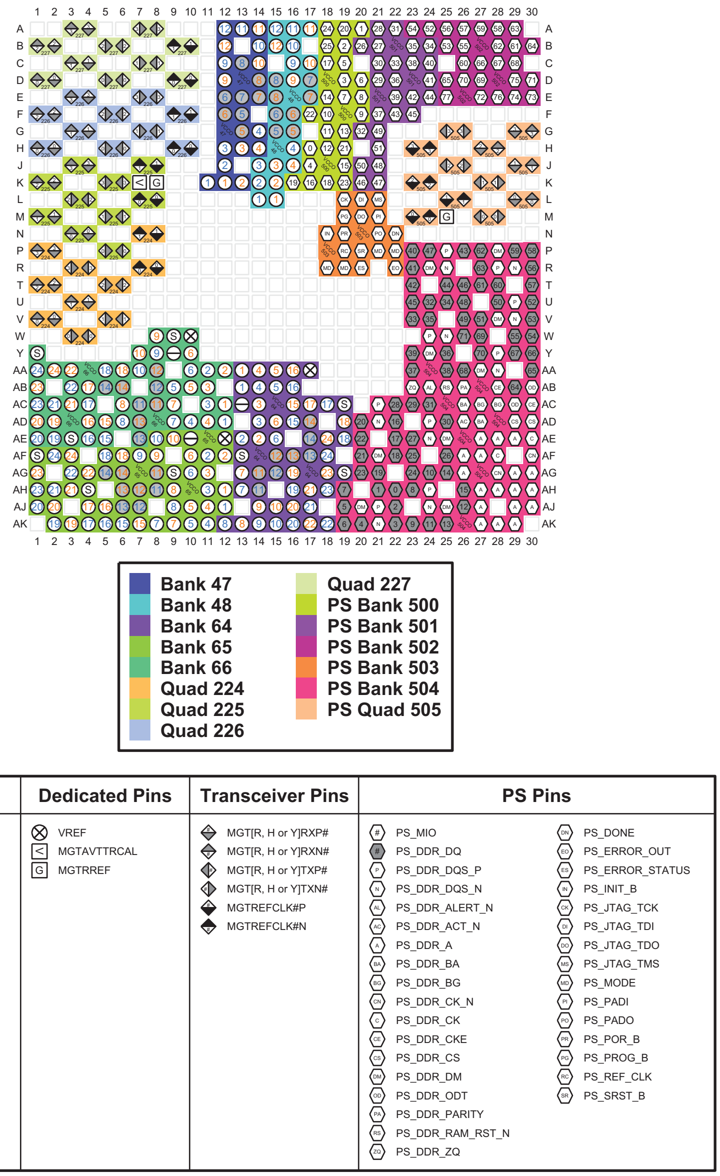
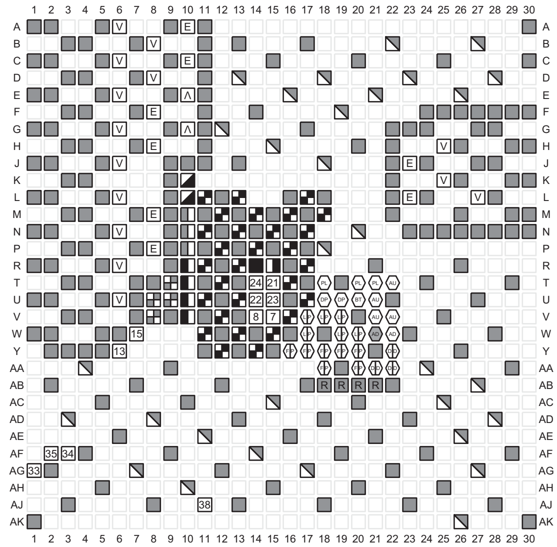


Figure 4-15: **FBVB900 Package—XCZU7CG and XCZU7EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi−Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-16: **FBVB900 Package—XCZU7CG and XCZU7EG Power, Dedicated, and Multi-function Pin Diagram**

FBVB900 Package–XCZU7EV

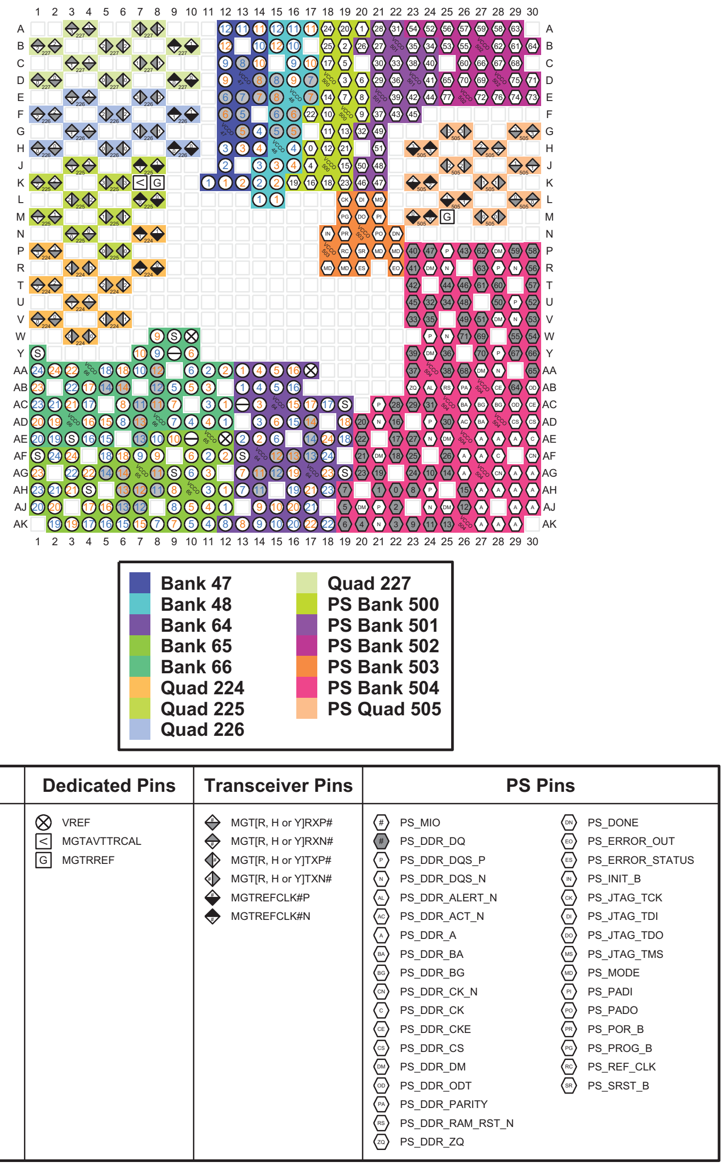
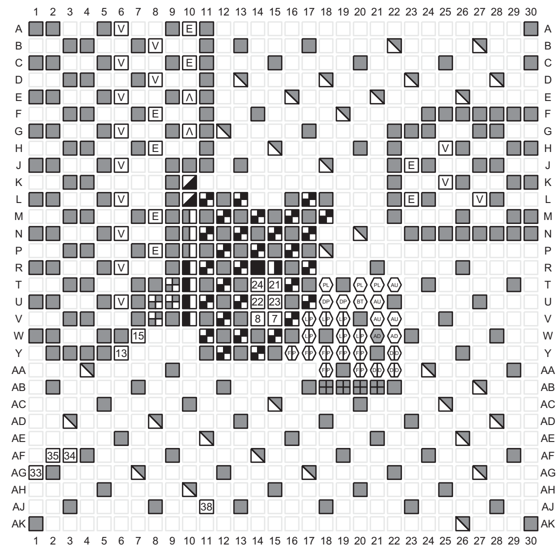


Figure 4-17: **FBVB900 Package—XCZU7EV I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi−Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-18: **FBVB900 Package—XCZU7EV**
Power, Dedicated, and Multi-function Pin Diagram

FFVC900 Package–XCZU6EG, XCZU9EG, and XCZU15EG

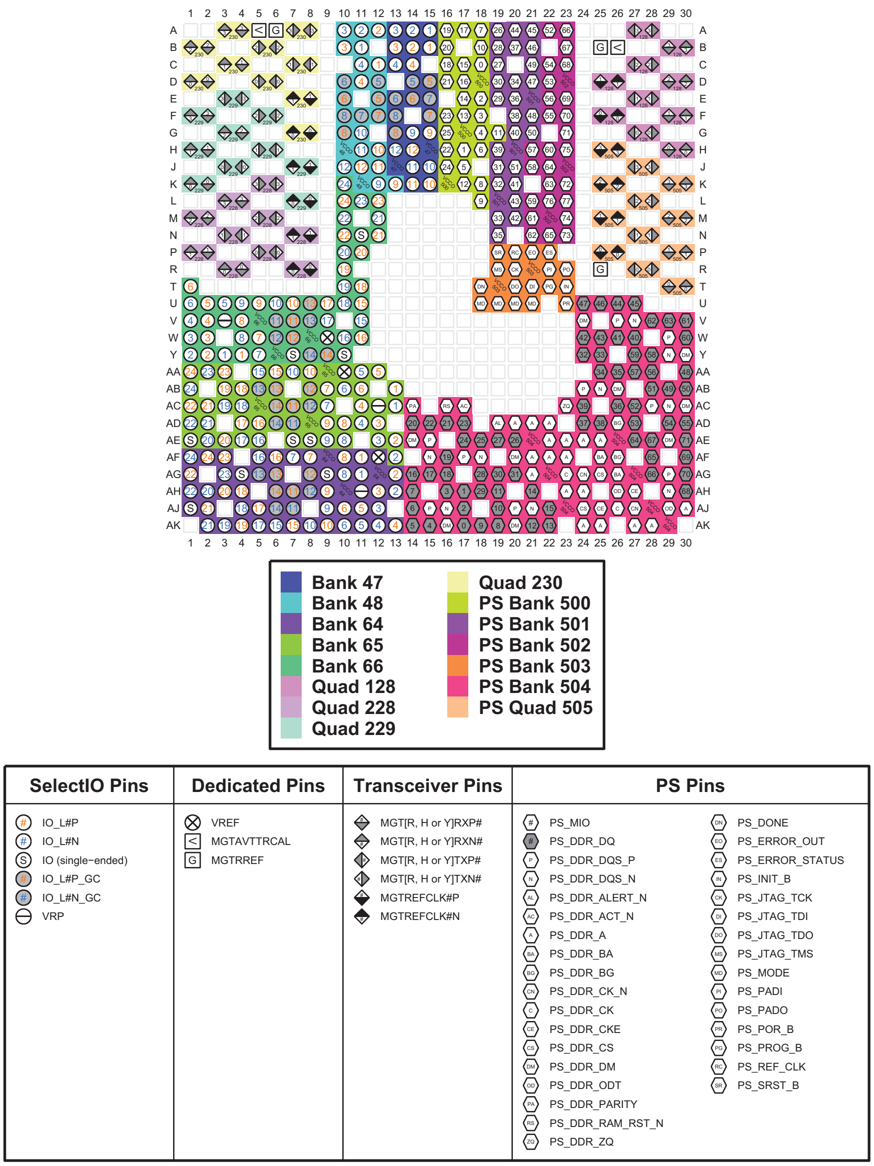
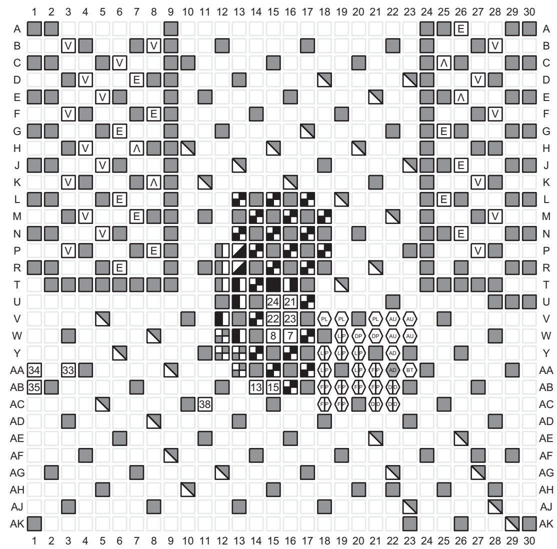


Figure 4-19: **FFVC900 Package—XCZU6EG, XCZU9EG, and XCZU15EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi−Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-20: **FFVC900 Package—XCZU6EG, XCZU9EG, and XCZU15EG Power, Dedicated, and Multi-function Pin Diagram**

FFVB1156 Package–XCZU6EG, XCZU9EG, and XCZU15EG

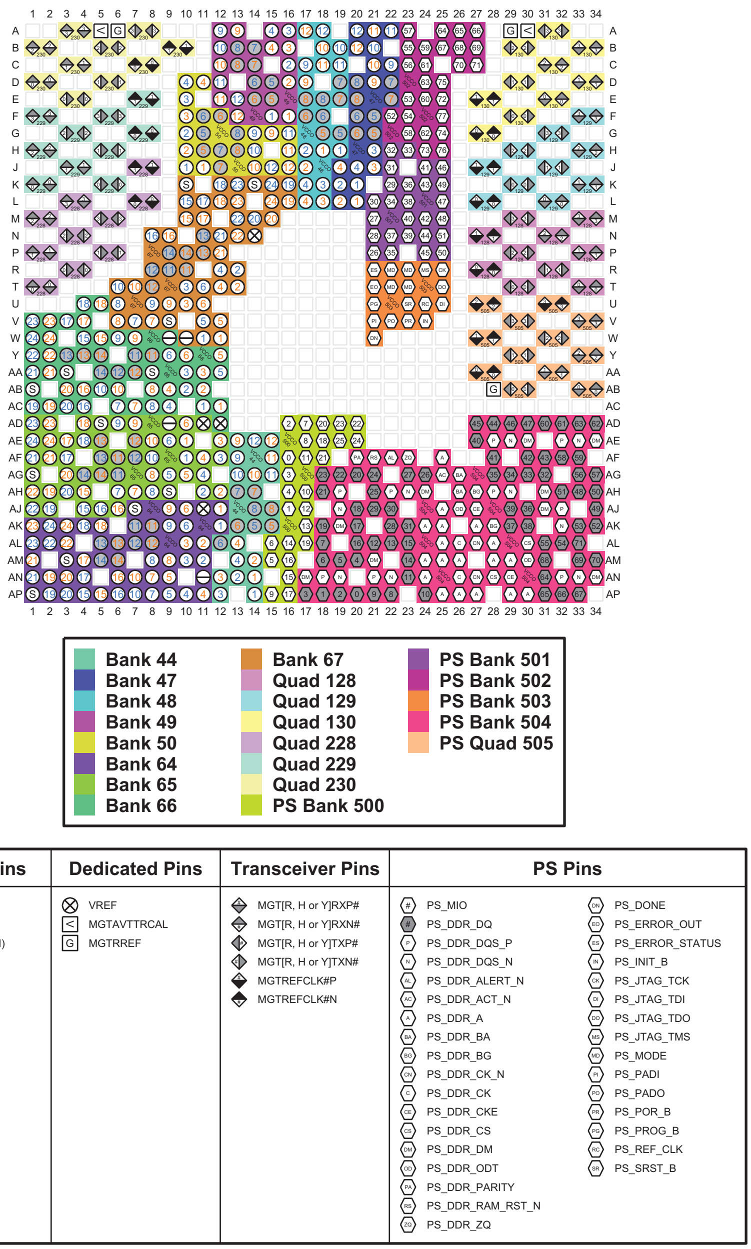


Figure 4-21: **FFVB1156 Package—XCZU6EG, XCZU9EG, and XCZU15EG I/O Bank Diagram**

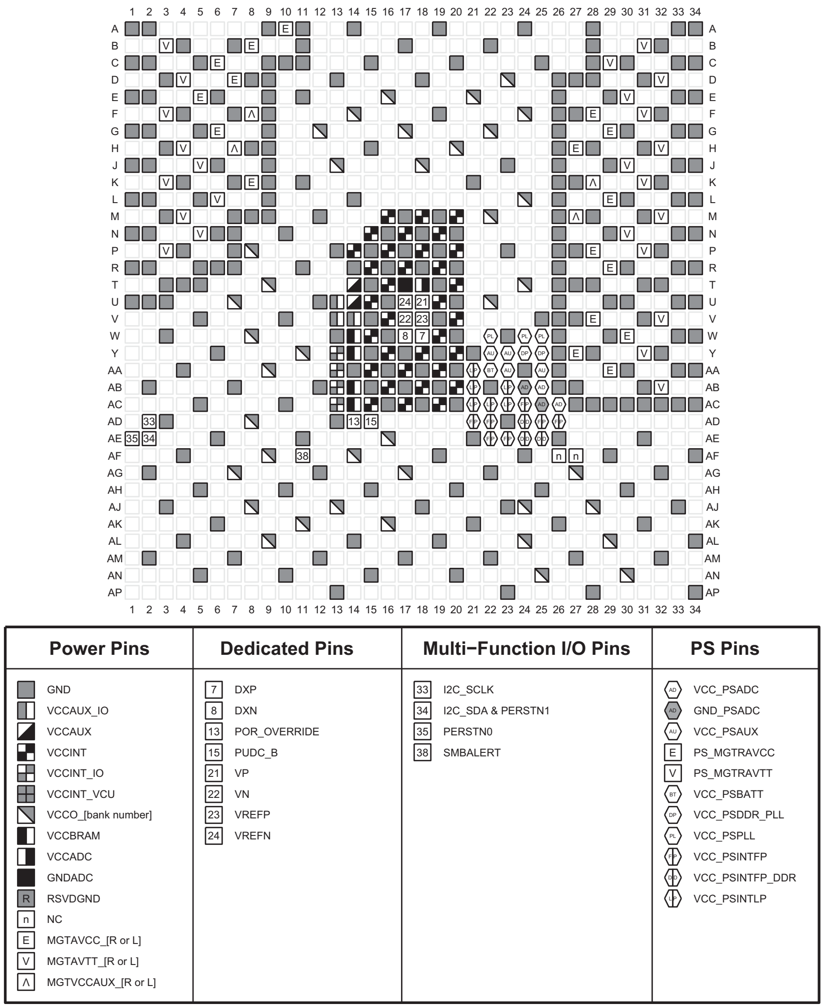


Figure 4-22: **FFVB1156 Package—XCZU6EG, XCZU9EG, and XCZU15EG Power, Dedicated, and Multi-function Pin Diagram**

FFVC1156 Package–XCZU7CG and XCZU7EG

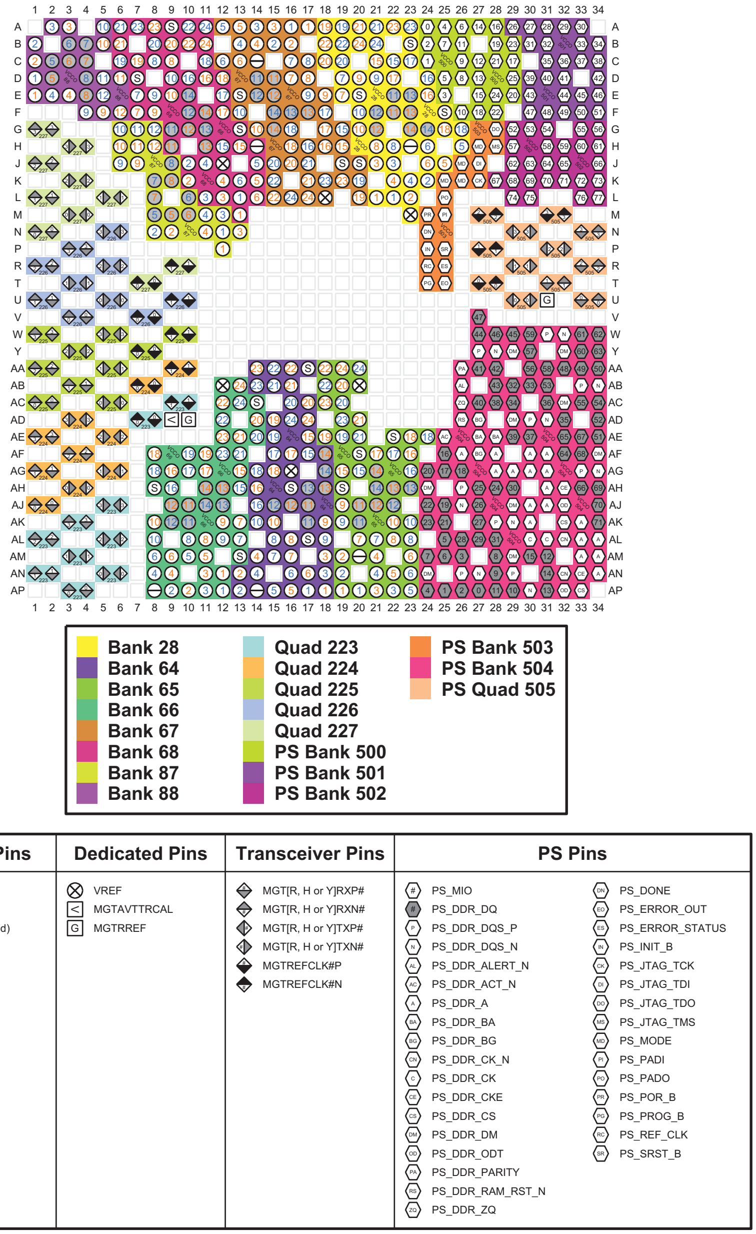
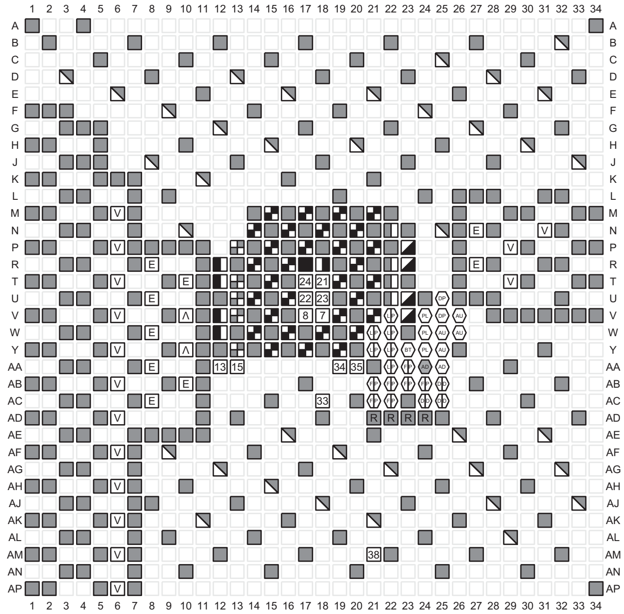


Figure 4-23: **FFVC1156 Package—XCZU7CG and XCZU7EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-24: **FFVC1156 Package—XCZU7CG and XCZU7EG Power, Dedicated, and Multi-function Pin Diagram**

FFVC1156 Package–XCZU7EV

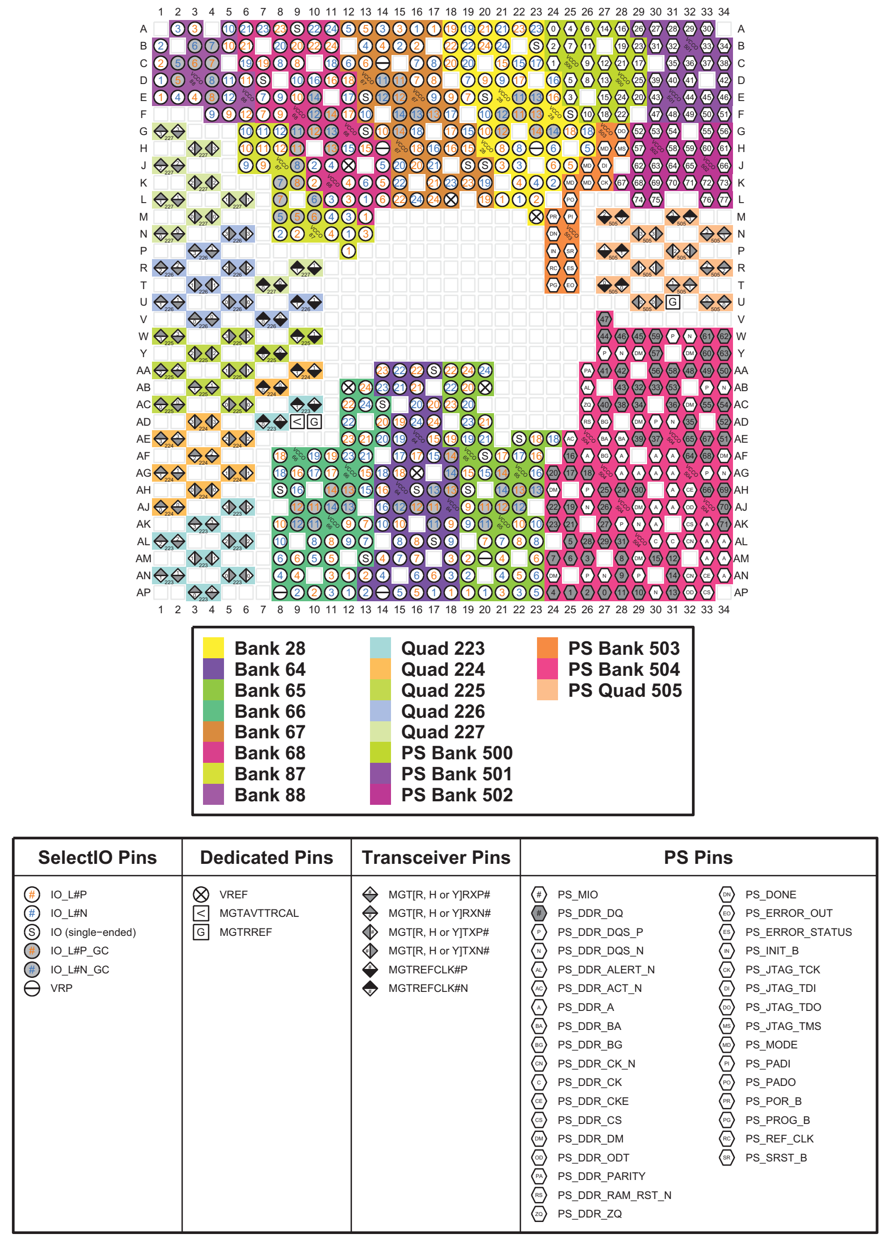
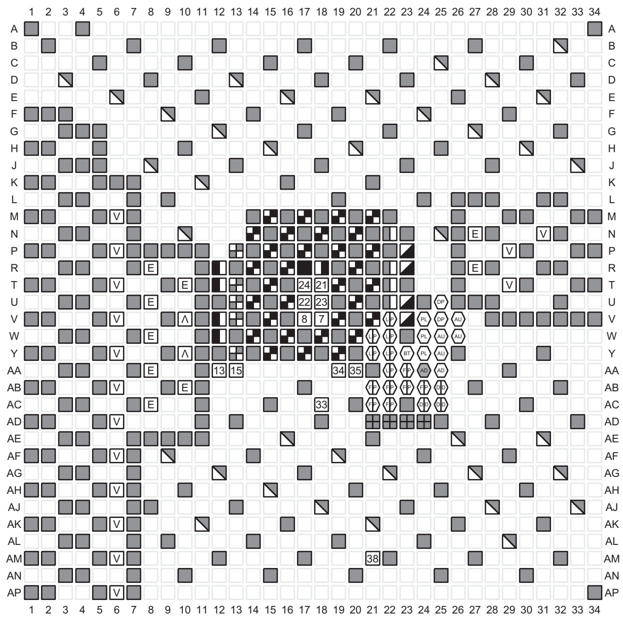


Figure 4-25: **FFVC1156 Package—XCZU7EV I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi–Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-26: **FFVC1156 Package—XCZU7EV Power, Dedicated, and Multi-function Pin Diagram**

FFVC1156 Package–XCZU11EG

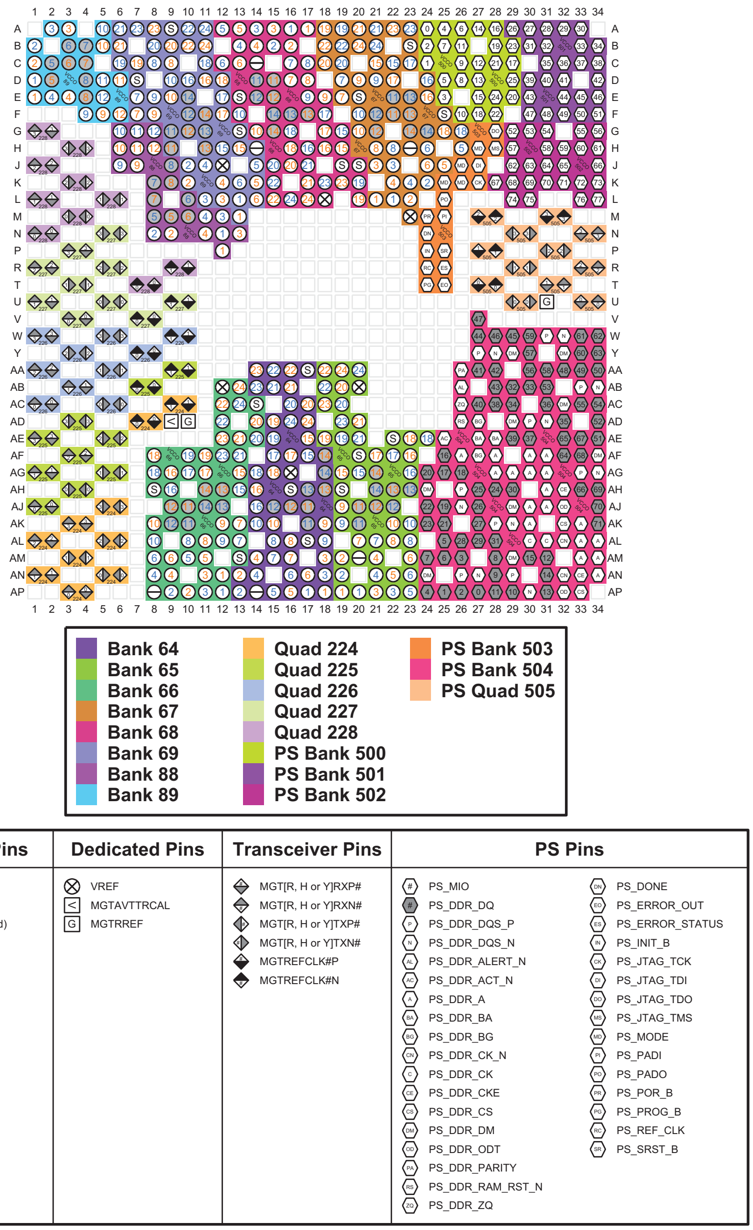
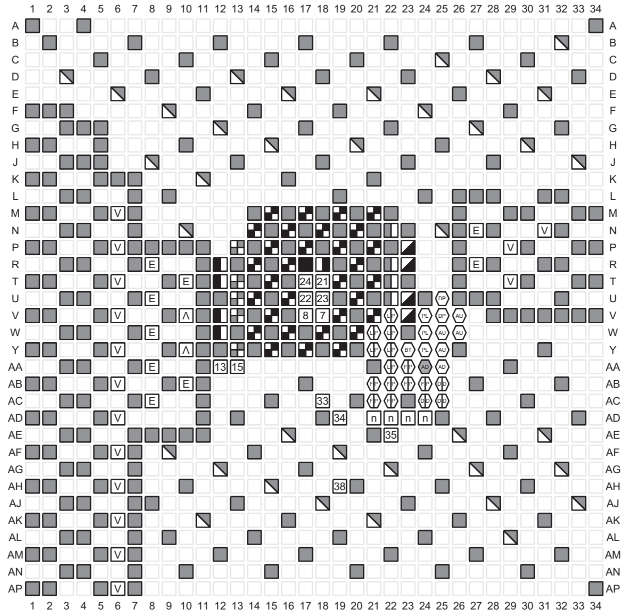


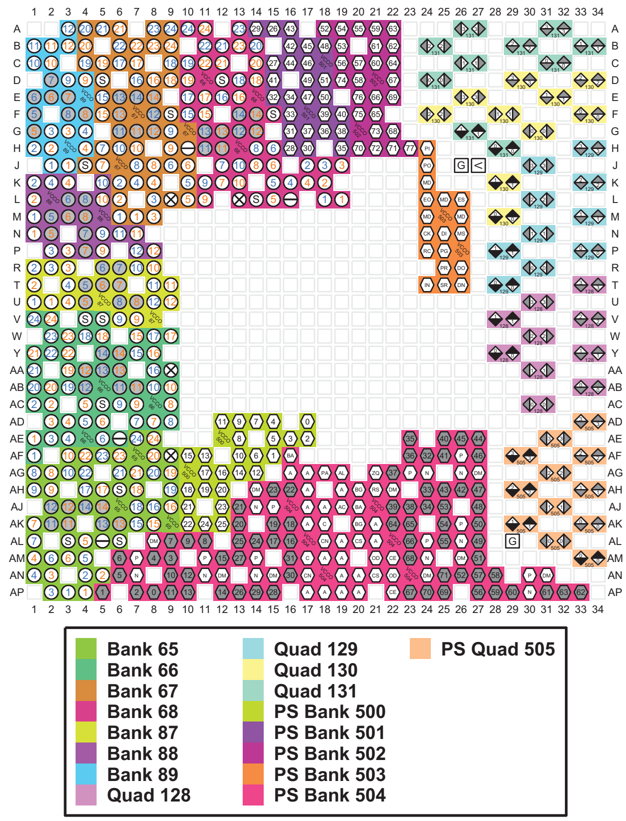
Figure 4-27: **FFVC1156 Package—XCZU11EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-28: **FFVC1156 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram**

FFVD1156 Package–XCZU21DR



SelectIO Pins	Dedicated Pins	Transceiver Pins	PS Pins	
IO_L#P	VREF	MGT[R, H or Y]RXP#	PS_MIO	PS_DONE
IO_L#N	MGTAVTTRCAL	MGT[R, H or Y]RXN#	PS_DDR_DQ	PS_ERROR_OUT
IO (single-ended)	MGTRREF	MGT[R, H or Y]TXP#	PS_DDR_DQS_P	PS_ERROR_STATUS
IO_L#P_GC		MGT[R, H or Y]TXN#	PS_DDR_DQS_N	PS_INIT_B
IO_L#N_GC		MGTREFCLK#P	PS_DDR_ALERT_N	PS_JTAG_TCK
VRP		MGTREFCLK#N	PS_DDR_ACT_N	PS_JTAG_TDI
			PS_DDR_A	PS_JTAG_TDO
			PS_DDR_BA	PS_JTAG_TMS
			PS_DDR_BG	PS_MODE
			PS_DDR_CK_N	PS_PADI
			PS_DDR_CK	PS_PADO
			PS_DDR_CKE	PS_POR_B
			PS_DDR_CS	PS_PROG_B
			PS_DDR_DM	PS_REF_CLK
			PS_DDR_ODT	PS_SRST_B
			PS_DDR_PARITY	
			PS_DDR_RAM_RST_N	
			PS_DDR_ZQ	

Figure 4-29: **FFVD1156 Package—XCZU21DR I/O Bank Diagram**

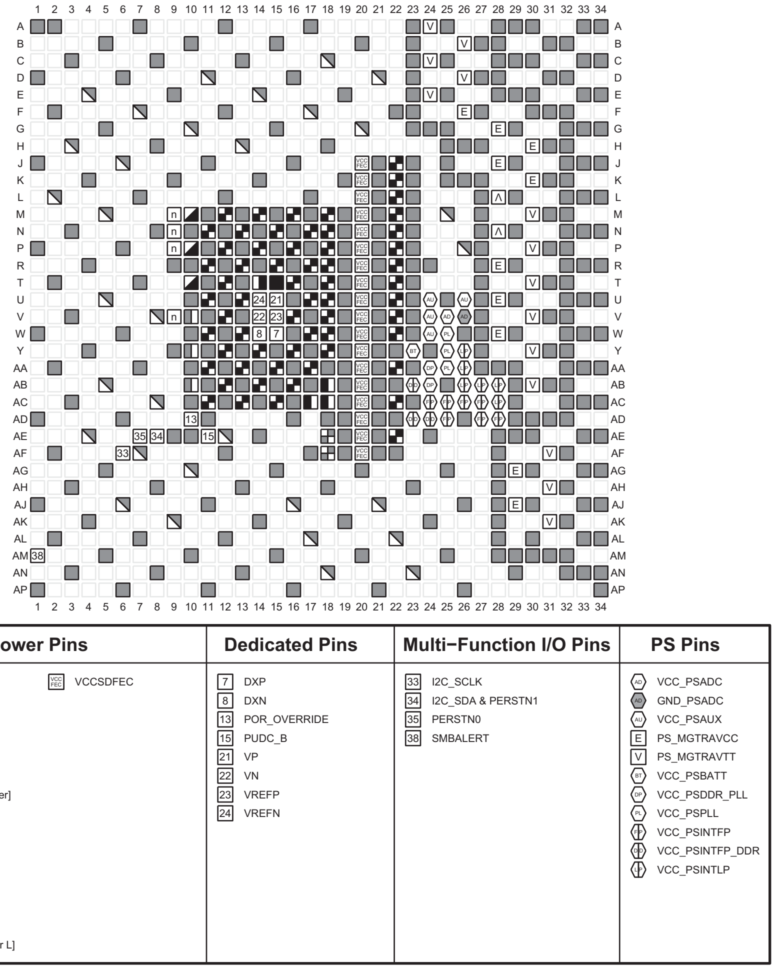


Figure 4-30: **FFVD1156 Package—XCZU21DR Power, Dedicated, and Multi-function Pin Diagram**

FFVE1156 and FSVE1156 Packages–XCZU25DR

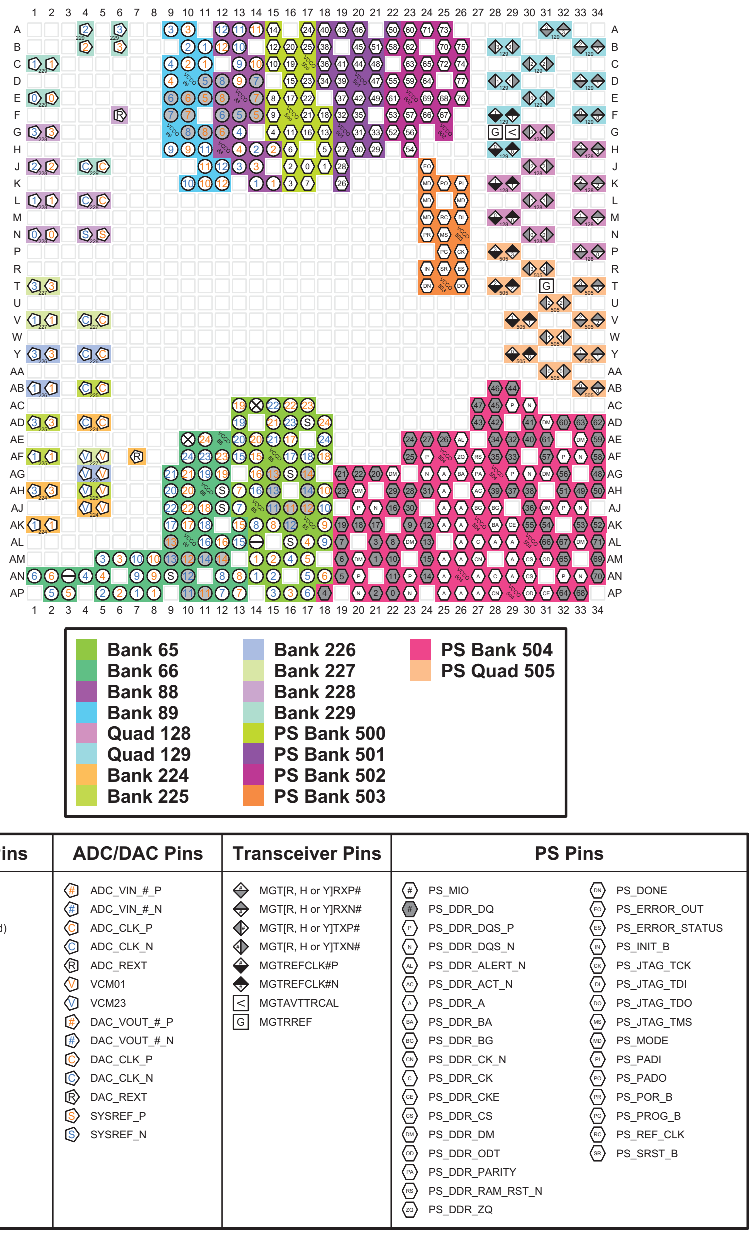


Figure 4-31: **FFVE1156 and FSVE1156 Packages—XCZU25DR I/O Bank Diagram**

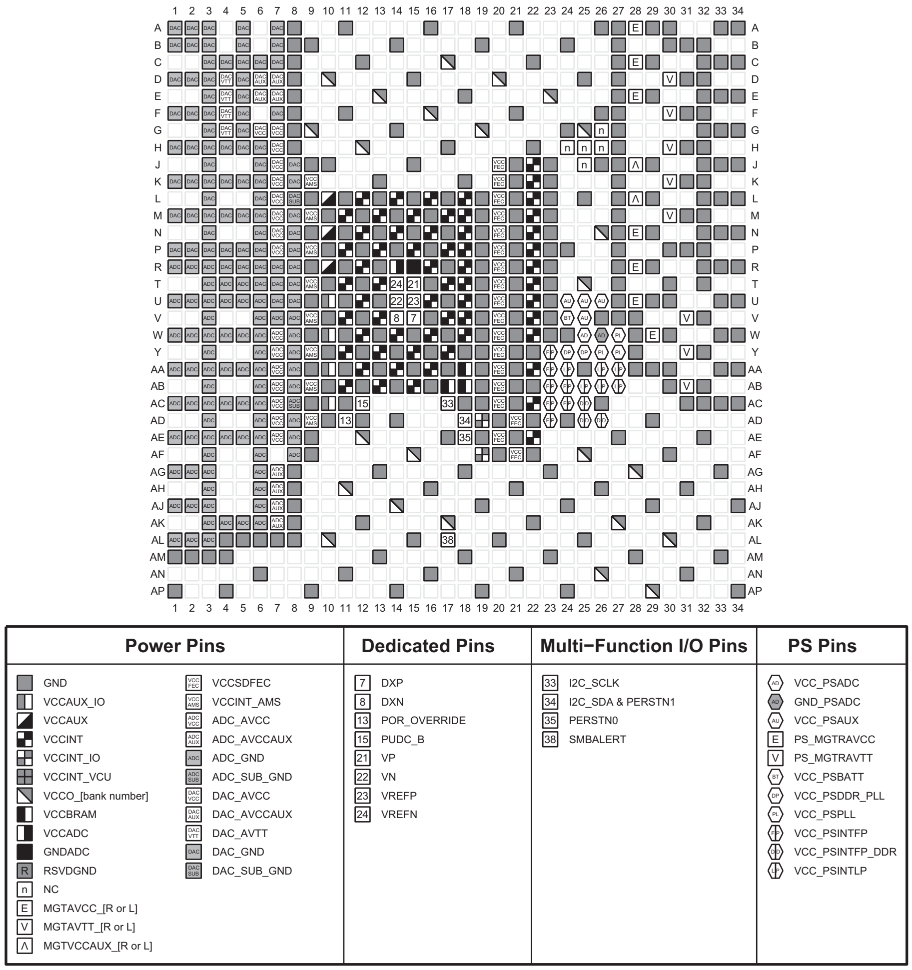
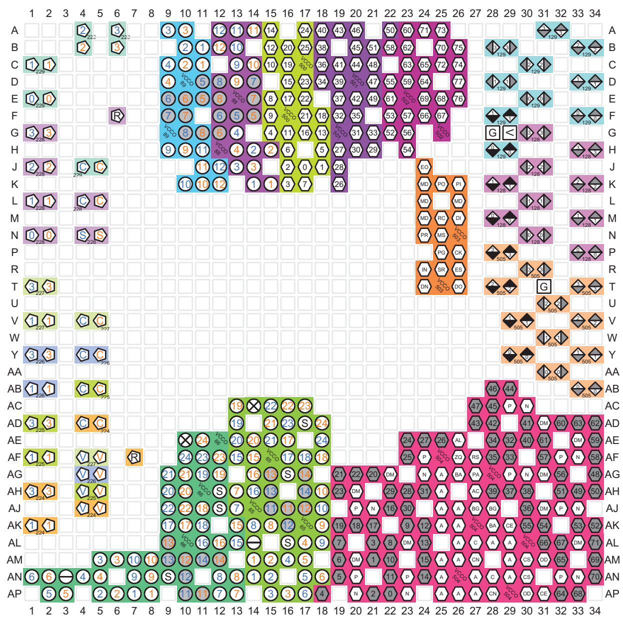


Figure 4-32: **FFVE1156 and FSVE1156 Packages—XCZU25DR Power, Dedicated, and Multi-function Pin Diagram**

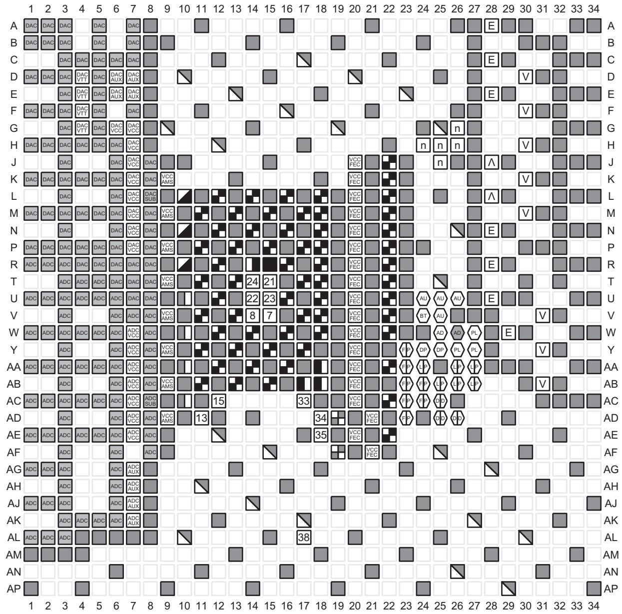
FFVE1156 and FSVE1156 Packages–XCZU27DR and XCZU28DR



- Bank 65
- Bank 66
- Bank 88
- Bank 89
- Quad 128
- Quad 129
- Bank 224
- Bank 225
- Bank 226
- Bank 227
- Bank 228
- Bank 229
- PS Bank 500
- PS Bank 501
- PS Bank 502
- PS Bank 503
- PS Bank 504
- PS Quad 505

SelectIO Pins	ADC/DAC Pins	Transceiver Pins	PS Pins	
IO_L#P	ADC_VIN_#_P	MGT[R, H or Y]RXP#	PS_MIO	PS_DONE
IO_L#N	ADC_VIN_#_N	MGT[R, H or Y]RXN#	PS_DDR_DQ	PS_ERROR_OUT
IO (single-ended)	ADC_CLK_P	MGT[R, H or Y]TXP#	PS_DDR_DQS_P	PS_ERROR_STATUS
IO_L#P_GC	ADC_CLK_N	MGT[R, H or Y]TXN#	PS_DDR_DQS_N	PS_INIT_B
IO_L#N_GC	ADC_REXT	MGTREFCLK#P	PS_DDR_ALERT_N	PS_JTAG_TCK
VRP	VCM01	MGTREFCLK#N	PS_DDR_ACT_N	PS_JTAG_TDI
VREF	VCM23	MGTAVTTRCAL	PS_DDR_A	PS_JTAG_TDO
	DAC_VOUT_#_P	MGTRREF	PS_DDR_BA	PS_JTAG_TMS
	DAC_VOUT_#_N		PS_DDR_BG	PS_MODE
	DAC_CLK_P		PS_DDR_CK_N	PS_PADI
	DAC_CLK_N		PS_DDR_CK	PS_PADO
	DAC_REXT		PS_DDR_CKE	PS_POR_B
	SYSREF_P		PS_DDR_CS	PS_PROG_B
	SYSREF_N		PS_DDR_DM	PS_REF_CLK
			PS_DDR_ODT	PS_SRST_B
			PS_DDR_PARITY	
			PS_DDR_RAM_RST_N	
			PS_DDR_ZQ	

Figure 4-33: **FFVE1156 and FSVE1156 Packages—XCZU27DR and XCZU28DR I/O Bank Diagram**



Power Pins		Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	VCCSDFEC	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	VCCINT_AMS	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	ADC_AVCC	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	ADC_AVCCAUX	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	ADC_GND	21 VP		V PS_MGTRAVTT
VCCINT_VCU	ADC_SUB_GND	22 VN		VCC_PSBATT
VCCO_[bank number]	DAC_AVCC	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	DAC_AVCCAUX	24 VREFN		VCC_PSPLL
VCCADC	DAC_AVTT			VCC_PSINTFP
GNDADC	DAC_GND			VCC_PSINTFP_DDR
R RSVDGND	DAC_SUB_GND			VCC_PSINTLP
n NC				
E MGTAVCC_[R or L]				
V MGTAVTT_[R or L]				
Λ MGTVCCAUX_[R or L]				

Figure 4-34: **FFVE1156 and FSVE1156 Packages—XCZU27DR and XCZU28DR Power, Dedicated, and Multi-function Pin Diagram**

FFVB1517 Package–XCZU11EG

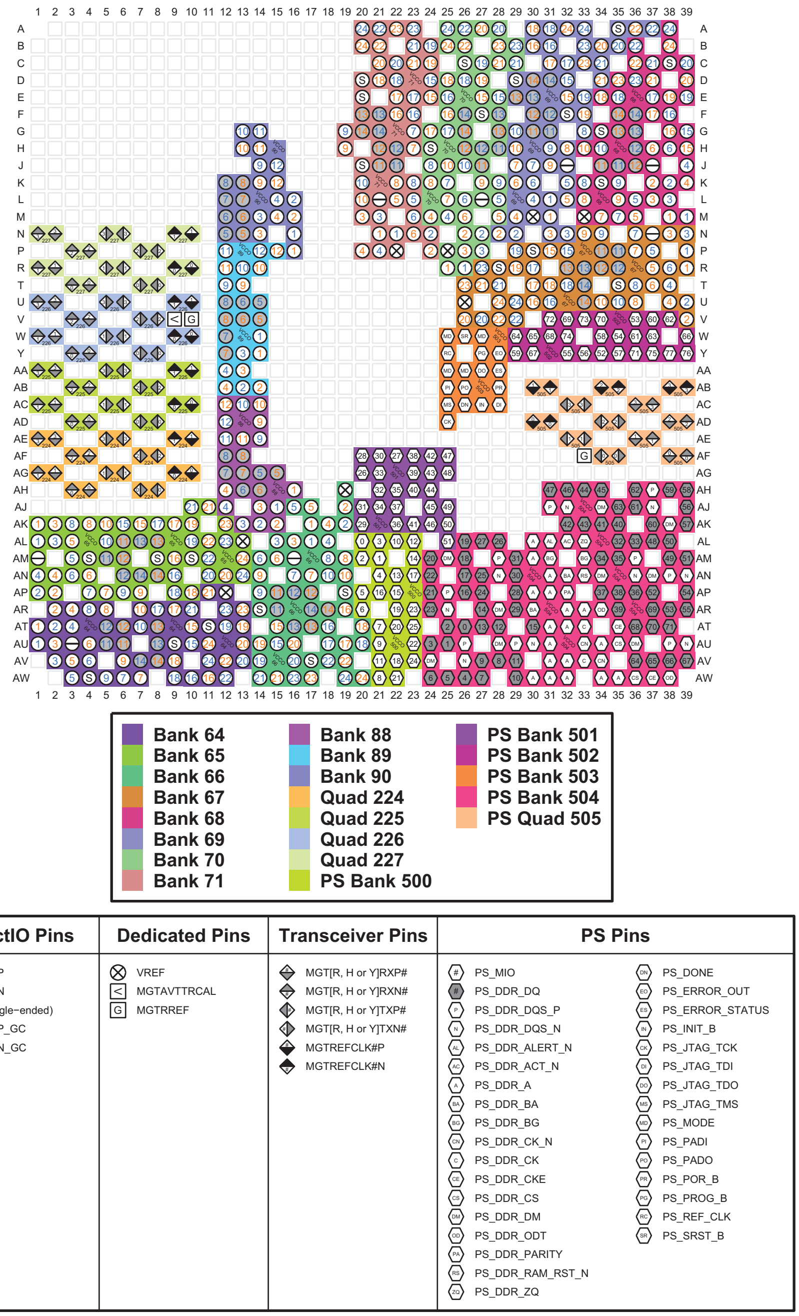
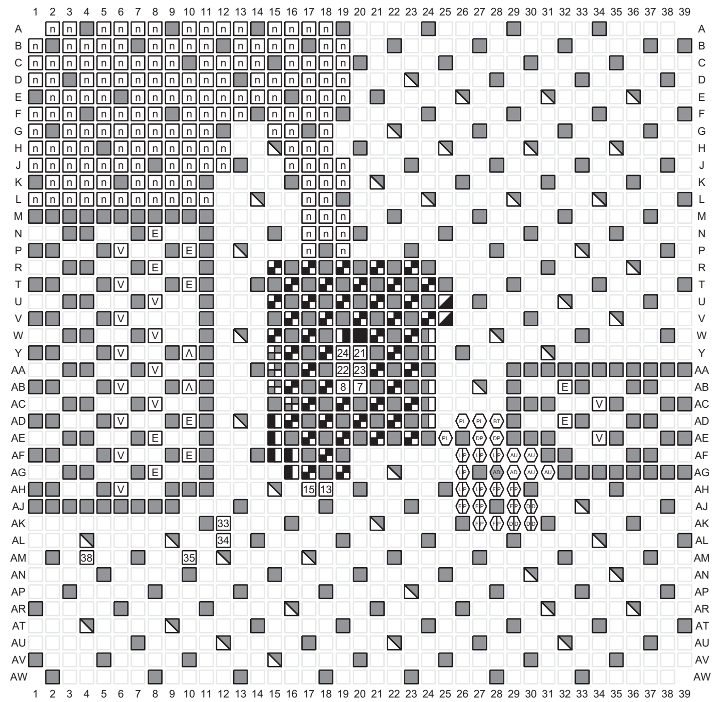


Figure 4-35: **FFVB1517 Package—XCZU11EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-36: **FFVB1517 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram**

FFVB1517 Package–XCZU17EG and XCZU19EG

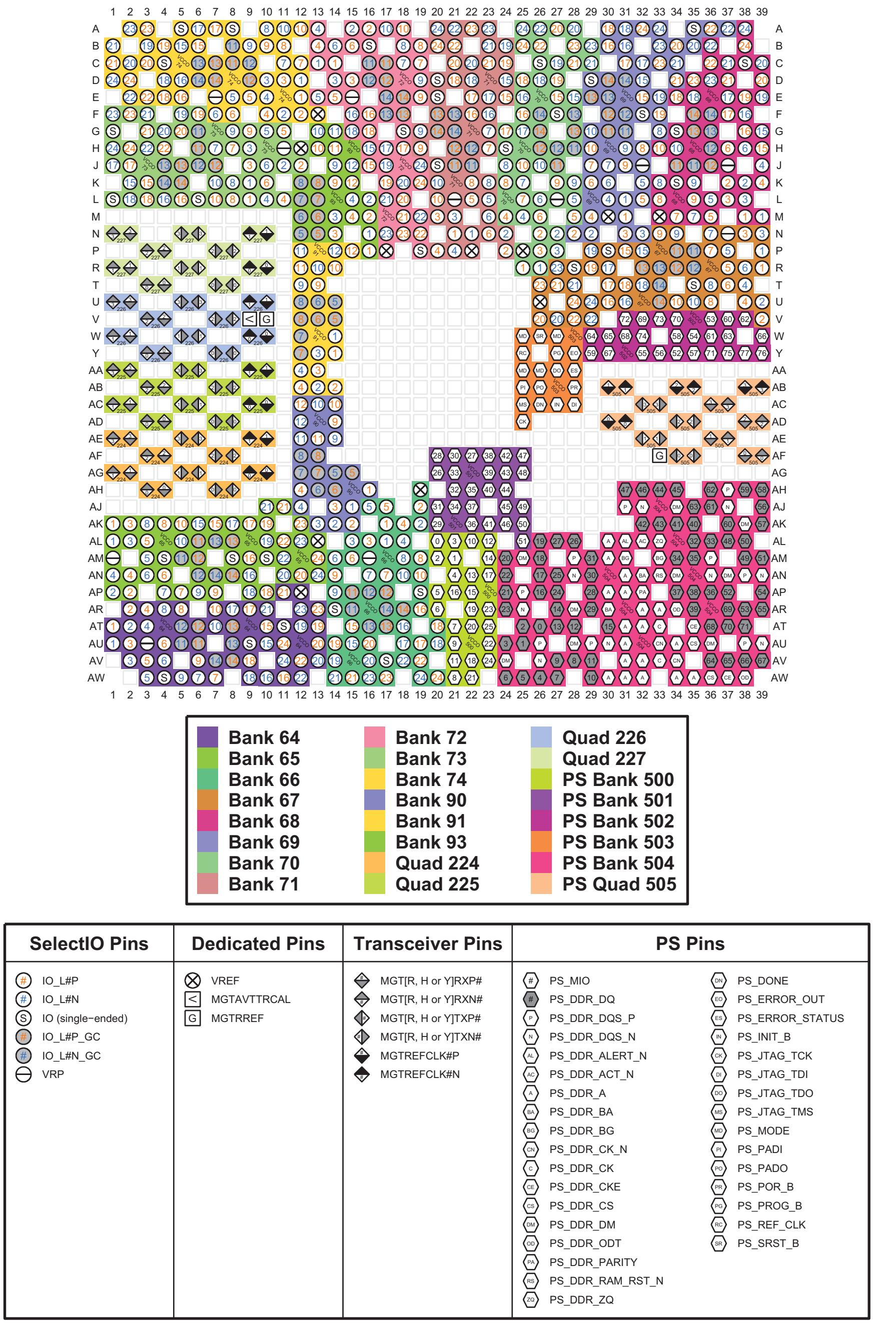
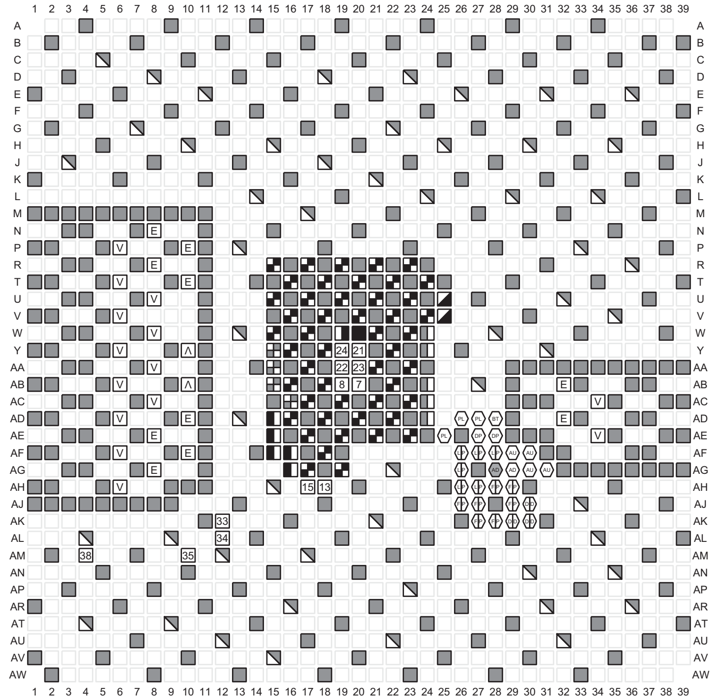


Figure 4-37: **FFVB1517 Package—XCZU17EG and XCZU19EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-38: **FFVB1517 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram**

FFVF1517 Package–XCZU7CG and XCZU7EG

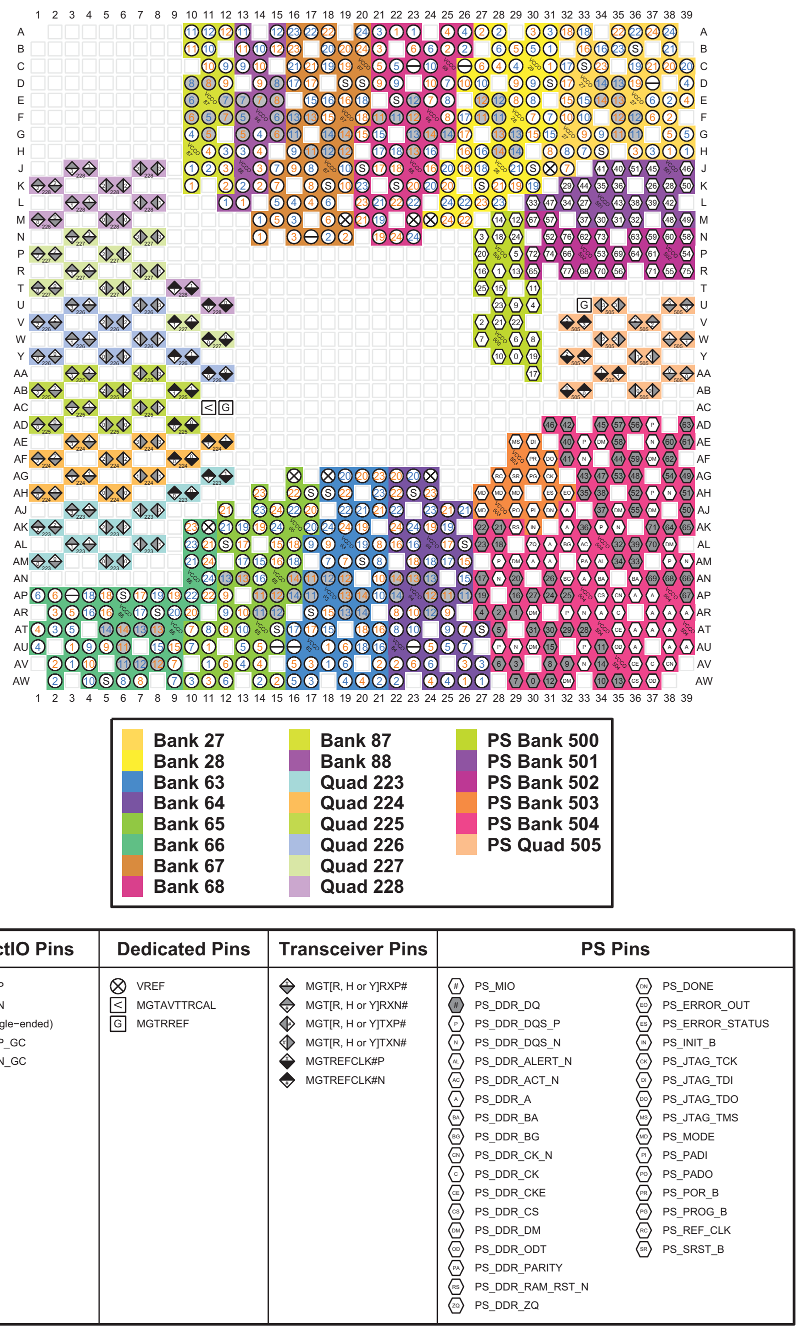
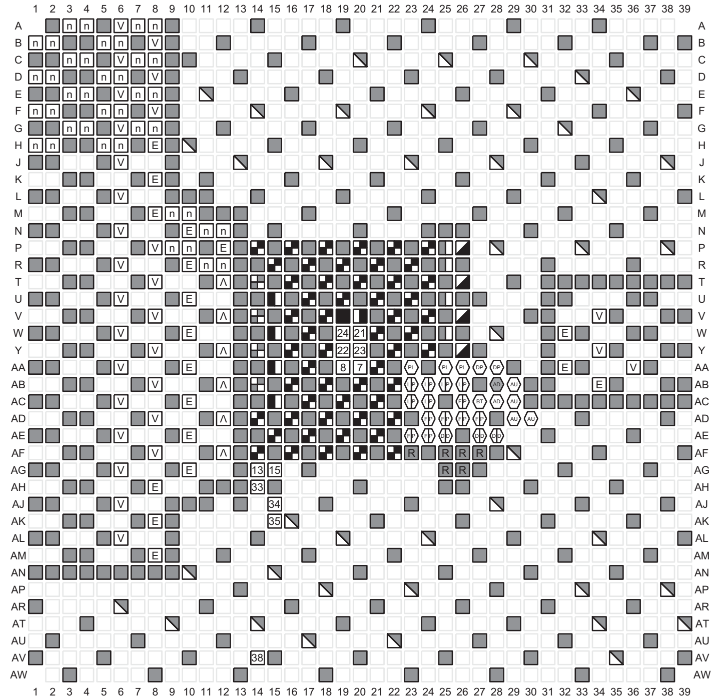


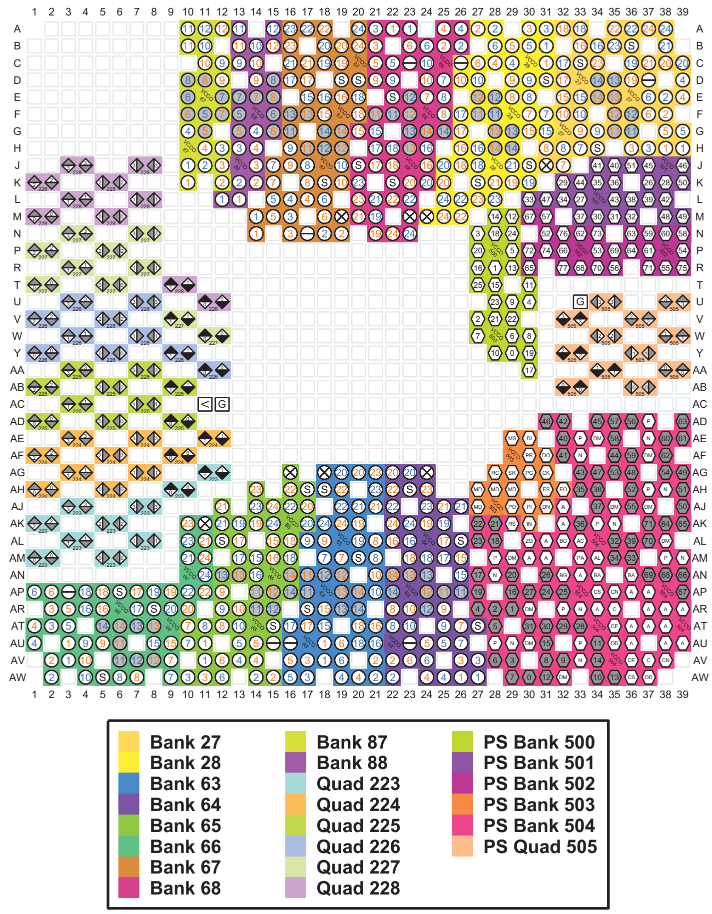
Figure 4-39: **FFVF1517 Package—XCZU7CG and XCZU7EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-40: **FFVF1517 Package—XCZU7CG and XCZU7EG Power, Dedicated, and Multi-function Pin Diagram**

FFVF1517 Package–XCZU7EV



SelectIO Pins	Dedicated Pins	Transceiver Pins	PS Pins	
IO_L#P	VREF	MGT[R, H or Y]RXP#	PS_MIO	PS_DONE
IO_L#N	MGTAVTTRCAL	MGT[R, H or Y]RXN#	PS_DDR_DQ	PS_ERROR_OUT
IO (single-ended)	MGTRREF	MGT[R, H or Y]TXP#	PS_DDR_DQS_P	PS_ERROR_STATUS
IO_L#P_GC		MGT[R, H or Y]TXN#	PS_DDR_DQS_N	PS_INIT_B
IO_L#N_GC		MGTREFCLK#P	PS_DDR_ALERT_N	PS_JTAG_TCK
VRP		MGTREFCLK#N	PS_DDR_ACT_N	PS_JTAG_TDI
			PS_DDR_A	PS_JTAG_TDO
			PS_DDR_BA	PS_JTAG_TMS
			PS_DDR_BG	PS_MODE
			PS_DDR_CK_N	PS_PADI
			PS_DDR_CK	PS_PADO
			PS_DDR_CKE	PS_POR_B
			PS_DDR_CS	PS_PROG_B
			PS_DDR_DM	PS_REF_CLK
			PS_DDR_ODT	PS_SRST_B
			PS_DDR_PARITY	
			PS_DDR_RAM_RST_N	
			PS_DDR_ZQ	

Figure 4-41: **FFVF1517 Package—XCZU7EV I/O Bank Diagram**

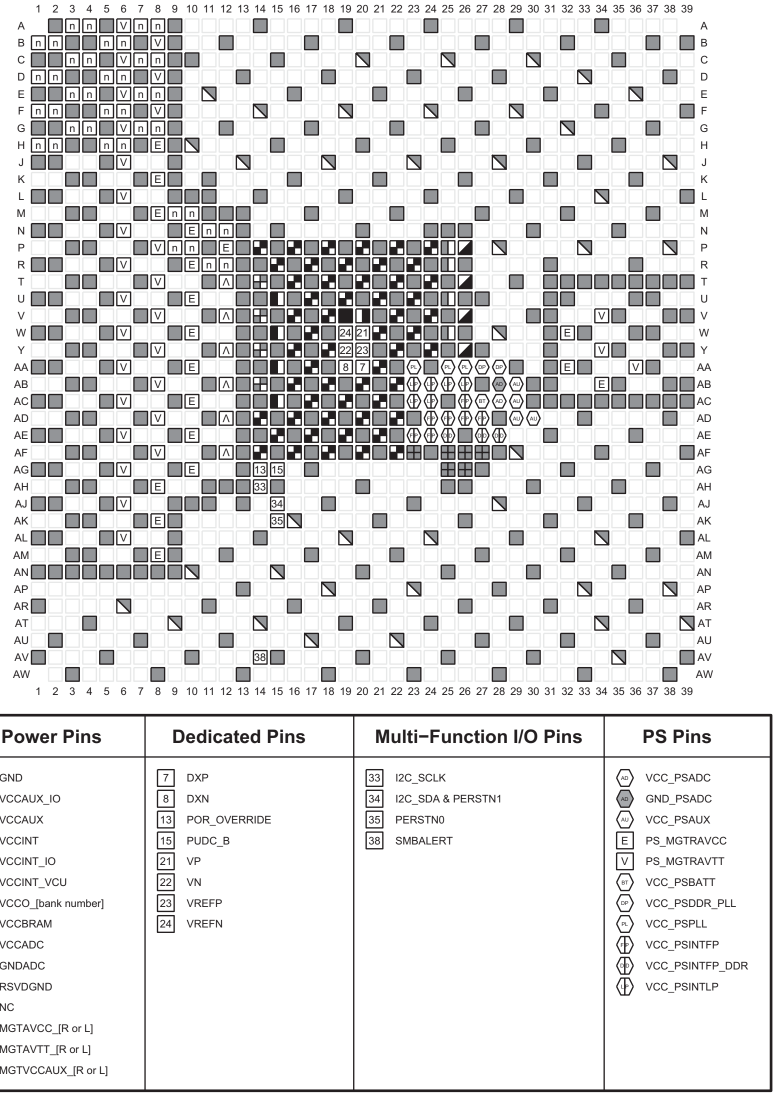


Figure 4-42: **FFVF1517 Package—XCZU7EV Power, Dedicated, and Multi-function Pin Diagram**

FFVF1517 Package–XCZU11EG

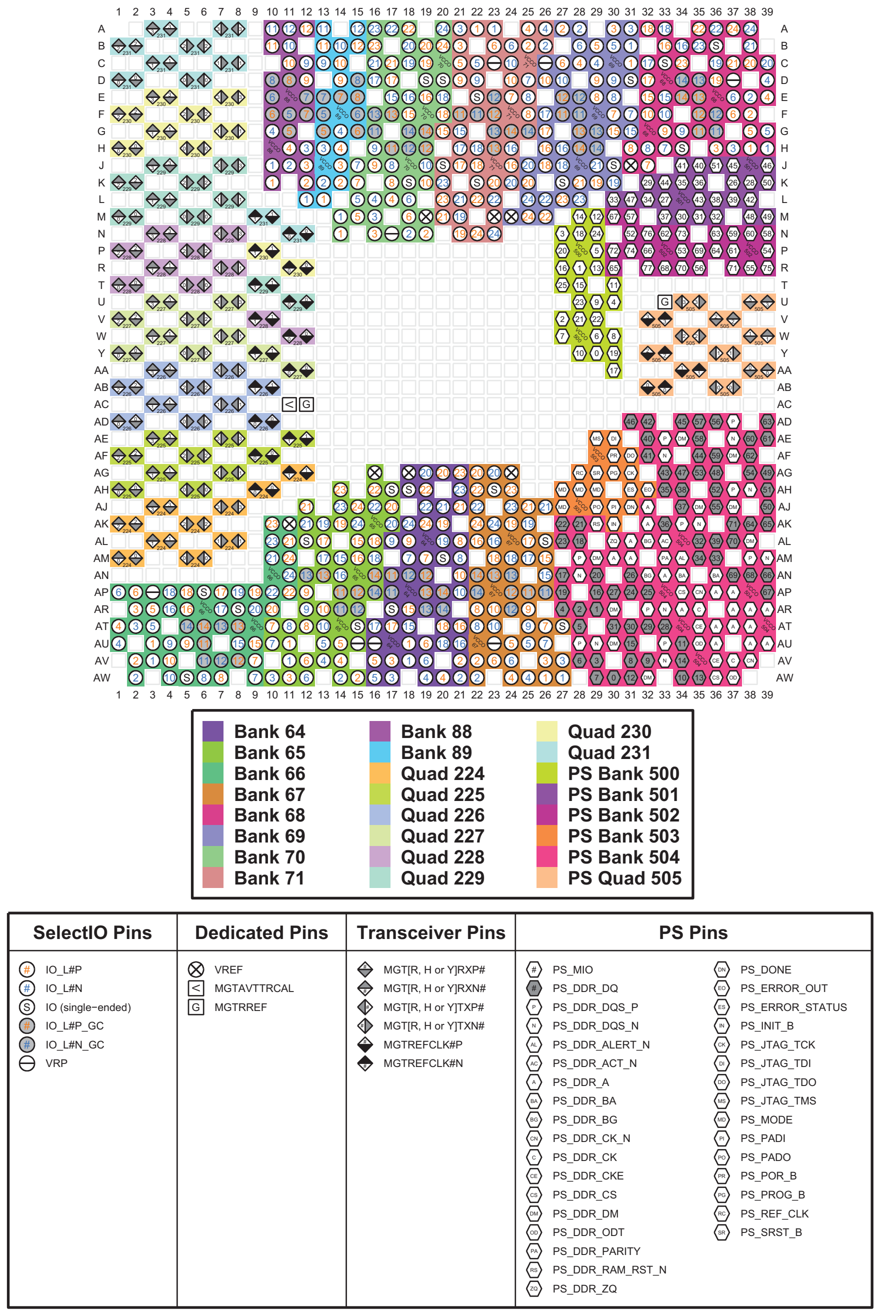
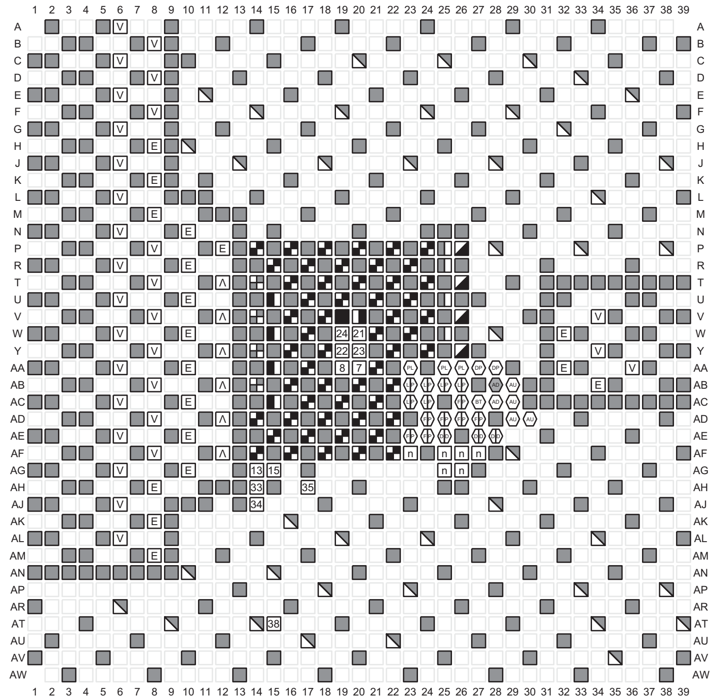


Figure 4-43: **FFVF1517 Package—XCZU11EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi–Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-44: **FFVF1517 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram**

FFVG1517 and FSVG1517 Packages–XCZU25DR

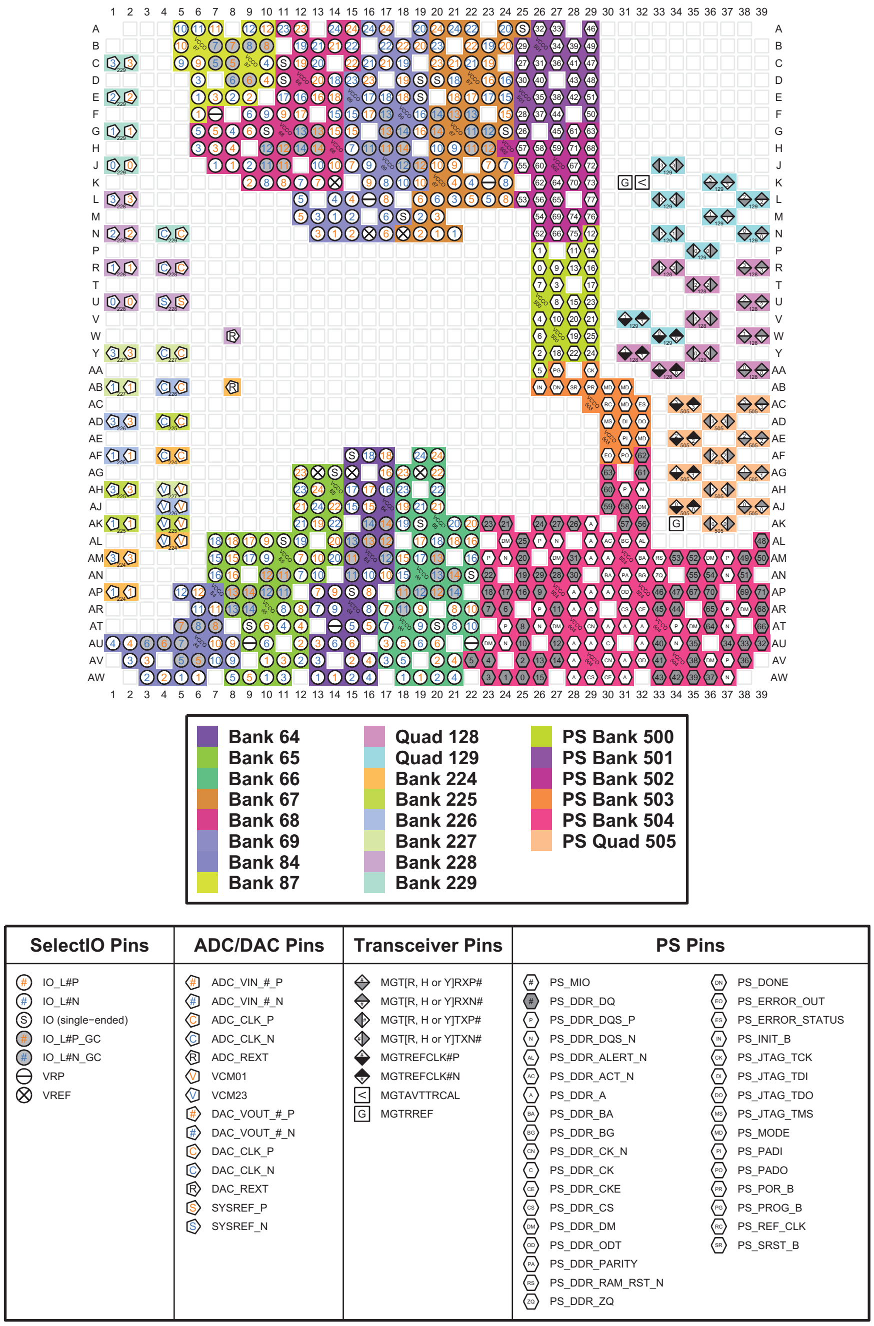
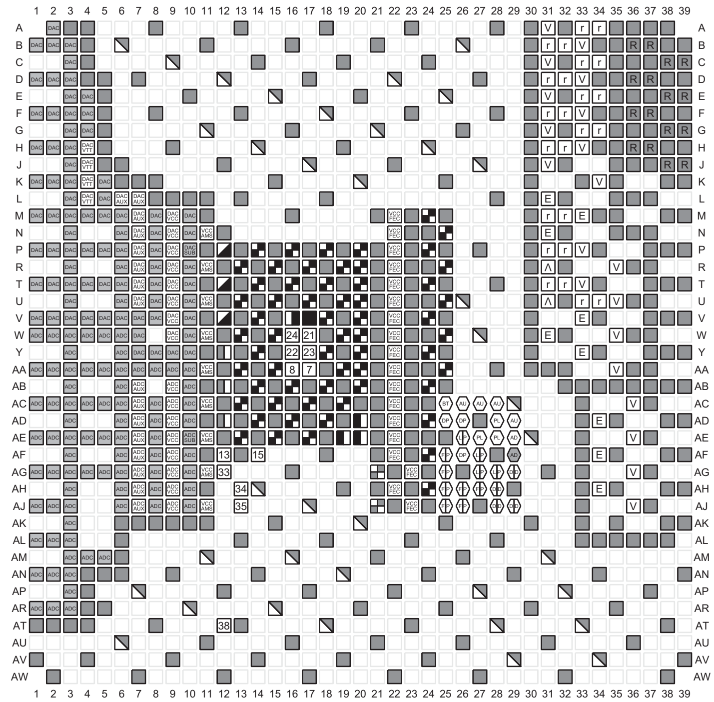


Figure 4-45: **FFVG1517 and FSVG1517 Packages—XCZU25DR I/O Bank Diagram**



Power Pins		Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	VCCSDFEC	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	VCCINT_AMS	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	ADC_AVCC	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	ADC_AVCCAUX	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	ADC_GND	21 VP		V PS_MGTRAVTT
VCCINT_VCU	ADC_SUB_GND	22 VN		VCC_PSBATT
VCCO_[bank number]	DAC_AVCC	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	DAC_AVCCAUX	24 VREFN		VCC_PSPLL
VCCADC	DAC_AVTT			VCC_PSINTFP
GNDADC	DAC_GND			VCC_PSINTFP_DDR
r RSVD	DAC_SUB_GND			VCC_PSINTLP
R RSVDGND	n NC			
E MGTAVCC_[R or L]				
V MGTAVTT_[R or L]				
Λ MGTVCCAUX_[R or L]				

Figure 4-46: **FFVG1517 and FSVG1517 Packages—XCZU25DR Power, Dedicated, and Multi-function Pin Diagram**

FFVG1517 and FSVG1517 Packages–XCZU27DR and XCZU28DR

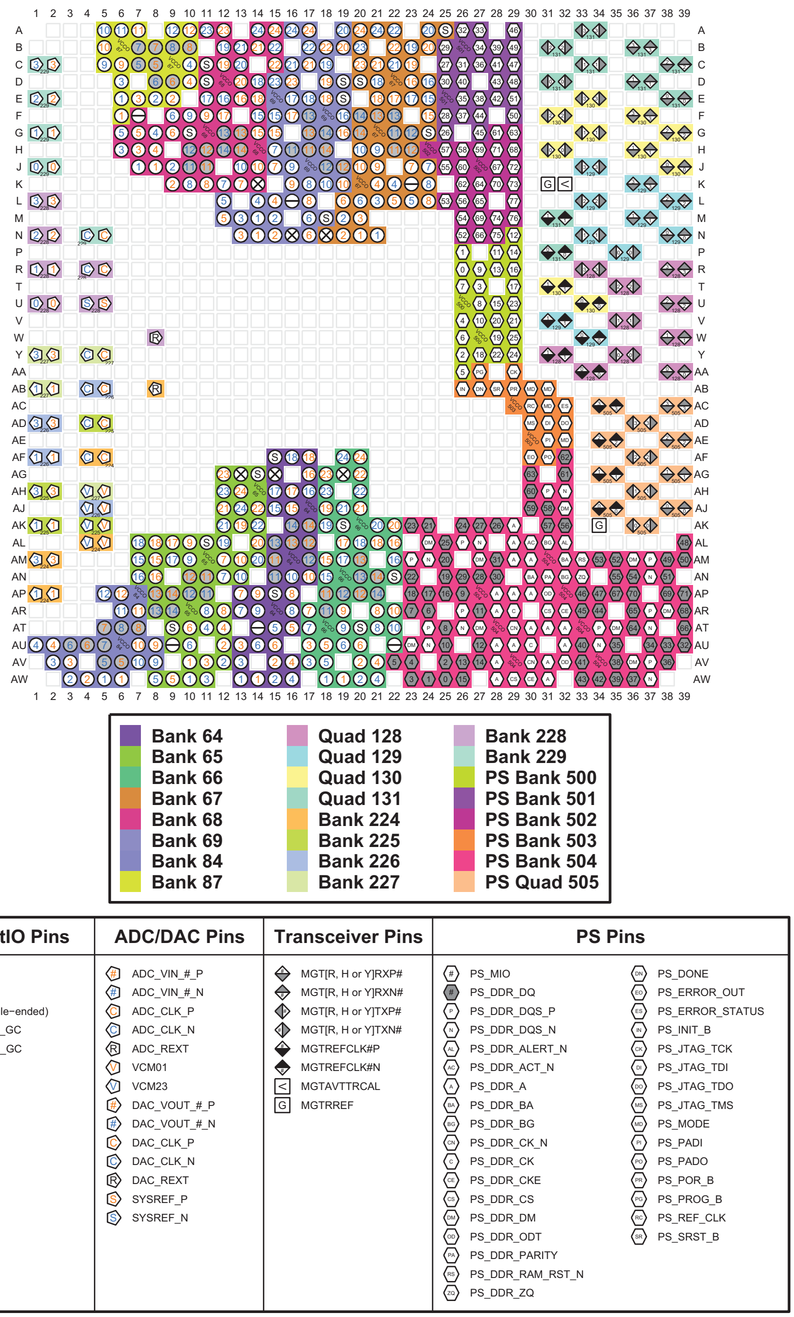


Figure 4-47: **FFVG1517 and FSVG1517 Packages—XCZU27DR and XCZU28DR I/O Bank Diagram**

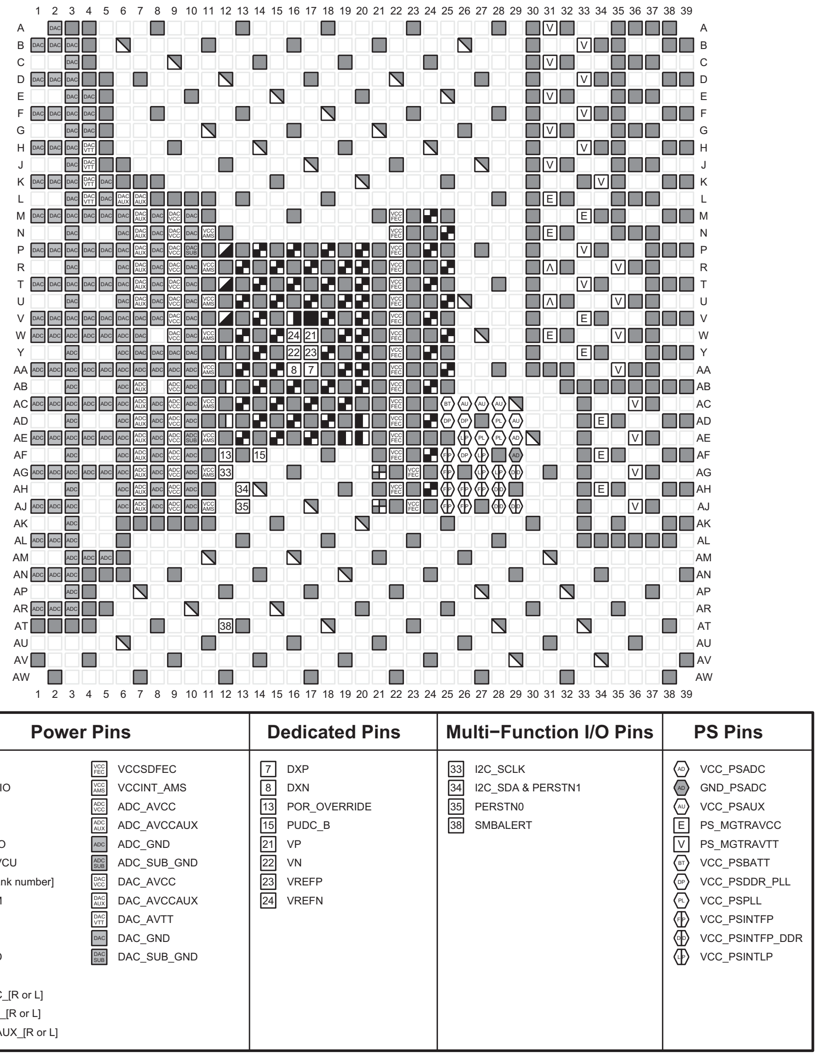


Figure 4-48: **FFVG1517 and FSVG1517 Packages—XCZU27DR and XCZU28DR Power, Dedicated, and Multi-function Pin Diagram**

FFVC1760 Package–XCZU11EG

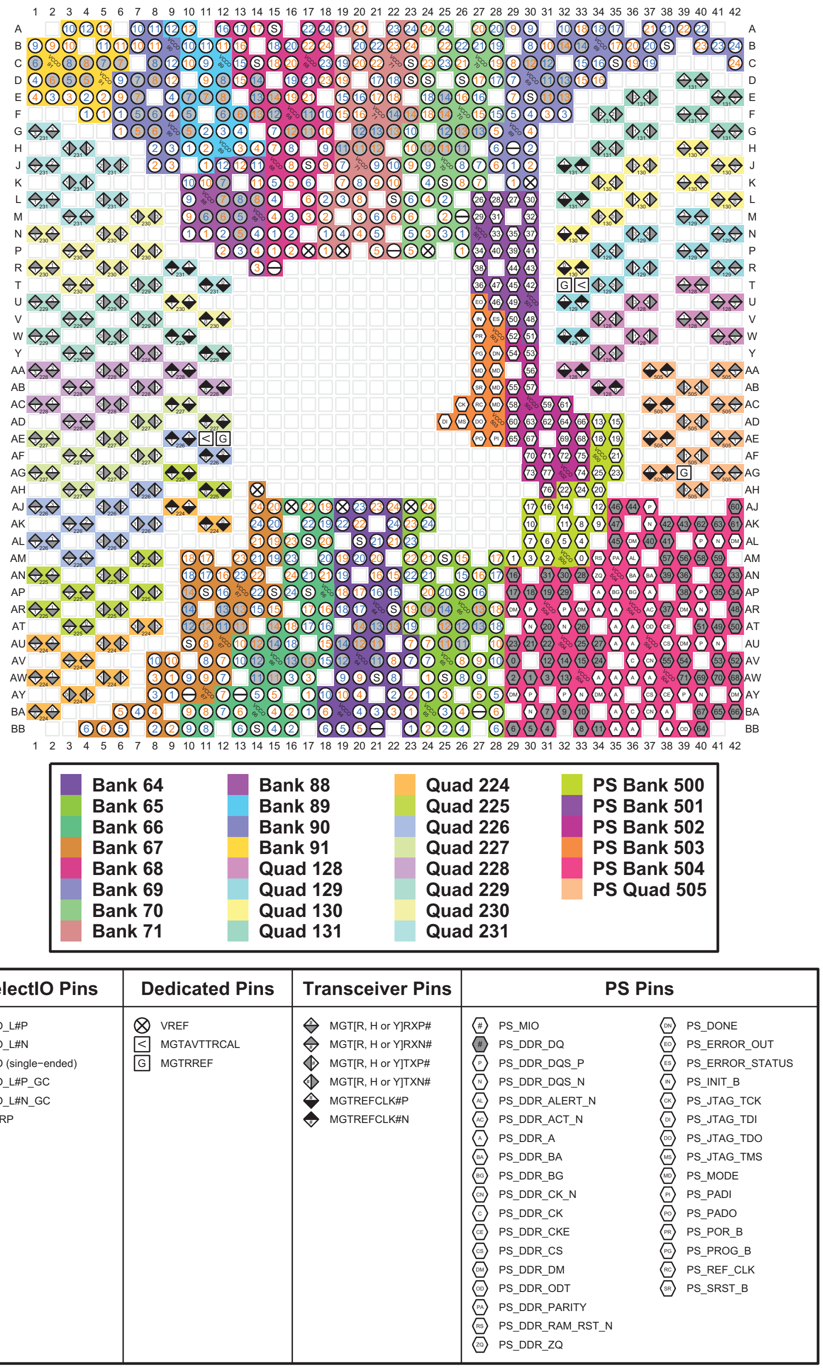
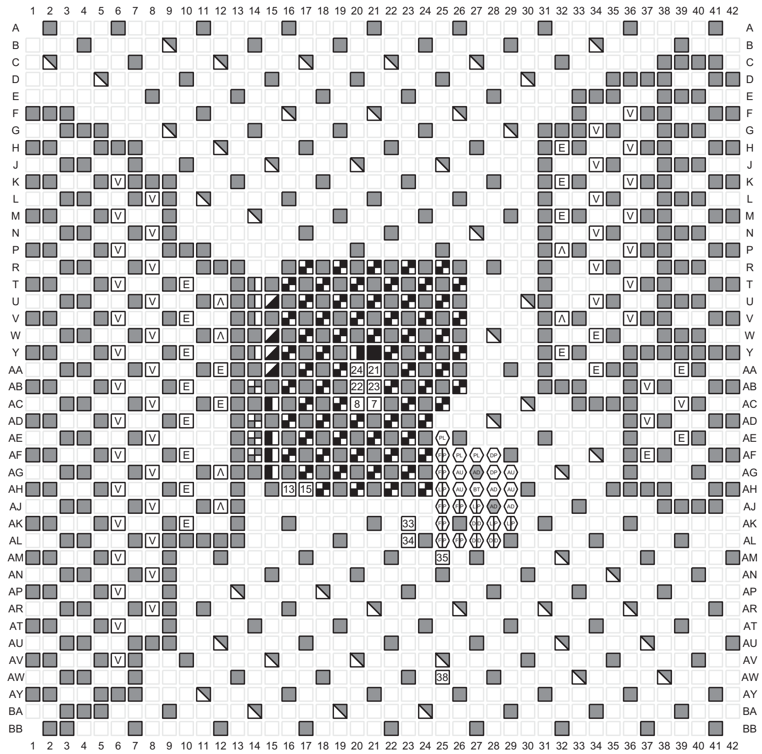


Figure 4-49: **FFVC1760 Package—XCZU11EG I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	21 VP		V PS_MGTRAVTT
VCCINT_VCU	22 VN		VCC_PSBATT
VCCO_[bank number]	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	24 VREFN		VCC_PSPLL
VCCADC			VCC_PSINTFP
GNDADC			VCC_PSINTFP_DDR
R RSVDGND			VCC_PSINTLP
n NC			
E MGTAVCC_[R or L]			
V MGTAVTT_[R or L]			
Λ MGTVCCAUX_[R or L]			

Figure 4-50: **FFVC1760 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram**

FFVC1760 Package–XCZU17EG and XCZU19EG

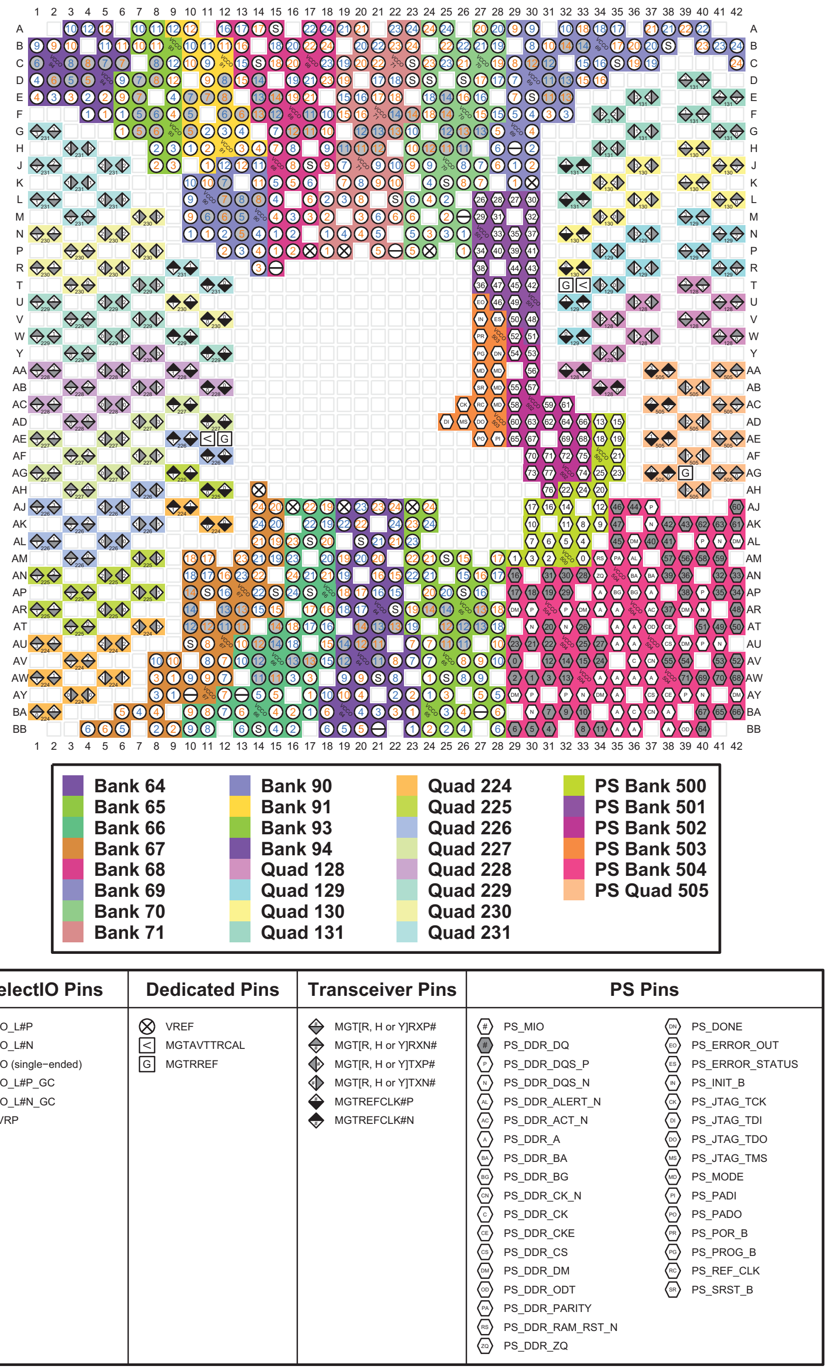


Figure 4-51: **FFVC1760 Package—XCZU17EG and XCZU19EG I/O Bank Diagram**

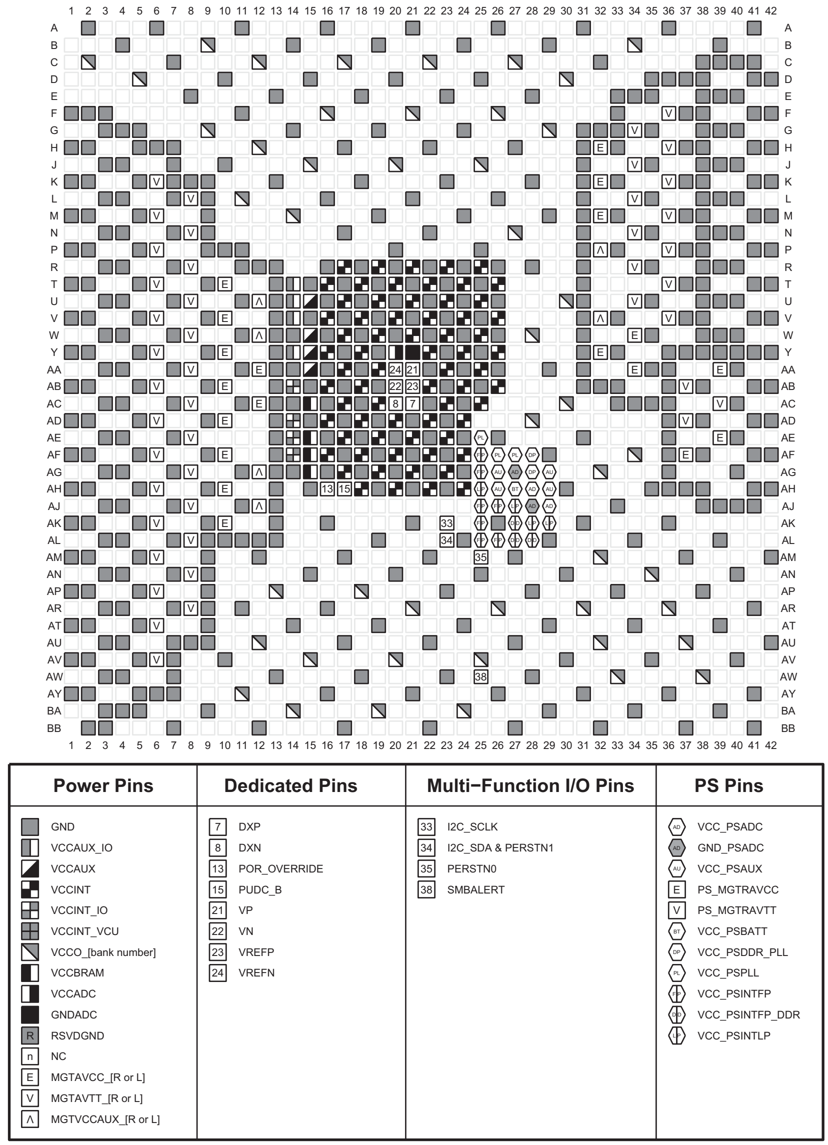


Figure 4-52: **FFVC1760 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram**

FFVD1760 Package–XCZU17EG and XCZU19EG

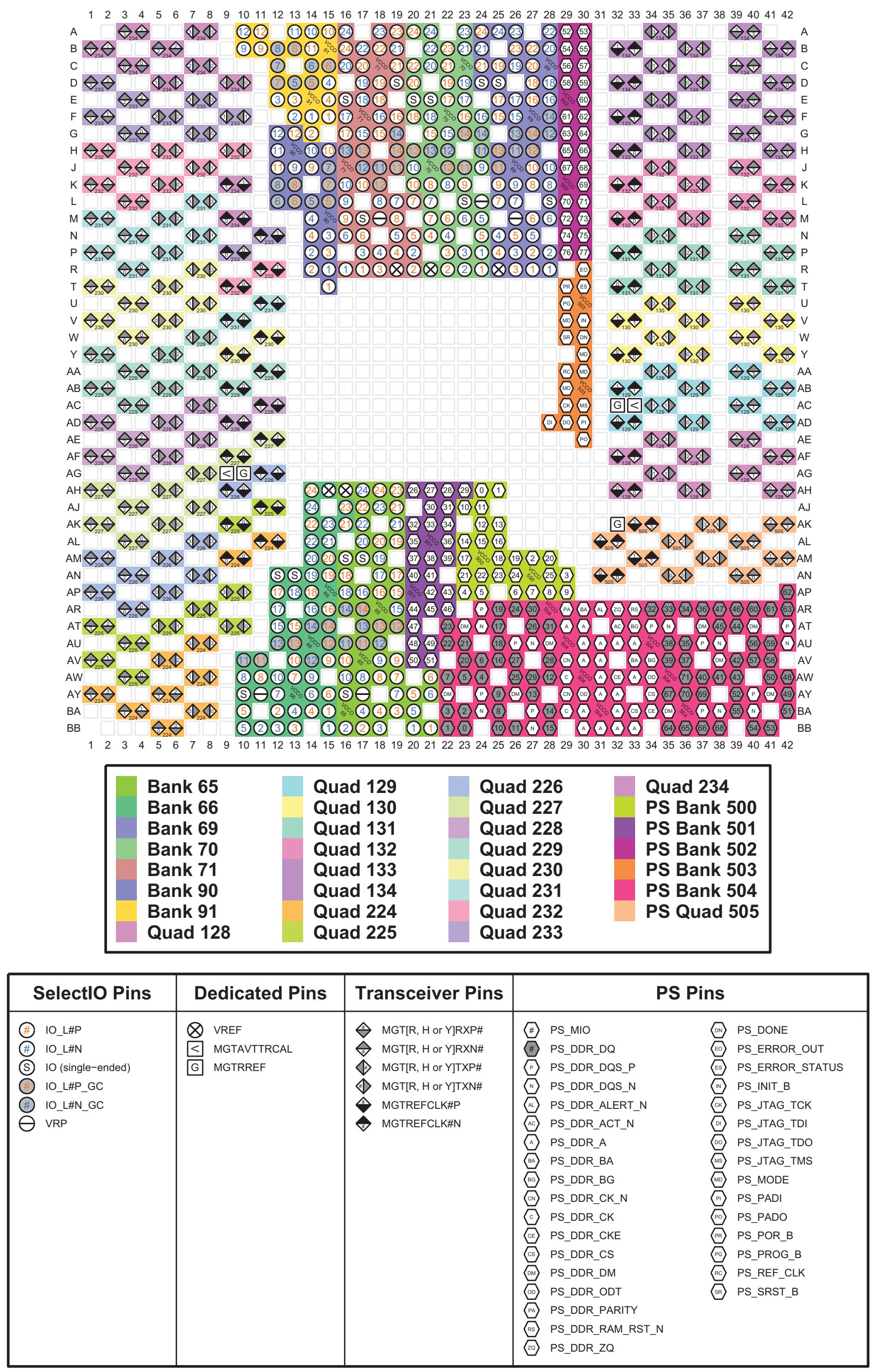


Figure 4-53: **FFVD1760 Package—XCZU17EG and XCZU19EG I/O Bank Diagram**

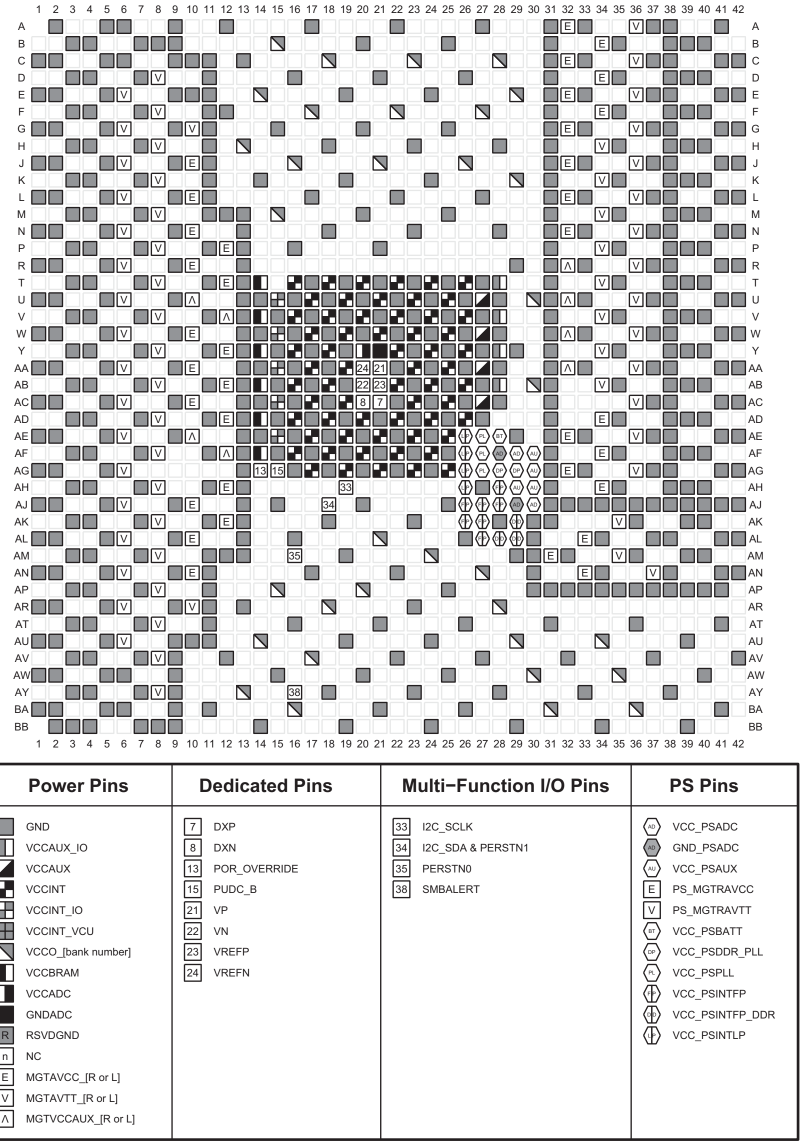


Figure 4-54: **FFVD1760 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram**

FFVF1760 and FSVF1760 Packages–XCZU29DR

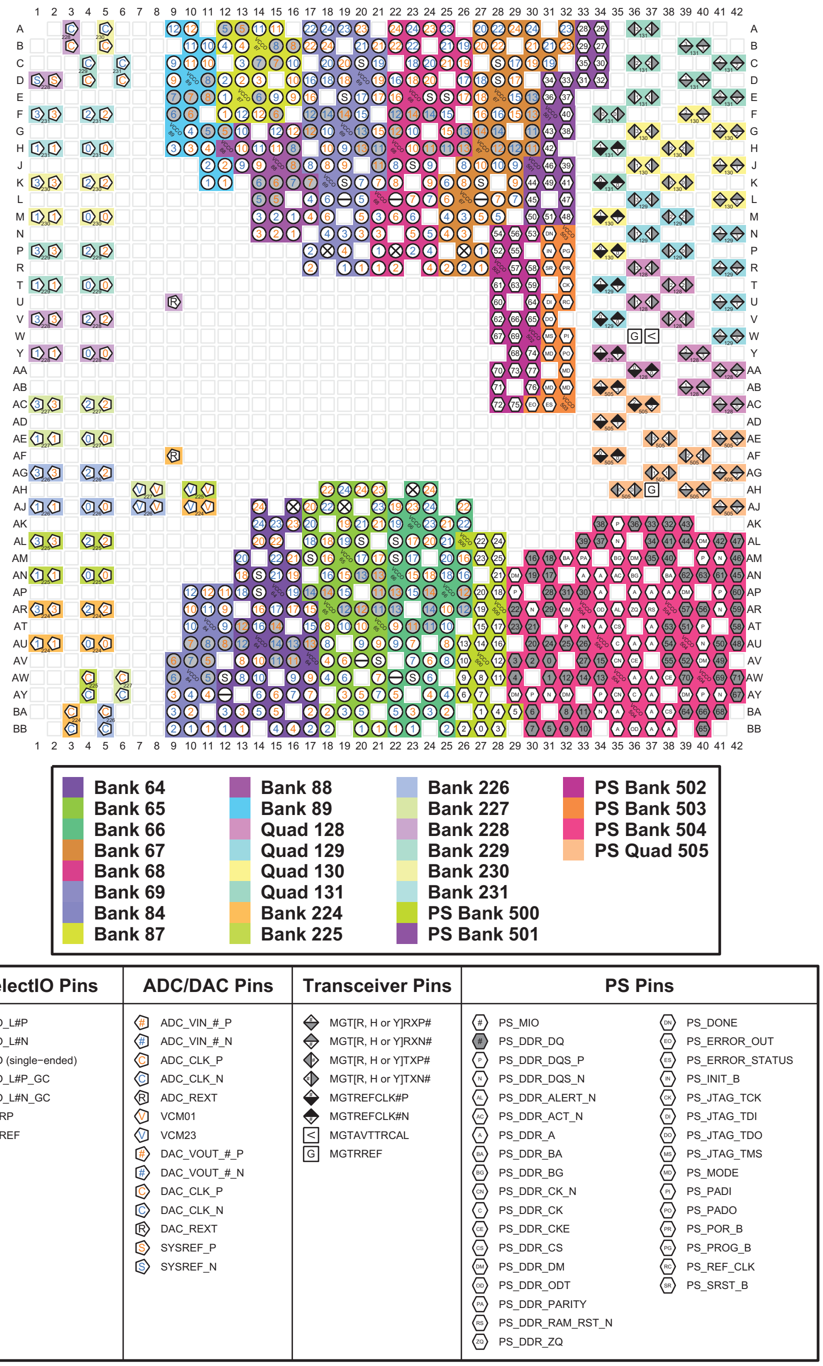
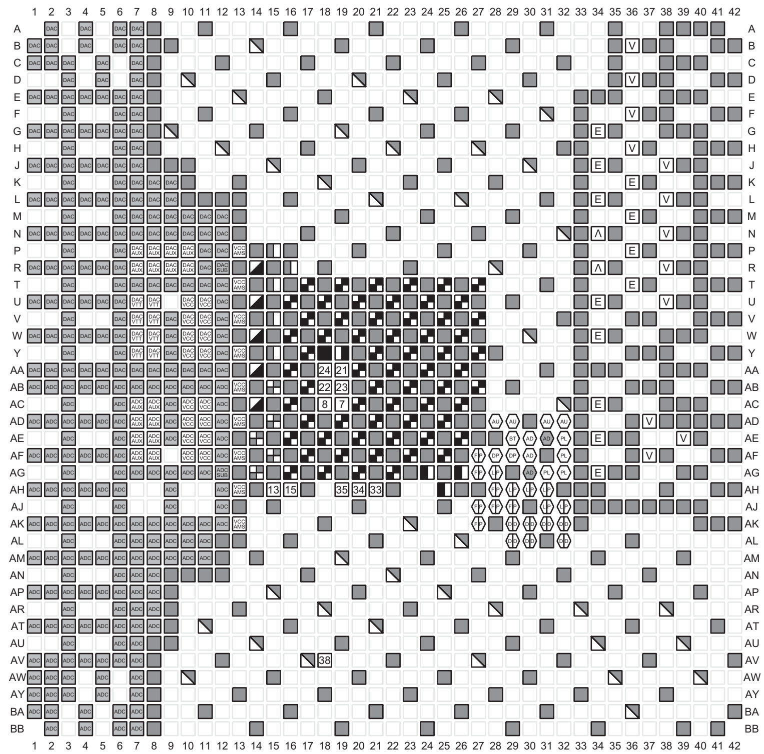


Figure 4-55: **FFVF1760 and FSVF1760 Packages—XCZU29DR I/O Bank Diagram**



Power Pins		Dedicated Pins	Multi-Function I/O Pins	PS Pins
GND	VCCSDFEC	7 DXP	33 I2C_SCLK	VCC_PSADC
VCCAUX_IO	VCCINT_AMS	8 DXN	34 I2C_SDA & PERSTN1	GND_PSADC
VCCAUX	ADC_AVCC	13 POR_OVERRIDE	35 PERSTN0	VCC_PSAUX
VCCINT	ADC_AVCCAUX	15 PUDC_B	38 SMBALERT	E PS_MGTRAVCC
VCCINT_IO	ADC_GND	21 VP		V PS_MGTRAVTT
VCCINT_VCU	ADC_SUB_GND	22 VN		VCC_PSBATT
VCCO_[bank number]	DAC_AVCC	23 VREFP		VCC_PSDDR_PLL
VCCBRAM	DAC_AVCCAUX	24 VREFN		VCC_PSPLL
VCCADC	DAC_AVTT			VCC_PSINTFP
GNDADC	DAC_GND			VCC_PSINTFP_DDR
R RSVDGND	DAC_SUB_GND			VCC_PSINTLP
n NC				
E MGTAVCC_[R or L]				
V MGTAVTT_[R or L]				
Λ MGTVCCAUX_[R or L]				

Figure 4-56: **FFVF1760 and FSVF1760 Packages—XCZU29DR Power, Dedicated, and Multi-function Pin Diagram**

FFVE1924 Package–XCZU17EG and XCZU19EG

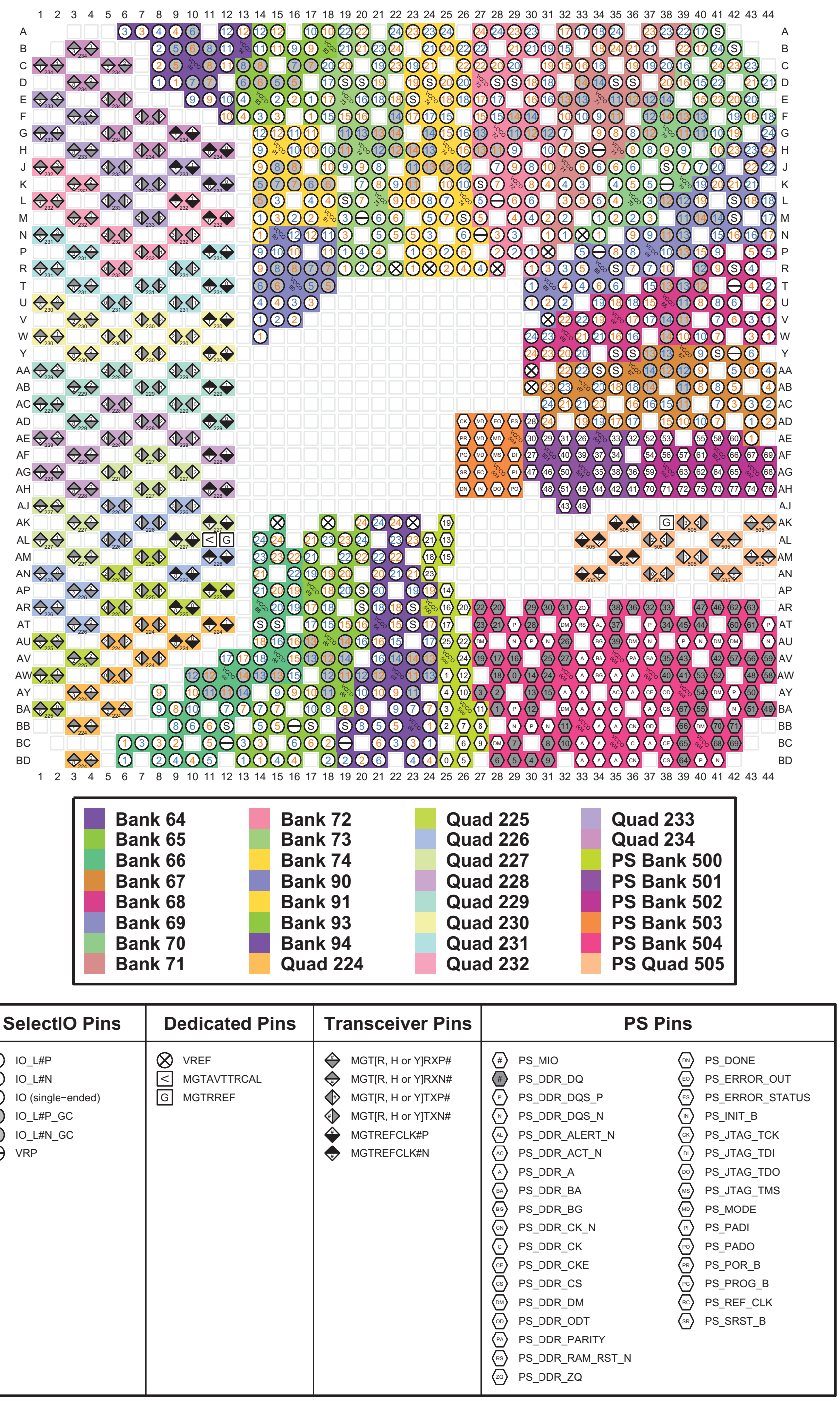


Figure 4-57: **FFVE1924 Package—XCZU17EG and XCZU19EG I/O Bank Diagram**

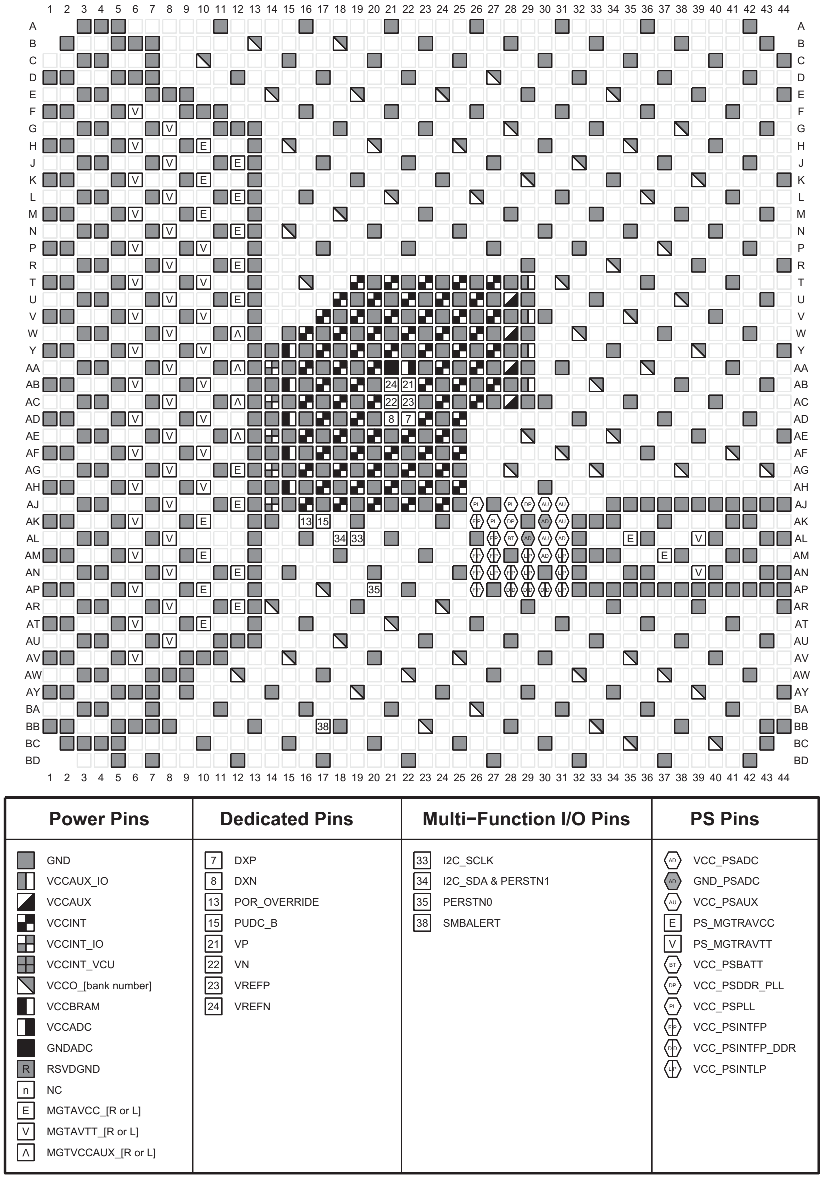


Figure 4-58: **FFVE1924 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram**

Chapter 5

Mechanical Drawings

Summary

This chapter provides mechanical drawings (package specifications) of the Zynq® UltraScale+™ devices. Table 5-1 is a cross-reference to the mechanical drawings by device and package combination. See Package Specifications Designations in Chapter 3 for definitions of Evaluation Only, Engineering Sample, and Production mechanical drawings.

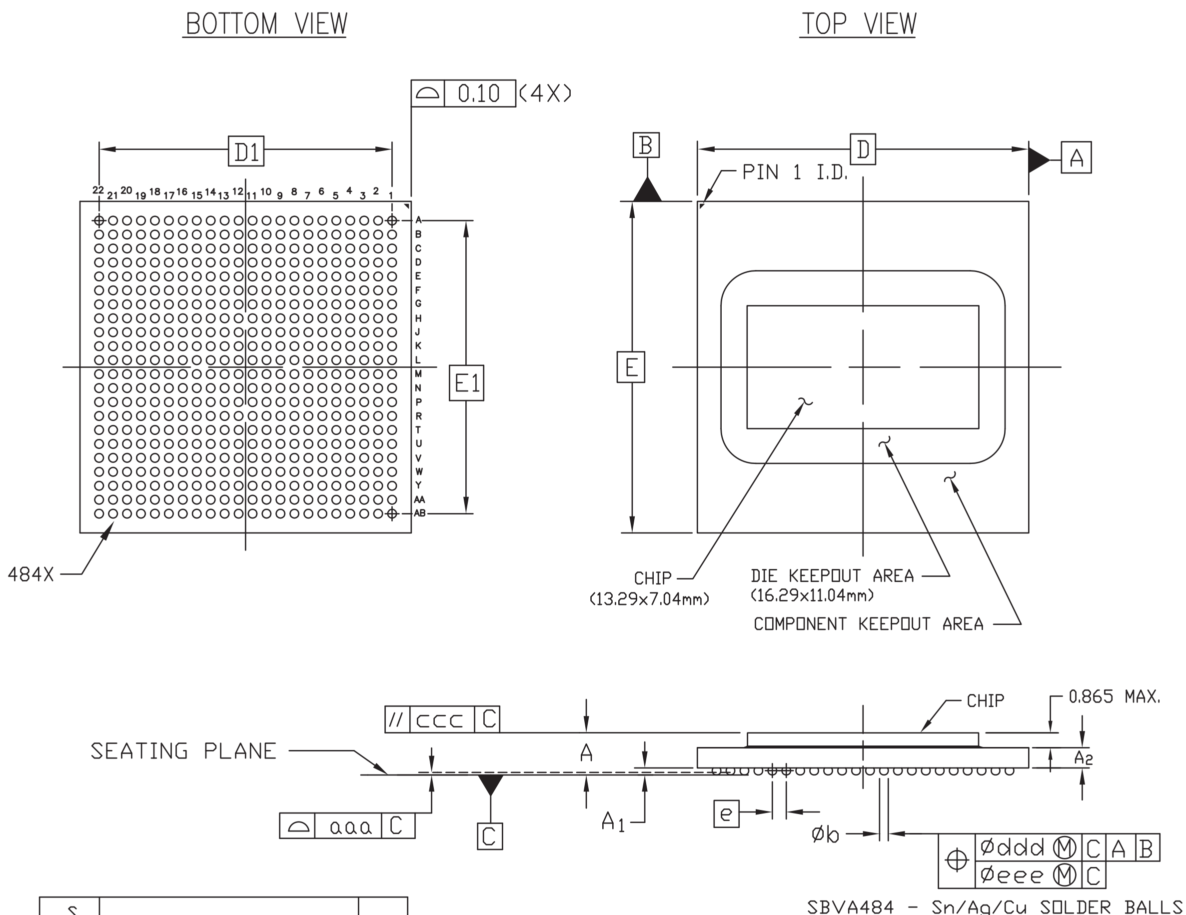
Table 5-1: **Cross-Reference to Zynq UltraScale+ MPSoC Mechanical Drawings by Package**

<table>
<tr><th rowspan="2">Package</th><th colspan="11">Device</th></tr>
<tr><th>XCZU2CG
XCZU2EG
XAZU2EG</th><th>XCZU3CG
XCZU3EG
XAZU3EG</th><th>XCZU4CG
XCZU4EG
XCZU4EV</th><th>XCZU5CG
XCZU5EG
XCZU5EV</th><th>XCZU6CG
XCZU6EG</th><th>XCZU7CG
XCZU7EG
XCZU7EV</th><th>XCZU9CG
XCZU9EG</th><th>XCZU11EG</th><th>XCZU15EG</th><th>XCZU17EG</th><th>XCZU19EG</th></tr>
<tr><td>SBVA484</td><td colspan="2">Figure 5-1
Production</td><td colspan="9"></td></tr>
<tr><td>SFVA625</td><td colspan="2">Figure 5-2
Production</td><td colspan="9"></td></tr>
<tr><td>SFVC784</td><td colspan="4">Figure 5-3
Production</td><td colspan="7"></td></tr>
<tr><td>FBVB900</td><td colspan="2"></td><td colspan="2">Figure 5-4
Production</td><td></td><td>Figure 5-5
Production</td><td colspan="5"></td></tr>
<tr><td>FFVC900</td><td colspan="4"></td><td>Figure 5-6
Production</td><td></td><td>Figure 5-6
Production</td><td></td><td>Figure 5-6
Production</td><td colspan="2"></td></tr>
<tr><td>FFVB1156</td><td colspan="4"></td><td>Figure 5-7
Production</td><td></td><td>Figure 5-7
Production</td><td></td><td>Figure 5-7
Production</td><td colspan="2"></td></tr>
<tr><td>FFVC1156</td><td colspan="5"></td><td>Figure 5-8
Production</td><td></td><td>Figure 5-8
Production</td><td colspan="3"></td></tr>
<tr><td>FFVB1517</td><td colspan="7"></td><td>Figure 5-11
Production</td><td></td><td colspan="2">Figure 5-11
Production</td></tr>
<tr><td>FFVF1517</td><td colspan="5"></td><td>Figure 5-11
Production</td><td></td><td>Figure 5-11
Production</td><td colspan="3"></td></tr>
<tr><td>FFVC1760</td><td colspan="7"></td><td>Figure 5-14
Production</td><td></td><td colspan="2">Figure 5-14
Production</td></tr>
<tr><td>FFVD1760</td><td colspan="9"></td><td colspan="2">Figure 5-14
Production</td></tr>
<tr><td>FFVE1924</td><td colspan="9"></td><td colspan="2">Figure 5-17
Production</td></tr>
</table>

Table 5-2: **Cross-Reference to Zynq UltraScale+ RFSoC Mechanical Drawings by Package**

Package	Device				
	XCZU21DR	**XCZU25DR**	**XCZU27DR**	**XCZU28DR**	**XCZU29DR**
FFVD1156	Figure 5-9 Engineering Sample				
FFVE1156		Figure 5-9 Engineering Sample	Figure 5-9 Engineering Sample	Figure 5-9 Engineering Sample	
FSVE1156		Figure 5-10 Engineering Sample	Figure 5-10 Engineering Sample	Figure 5-10 Engineering Sample	
FFVG1517		Figure 5-12 Engineering Sample	Figure 5-12 Engineering Sample	Figure 5-12 Engineering Sample	
FSVG1517		Figure 5-13 Engineering Sample	Figure 5-13 Engineering Sample	Figure 5-13 Engineering Sample	
FFVF1760					Figure 5-15 Engineering Sample
FSVF1760					Figure 5-16 Engineering Sample

SBVA484 Flip-Chip, Fine-Pitch BGA (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.21	2.41	2.61	
A_1	0.36	0.40	0.44	
A_2	1.01	1.16	1.31	
D/E	19.00 BASIC			
D_1/E_1	16.80 BASIC			
e	0.80 BASIC			
Øb	0.45	0.50	0.55	
aaa	-	-	0.12	
ccc	-	-	0.20	
ddd	-	-	0.15	
eee	-	-	0.08	
M	25			2

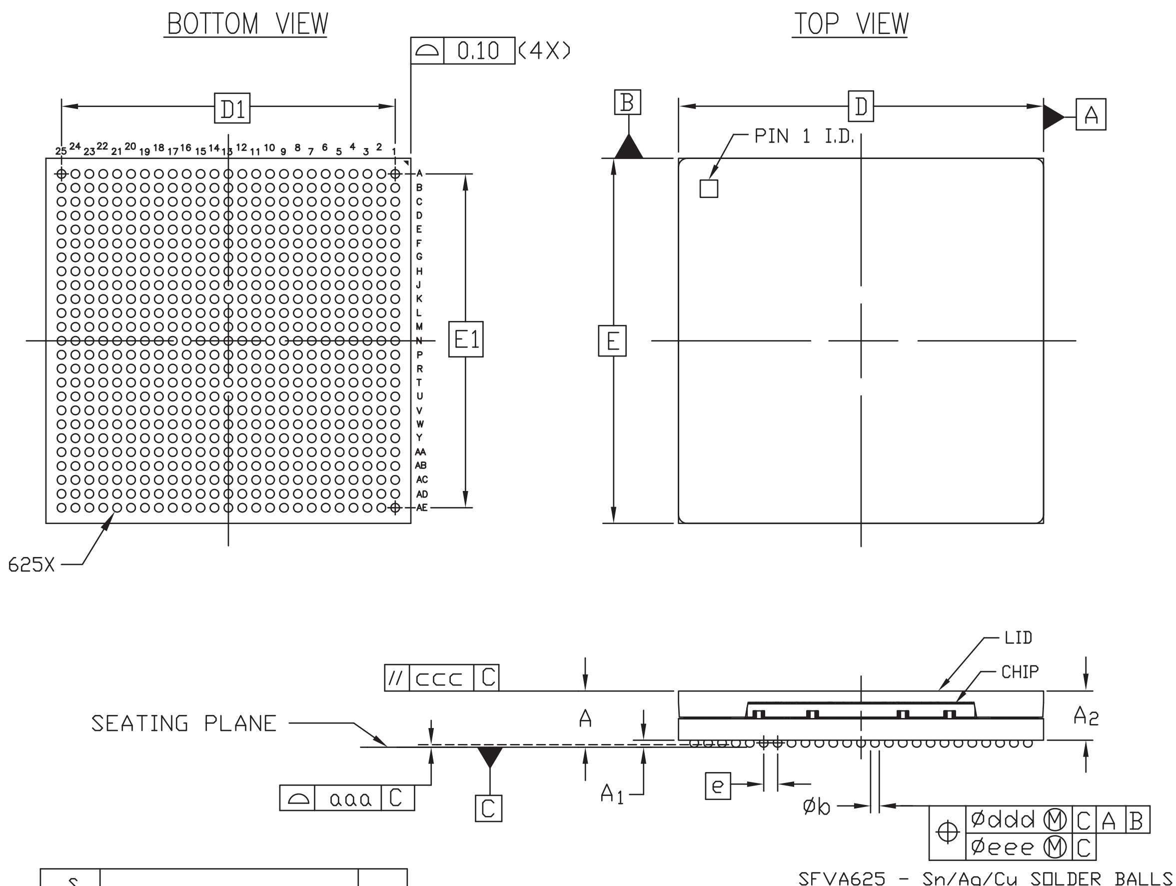
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-216 BAP-2

ug1075_c5_073116

Figure 5-1: **Package Dimensions for SBVA484 (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)**

SFVA625 Flip-Chip, Fine-Pitch BGA (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.03	3.23	3.43	
A1	0.36	0.40	0.44	
A2	2.63	2.83	3.03	
D/E	21.00 BASIC			
D1/E1	19.20 BASIC			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa	~	~	0.12	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	25			2

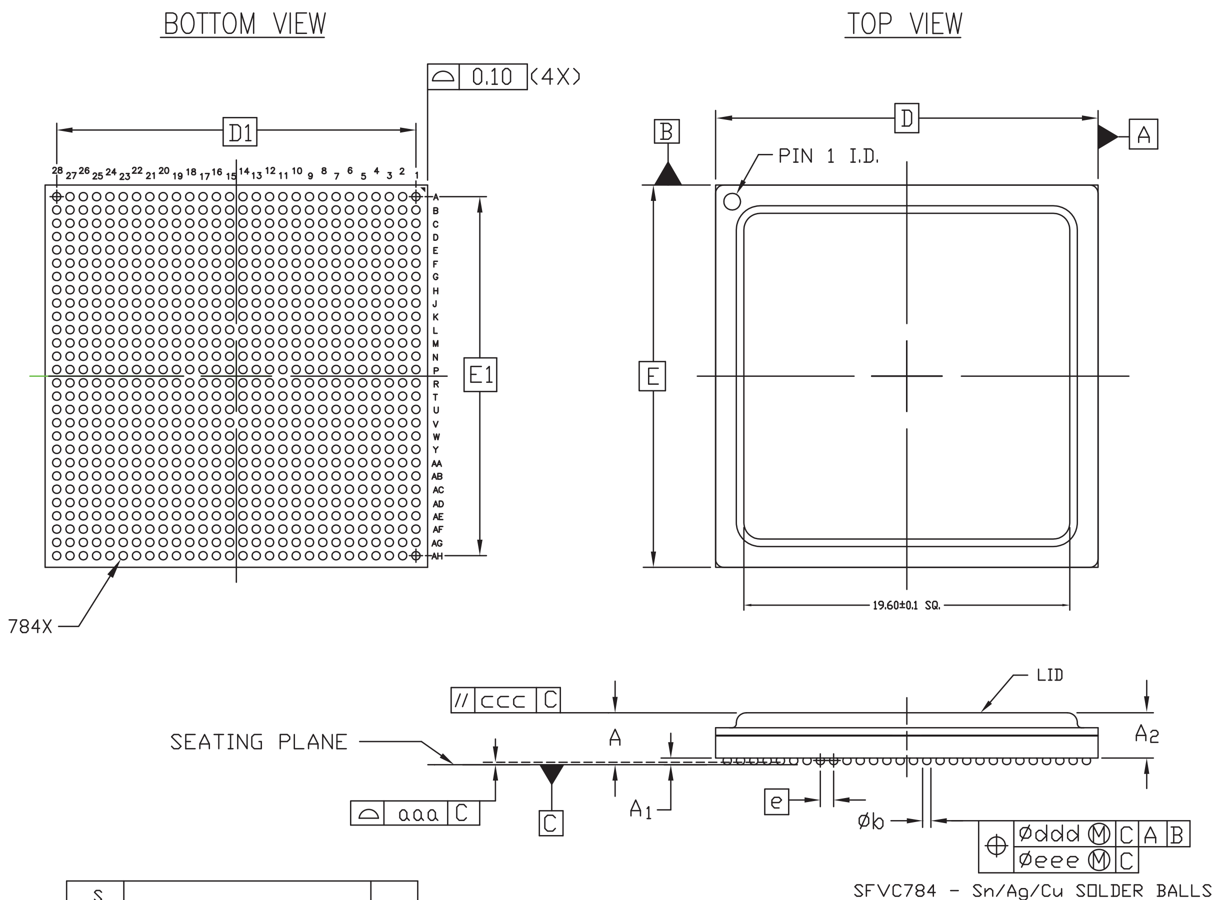
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-216 BAS-1

ug1075_c5_073116

Figure 5-2: **Package Dimensions for SFVA625 (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)**

SFVC784 Flip-Chip, Fine-Pitch BGA (XCZU2, XCZU3, XCZU4, XCZU5, XAZU2EG, and XAZU3EG)



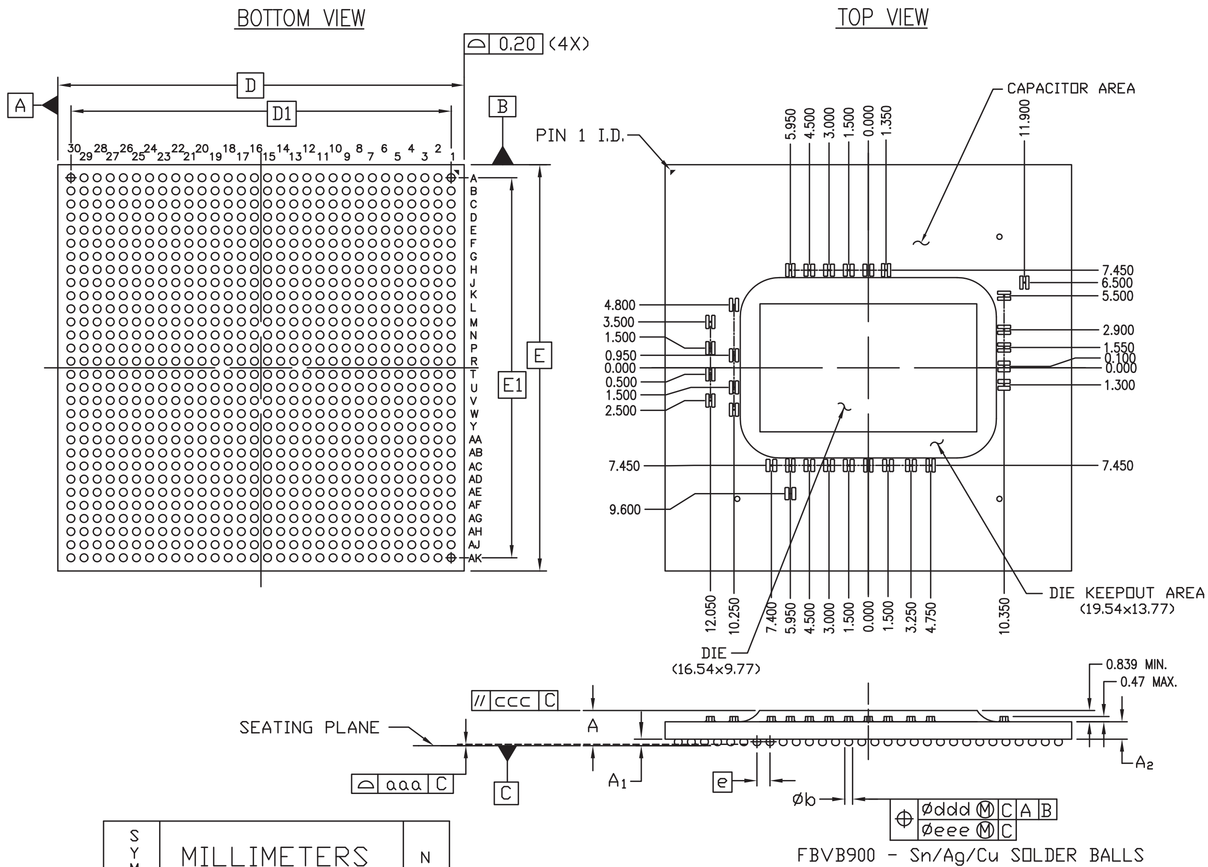
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.92	3.12	3.32	
A_1	0.36	0.40	0.44	
A_2	2.52	2.72	2.92	
D/E	23.00 BASIC			
D_1/E_1	21.60 BASIC			
e	0.80 BASIC			
Øb	0.45	0.50	0.55	
aaa	~	~	0.12	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	28			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–216 BAU–1

Figure 5-3: **Package Dimensions for SFVC784 (XCZU2, XCZU3, XCZU4, XCZU5, XAZU2EG, and XAZU3EG)**

FBVB900 Flip-Chip, Fine-Pitch BGA (XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, and XCZU5EV)



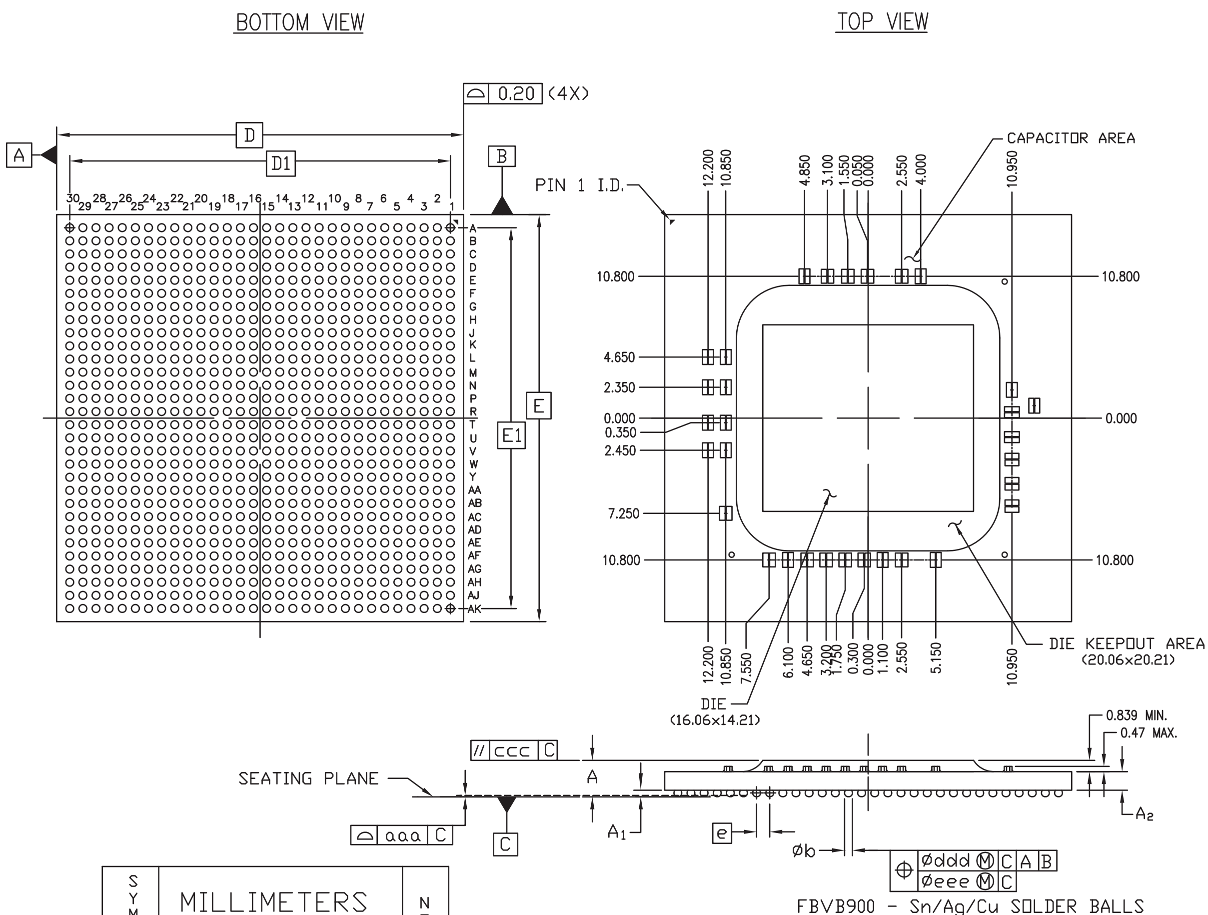
SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	2.48	2.68	2.88	
A1	0.40	0.50	0.60	
A2	1.18	1.33	1.48	
D/E	31.00 BASIC			
D1/E1	29.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034 (DEPOPULATED)

Figure 5-4: **Package Dimensions for FBVB900 (XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, and XCZU5EV)**

FBVB900 Flip-Chip, Fine-Pitch BGA (XCZU7CG, XCZU7EG, and XCZU7EV)



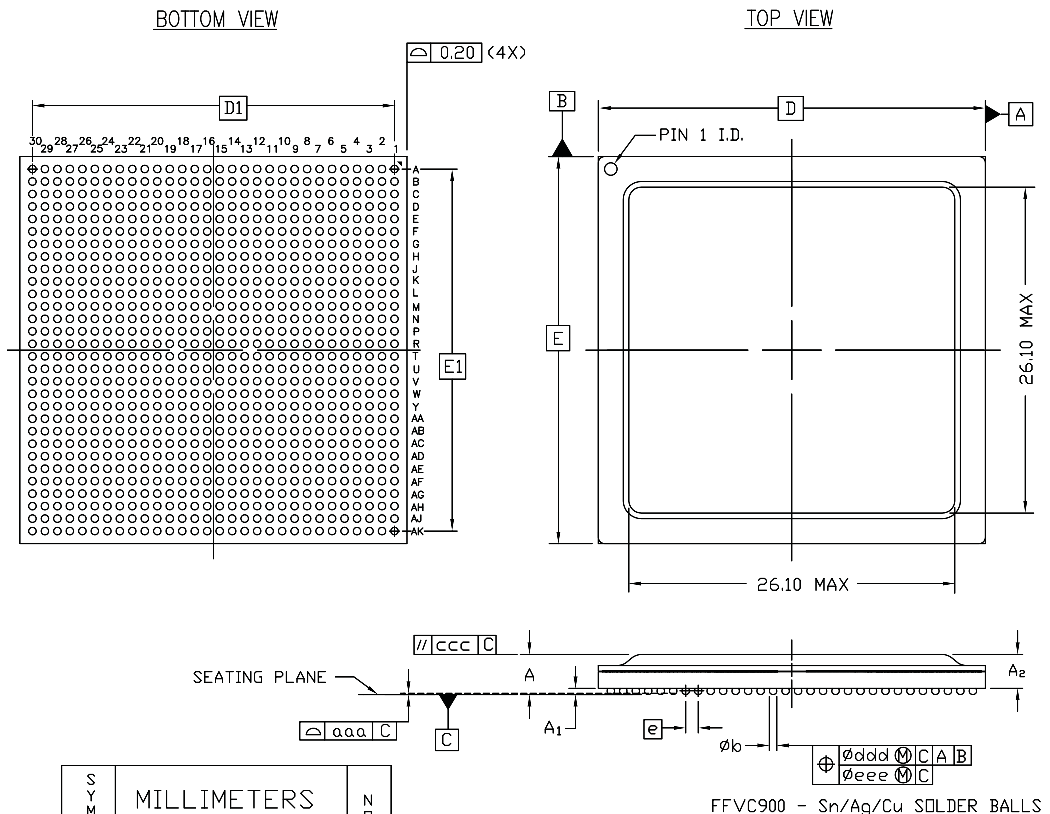
SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	2.57	2.77	2.97	
A_1	0.40	0.50	0.60	
A_2	1.27	1.42	1.57	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034 (DEPOPULATED)

Figure 5-5: **Package Dimensions for FBVB900 (XCZU7CG, XCZU7EG, and XCZU7EV)**

FFVC900 Flip-Chip, Fine-Pitch BGA (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.02	3.22	3.42	
A_1	0.40	0.50	0.60	
A_2	2.52	2.72	2.92	
D/E	31.00 BASIC			
D_1/E_1	29.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

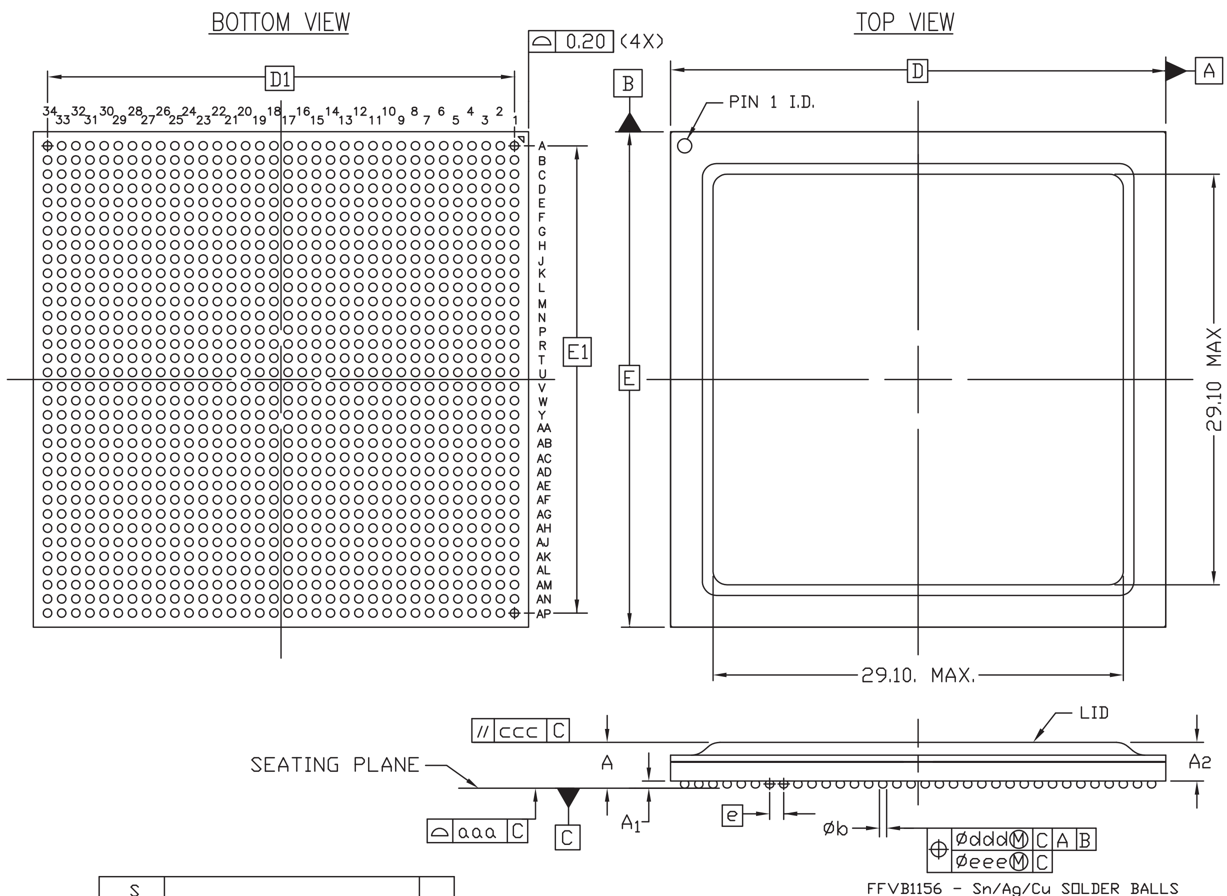
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS-034 (DEPOPULATED)

ug1075_c5_073116

Figure 5-6: **Package Dimensions for FFVC900 (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)**

FFVB1156 Flip-Chip, Fine-Pitch BGA (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.02	3.22	3.42	
A_1	0.40	0.50	0.60	
A_2	2.52	2.72	2.92	
D/E	35.00 BASIC			
D1/E1	33.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	34			2

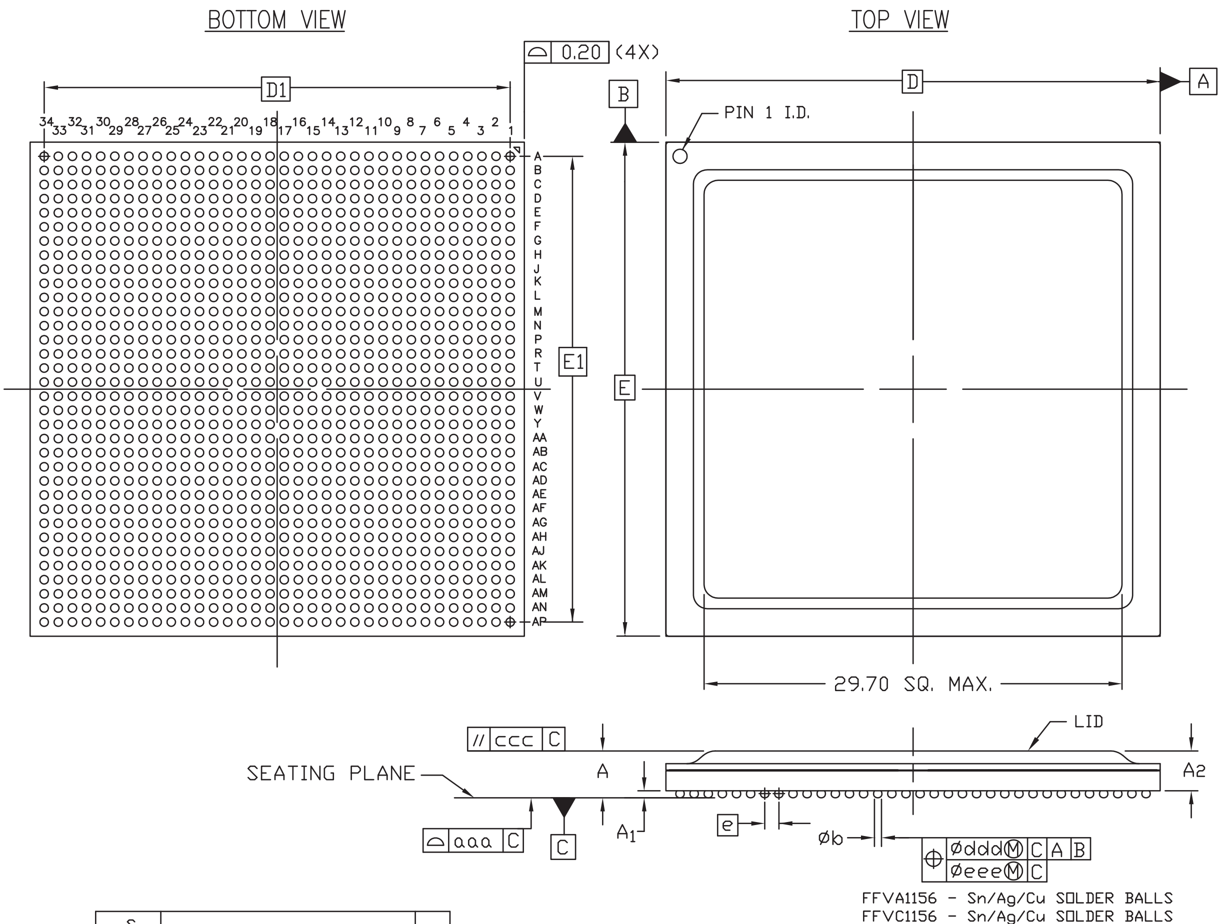
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS-034-AAR-1

ug1075_c5_073116

Figure 5-7: **Package Dimensions for FFVB1156 (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)**

FFVC1156 Flip-Chip, Fine-Pitch BGA (XCZU7CG, XCZU7EG, XCZU7EV, and XCZU11EG)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.11	3.31	3.51	
A_1	0.40	0.50	0.60	
A_2	2.61	2.81	3.01	
D/E	35.00 BASIC			
D1/E1	33.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	-	-	0.20	
ccc	-	-	0.35	
ddd	-	-	0.30	
eee	-	-	0.10	
M	34			2

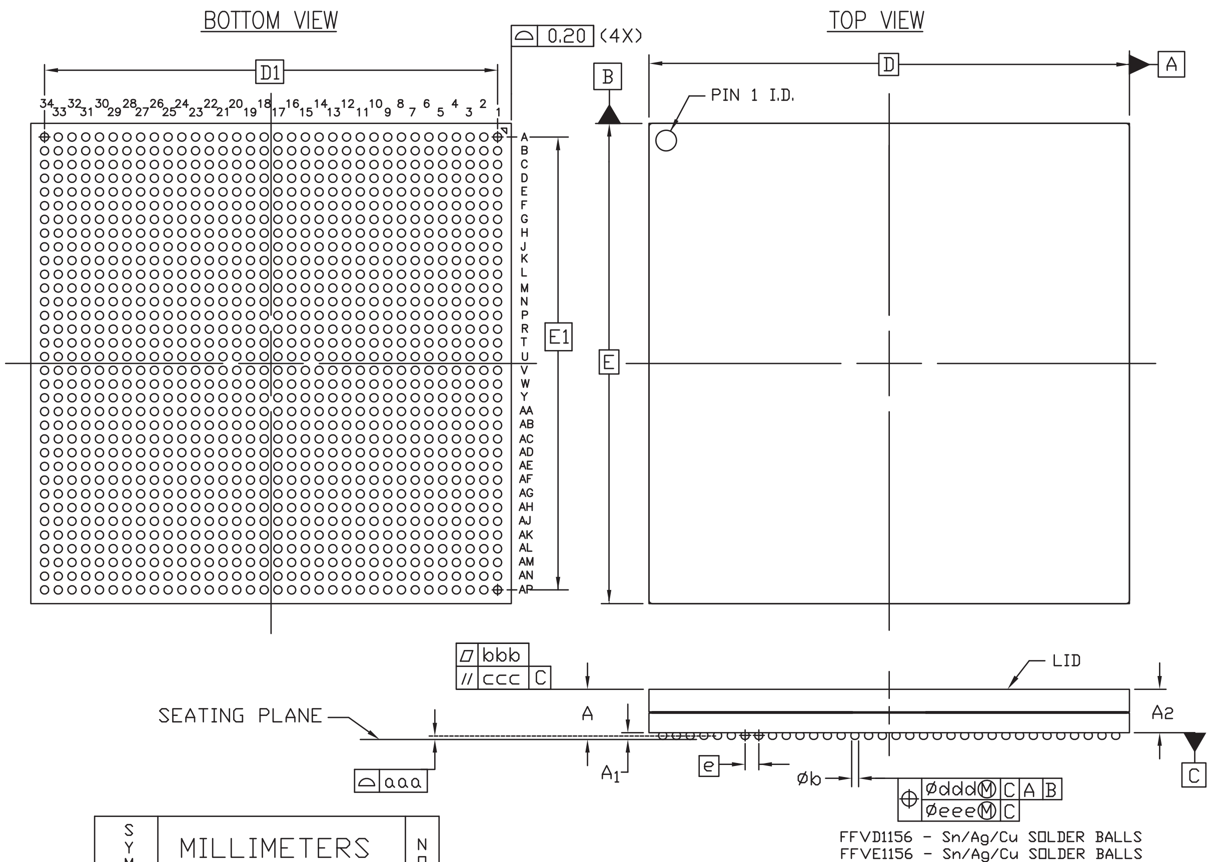
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1

ug1075_c5_073116

Figure 5-8: **Package Dimensions for FFVC1156 (XCZU7CG, XCZU7EG, XCZU7EV, and XCZU11EG)**

FFVD1156 (XCZU21DR) and FFVE1156 (XCZU25DR, XCZU27DR, and XCZU28DR) Flip-Chip, Fine-Pitch BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.46	3.66	3.86	
A_1	0.40	0.50	0.60	
A_2	2.96	3.16	3.36	
D/E	35.00 BASIC			
D1/E1	33.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	--	--	0.20	
bbb	--	--	0.10	
ccc	--	--	0.10	
ddd	--	--	0.30	
eee	--	--	0.10	
M	34			2

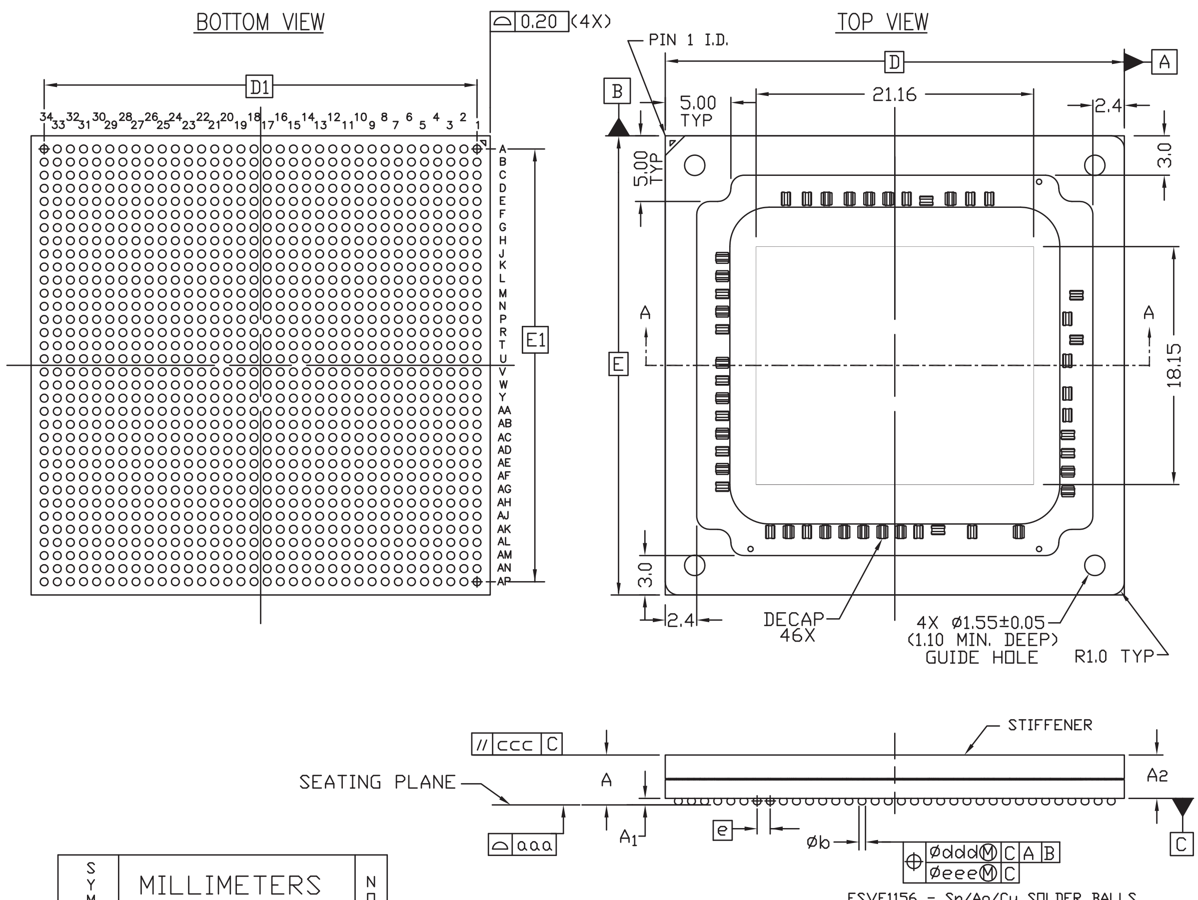
NOTES:

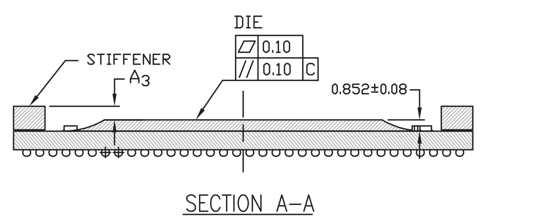
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1

ug1075_ffvd1156_ffve1156_030518

Figure 5-9: **Package Dimensions for FFVD1156 (XCZU21DR) and FFVE1156 (XCZU25DR, XCZU27DR, and XCZU28DR)**

FSVE1156 (XCZU25DR, XCZU27DR, and XCZU28DR) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring BGA





SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.61	3.81	4.01	
A_1	0.40	0.50	0.60	
A_2	3.11	3.31	3.51	
A_3	0.94	1.04	1.14	
D/E	35.00 BASIC			
D_1/E_1	33.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	34			2

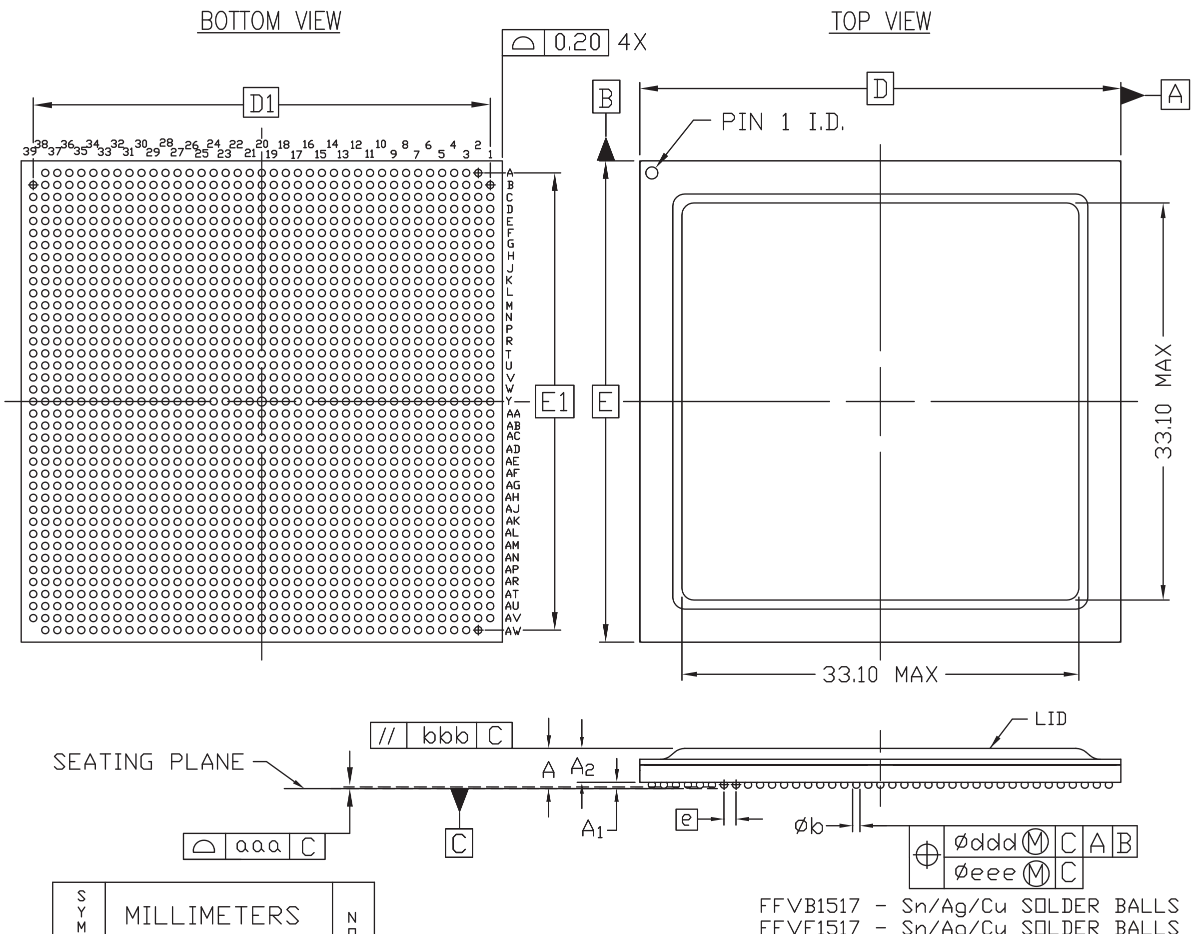
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–318 P35.0x35.0–EF–1156

ug1075_fsve1156_030518

Figure 5-10: **Package Dimensions for FSVE1156 (XCZU25DR, XCZU27DR, and XCZU28DR)**

FFVB1517 (XCZU11EG, XCZU17EG, and XCZU19EG) and FFVF1517 (XCZU7CG, XCZU7EG, XCZU7EV, and XCZU11EG) Flip-Chip, Fine-Pitch BGA



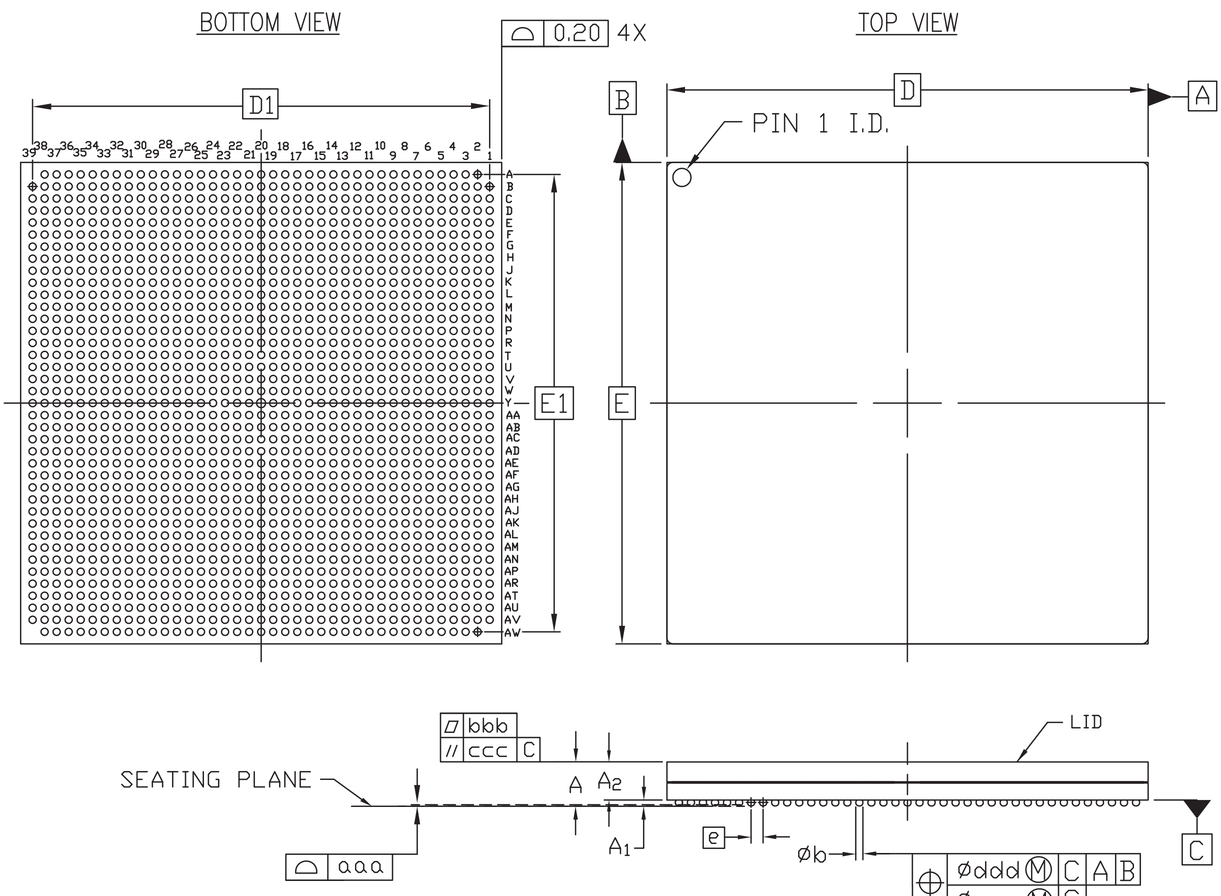
SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.11	3.31	3.51	
A_1	0.40	0.50	0.60	
A_2	2.61	2.81	3.01	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M		39		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAU-1 (DEPOPULATED)

Figure 5-11: **Package Dimensions for FFVB1517 (XCZU11EG, XCZU17EG, and XCZU19EG) and FFVF1517 (XCZU7CG, XCZU7EG, XCZU7EV, and XCZU11EG)**

FFVG1517 (XCZU25DR, XCZU27DR, and XCZU28DR) Flip-Chip, Fine-Pitch BGA



FFVG1517 – Sn/Ag/Cu SOLDER BALLS

SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.46	3.66	3.86	
A_1	0.40	0.50	0.60	
A_2	2.96	3.16	3.36	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
bbb	—	—	0.10	
ccc	—	—	0.10	
ddd	—	—	0.25	
eee	—	—	0.10	
M		39		2

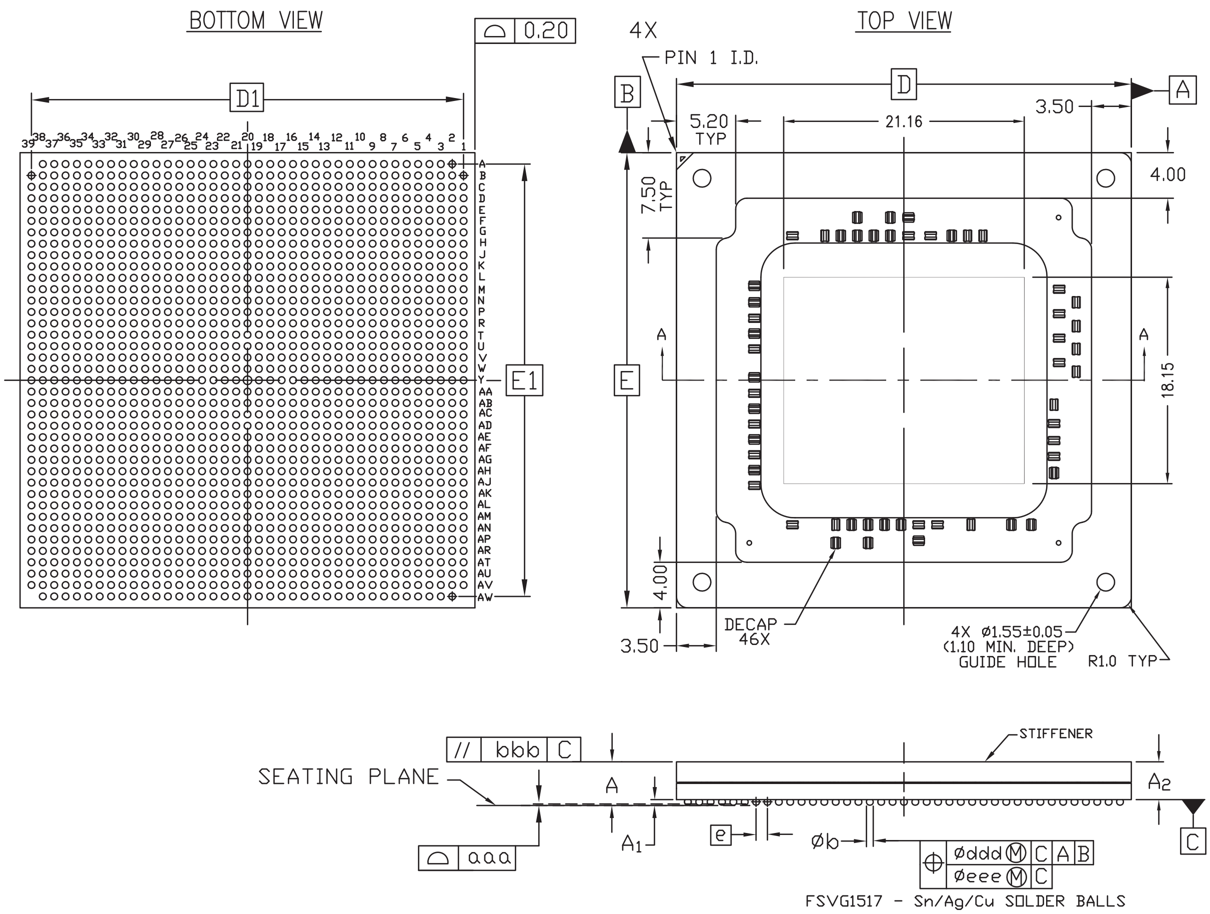
NOTES:

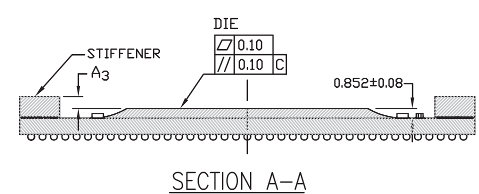
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

ug1075_ffvg1517_030518

Figure 5-12: **Package Dimensions for FFVG1517 (XCZU25DR, XCZU27DR, and XCZU28DR)**

FSVG1517 (XCZU25DR, XCZU27DR, and XCZU28DR) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring BGA





SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.61	3.81	4.01	
A_1	0.40	0.50	0.60	
A_2	3.11	3.31	3.51	
A_3	0.94	1.04	1.14	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	–	–	0.20	
bbb	–	–	0.35	
ddd	–	–	0.25	
eee	–	–	0.10	
M		39		2

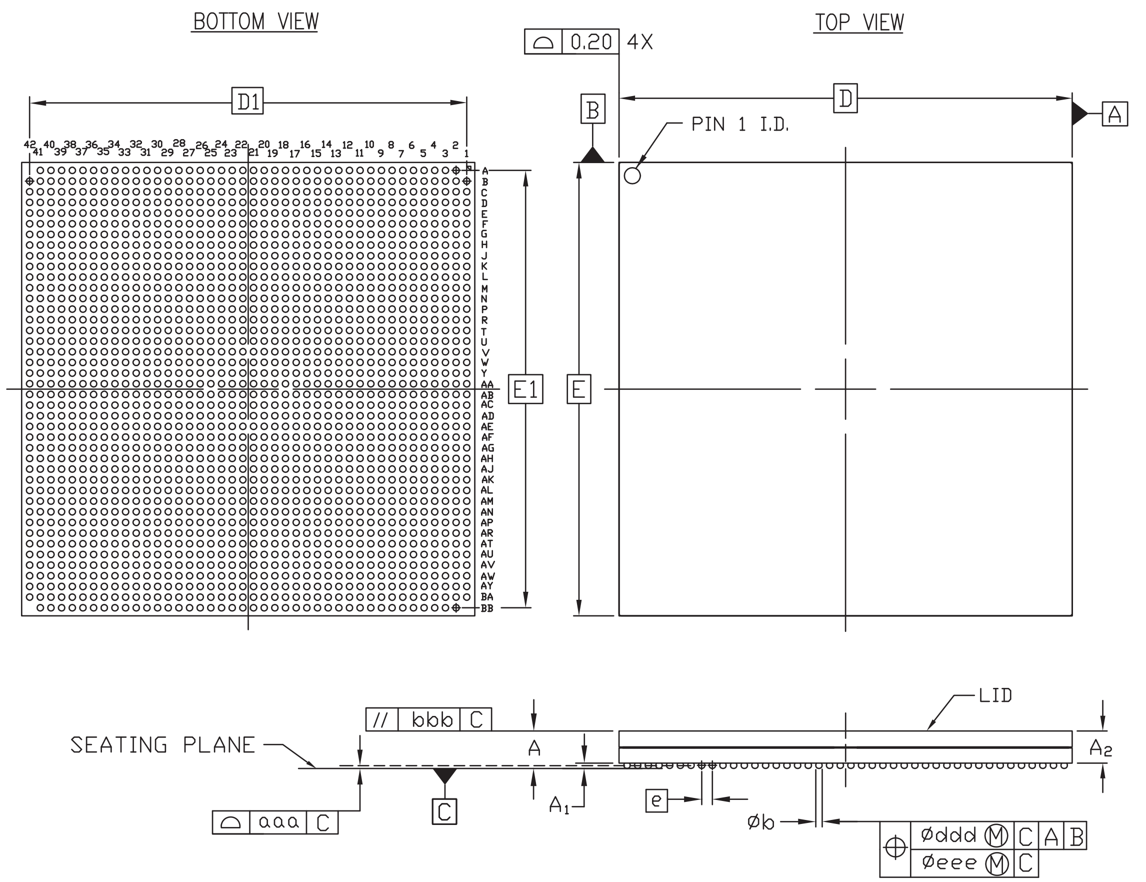
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–318 P40.0x40.0–EF–1521 (DEPOPULATED)

ug1075_fsvg1517_030618

Figure 5-13: **Package Dimensions for FSVG1517 (XCZU25DR, XCZU27DR, and XCZU28DR)**

FFVC1760 and FFVD1760 Flip-Chip, Fine-Pitch BGA (XCZU11EG, XCZU17EG, and XCZU19EG)



FFVC1760 – Sn/Ag/Cu SOLDER BALLS
FFVD1760 – Sn/Ag/Cu SOLDER BALLS

SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	42			2

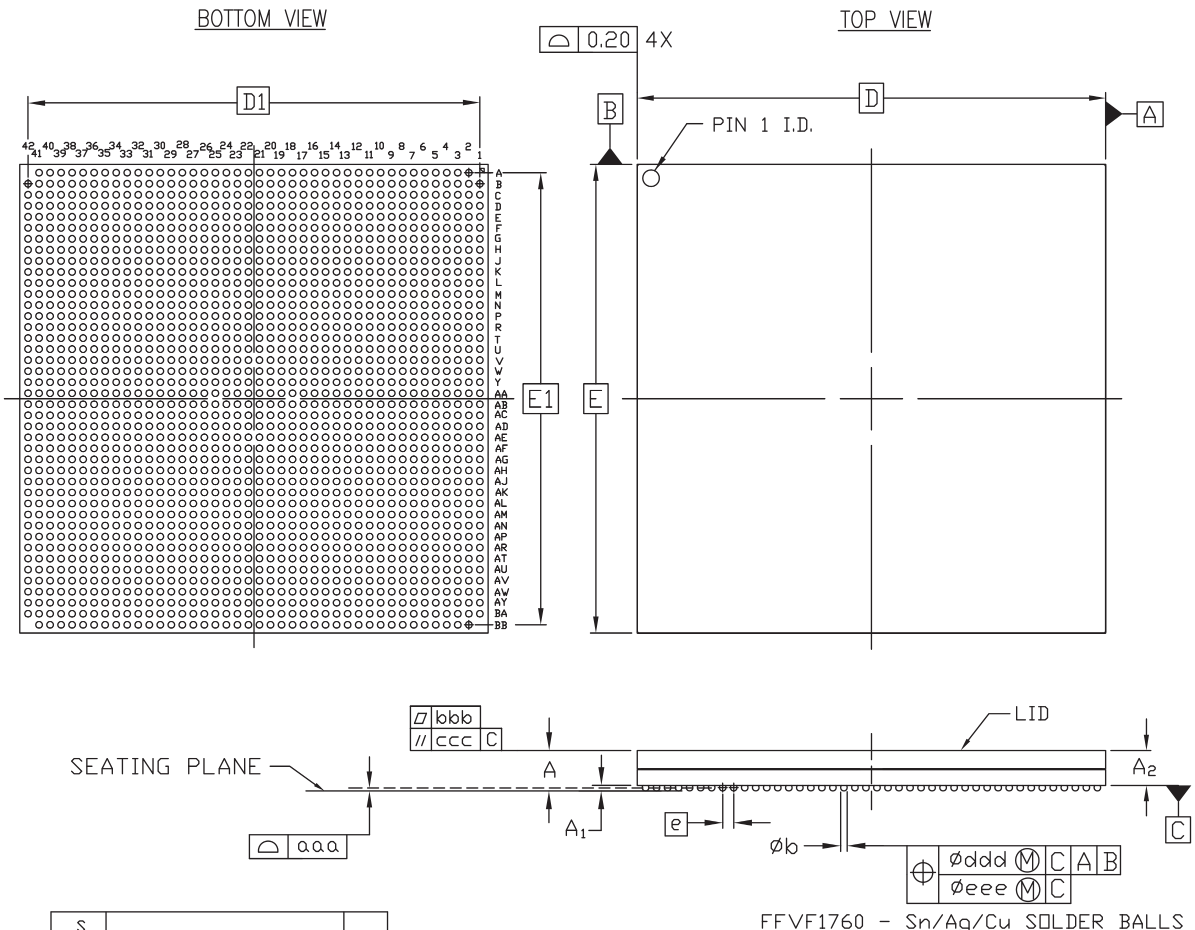
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

ug1075_c5_073116

Figure 5-14: **Package Dimensions for FFVC1760 and FFVD1760 (XCZU11EG, XCZU17EG, and XCZU19EG)**

FFVF1760 (XCZU29DR) Flip-Chip, Fine-Pitch BGA



SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	3.46	3.66	3.86	
A_1	0.40	0.50	0.60	
A_2	2.96	3.16	3.36	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.10	
ccc	~	~	0.10	
ddd	~	~	0.25	
eee	~	~	0.10	
M	42			2

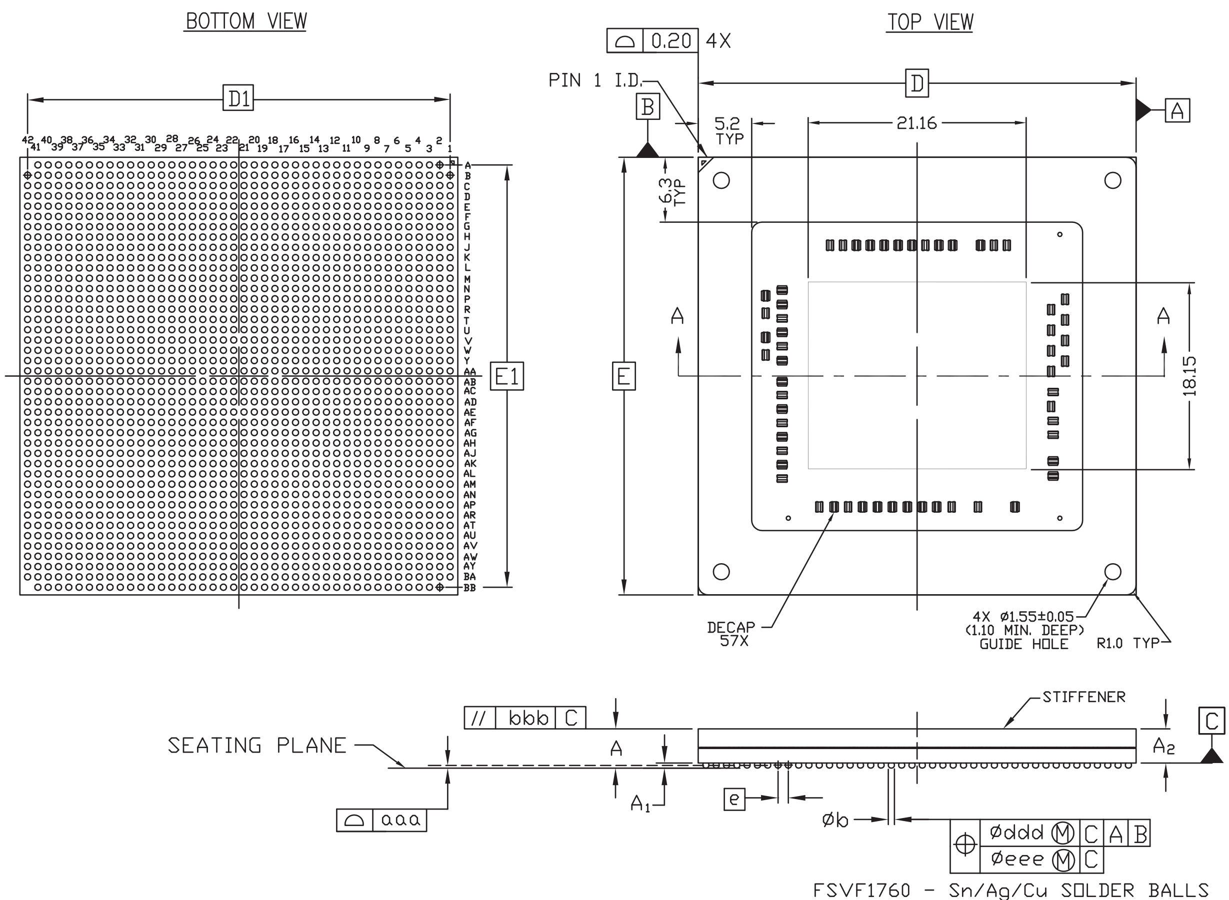
NOTES:

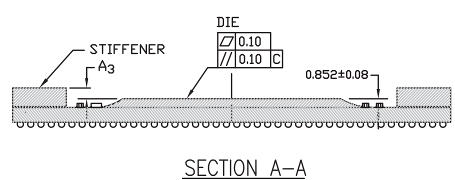
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

ug1075_ffvf1760_030518

Figure 5-15: **Package Dimensions for FFVF1760 (XCZU29DR)**

FSVF1760 (XCZU29DR) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring BGA





SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.61	3.81	4.01	
A_1	0.40	0.50	0.60	
A_2	3.11	3.31	3.51	
A_3	0.94	1.04	1.14	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.35	
ddd	~	~	0.25	
eee	~	~	0.10	
M	42			2

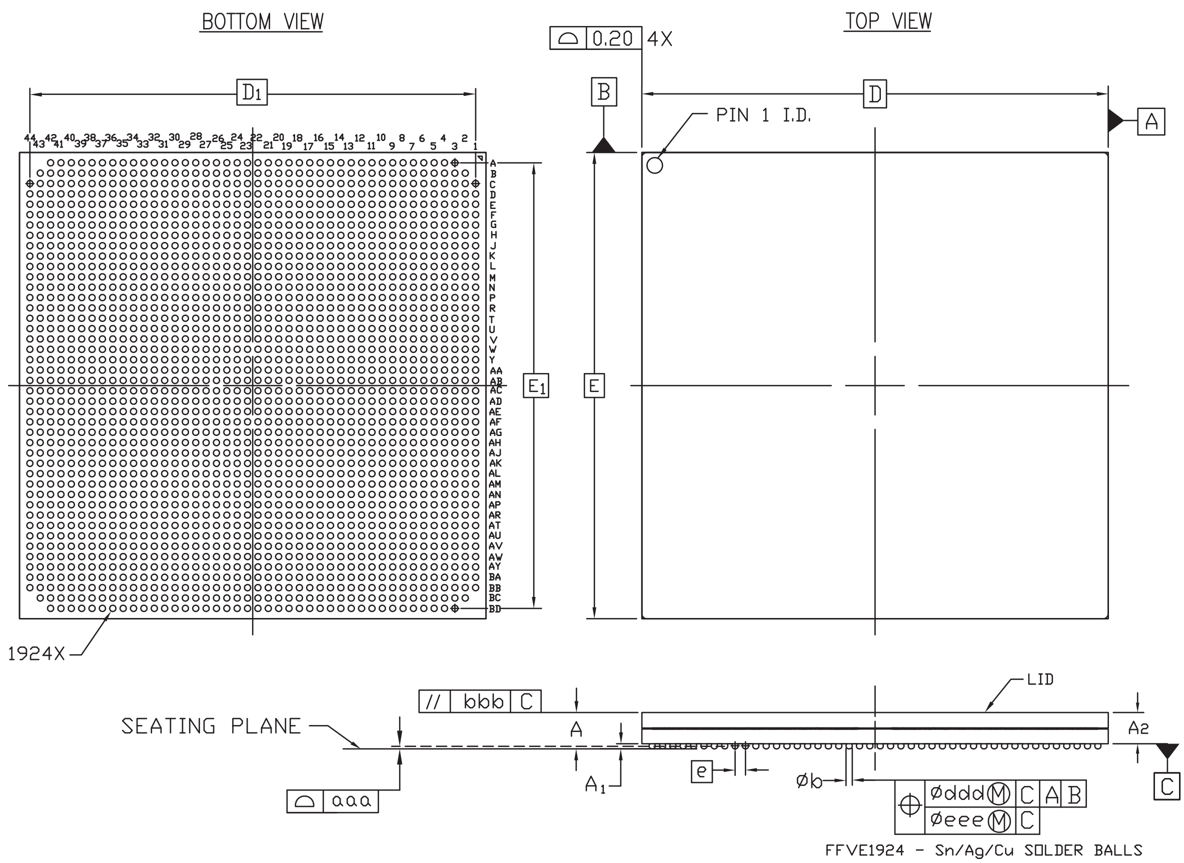
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–318 P42.5x42.5–EF–1764 (DEPOPULATED)

ug1075_fsvf1760_030618

Figure 5-16: **Package Dimensions for FSVF1760 (XCZU29DR)**

FFVE1924 Flip-Chip, Fine-Pitch BGA (XCZU17EG, and XCZU19EG)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	3
aaa	~	~	0.20	
bbb	~	~	0.10	
ddd	~	~	0.25	
eee	~	~	0.10	
M	44			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

Figure 5-17: **Package Dimensions for FFVE1924 (XCZU17EG and XCZU19EG)**

Package Marking

Introduction

The package top-markings for the Zynq® UltraScale+™ devices are similar to the examples shown in Figure 6-1. There are two top markings, the first was In addition to the markings explained in Table 6-1, refer to the *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424) [Ref 15].

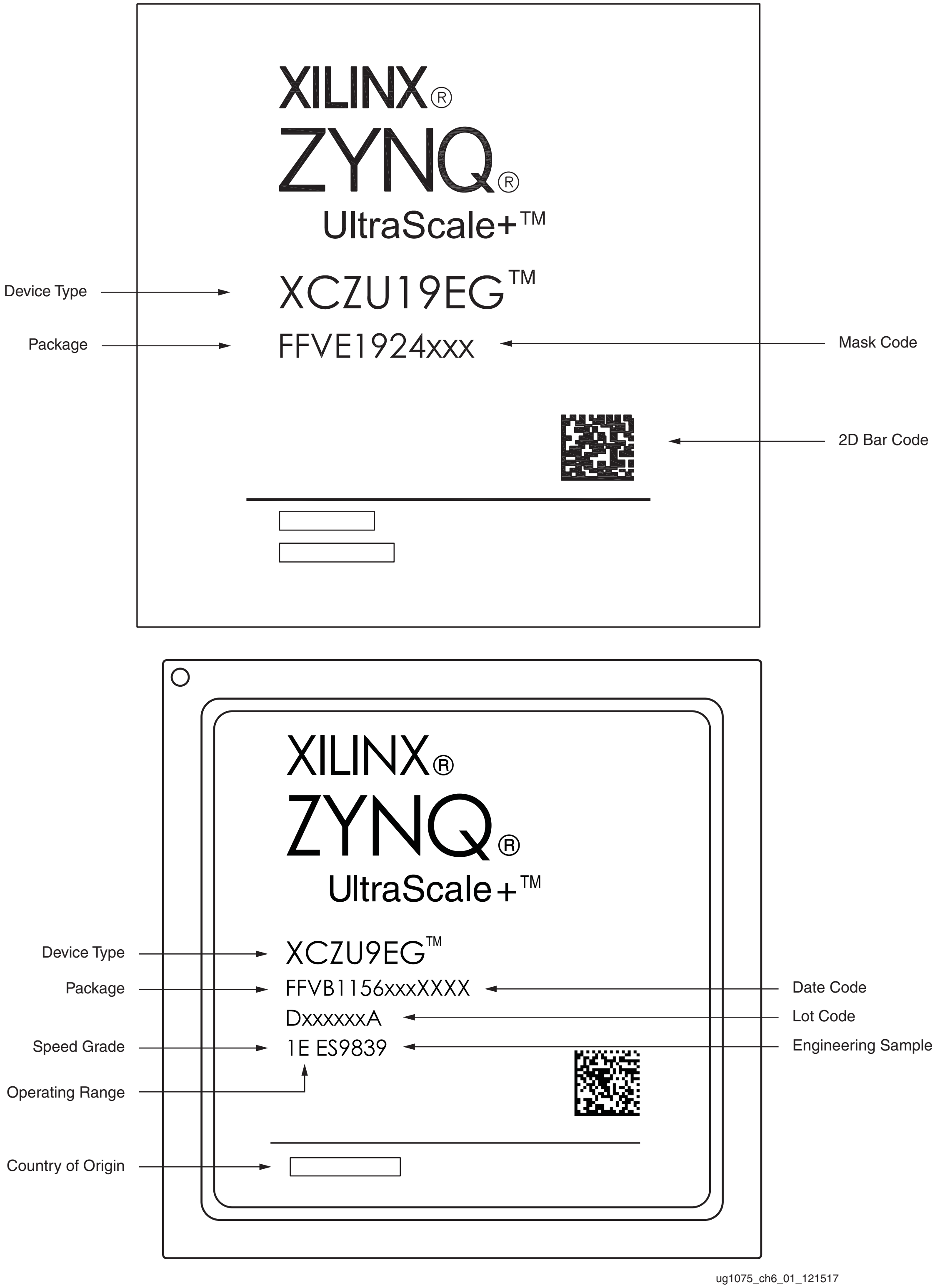


Figure 6-1: **Zynq UltraScale+ Devices Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

<table>
<tr><th>Item</th><th colspan="2">Definition</th></tr>
<tr><td>Xilinx Logo</td><td colspan="2">Xilinx logo, Xilinx name with trademark, and trademark-registered status.</td></tr>
<tr><td>Family Brand Logo</td><td colspan="2">Device family name with trademark and trademark-registered status. This line is optional and could appear blank.</td></tr>
<tr><td>1st Line</td><td colspan="2">Device name.</td></tr>
<tr><td>2nd Line</td><td colspan="2">• Package code: FF
1st digit: F for flip-chip BGA, S for flip-chip BGA with 0.8 mm ball pitch.
2nd digit: F for lidded, B for bare-die.
• 3rd digit: Pb-free code: V for RoHS 6/6.
All Zynq UltraScale+ devices have Pb-free RoHS compliant packaging. For more details on Xilinx Pb-free and RoHS compliant products, see: www.xilinx.com/pbfree.
• 4th digit: This is the pin out (net list) identifier.
• 5th–8th digits: These are the physical pin count identifiers: B1156 is shown in the Figure 6-1 example marking drawing. Example: A package code of FFVB1517 and FFVF1517 means they have a different pinout (net list) but the same physical ball count and physical dimensions.
• Three letter circuit design revision, the location code for the wafer fab, and the geometry code (xxx).
• When marked, the date code: YYWW. This code is not marked on some devices. Refer to the bar code for more information.</td></tr>
<tr><td>3rd Line</td><td colspan="2">When marked, this line describes ten alphanumeric characters for assembly location, 7-digit lot number, and step information. The last digit is usually an A or an M if a stepping version does not exist.
This line is not marked on some devices. Refer to the bar code for more information.</td></tr>
<tr><td rowspan="4">4th Line</td><td colspan="2">When marked, this line describes the device speed grade (1) and temperature operating range (E). When not marked on the package, the product is considered to operate at the extended (E) temperature range. If a bar code is present on the device, the 4th line might be blank or unmarked. In this case, refer to the bar code for speed grade and temperature range information. For more information on the ordering codes, see the Zynq UltraScale+ MPSoC Overview (DS891) [Ref 1].
Other variations for the 4th line:</td></tr>
<tr><td>L1I</td><td>The L1I indicates a -1LI device. The -1LI speed grade offers reduced maximum power consumption. For more information, see the Zynq UltraScale+ MPSoC data sheet [Ref 6].</td></tr>
<tr><td>1E xxxx</td><td>The xxxx indicates a 4-digit SCD device option. An SCD is a special ordering code that is not always marked in the device top mark.</td></tr>
<tr><td>1E ES
2I ES
L1I ES</td><td>The addition of an ES after the operating temperature range code indicates an engineering sample.</td></tr>
<tr><td>Bar Code</td><td colspan="2">A device-specific bar code is marked on each device. Refer to the FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products (XTP424) [Ref 15].</td></tr>
</table>

Packing and Shipping

Introduction

Zynq® UltraScale+™ devices are packed in trays. Trays are used to pack most of Xilinx surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using antistatic material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C. The maximum operating temperature is 140°C.

Table 7-1: **Standard Device Counts per Tray and Box**

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
SBVA484	84	420
SFVA625	60	300
SFVC784	60	300
FBVB900	27	135
FFVC900	27	135
FFVB1156, FFVC1156, FFVD1156, and FFVE1156	24	120
FSVE1156	24	72
FFVB1517 and FFVF1517	21	105
FFVG1517	21	63
FSVG1517	21	63
FFVC1760, FFVD1760, and FFVF1760	12	60
FSVF1760	12	36
FFVE1924	12	36

Soldering Guidelines

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the Pb-free solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

RECOMMENDED: *Xilinx recommends that customers qualify their custom PCB assembly processes using package samples.*

The primary phases of the Pb-free reflow process are:

- Melting the particles in the solder paste
- Wetting the surfaces to be joined
- Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages (220°C for eutectic packages), and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

IMPORTANT: *Following the initial reflow process, devices should not be reworked more than once. Any additional rework beyond that is likely to cause irreparable damage to the device.*

Pb-Free Reflow Soldering

Xilinx uses SnAgCu solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

Xilinx does not recommend soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

Table 8-1 and Figure 8-1 provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders (Figure 8-1). This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for the Sn/Pb system. SnAgCu alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to Table 8-1 for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 8-1: **Pb-Free Reflow Soldering Guidelines**

Profile Feature	Convection, IR/Convection
Ramp-up rate	2°C/s maximum. 1°C/s maximum for lidless packages with stiffener ring.
Preheat temperature 150°–200°C	60–120 seconds.
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical).
Time within 5°C of actual peak temperature	30 seconds maximum.
Peak temperature (lead/ball)	230°C—245°C typical (depends on solder paste, board size, component mixture).
Peak temperature (body)	240°C—250°C, package body size dependent (see the *Zynq UltraScale+ MPSoC data sheet* (DS925) [Ref 6]).
Ramp-down rate	2°C/s maximum.
Time 25°C to peak temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum.

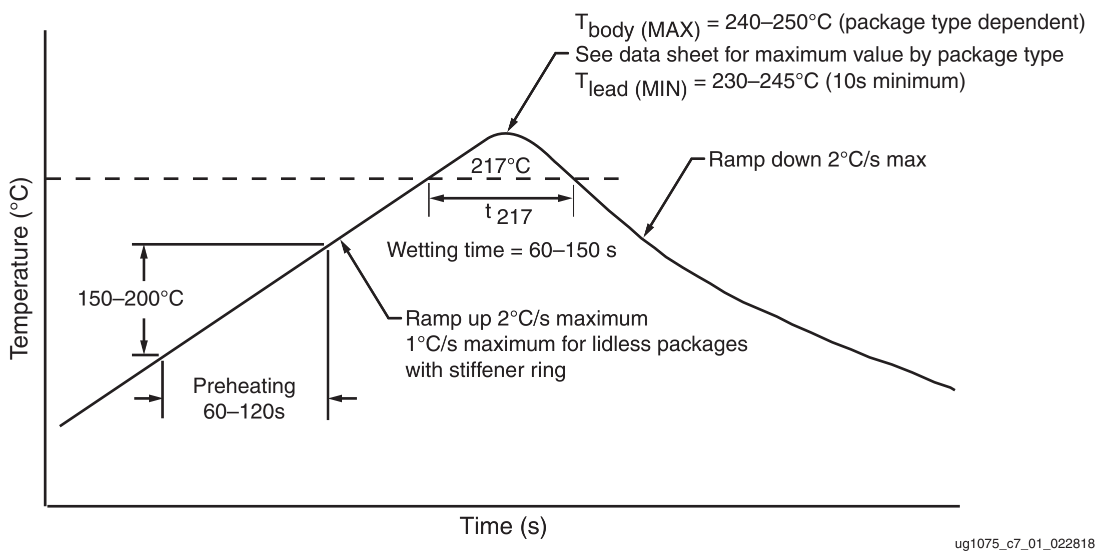


Figure 8-1: **Typical Conditions for Pb-Free Reflow Soldering**

Table 8-2: **Peak Package Reflow Body Temperature for Xilinx Pb-Free Packages (Based on J-STD-020 Standard)**

Package		Peak Package Reflow Body Temperature[(1)]	JEDEC Moisture Sensitivity Level (MSL)
BGA			
Flip-Chip	SBVA484 SFVA625 SFVC784	Mass reflow: 250°C Dry rework: 260°C	4
	FBVB900, FFVC900 FFVB1156, FFVC1156 FFVB1517, FFVF1517 FFVC1760, FFVD1760 FFVE1924	Mass reflow: 245°C Dry rework: 260°C	4
	FFVD1156, FFVE1156 FFVG1517 FFVF1760	Mass reflow: 245°C Dry rework: 260°C	4
	FSVE1156 FSVG1517 FSVF1760	Mass reflow: 240°C Dry rework: 260°C	4

Notes:
1. See the specific *Zynq UltraScale+ MPSoC data sheet* [Ref 6] for the most up-to-date specifications.

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than 1°C/s during the preheating and soaking stages, in combination with a heating rate of not more than 3°C/s throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, Xilinx recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

Conformal Coating

Xilinx has no information about the reliability of flip-chip BGA packages on a board after exposure to conformal coating. Any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

IMPORTANT: *When a conformal coating is required, Parylene-based material should be used to avoid potential risk of weakening the lid adhesive used in Xilinx packages.*

Recommended PCB Design Rules for BGA Packages

BGA Packages

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure 9-1 and summarized in Table 9-1 for 1.0 mm pitch packages. For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 9-1. An example of an NSMD PCB pad solder joint is shown in Figure 9-2. It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

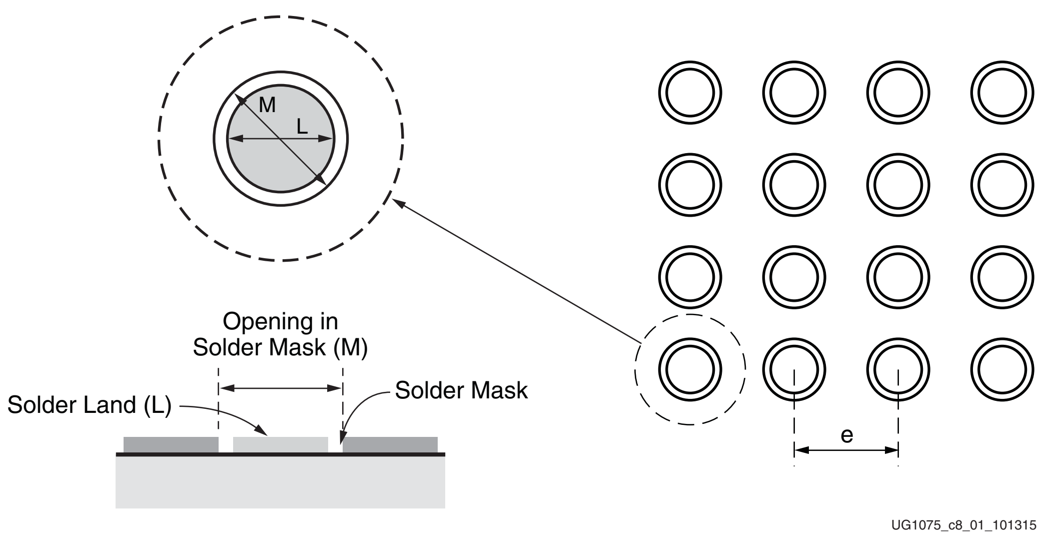


Figure 9-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

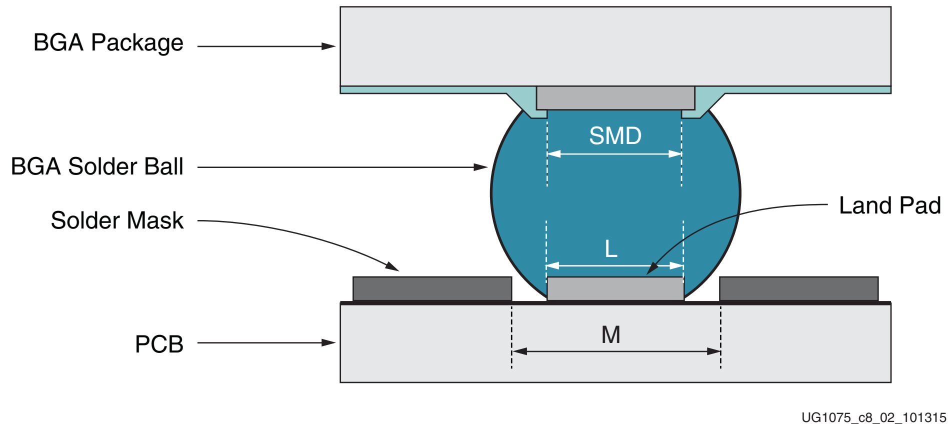


Figure 9-2: **Example of an NSMD PCB Pad Solder Joint**

Table 9-1: **BGA Package Design Rules**

Flip-Chip BGA Packages	1.0 mm Pitch	0.8 mm Pitch
Design Rule	**Dimensions in mm (mils)**	
Package land pad opening (SMD)	0.53 mm (20.9 mils)	0.40 mm (15.7 mils)
Maximum PCB solder land (L) diameter	0.53 mm (20.9 mils)	0.40 mm (15.7 mils)
Opening in PCB solder mask (M) diameter	0.63 mm (24.8 mils)	0.50 mm (19.7 mils)
Solder ball land pitch (e)	1.00 mm (39.4 mils)	0.80 mm (31.5 mils)

Notes:

1. Controlling dimension in mm.

Thermal Specifications

Introduction

Zynq® UltraScale+™ devices are offered exclusively in thermally efficient flip-chip BGA packages. These flip-chip packages range in pin-count from the smaller 19 x 19 mm SBVA484 to the 45 x 45 mm FFVE1924. This suite of packages is used to address the various power requirements of the Zynq UltraScale+ devices. Zynq UltraScale+ devices are implemented in the 16 nm process technology.

Unlike features in an ASIC, the combination of Zynq UltraScale+ device features used in a user application is not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given Zynq UltraScale+ device when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Zynq UltraScale+ devices are supported similarly to previous products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. Your design's operating conditions dictate the appropriate solution.

Thermal Resistance Data

Table 10-1 shows the thermal resistance data for Zynq UltraScale+ devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

IMPORTANT: *The data in Table 10-1 is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.*

TIP: *The thermal data query for all available devices by package is available on the Xilinx website:* www.xilinx.com/cgi-bin/thermal/thermal.pl.

Table 10-1: **Thermal Resistance Data**

Package	Package Body Size	Devices	θ_{JB}[1] (°C/W)	θ_{JC}[1] (°C/W)	θ_{JA}[1] (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)[2]		
						@250 LFM	@500 LFM	@750 LFM
SBVA484	19 x 19	XCZU2	2.46	0.06	14.9	11.5	9.6	8.9
		XCZU3	2.46	0.06	14.9	11.5	9.6	8.9
		XAZU2EG	2.46	0.06	14.9	11.5	9.6	8.9
		XAZU3EG	2.46	0.06	14.9	11.5	9.6	8.9
SFVA625	21 x 21	XCZU2	2.22	0.38	13.2	9.9	8.3	7.8
		XCZU3	2.22	0.38	13.2	9.9	8.3	7.8
		XAZU2EG	2.22	0.38	13.2	9.9	8.3	7.8
		XAZU3EG	2.22	0.38	13.2	9.9	8.3	7.8
SFVC784	23 x 23	XCZU2	2.67	0.50	12.8	9.2	7.8	7.2
		XCZU3	2.67	0.50	12.8	9.2	7.8	7.2
		XCZU4	2.28	0.27	12.2	8.9	7.4	7.0
		XCZU5	2.28	0.27	12.2	8.9	7.4	7.0
		XAZU2EG	2.28	0.27	12.2	8.9	7.4	7.0
		XAZU3EG	2.28	0.27	12.2	8.9	7.4	7.0
FBVB900	31 x 31	XCZU4	2.62	0.04	9.6	6.3	5.3	5.0
		XCZU5	2.62	0.04	9.6	6.3	5.3	5.0
		XCZU7	2.32	0.03	9.2	6.1	5.1	4.8
FFVC900	31 x 31	XCZU6	2.33	0.25	9.2	6.1	5.1	4.9
		XCZU9	2.33	0.25	9.2	6.1	5.1	4.9
		XCZU15	2.25	0.18	9.1	6.1	5.1	4.8
FFVB1156	35 x 35	XCZU6	2.40	0.20	8.3	5.3	4.5	4.2
		XCZU9	2.40	0.20	8.3	5.3	4.5	4.2
		XCZU15	2.09	0.23	7.9	5.1	4.3	4.1
FFVC1156	35 x 35	XCZU7	2.39	0.21	8.3	5.3	4.5	4.2
		XCZU11	2.20	0.16	8.0	5.2	4.3	4.1
FFVD1156	35 x 35	XCZU21DR	1.94	0.16	7.8	5.1	4.2	4.0
FFVE1156	35 x 35	XCZU25DR	1.94	0.16	7.8	5.1	4.2	4.0
		XCZU27DR	1.94	0.16	7.8	5.1	4.2	4.0
		XCZU28DR	1.94	0.16	7.8	5.1	4.2	4.0
FSVE1156	35 x 35	XCZU25DR	2.40	0.02	8.3	5.3	4.4	4.2
		XCZU27DR	2.40	0.02	8.3	5.3	4.4	4.2
		XCZU28DR	2.40	0.02	8.3	5.3	4.4	4.2

Table 10-1: **Thermal Resistance Data *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB}[(1)] (°C/W)	θ_{JC}[(1)] (°C/W)	θ_{JA}[(1)] (°C/W)	$\theta_{JA\text{-Effective}}$ (°C/W)[(2)]		
						@250 LFM	@500 LFM	@750 LFM
FFVB1517	40 x 40	XCZU11	2.22	0.16	7.1	4.4	3.7	3.5
		XCZU17	2.17	0.11	7.0	4.4	3.7	3.5
		XCZU19	2.17	0.11	7.0	4.4	3.7	3.5
FFVF1517	40 x 40	XCZU7	2.38	0.21	7.3	4.5	3.8	3.6
		XCZU11	2.22	0.16	7.1	4.4	3.7	3.5
FFVG1517	40 x 40	XCZU25DR	1.93	0.16	6.8	4.3	3.6	3.4
		XCZU27DR	1.93	0.16	6.8	4.3	3.6	3.4
		XCZU28DR	1.93	0.16	6.8	4.3	3.6	3.4
FSVG1517	40 x 40	XCZU25DR	2.43	0.02	7.3	4.5	3.8	3.6
		XCZU27DR	2.43	0.02	7.3	4.5	3.8	3.6
		XCZU28DR	2.43	0.02	7.3	4.5	3.8	3.6
FFVC1760	42.5 x 42.5	XCZU11	1.96	0.14	6.4	4.0	3.3	3.2
		XCZU17	1.77	0.10	6.3	3.9	3.2	3.1
		XCZU19	1.77	0.10	6.3	3.9	3.2	3.1
FFVD1760	42.5 x 42.5	XCZU17	1.77	0.10	6.3	3.9	3.2	3.1
		XCZU19	1.77	0.10	6.3	3.9	3.2	3.1
FFVF1760	42.5 x 42.5	XCZU29DR	2.04	0.17	6.5	4.0	3.3	3.2
FSVF1760	42.5 x 42.5	XCZU29DR	2.47	0.02	7.0	4.3	3.5	3.6
FFVE1924	45 x 45	XCZU17	1.77	0.10	5.9	3.6	3.0	2.9
		XCZU19	1.77	0.10	5.9	3.6	3.0	2.9

Notes:

1. This data is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.
2. All $\theta_{JA\text{-Effective}}$ values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The Xilinx power estimation tools (Vivado® Power Analysis, and Xilinx Power Estimator), which require detailed board dimensions and layer counts, are useful for deriving more precise $\theta_{JA\text{-Effective}}$ values.

Support for Thermal Models

Table 10-1 provides the traditional thermal resistance data for Zynq UltraScale+ devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect your actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required.

Though Xilinx continues to support these figures of merit data, for Zynq UltraScale+ devices, boundary conditions independent thermal resistor network (Delphi) models are offered for all Zynq UltraScale+ devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 10-1.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi models are available for download on the Xilinx website (under the Device Model tab).

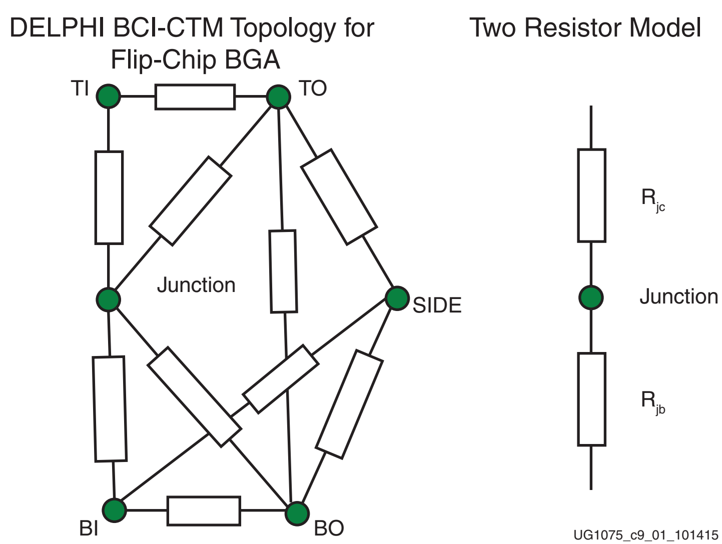


Figure 10-1: **Thermal Model Topologies**

RECOMMENDED: *Xilinx recommends the use of the Delphi thermal model. Xilinx also recommends a best practice review of manufacturing variations on the thermal performance of the device from both the thermal interface material parameters and thermal solution variations. Examples of manufacture variations include the tolerance in airflow from a fan, the tolerance on performance of the heat pipe and vapor chamber, and manufacturing variations of the attachment of fins to the heat-sink base and the flatness of the surface.*

Chapter 11

Thermal Management Strategy

Introduction

As described in this section, Xilinx relies on a multi-pronged approach to consuming less power and dissipating heat for systems using Zynq® UltraScale+™ devices.

Flip-Chip Packages

Zynq UltraScale+ devices are offered in flip-chip BGA packages, which present a low thermal path. With the exception of the bare-die packages, the flip-chip BGA packages incorporate a heat spreader with an additional thermal interface material (TIM), as shown in Figure 11-1.

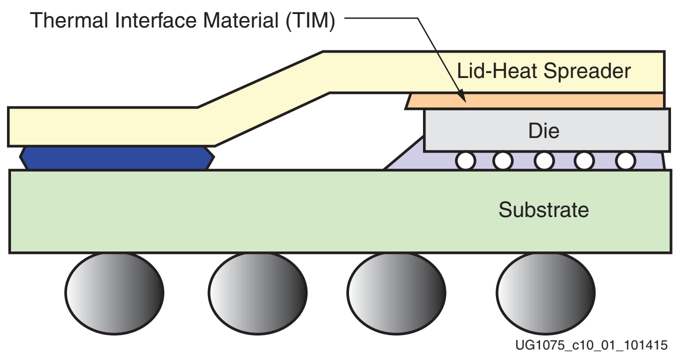


Figure 11-1: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process deliver low thermal resistance to the heat spreader.

A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity.

System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

By considering the system's physical, mechanical, and environmental constraints, the overall thermal budget is maintained and does not exceed the device's maximum operating temperature. The heat sink is an integral part of the thermal management solution to maintain a safe operating temperature. As a result, the system-level designer must be aware of the following:

- For lidless packages, the nominal stiffener height can be different from the height of the die. Therefore, the heat sink must have an island to contact the die.
- Especially for lidless packages, Xilinx advises against direct use of the θ_{JC} parameters (see Table 10-1) to determine the thermal performance of the device in your application. The calculation of these parameters are done in accordance with the JEDEC standard JESD51 where system parameters differ greatly from most applications. Instead, run thermal simulations of the system in worst-case environmental conditions using Delphi thermal models, which more accurately represent the device thermal performance under all boundary conditions.
- Consider the mechanical specifications of the package as well as the selection of the thermal interface between the die and the thermal management solution to ensure the lowest thermal contact resistance.
- The total thermal contact of the thermal interface material is determined based on parameters from the thermal interface supplier's data sheet.
- See the applied pressure recommendation on page 191. Lower pressure runs the risk of poor thermal contact and higher pressure runs the risk of damaging the device; therefore, strict control of pressure is required.
- Consider all uncertainties in thermal modeling, including manufacturing variations from the thermal solutions (for example, fan airflow tolerance, heat pipe or vapor chamber performance tolerance, variation of the attachment of fins to heat sink base, and surface flatness).

Thermal Interface Material

When installing heat sinks for Zynq UltraScale+ devices, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGA and lidded flip-chip BGAs are different. Xilinx recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an Zynq UltraScale+ device unless there is good physical contact between the base of the heat sink and the top of the Zynq UltraScale+ device. The surfaces of both the heat sink and the Zynq UltraScale+ device silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the Zynq UltraScale+ device die and the heat sink.

The selection of the thermal interface (TIM) between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.
2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in step 1 and step 2, which are published in the data sheet of the thermal interface supplier.

Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase change material
- Thermal paste
- Thermal adhesives
- Thermal tape

Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- Thermal Conductivity of the Material
- Electrical Conductivity of the Material
- Spreading Characteristics of the Material
- Long-Term Stability and Reliability of the Material
- Ease of Application
- Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the Zynq UltraScale+ device die itself, but other elements on the Zynq UltraScale+ device or motherboard can be at risk if they become contaminated by the compound. For this reason, Xilinx does not recommend the use of electrically conductive thermal interface material.

Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the Zynq UltraScale+ device and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the Zynq UltraScale+ device. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on bare-die devices.

Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

RECOMMENDED: *Xilinx recommends that the applied pressure on the package be in the range of 20 to 40 PSI for optimum performance of the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure (in the 20 to 40 PSI range) for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package (with the thermal solution to pass all mechanical stress and vibration qualification tests).*

RECOMMENDED: *Xilinx recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See Figure 11-2.*

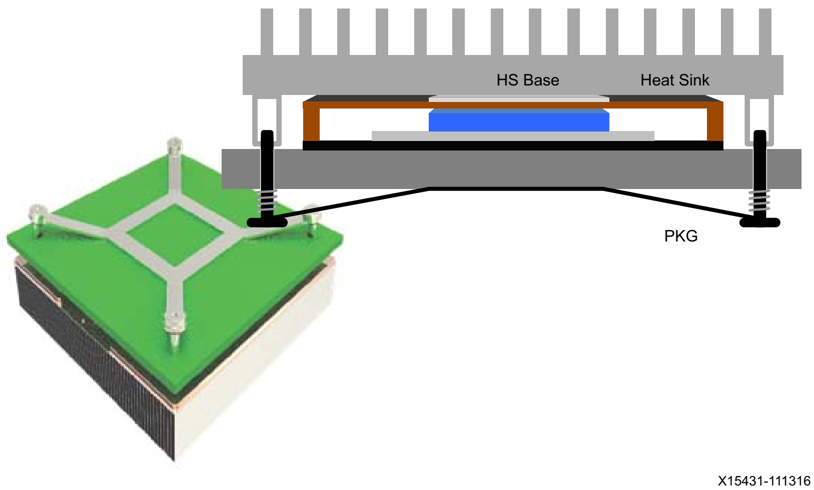


Figure 11-2: **Dynamic Mounting and Bracket Clips on Heat Sink Attachment**

Heat Sink Removal

When removing or reworking heat sinks, the phase-change material residue must be removed from the surface of the die. Laird Technologies, Inc. provides the following guidance for complete removal of the phase-change material from the component.

Instructions for Removal of Phase-change Material

1. Separate the Components
2. Scrape Away Thick Residue
3. Clean Remaining Residue with Solvent
4. Working with Laird Material

Separate the Components

At room temperature, if possible, use a back and forth twisting motion to break the bond between the phase-change thermal interface material and mated components (i.e., heat sink and Zynq UltraScale+ device). See Figure 11-3.

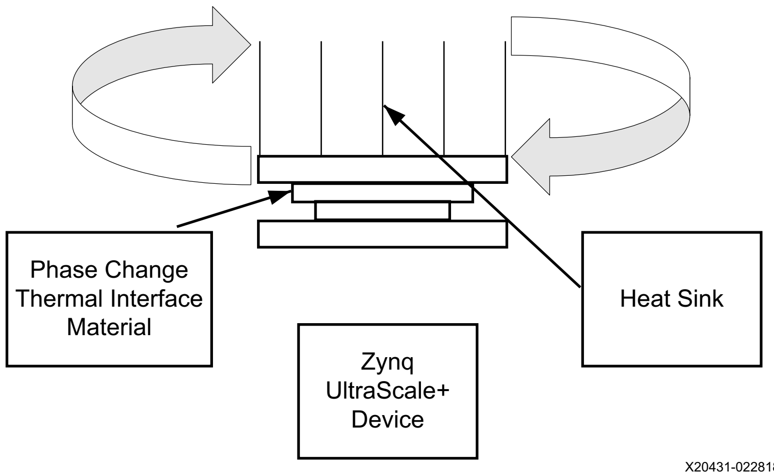


Figure 11-3: **Breaking the Bond between Thermal Interface Material and Mated Components**

For smaller components (typically 15 mm x 15 mm or less), the bond usually breaks free easily at room temperature. For larger components, in situations where minimal movement is available, or if using fragile components, heat the component (preferred) or heat sink to about 40°C–60°C before removal.

The guideline is 40°C–60°C, however, you might find that for your application, heating to 35°C is adequate. You might prefer to heat to 70°C which makes the phase-change thermal interface material very soft and the components can be easily separated.

Scrape Away Thick Residue

For a faster clean-up once components are separated, scrape away any large residual material amounts with a plastic spatula or a wooden tongue depressor. A clean dry rag can be used to wipe away excess material.

Clean Remaining Residue with Solvent

Using a clean cloth/wipe, wet it with your choice of solvent (see the following list) and wipe away any remaining residue.

- Toluene (easiest)
- Acetone (very good)
- Isoparaffinic hydrocarbon: Isopar, Soltrol (trade names) (very good)
- Isopropyl alcohol (OK)

Working with Laird Material

Safe handling, disposal, and first-aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website, www.lairdtech.com.

Measurement Debug

When performing in-system thermal testing, to ensure accurate data and not incur damage to the device, do not place a thermocouple in between the device and the heat sink. On the extreme side, it might cause additional mechanical and/or thermal stress to the device, leading to damage. Even if damage does not occur, it often leads to a thicker and or uneven thermal interface material thickness, leading to a thermal performance difference from a system without a thermocouple. To obtain the device temperature, use the System Monitor as a non-invasive means to get accurate device measurements while debugging the system.

Heat Sink Guidelines for Bare-die Flip-Chip Packages

Heat Sink Attachments for Bare-die FB Packages

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure 12-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

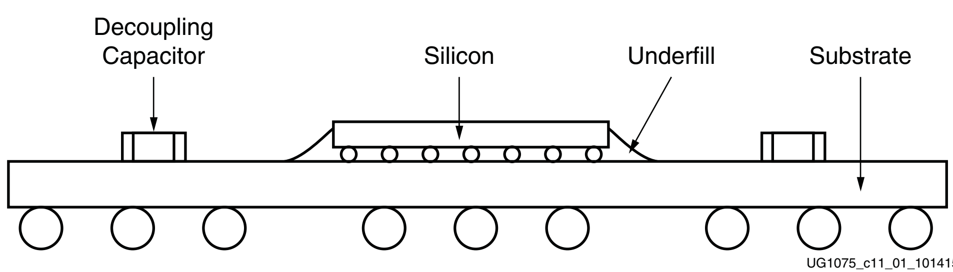


Figure 12-1: **Cross Section of Bare-die Flip-chip BGA**

Types of Heat Sink Attachments

There are six main methods for heat sink attachment. Table 12-1 lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

Table 12-1: **Heat Sink Attachment Methods**

Attachment Method	Advantages	Disadvantages
Thermal tape	• Generally easy to attach and is inexpensive. • Lowest cost approach for aluminum heat sink attachment. • No additional space required on the PCB.	• The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly. • Because of the small contact area, the tape might not provide sufficient bond strength. • Tape is a moderate to low thermal conductor that could affect the thermal performance.
Thermally conductive adhesive or glue	• Outstanding mechanical adhesion. • Fairly inexpensive, costs a little more than tape. • No additional space required on the PCB.	• Adhesive application process is challenging and it is difficult to control the amount of adhesive to use. • Difficult to rework. • Because of the small contact area, the adhesive might not provide sufficient bond strength.
Wire form Z-clips	• It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary. • Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device). • It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance.	• Requires additional space on the PCB for anchor locations.

Table 12-1: **Heat Sink Attachment Methods *(Cont'd)***

Attachment Method	Advantages	Disadvantages
Plastic clip-ons	• Suitable for designs where space on the PCB is limited. • Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board. • Can provide a strong enough mechanical attachment to pass shock and vibration test.	• Needs a keep out area around the silicon devices to use the clip. • Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.
Threaded stand-offs (PEMs) and compression springs	• Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis. • Suitable for high mass heat sinks. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Holes are required in the PCB taking valuable space that can be used for trace lines. • Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.
Push-pins and compression springs	• Provides a stable attachment to a heat source and transfers load to the PCB. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Requires additional space on the PCB for push-pin locations.

Heat Sink Attachment

Component Pick-up Tool Consideration

For pick-and-place machines to place bare-die flip-chip BGAs onto PCBs, Xilinx recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure 12-2).

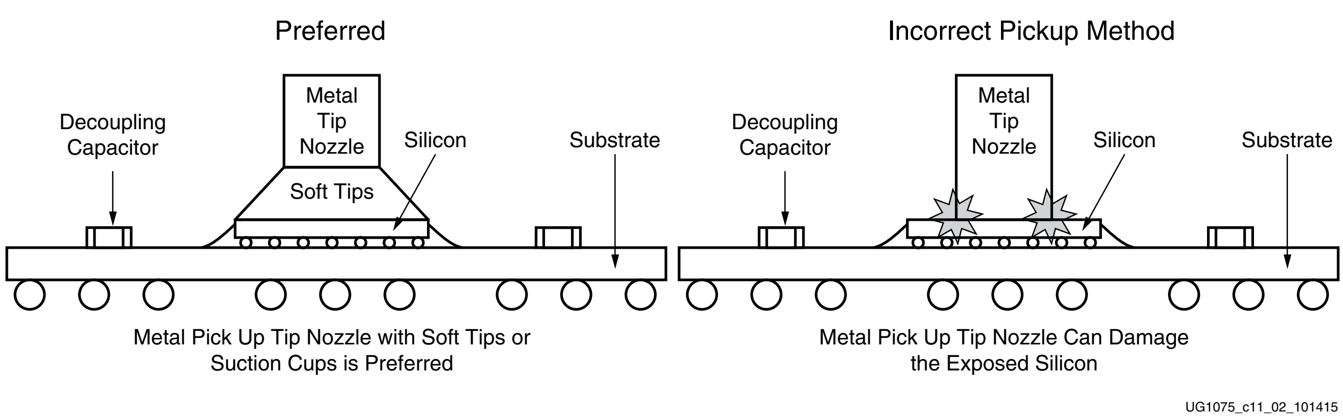


Figure 12-2: **Recommended Method For Using Pick-up Tools**

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the bare-die package, the factors in Table 12-2 must be carefully considered (see Figure 12-3).

Table 12-2: **Heat Sink Attachment Considerations**

Consideration(s)	Effect(s)	Recommendation(s)
In heat sink attach process, what factors can cause damage to the exposed die and passive capacitors?	• Uneven heat sink placement • Uneven TIM thickness • Uneven force applied when placing heat sink placement	• Even heat sink placement • Even TIM thickness • Even force applied when placing heat sink placement
Does the heat sink tilt or tip the post attachment?	Uneven heat sink placement will damage the silicon and can cause field failures.	• Careful handling not to contact the heat sink with the post attachment. • Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.

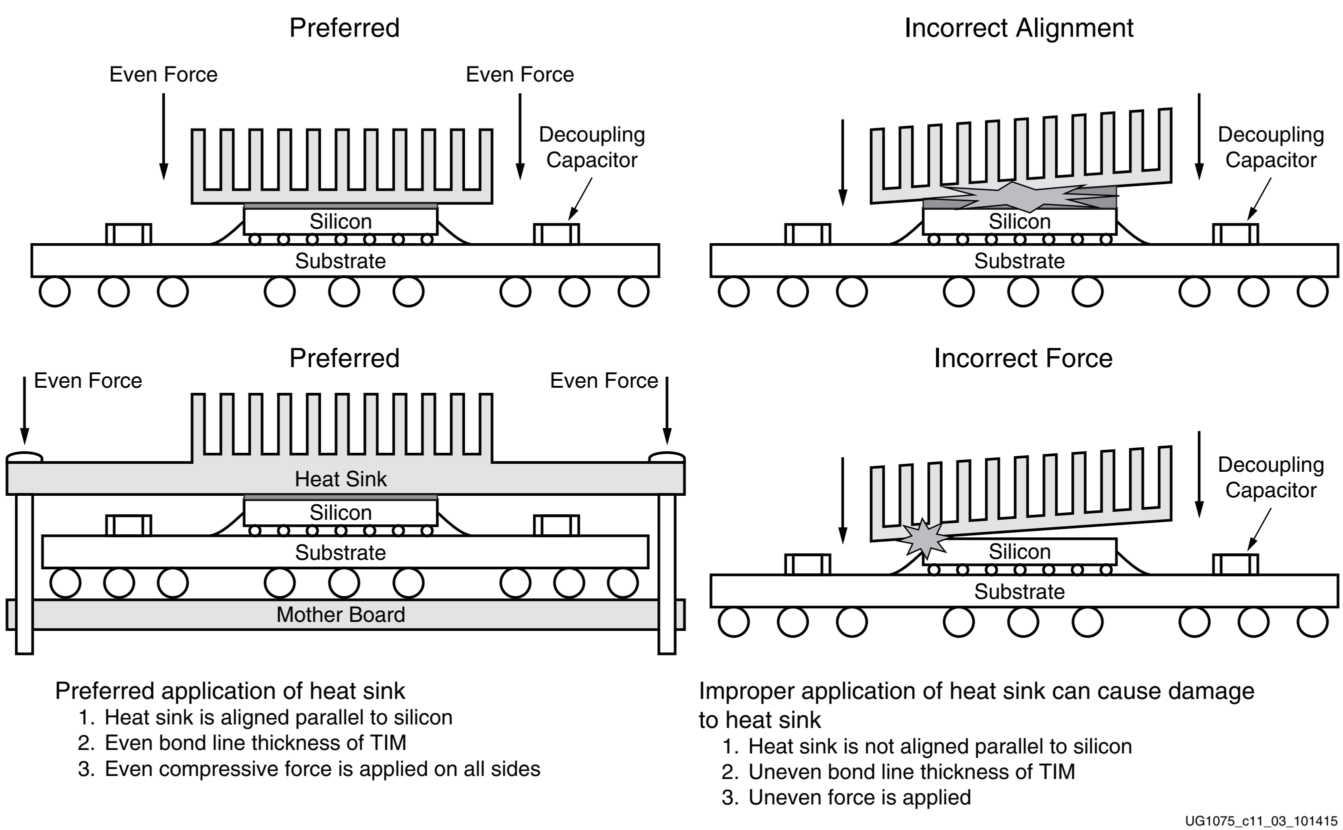


Figure 12-3: **Recommended Application of Heat Sink**

Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the Zynq UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

   Note: Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

   Note: The epoxy curing temperature and time is based on manufacturer's specifications.

Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the Zynq UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

   Note: The thermal adhesive tape hold time is based on manufacturer's specifications.

Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the Zynq UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

   Note: The jig or fixture needs to account for the push pin depth of the heat sink.

2. PCM tape, cut to the size of the heat sink, is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.

3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

   Note: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

1. *Zynq UltraScale+ MPSoC Overview* (DS891) (DS891)
2. *Zynq UltraScale+ RFSoC Overview* (DS889) (DS889)
3. Zynq UltraScale+ device Packaging Specifications
4. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
5. *UltraScale Architecture Clocking Resources User Guide* (UG572)
6. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
7. *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
8. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
9. *UltraScale Architecture GTH Transceiver User Guide* (UG576)
10. *UltraScale Architecture GTY Transceiver User Guide* (UG578)
11. *UltraScale Architecture System Monitor User Guide* (UG580)
12. *UltraScale Architecture PCB Design Guide* (UG583)
13. *UltraScale Architecture-Based Memory Interface Solutions Product Guide* (PG150)
14. *UltraScale Architecture Configuration User Guide* (UG570)
15. *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424)
16. The following websites contain additional information on heat management and contact information.
    - Wakefield: www.wakefield-vette.com
    - Aavid: www.aavid.com
    - Advanced Thermal Solutions: www.qats.com
    - Radian Thermal Products: www.radianheatsinks.com
    - Thermo Cool: www.thermocoolcorp.com
    - CTS: www.ctscorp.com
17. Refer to the following websites for interface material sources:
    - Henkel: www.henkel.com
    - Bergquist Company: www.bergquistcompany.com
    - AOS Thermal Compound: www.aosco.com
    - Chomerics: www.chomerics.com
    - Kester: www.kester.com

18. Refer to the following websites for CFD tools Xilinx supports with thermal models.
    - Mentor Flotherm: www.mentor.com/products/mechanical/flotherm/flotherm/
    - ANSYS Icepak: www.ansys.com
19. Refer to the thermal device models on xilinx.com.
20. The following papers are referenced for more information on thermal modelling.

    - Lemczyk, T.F., Mack, B., Culham, J.R. and Yovanovich, M.M., 1992, "Printed Circuit Board Trace Thermal Analysis and Effective Conductivity", ASME J. Electronic Packaging, Vol. 114, pp. 413 - 419.50.
    - Refai-Ahmed, G. and Karimanal, K., 2003, "Validation of Compact Conduction Models of BGA Under Realistic Boundary," J. of Components and Packaging Technology, Vol. 26, No. 3, pp. 610-615.
    - Sansoucy, E, Refai-Ahmed, G., and Karimanal, K., 2002, "Thermal Characterization of TBGA Package for an integration in Board Level Analysis," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego., USA.
    - Karimanal,K and Refai-Ahmed, G., and., 2002, "Validation of Compact Conduction Models of BGA Under Realistic Boundary Conditions," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego, USA.
    - "Karminal, K. and Refai-Ahmed, G., 2001, ``Compact conduction Model (CCM) of Microelectronic Packages- A BGA Validation Study,'' APACK Conference on Advance in Packaging, Singapore.

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