LS1012A Reference Design Board Errata

This document lists and describes all known errata for the LS1012ARDB. It also describes the available workaround for each erratum and detailed erratum explanation, where needed.

The table below lists the revision history of this document.

Table 1. Revision history

Revision	Date	Description
Rev. 0	06/2016	Initial public release
Rev. 1	07/2016	Added E-00005 and E-00006
Rev. 2	02/2017	Updated Fix plan for E-00004 and E-00006 from Rev. E to Rev. D

This table summarizes all known errata and their workaround for the LS1012ARDB.

Table 2. LS1012RDB errata summary

Errata	Name	Board revision	
		Found on	Fixed on
E-00001	LS1012A and Ethernet PHY clock inputs from same 25 MHz clock source	Rev. C1	Rev. D and higher
E-00002	USB 3.0 HDD drives having intermittent failures during enumeration and data transfer	Rev. B and C1	
E-00003	Reset issue on Rev C	Rev. C1	
E-00004	DDR3L write levelling issue	Rev. A to C1	Rev. D and higher
E-00005	Chassis silk markings for Ethernet ports	Rev. C1	Rev. D and higher
E-00006	Decoupling capacitors	Rev. C1	Rev. D and higher

E-00001: LS1012A and Ethernet PHY clock inputs from same 25 MHz clock source

Description: Due to the SGMII PCS bug identified in the LS1012A SoC, the Ethernet PHY 25 MHz input and LS1012A 25 MHz clock input need to be sourced from same source.

Impact: SGMII CRC errors observed on link and the link is not stable.

Workaround: It is not possible to make any workaround on the Rev C boards. Refer to Rev D schematics for implementation of updated clock architecture.

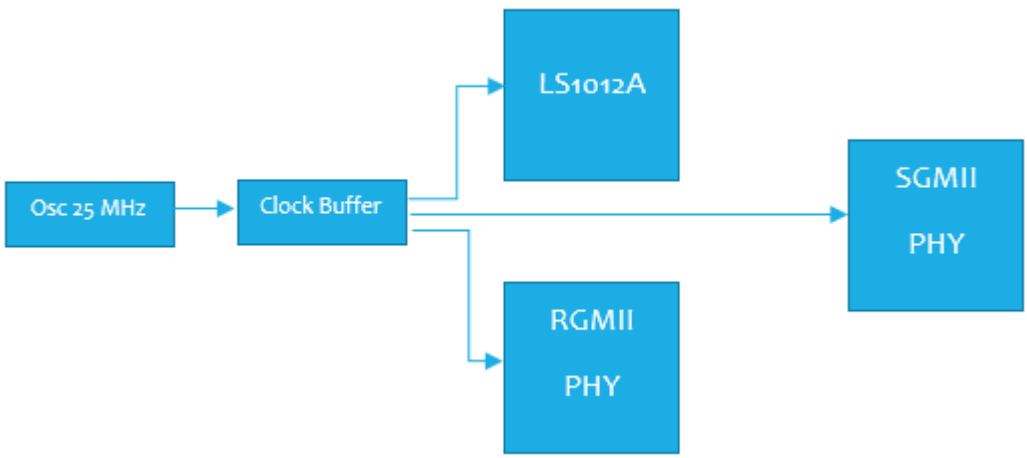

Figure 1. E-00001 workaround

Fix plan: The permanent fix will be available on the Rev D and higher boards.

E-00002: USB 3.0 HDD drive is showing intermittent failures during enumeration and data transfer

Description: USB 3.0 HDD fail during data transfer and enumeration. The USB power switch asserts power fault. The root cause is traced to battery charger and power mux circuitry. This circuitry loads the VBUS and the power switch disables VBUS along with the POWERFAULT assertion.

Impact: All USB 3.0 based use cases is impacted.

Workaround:
1. Remove the Li-Ion battery, if it is connected on connector J2.
2. Unmount R3601.
3. Cut the trace from R3601 to the U6.4 pin.

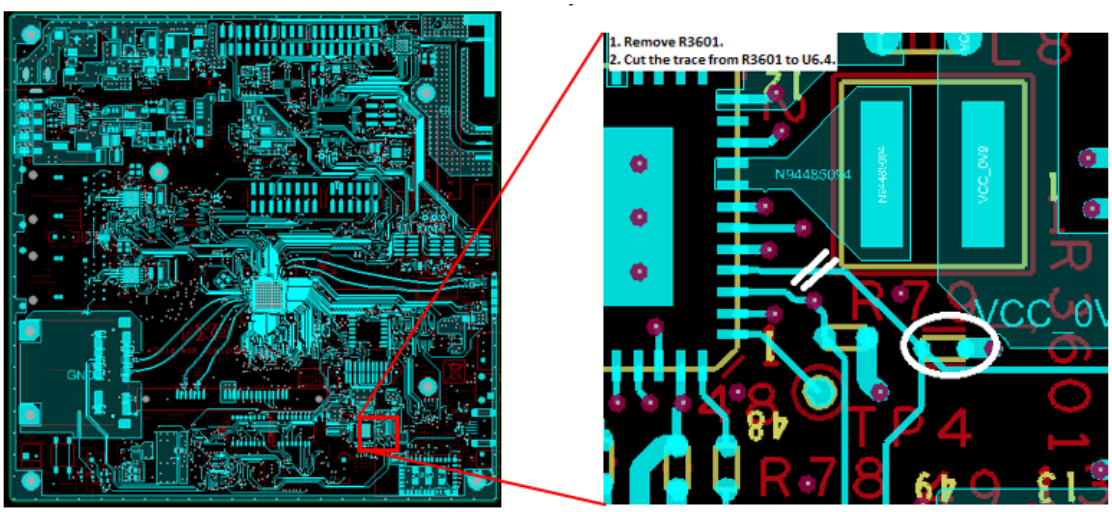

Figure 2. E-00002 workaround

Fix plan: The permanent fix will be available on the Rev D and higher boards.

E-00003: Reset issue on Rev C

Description: Some of the board peripherals are in reset due a potential divider on 3V3LO_EN_B trace.

Impact: Ethernet, Accelerometer, PeX based WIFI and Accelerometer are in reset.

Workaround: Unmount the R3666 resistor on BOT layer near the U643 (in Mini PCIe connector J22 area).

Fix plan: A permanent fix will be available on the Rev. D and and higher boards.

E-00004: DDR3L write levelling issue

Description: The board layout does not meet the write levelling requirements mentioned in the LS1012A design checklist.

Impact: The DDR3 memory fails during write leveling calibration.

Workaround: Currently, the board does not support this layout. There is no workaround available for the impacted revisions.

Fix plan: The Rev. D and higher boards will include changes related to the CK/CK# and DQS/DQS# length requirements.

E-00005: Chassis silk markings for Ethernet ports

Description: ETH_1 and ETH_2 port names on the chassis silk are swapped.

Impact: The naming creates confusion with the port mappings in the U-Boot and Linux software releases.

Workaround: If the ETH_1 and ETH_2 port markings on the chassis silk of your LS1012ARDB are as shown in the figure below, then paste stickers on the chassis silk to correct the markings, as given in the table below.

Old marking	New sticker marking
ETH_1	ETH_2
ETH_2	ETH_1

Figure 3. Incorrect ETH_1 and ETH_2 port markings on LS1012ARDB chassis

The figure below shows the correct Ethernet port markings on the LS1012ARDB chassis.

Figure 4. Correct ETH_1 and ETH_2 port markings on LS1012ARDB chassis

Fix plan: A permanent fix will be available on the Rev. D and and higher boards.

E-00006: Decoupling capacitors

Description: The board layout does not meet the decoupling requirements mentioned in the LS1012A design checklist.

Impact: This erratum may result in random failures while switching to high power consumption use cases.

Workaround: Currently, the board does not support this layout. There is no workaround available for the impacted revisions.

Fix plan: The Rev. D and higher boards will have the decoupling capacitors as mentioned in the LS1012A design checklist.

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