QorIQ LS1043A Reference Design Board Reference Manual

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Chapter 1
Introduction

The LS1043A reference design board (RDB) is a high-performance computing, evaluation, and development platform for the QorIQ LS1043A processor. It can also be used as a software development and debugging platform for the LS1043A processor. It functions as a desktop computer and operates as a development and evaluation system. The LS1043ARDB is lead-free and RoHS-compliant.

NOTE

Use the part number *LS1043ARDB-PD* to order the LS1043ARDB.

You can perform the following operations using the LS1043ARDB onboard resources and debugging devices:

- Upload and run code
- Set breakpoints
- Display memory and registers
- Connect and incorporate proprietary hardware into the target systems, using the LS1043A processor as a host processor
- Use the LS1043ARDB as a demonstration tool

A software application developed for the LS1043ARDB can run with various input/output data streams, for example, PCIe or XFI connections.

The board support package (BSP) is developed using the Linux operating system.

1.1 Acronyms and abbreviations

The table below lists and describes the acronyms and abbreviations used in this document.

Table 1-1. Acronyms and abbreviations

Acronym/abbreviation	Description
AVDD	Supply voltages for the core, platform, DDR, and SerDes PLLs
BCSR	Board control and status register
BGA	Ball grid array
BRDCFG	Board configuration
CLKIN	Clock input (interchangeable with SYSCLK)
COP	Common on-chip processor
CPLD	Complex programmable logic device
CTS	Clear to send
CVDD	Supply voltage for the DSPI block
DDR	Double data rate
DIP	Dual inline package
DMA	Direct memory access
DRAM	Dynamic random access memory
DSPI	Deserial serial peripheral interface
DVDD	Supply voltage for UART/I2C/DMA
EC	Ethernet controllers
ECC	Error checking and correction
EEPROM	Electrically erasable programmable ROM
EMI	Ethernet management interface
eMMC	Embedded multimedia card
eSDHC	Enhanced secure digital high capacity card
FCM	NAND flash control machine
FMan	Frame manager
FPGA	Field programmable gate array
G1VDD	Supply voltage for the DDR module
GETH	Gigabit Ethernet (GbE)
GPCM	General-purpose chip-select machine
GPINPUT	General purpose input
GPIO	General purpose input/output
HRESET	Hard reset
I2C	Inter-integrated circuit multi-master serial computer bus
IFC	Integrated flash controller
IPL	Initial program load
JTAG	Joint Test Action Group (IEEE® standard 1149.1™)
LBMAP	Local bus map

Table continues on the next page...

Table 1-1. Acronyms and abbreviations (continued)

Acronym/abbreviation	Description
LDO	Low-dropout
LED	Light-emitting diode
LSB	Least significant bit
LVDD	Supply voltage for the GETH block
MAC	Medium access control
MMC	Multimedia card
MSB	Most significant bit
MSD	Mass storage device
OCM	Offline Configuration Manager (FPGA-embedded)
OVDD	Supply voltage for general purpose I/O
PCBA	Printed circuit board assembly
PLL	Phase-locked loop
PMIC	Power management integrated circuit
POR	Power-on reset
POVDD	Security fuse programming override supply voltage (PROG_SFP)
ppm	Parts per million
PROMJet	Memory emulator by EmuTec Inc.
QSGMII	Quad serial gigabit media-independent interface
RCW	Reset configuration word
REFCLK	Reference clock (clock synthesizer input value)
RGMII	Reduced gigabit media-independent interface
ROM	Read-only memory
RTC	Real-time clock
RTS	Request to send
SATA	Serial advanced technology attachment
SCL/SCLK	Serial clock
SD	Secure digital card
SDHC	Secure digital high capacity card
SDRAM	Synchronous dynamic random access memory
SDREFCLK	SerDes reference clock
SERCLK	SerDes clock
SerDes (SRDS)	Serializer/deserializer, for example, PEX, XAUI, SGMII, SATA, sRIO, AURORA, and XFI
SGMII	Serial gigabit media-independent interface
SIP	Secure interfaces and power
SLAC	Subscriber line access controller
SLC	Single-level cell
SLIC	Subscriber line interface controller
SMB	Subminiature version B connector
SPD	Serial presence detect

Table continues on the next page...

Table 1-1. Acronyms and abbreviations (continued)

Acronym/abbreviation	Description
SPI	Serial peripheral interface
SRAM	Static random-access memory
S1VDD	Supply voltage for SerDes1 and SerDes2 core logic
SYSCLK	System clock
TAP	Test access port, for example, USB TAP or Ethernet TAP
TESTSEL	Test select
TH_VDD	Supply voltage for the Thermal Monitor unit
TRIG_IN/OUT	Trigger input/output
TSEC	Three-speed Ethernet controller
UART	Universal asynchronous receiver/transmitter
uDIMM	Unbuffered dual inline memory module form factor
USB	Universal serial bus
USBCLK	USB clock
VDD	Supply voltage for core and platform
TA_BB_VDD	Supply voltage for low power security monitor
XAUI	Ten gigabit attachment unit interface
XVDD	Supply voltage for SerDes1 and SerDes2 transceivers

1.2 Related documentation

This table lists and describes the additional documents available for more information on the LS1043ARDB.

Table 1-2. Related documentation

Document	Description
QorIQ LS1043ARDB Getting Started Guide (LS1043ARDBGSG)	Describes the LS1043ARDB hardware kit, provides settings for the onboard switches, connectors, jumpers, and LEDs, and explains the basic board operations in a step-by-step manner
QorIQ LS1043A Reference Manual (LS1043ARM)	Provides a detailed description on the LS1043A multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information
QorIQ LS1043A Data Sheet	Contains information on the LS1043A pin assignments, electrical characteristics, hardware design considerations, package information, and ordering information
LS1043A Chip Errata	Provides details of all known silicon errata for the LS1043A processor

NOTE

Some of the documents listed in the table above, may be available only under a non-disclosure agreement (NDA). To

request access to such documents, contact your local NXP field applications engineer or sales representative.

1.3 Board features

The table below lists the features of the LS1043ARDB.

Table 1-3. LS1043ARDB features

LS1043ARDB feature	Specification	Description
Processor support	Core processors	4x64-bit up to 1.6 GHz ARM® Cortex®-v8 A53 cores

	High-speed serial ports (SerDes)	• Supports 4 lanes, up to 10.3125 GHz SerDes
		• Supports PCIe 2.0, QSGMII, and XFI
		• Two PCIe connectors supporting:
		  • Mini-PCIe card
		  • Standard PCIe card
		• X1 RJ45 connector for Ethernet 10G support
		• X4 RJ45 connector for QSGMII support

	DDR	• Supports 2 GB DDR4 SDRAM discrete devices • 32-bit DDR4 bus • Supports data rates of up to 1600 MT/s
	USB 3.0	• Two super-speed USB 3.0 type A ports • Supports x1 USB 2.0 connection on the mini-PCIe connector
	IFC	• One 128 MB NOR flash 16-bit data bus (1.8 V) • One 512 MB SLC NAND flash with ECC support (1.8 V) • CPLD connection: 8-bit registers in CPLD to configure some mux/demux selections
	eSDHC	• SDHC port connects directly to a full SD/MMC slot.
	DSPI	• 16 MB high-speed flash memory (up to 108 MHz in the Single-Transfer Rate mode)
	DUART	• One RJ45 to DB9 connector with two UART ports • UART1 is routed to CMSISDAP circuit and supports USB port to access serial port as console
	Package	• 21 x 21 mm, 621 flip-chip, plastic-ball, grid array (FC-PBGA)
System logic	CPLD	• Manages system power and reset sequencing • Latches IFC address/data multiplexed signals • Controls signal muxing/demuxing
Clock	SYSCLK	• Supports single-ended SYSCLK, DDRCLK clock input, with default value as 100 MHz • Supports single-source differential DIFF_SYCLK_/ DIFF_SYSCLK_N, 100 MHz
	SerDes	• Provides clocks to all SerDes blocks and slots • 100 MHz or 156.25 MHz for PLL1 • 100 MHz for PLL2
	RTC	• Supports 32.768 kHz for RTC

Table continues on the next page...

Table 1-3. LS1043ARDB features (continued)

LS1043ARDB feature	Specification	Description
Power	One dedicated programmable regulator supplying the LS1043A core and DDR power domains.	Power supply details for the LS1043ARDB are given below: • 1.0 V for core VDD, USB_SVDD, and USB_SDVDD • 1.2 V for GVDD • 1.8 V for LS1043A PROG_SFP and PROG_MTR (POVDD) • 3.3 V / 1.8 V for CPLD • 1.35 V for XVDD • 1.0 V for S1VDD • 1.8 V for LS1043A general I/O • 3.3 V for UART/I2C • 3.3 V for USB HVDD • 0.6 V for DDR4 VTT/VREF • 3.3 V / 1.8 V for eSDHC • 1.0 V for security monitor (TA_BB_VDD) **NOTE:** For core VDD, USB_SVDD, USB_SDVDD, and TA_BB_VDD, the LS1043A processor supports 1.0 V as well as 0.9 V; however, the LS1043ARDB only supports 1.0 V.

1.4 Block diagrams

The figure below shows the LS1043A processor block diagram.

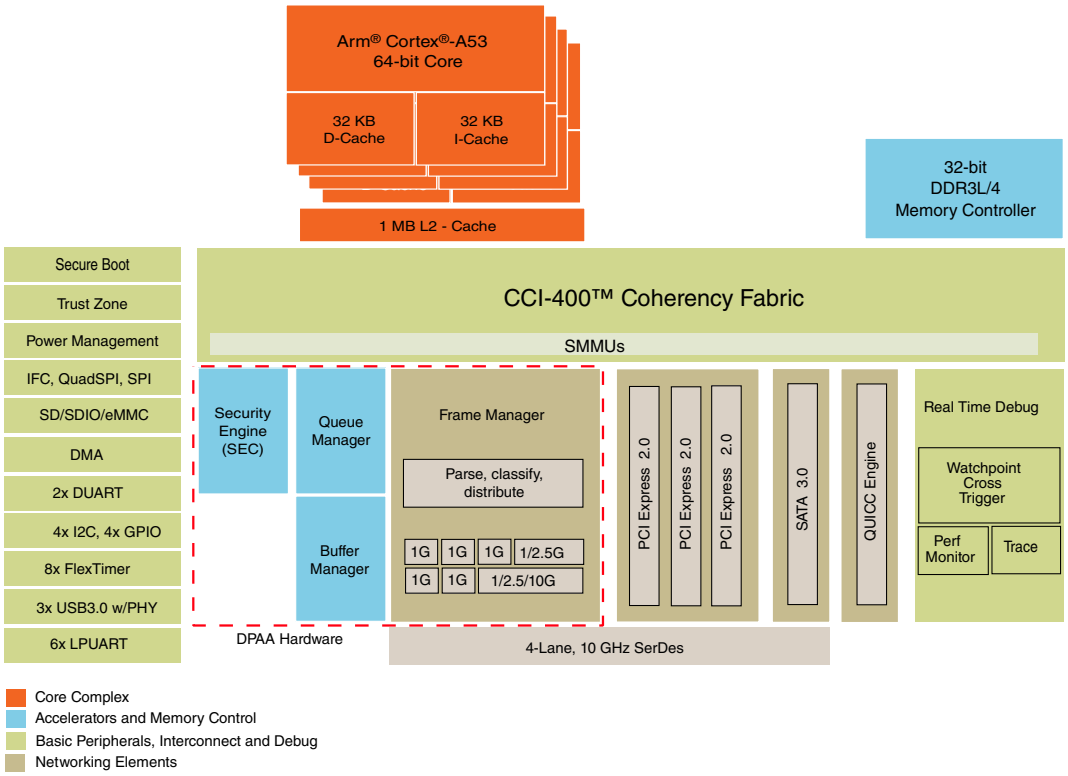

Figure 1-1. LS1043A processor block diagram

The figure below shows the LS1043ARDB block diagram.

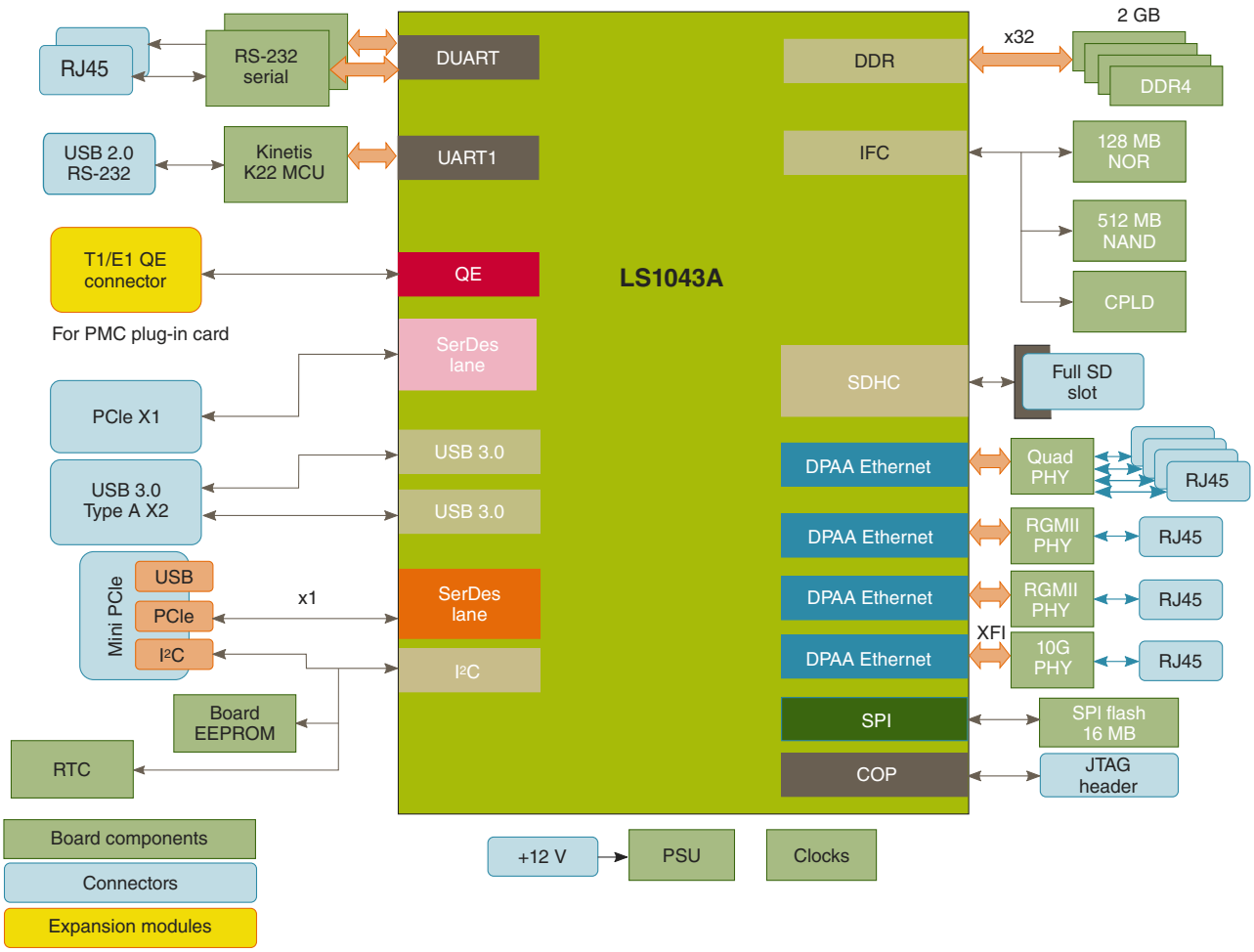

Figure 1-2. LS1043ARDB block diagram

1.5 Board views

The figure below shows the LS1043ARDB top view.

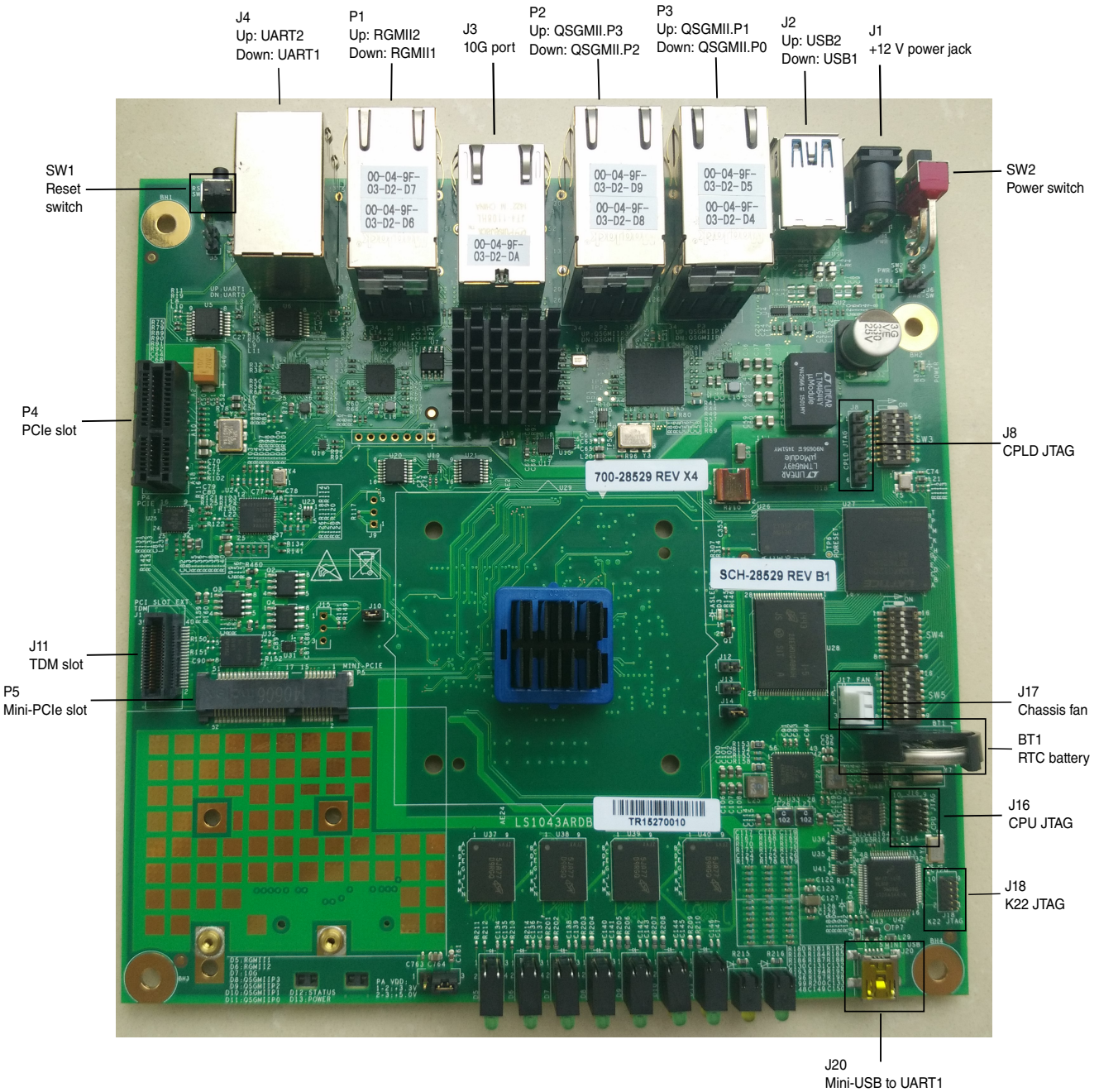

Figure 1-3. LS1043ARDB top view

The figure below shows the LS1043ARDB bottom view.

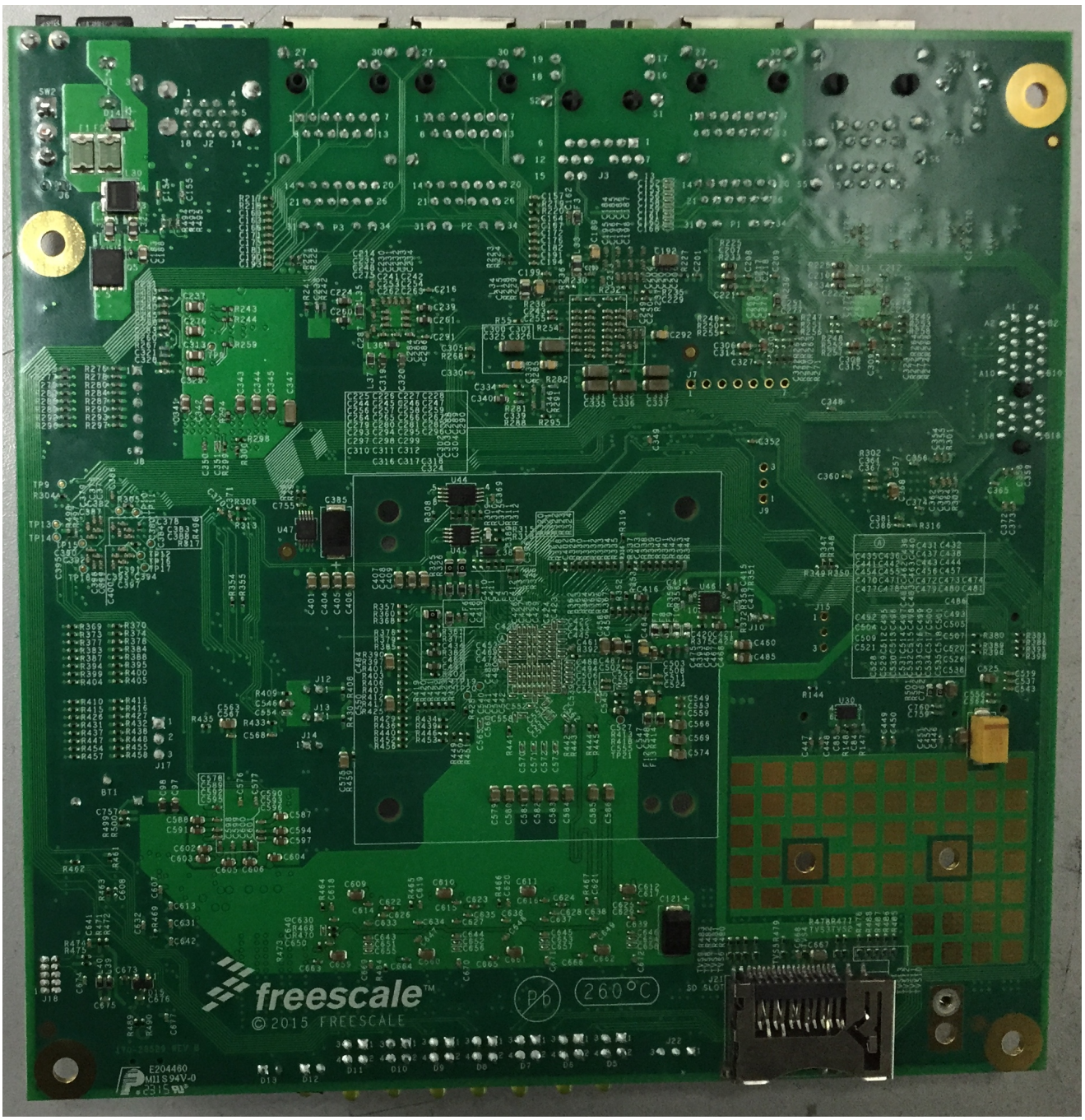

Figure 1-4. LS1043ARDB bottom view

Chapter 2
Interfaces

The LS1043ARDB architecture is primarily determined by the LS1043A processor with the need to evaluate LS1043A processor features and to test its ability to deliver an easily usable off-the-shelf software development platform. Following are the main interfaces that form the LS1043ARDB architecture:

- DDR interface
- IFC interface
- Serial interfaces
- Ethernet interface
- SerDes interface
- USB interface
- I2C interface

2.1 DDR interface

The LS1043ARDB supports high-speed DRAM with 2 GB double data rate 4 (DDR4) SDRAM discrete devices (32-bit bus). The memory interface includes all necessary termination and I/O powers. It is routed such that maximum performance of the memory bus can be achieved. The figure below shows the DDR memory architecture.

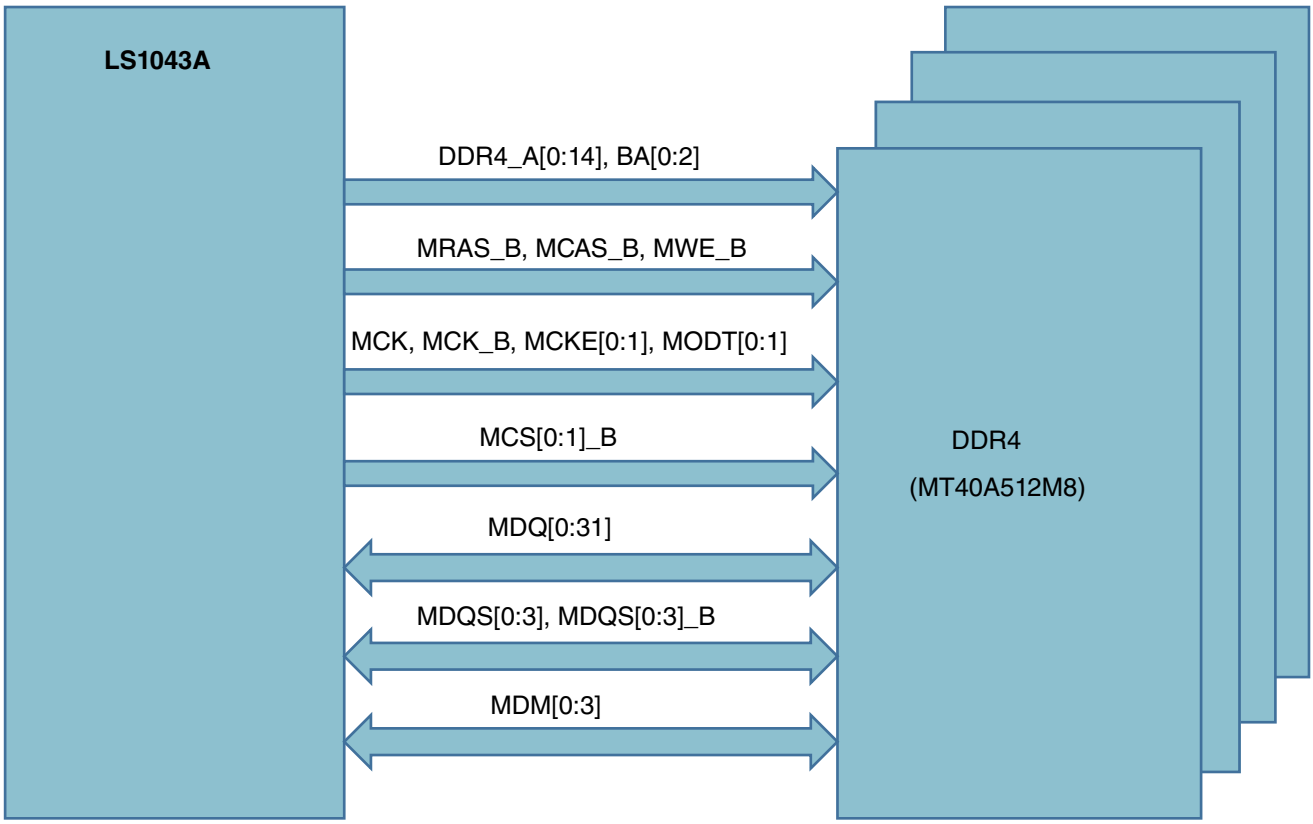

Figure 2-1. DDR memory architecture

For power supply details for the DDR interface, see DDR supply.

2.2 IFC interface

The LS1043ARDB integrated flash controller (IFC) has the following features:

- Supports 1.8 V I/O voltage
- Implements little endian support
- Supports 28-bit addressing and 16-bit data bus
- Supports GPCM, NOR, and NAND FCM
- Supports the following IFC clients on the LS1043ARDB:
  - NAND flash (async/sync - ONFI 1.0 compatible)
  - NOR flash 16-bit

The figure below shows the IFC block diagram.

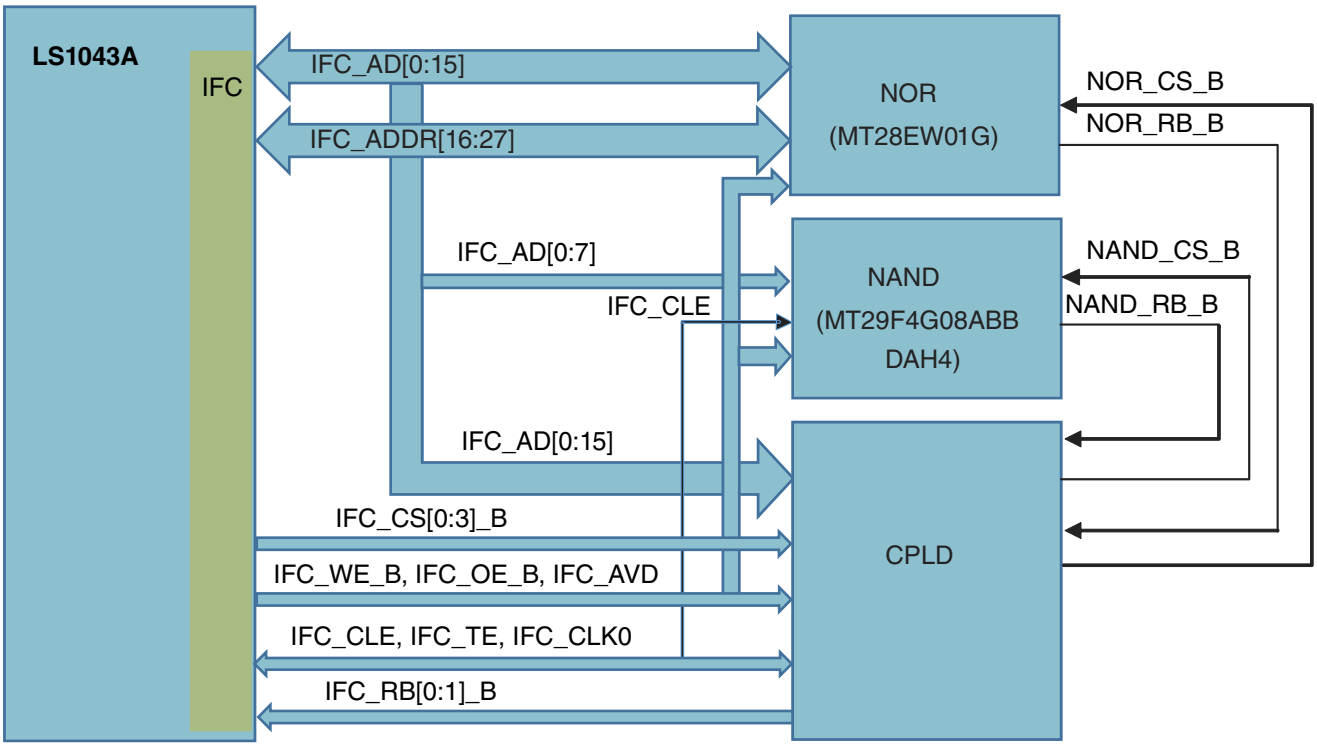

Figure 2-2. IFC block diagram

LS1043ARDB uses a combination of the IFC chip select signals and DIP switches to allow dynamic reconfiguration of the IFC boot device (which addresses IFC_CS_B[0] only).

The table below summarizes the IFC chip select routing.

Table 2-1. IFC chip select device mapping

SW4[1:8]+SW5[1]=	Chip select	Memory	Data width
000100101	CS0	NOR flash	16 bits
	CS1	NAND flash	8 bits
	CS2	CPLD registers	8 bits
100000110	CS0	NAND flash	8 bits
	CS1	NOR flash	16 bits
	CS2	CPLD registers	8 bits

2.2.1 NOR flash memory

The LS1043ARDB has a Micron NOR flash memory (MT28EW01G) with 128 MB size and 16-bit data bus. The NOR flash memory is powered from a 3.3 V power supply but the signals are driven with the 1.8 V I/O level. The NOR flash memory is controlled by the NOR IFC machine.

Flash controls are explained below:

- IFC OE_B controls flash OE, whereas IFC WE0_B controls the flash WE_B signal.
- Flash RY/BY_B output signal shows the ready/busy status of the flash. This signal is connected to the CPLD.
- IFC_NOR_CS_B driven by CPLD selects either IFC_CS0_B or IFC_CS1_B to the NOR flash memory based on CFG_RCW_SRC[0:8].

CPLD-generated signals are used to re-arrange internal addresses according to user configuration options CFG_RCW_SRC[0:8]. For details, see CPLD Programming.

2.2.2 NAND flash memory

The LS1043ARDB has an ONFI 1.0 compatible Micron NAND flash memory (MT29F4G08ABBDAH4-ITX) with 512 MB size and 8-bit data bus. The NAND flash memory is powered from a 1.8 V power supply. It has signals going to and coming from the LS1043A processor directly. The NAND flash memory is controlled by the LS1043A IFC FCM machine.

Flash controls are explained below:

- Flash R/B_B output indicates the status of the NAND operation. This open drain output connects to complex programmable logic device (CPLD).
- IFC_NAND_CS_B from CPLD drives the NAND flash according to CFG_RCW_SRC[0:8]. For details, see CPLD Programming.

2.3 Serial interfaces

The LS1043ARDB has several serial interfaces, such as RS-232, DSPI, eSDHC/eMMC, and I2C. This section describes the following main serial interfaces used in the LS1043ARDB:

- UART interface
- eSDHC interface
- DSPI interface

2.3.1 UART interface

The figure below shows the LS1043ARDB universal asynchronous receiver/transmitter (UART) connections.

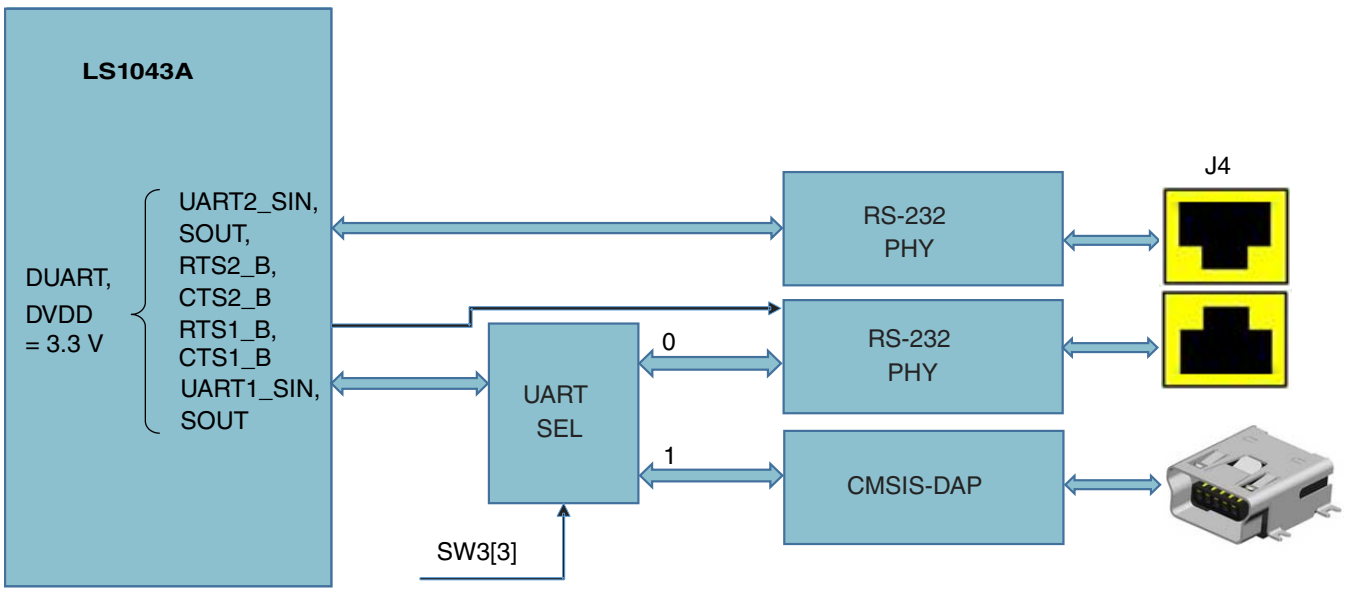

Figure 2-3. UART interface

The LS1043ARDB has two UART connectors; therefore, two UART ports are available at a time. Two RS-232 transceivers (SP3232) available on the LS1043ARDB help in user application development and provide convenient communication channels to both terminal and host computers. The transceivers are connected to the dedicated UART ports on the LS1043ARDB by 4 wires. They support RTS/CTS flow control.

The table below describes the LS1043ARDB RS-232 interface.

Table 2-2. LS1043ARDB RS-232 interface

UART port	Destination	Power supply	Flow control	External connector
UART1	Terminal (host computer)	3.3 V	Supported	UART1 (J4 bottom)
UART2			Supported	UART2 (J4 top)

2.3.2 eSDHC interface

The LS1043ARDB enhanced secure digital high capacity card (eSDHC) has the following features:

- x1/x4-bit SD card supporting SD Rev 2.0 and 3.0.

- The SDHC_VS pin is used to select EVDD between 1.8 V and 3.3 V SD card I/O voltages.
- MMC 8-bit data high-speed operation is limited by voltage translation hardware. SDHC/SDHX is supported in either 1-bit or 4-bit data mode for either 3.3 V or 1.8 V bus operation. Bus frequency above 50 MHz requires dynamically changing the LS1043ARDB EVDD voltage supply rail from 3.3 V to 1.8 V as described in SD Physical Layer Specification version 3.01.

The figure below shows the eSDHC signal connections supported on the LS1043ARDB.

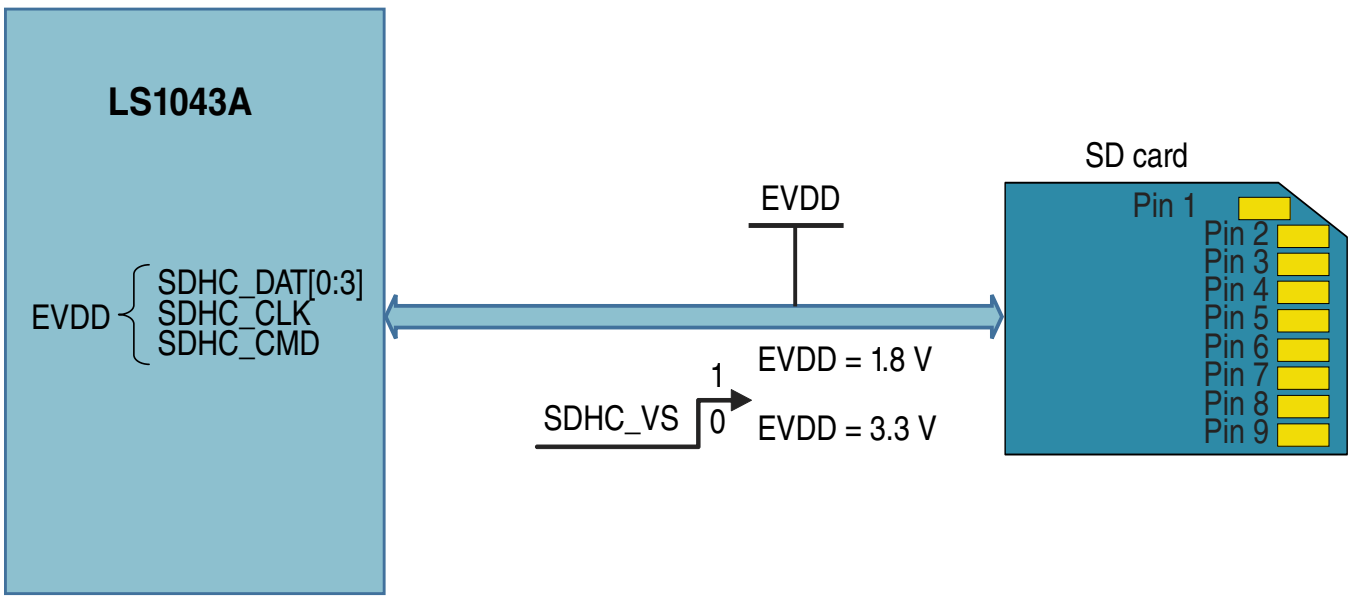

Figure 2-4. eSDHC connections

The table below shows the pinout configuration of the SD card shown in the figure above.

Table 2-3. SD card pinout configuration

Pin number	Signal name	Description
Pin 1	DAT2	Data signal 2
Pin 2	DAT3	Data signal 3
Pin 3	CMD I/O	Input/output command
Pin 4	GND	Supply voltage negative
Pin 5	VDD	Supply voltage positive
Pin 6	CLK	Clock signal
Pin 7	GND	Supply voltage negative
Pin 8	DAT0	Data signal 0
Pin 9	DAT1	Data signal 1

2.3.3 DSPI interface

Serial peripheral interface (SPI) usually means deserial serial peripheral interface (DSPI) on the LS1043ARDB. The SPI pins of the LS1043ARDB can be used to access the following devices:

- Onboard SPI devices: For various SPI memory devices
- Offboard (TDM riser) device: For SLIC/SLAC interface circuitry

The LS1043ARDB has a DSPI master controller that is used to communicate with various peripherals. The LS1043ARDB DSPI has the following features:

- SPI flash memory
- 4-pin DSPI jumper header
- LS1043A OVDD supports 1.8 V on the LS1043ARDB.

The figure below shows the LS1043A connections for DSPI.

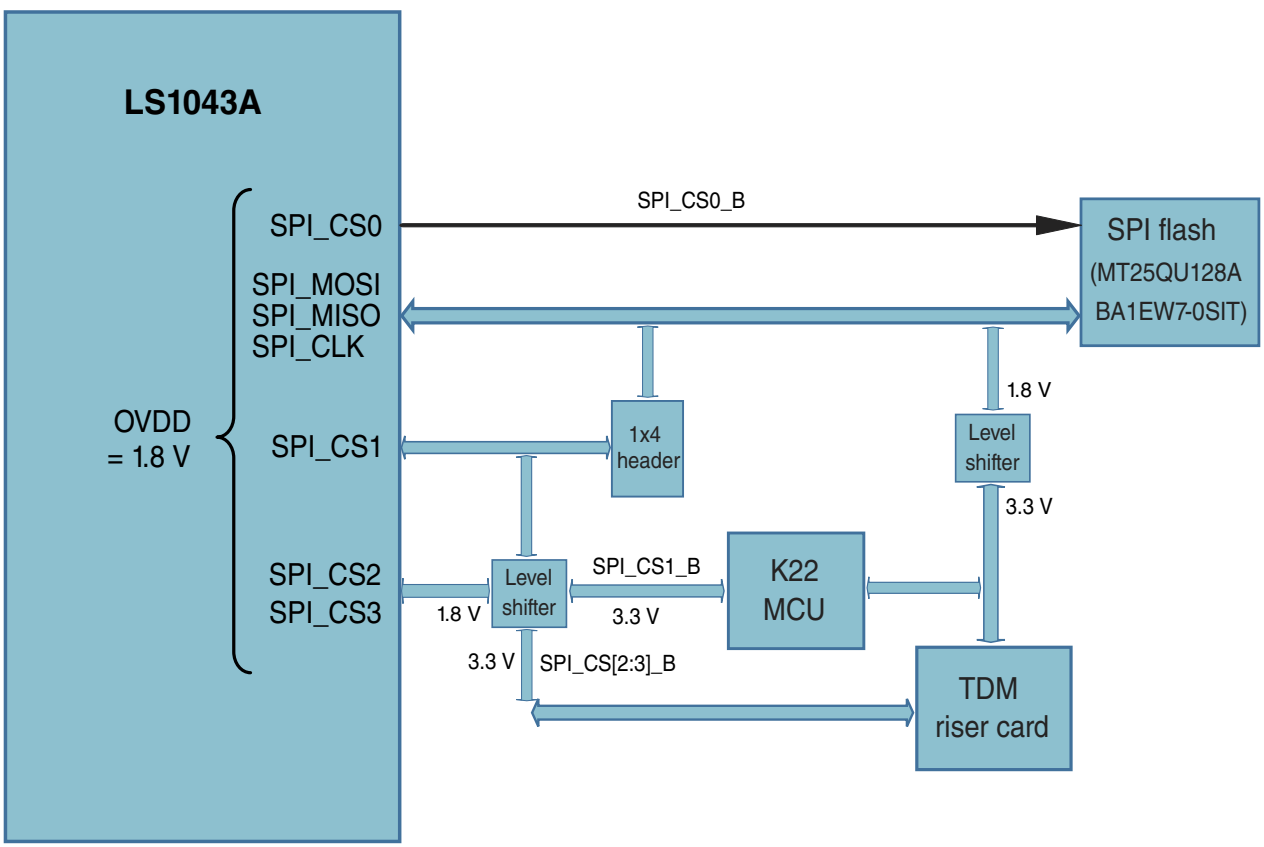

Figure 2-5. DSPI connections

NOTE

Some DSPI pins are muxed with eSDHC pins; therefore, DSPI functionality depends on the eSDHC configuration.

The table below describes the LS1043ARDB SPI flash memory.

Table 2-4. DSPI slave devices

Device	Maximum clock frequency	Voltage range	Capacity	Chip select
Micron MT25QU128ABA1EW7 -0SIT	166 MHz	1.7 V - 2 V	16 MB	CS0

2.4 Ethernet interface

The LS1043A processor supports the following two Ethernet controllers (ECs):

- EC1 port: Operates in the RGMII mode
- EC2 port: Operates in the RGMII mode

Each of these ports can connect to an Ethernet PHY using the RGMII protocol. The figure below shows each EC port connected to a Realtek RTL8211FS PHY on the LS1043ARDB.

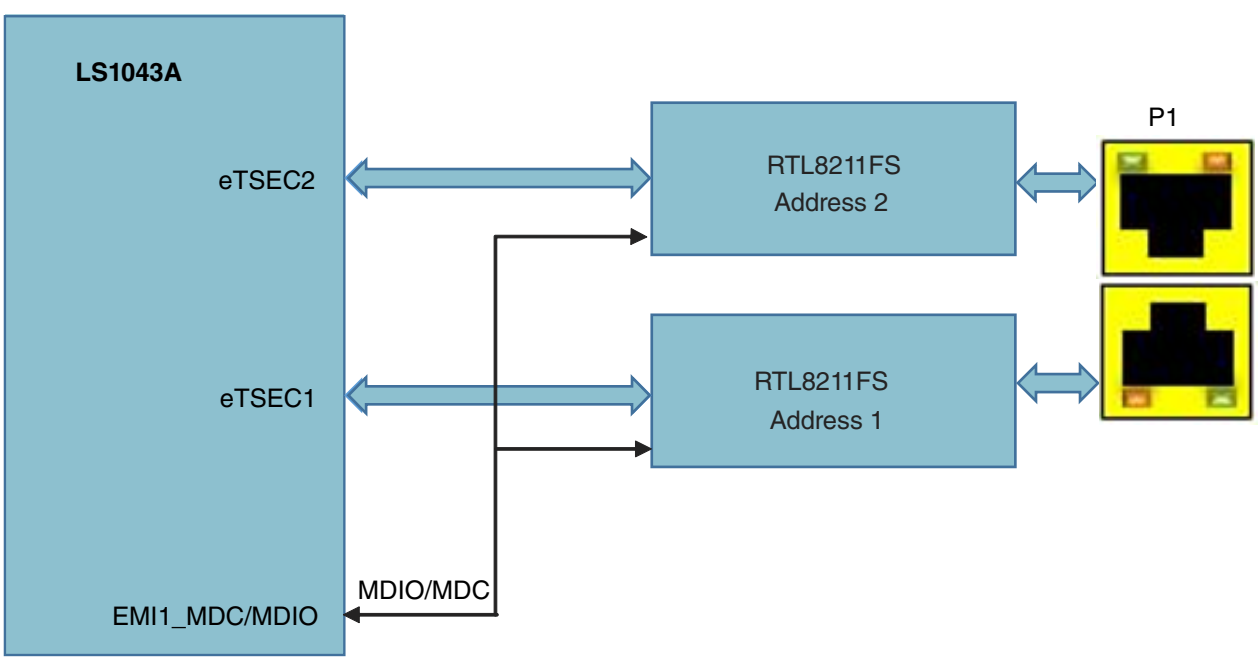

Figure 2-6. Ethernet interface

Connections and routing for the three-speed Ethernet controller (TSEC) are summarized in the table below.

Table 2-5. Ethernet port locations

Ethernet in Linux	EC number	Interface voltage	PHY address	Connector location (from chassis/board back)	Status indicator
eth2	EC1	LVDD (1.8 V)	1	Bottom	• R: Transmit or receive activity • L: Link
eth3	EC2	LVDD (1.8 V)	2	Top	• R: Transmit or receive activity • L: Link

2.4.1 Ethernet management interfaces

The LS1043ARDB has two Ethernet management interfaces (EMIs): EMI1 and EMI2. The EMIs control two PHY transceivers connected with them separately. The table below lists the PHYs connected with the EMIs.

Table 2-6. PHYs connected with EMIs

Manufacturer part number	Manufacturer name	PHY type
RTL8211FS	Realteck	RGMII
F104S8A	NXP Semiconductors	QSGMII
AQR105-B1	Aquantia	XFI

The figure below shows how PHY transceivers are connected with EMIs.

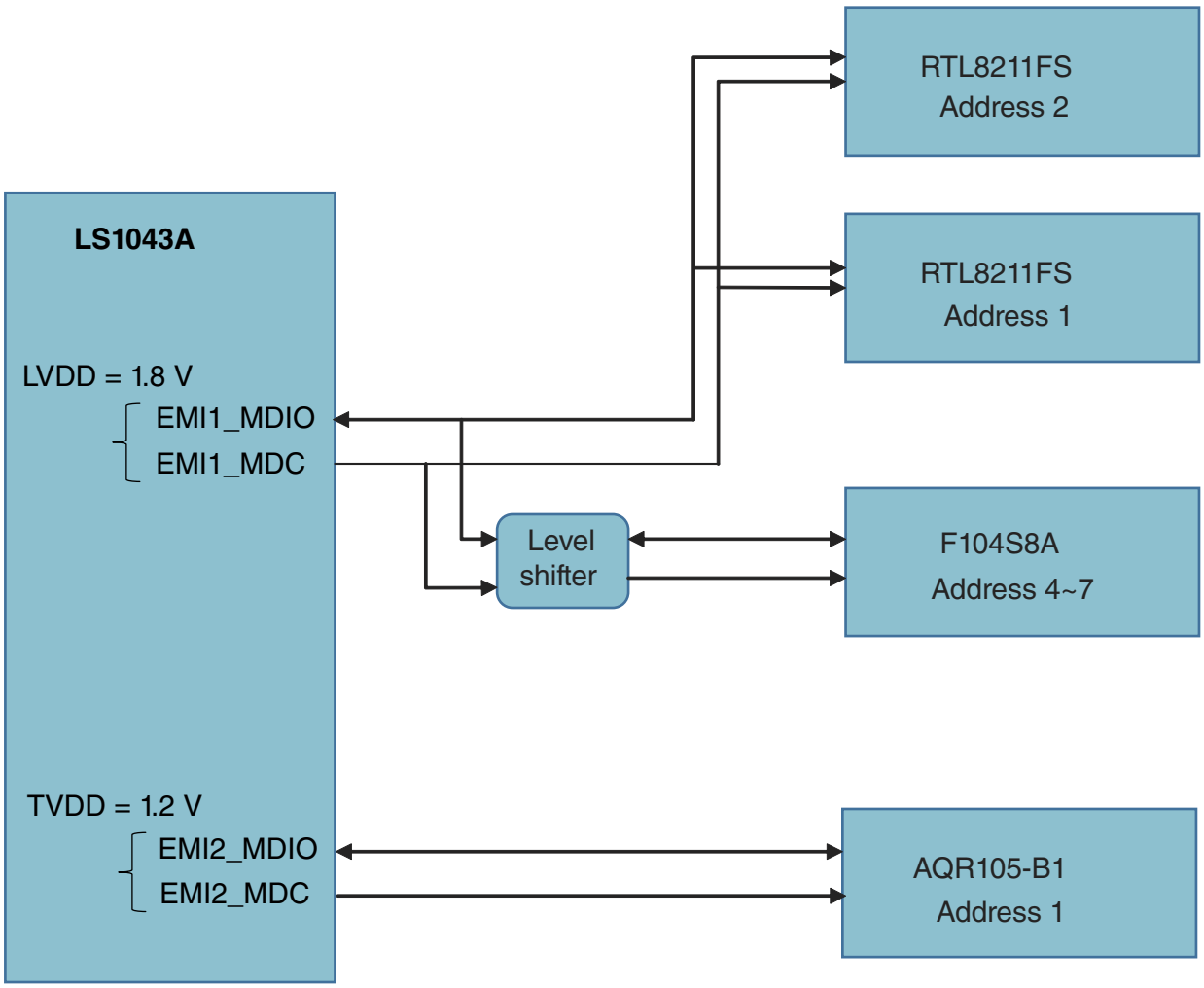

Figure 2-7. EMI-PHY connection

2.5 SerDes interface

The serializer/deserializer (SerDes) block of the LS1043ARDB supports several protocols that includes four serial lanes. See *QorIQ LS1043A Reference Manual* (LS1043ARM) for information on supported SerDes combinations.

The table below lists the SerDes embedded devices used on the LS1043ARDB.

Table 2-7. LS1043ARDB SerDes embedded devices

Part number	Manufacturer	Description
AQR105-B1	Aquantia	Ethernet single-port AQrate 10GBase-T PHY FCBGA324
F104S8A	NXP Semiconductors	VSC8514, quad-port 10/100/1000Base-T PHY with QSGMII MAC

Table continues on the next page...

Table 2-7. LS1043ARDB SerDes embedded devices (continued)

Part number	Manufacturer	Description
05Y621A0311-R-36LF	Anytronic	2X26 mini-PCIe SMT 0.8 mm connector, supporting mini-PCIe form Wi-Fi cards
WPES-036AN41B22UWC	WIN-WIN	36 PCIe card slot (connector), supporting standard PCIe x1 cards

The table below describes the possible SerDes1 protocol combination for LS1043ARDB.

Table 2-8. LS1043ARDB SerDes1 protocol combination

IPD protocol combo (hexadecimal)	SRDS_PRTCL_S1[128:143] RCW (hexadecimal)	A	B	C	D
0F	1455	XFI	QSGMII	PCIe 2 (x1)	PCIe 3 (x1)

The figure below shows the LS1043ARDB SerDes lane connections.

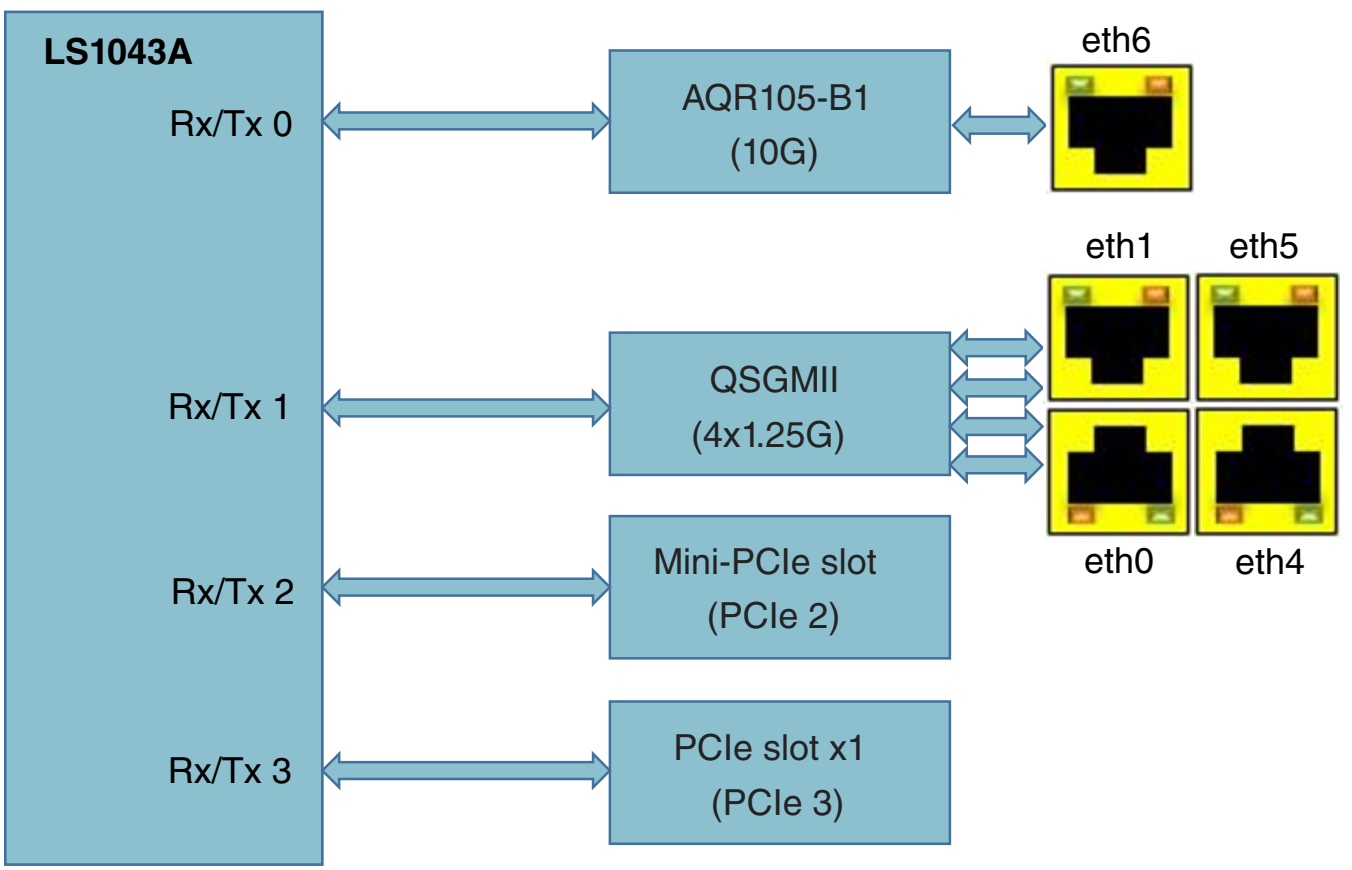

Figure 2-8. LS1043ARDB SerDes lane connections

2.5.1 Mini-PCIe card

Starting Rev. B version of the LS1043ARDB, support can be added for the wider QCA WAVE2 card. To add this support, perform the following steps:

1. Clean up the top and bottom layer parts on the mini-PCIe card area.
2. Pour ground copper on the top and bottom of the mini-PCIe card area.
3. Add support for the additional PA voltage (+5 V or +3.3 V) on the mini-PCIe slot (P5) reserved pins, as shown in the table below.

Pin number on P5	Standard pin definition on mini-PCIe slot	LS1043ARDB	Jumper settings (J22: 1-2)	Jumper settings (J22: 2-3)
39	Reserved pin	3.3 V		
41	Reserved pin	3.3 V		
45	Reserved pin	+VPA	+3.3 V	+5.0 V
47	Reserved pin	+VPA		
49	Reserved pin	+VPA		
51	Reserved pin	+VPA		

2.6 USB interface

The LS1043A processor has three integrated USB 3.0 controllers (USB1, USB2, and USB3) that allow direct connection to the USB ports with appropriate protection circuitry and power supplies. Each USB port is powered by an NXP NX5P3090UK device, which is an adjustable current-limited power switch that supplies 5 V power. The power enable and power-fault-detect pins are connected to the LS1043A processor via CPLD for individual port management.

The figure below shows the LS1043ARDB USB architecture.

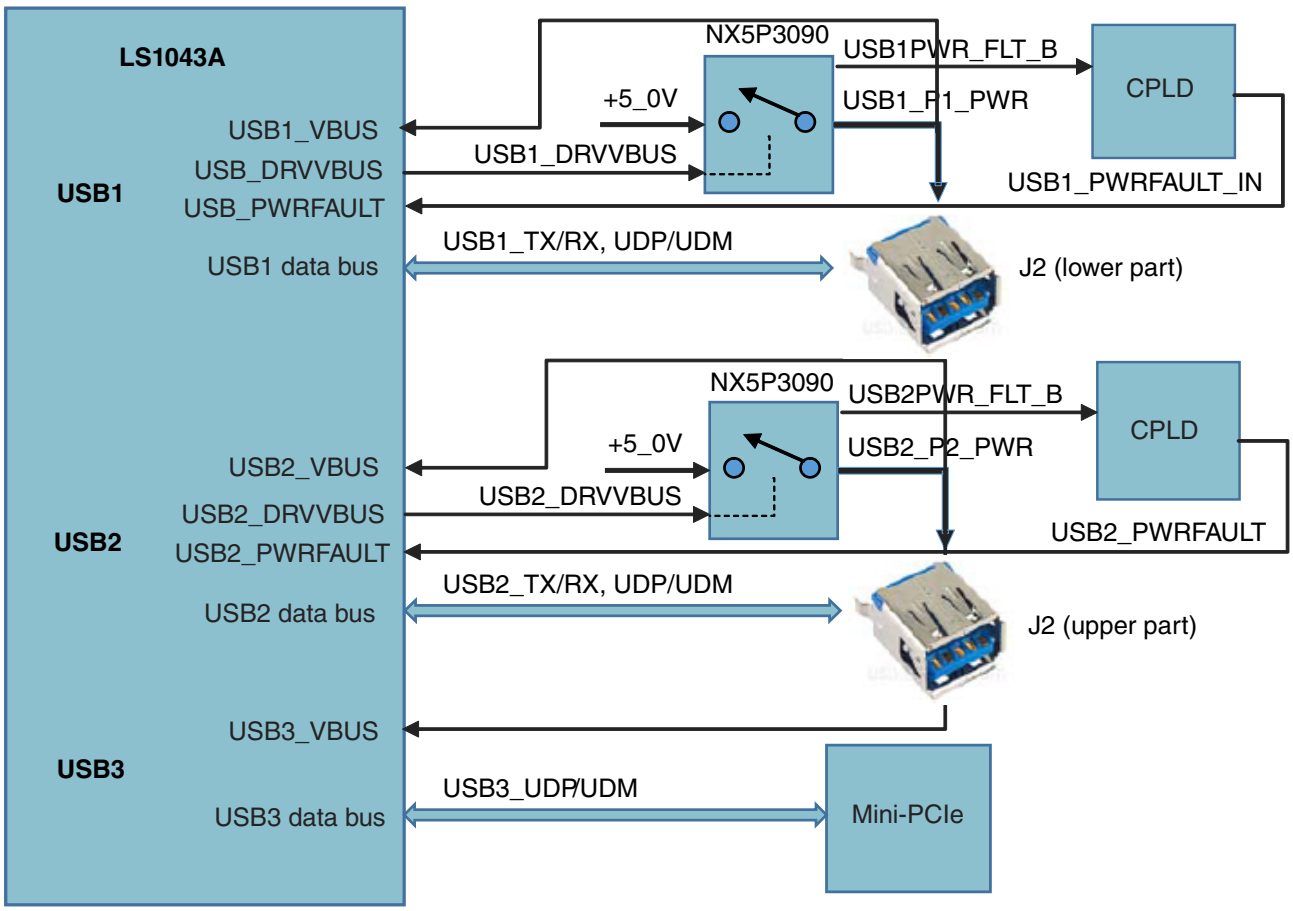

Figure 2-9. USB architecture

2.7 I2C interface

Although the LS1043A processor has up to four I2C buses, most of them are multiplexed pins. To simplify the circuit and save many mux/demux parts, LS1043ARDB attach all devices to I2C1 port.

The LS1043ARDB I2C has the following features:

- LS1043A I2C1 is attached to all local devices on the LS1043ARDB.
- I2C1 is also connected to the PCIe and mini-PCIe connectors. The slave address depends on the PCIe cards.
- LS1043A I2C2, I2C3, and I2C4 are not used as I2C but they are used as other multiplexed pin functions.

The figure below shows the overall I2C scheme connections.

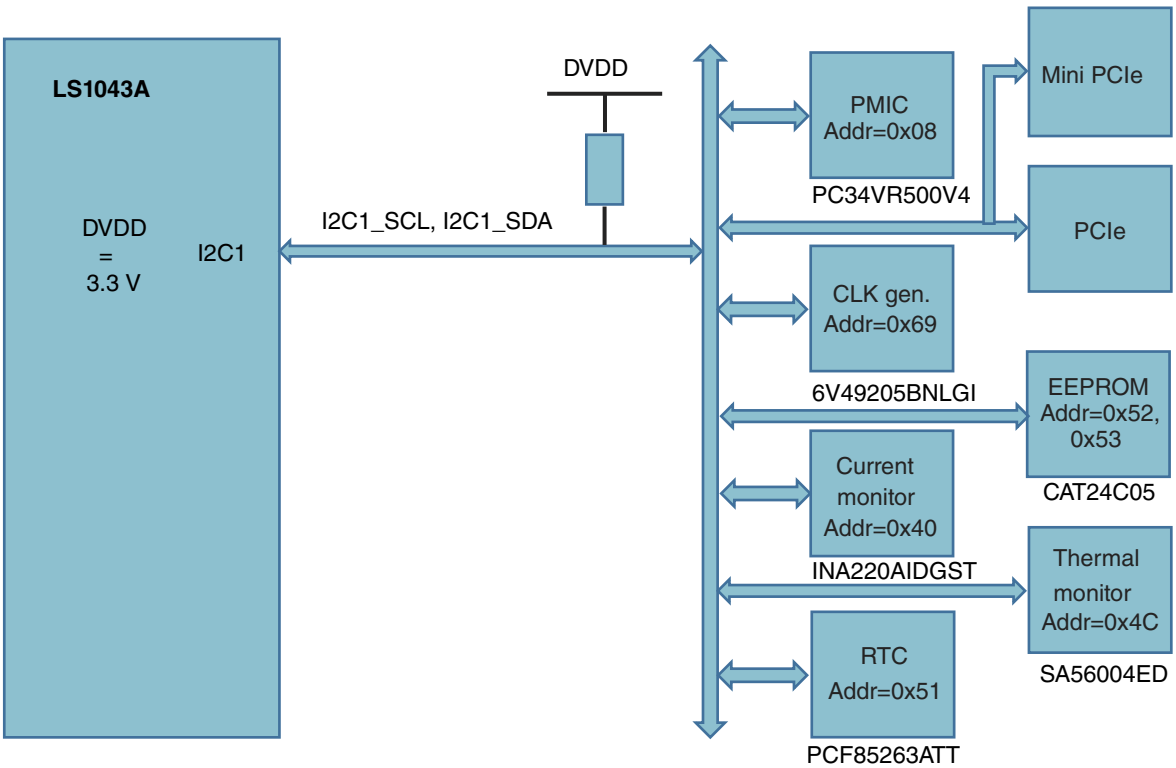

Figure 2-10. I2C scheme

The table below summarizes the I2C bus device addresses.

Table 2-9. I2C bus device map

I2C bus	I2C address	Device	Manufacturer	Description
I2C1	0x52, 0x53	CAT24C05	ON Semiconductor	Half of the device is used as an SPD EEPROM for DDR. The other half is used as a store system ID and MAC address.
	0x4C	SA56004ED	NXP Semiconductors	Thermal monitor
	0x08	PC34VR500V4	NXP Semiconductors	Power management integrated circuit (PMIC) for the onboard powers
	0x69	6V49205BNLGI	IDT	Clock generator
	0x40	INA220AIDGST	Texas Instruments	Current/power monitor
	0x51	PCF85263ATT	NXP Semiconductors	Real-time clock (RTC)
	I2C address is defined by the plugged-in PEX card	Mini-PCIe slot		
	I2C address is defined by the plugged-in PEX card	X1 PEX slot		

NOTE

7-bit addresses do not include the R/W bit as an address member, though some datasheets might do so. For consistency, all I2C addresses are of 7 bits only.

Chapter 3
Power Supplies and CPLD Controller

The LS1043ARDB power supplies provide all voltages necessary for the correct operation of the LS1043A device, DDR4, CPLD, Aquantia PHY, Realtek PHY, and all onboard peripherals.

The LS1043ARDB has an onboard CPLD that is used to configure the board for the required functionality, for example, managing system power and reset sequencing and controlling signal muxing/demuxing.

3.1 Power supply block diagram

The figure below shows the LS1043ARDB power supply block diagram.

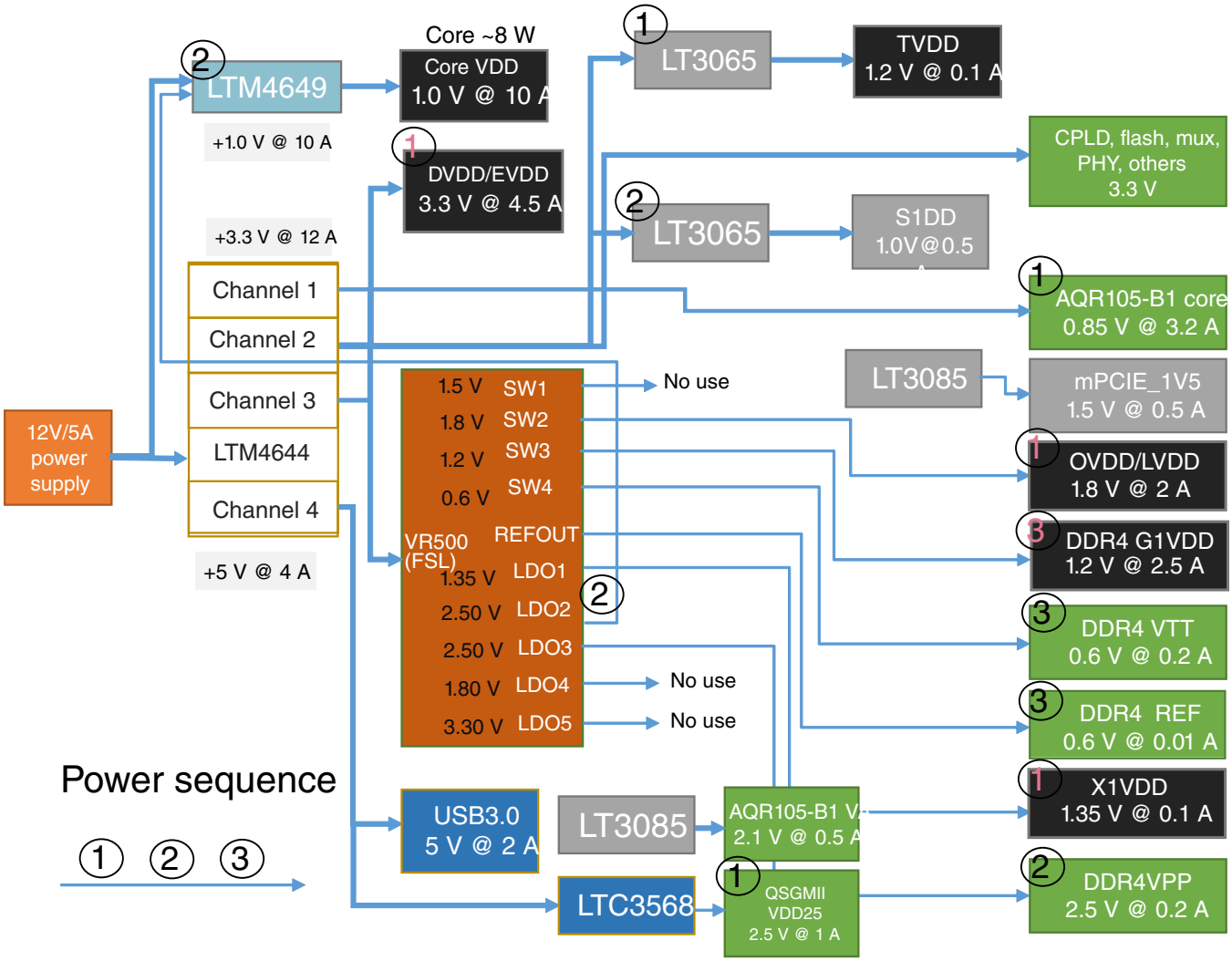

Figure 3-1. Power supply block diagram

3.2 Power supply operation

The power supply operation involves the following two activities:

- Power ON
- Power sequencing

3.2.1 Power ON

The SW2 switch, which is on the rear panel enables the 12 V power supply for the board.

3.2.2 Power sequencing

After 12 V power supply becomes available on the board, all power rails feeding the LS1043ARDB are automatically turned ON and sequenced by CPLD. Power is enabled in the following sequence:

1. TVDD, AVDD_SD1_PLL1, AVDD_SD1_PLL2, OVDD, DVDD, LVDD, EVDD, USB_HVDD, X1VDD
2. Core VDD, S1VDD, TA_BB_VDD, USB_SVDD, USB_SDVDD
3. G1VDD, DDR_VREF, DDR_VTT

3.3 CPLD controller

The LS1043ARDB complex programmable logic device (CPLD) controller allows you to control the functionality of the board. CPLD is powered from the local power supplies and gets clock input from an independent oscillator. This allows CPLD to control all aspects of board bring-up, including memory and reset. CPLD is implemented in a Lattice LCMXO1200C-3FTN256C, 256-ball BGA.

3.3.1 CPLD features

The LS1043ARDB contains a CPLD controller that implements the following functions:

- Reset signal generation and distribution. System reset features are:
  - Power-on reset (POR) for the LS1043A processor, NOR flash, PCIe, DDR, and PHY devices with initialization of all CPLD registers to their default values.
  - Manual reset: System resets and initializes all CPLD registers to their default values, after pressing the reset button.
  - Global register reset: Set register to reset the whole system, initializing all CPLD registers to their default values.
  - Local register reset: Set register to reset the whole system, maintaining all CPLD registers' current values.
- Power sequencing for the LS1043A regulators, including core VDD, GVDD, and others powers.
- Control POR sequencing: Configure the POR signals according to the external DIP switches or board requests.
- Control status LED
- Map/re-map the LS1043A local bus chip selects and ready and busy signals to NOR flash and NAND flash
- IFC bus control:

    - Latch out address lines IFC_ADDR[0:15] from multiplexed data and address lines
    - Read/write CPLD BCSR registers for board configuration
- Multiplexed pin selection:
    - Mux SDHC_CD_B, SDHC_WP, USB2_DRVVBUS, USB2_PWRFAULT, and TDM_CLK[9:12]
    - Select SD_DATA[4:7] and SPI_CS[0:3]_B
- NOR bank selection: Split NOR flash into 8 banks.

3.3.2 CPLD block diagram

The figure below shows a detailed block diagram of the CPLD controller on the LS1043ARDB.

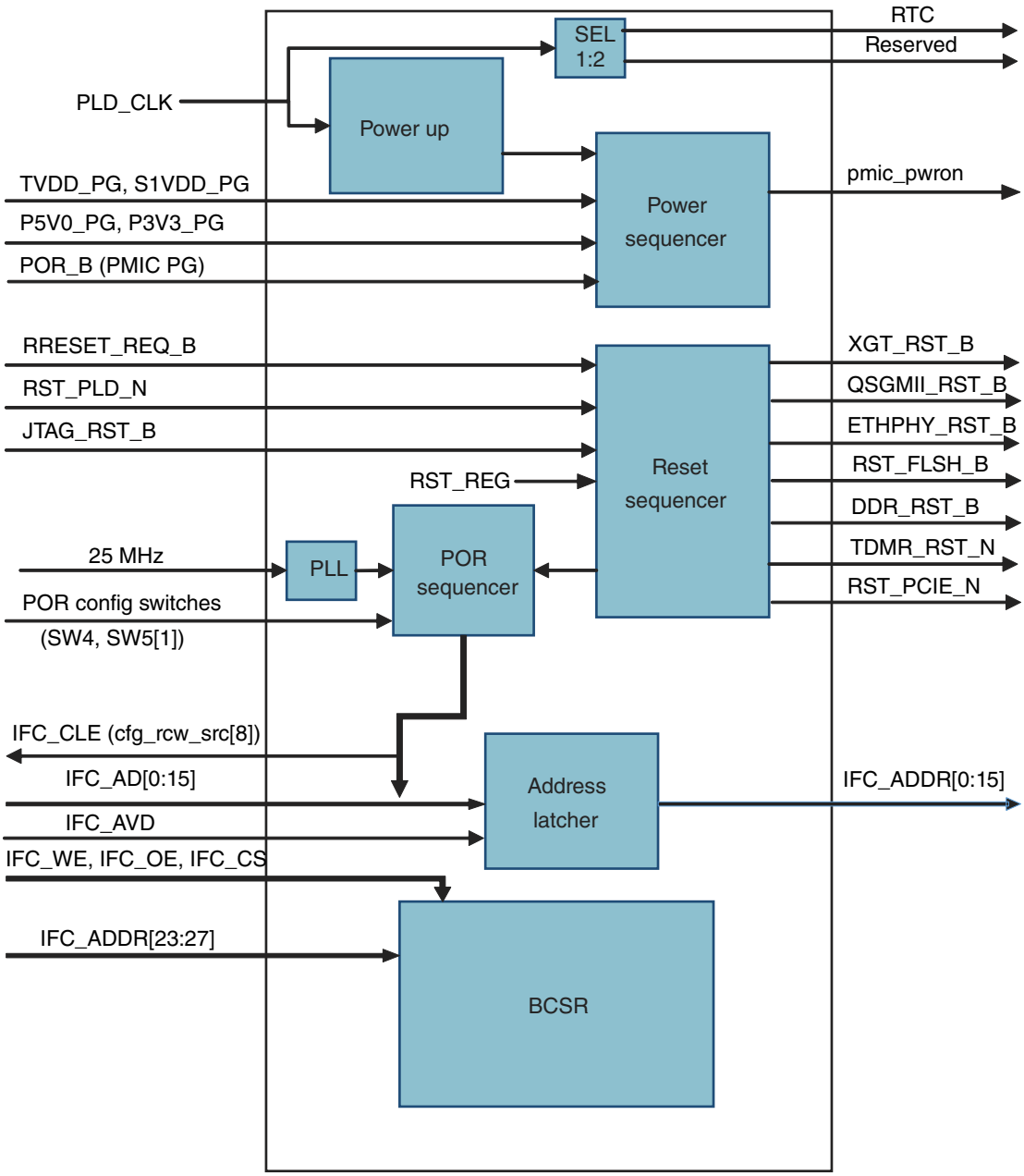

Figure 3-2. CPLD block diagram

3.3.3 CPLD registers

CPLD has a board control and status register (BCSR) address domain that contains registers memory mapped to the LS1043ARDB. These registers can be accessed from CPLD using IFC. The table below shows the peripheral data bus width and memory map for CPLD.

Table 3-1. CPLD memory map

Address	Chip select	Bank size	Device	Data width	Access
0x7FB00000 - 0x7FB0FFFF	CS2	64 KB	CPLD	8 bits	Read/write

For details on the CPLD registers, see CPLD Programming.

3.4 Power-on reset

The figure below shows a timing diagram of the power-on reset (POR) sequence.

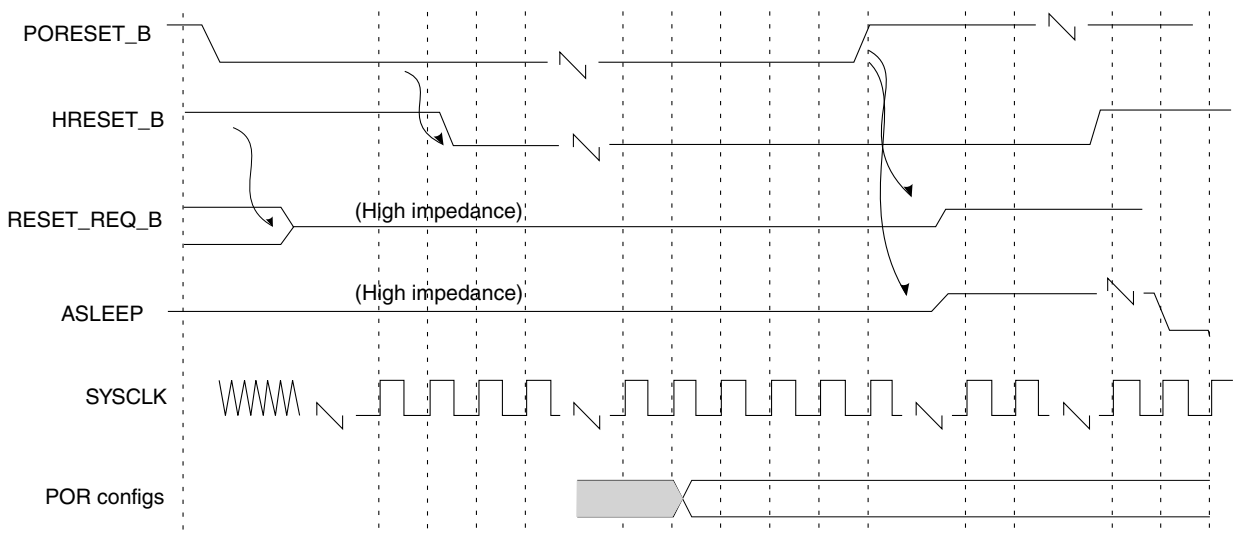

Figure 3-3. POR sequence

NOTE

Reset configuration input signals are only sampled at the negation of POR. Reset configuration input pins, such as CFG_RCW_SRC[0:8], CFG_GPINPUT[0:7], CFG_ENG_USE[0:2], and CFG_DRAM_TYPE function differently when the device is not in the Reset state.

The LS1043A control group signals are basically used to stop or restart an execution. PORESET_B indicates the power-on reset input signal. Use it for reset assertion. HRESET_B indicates the hard reset input signal. It is a bi-directional open drain signal. It functions as an output signal during initial steps in the POR sequence.

The table below describes the POR sequence.

Table 3-2. PORESET_B sequence

Step	Sequence stage	Description
1	PORESET_B: General information	1. PORESET_B is asserted. 2. CPLD drives CFG_RCW_SRC[0..8] and all reset configuration input signals to the LS1043A processor (see Reset configuration signals). 3. CPLD deasserts PORESET_B and the LS1043A processor samples the configuration pins. 4. The LS1043A processor asserts HRESET_B and loads RCW. 5. After RCW is loaded, the LS1043A processor deasserts HRESET_B.
2	PORESET_B: During negation	1. The LS1043A processor samples the configuration signals, and determines the interface to load RCW. 2. The LS1043A processor asserts HRESET_B throughout PORESET_B.
3	PORESET_B: After negation	The LS1043A processor begins the configuration process and starts loading RCW.
4	POR configuration input	The reset configuration inputs are sampled to determine: • Configuration source: CFG_RCW_SRC[0:8] • CFG_ENG_USE[0:2] • CFG_SOC_USE • CFG_GPINPUT[0:3] • DRAM type (DDR4 or DDR3L): CFG_DRAM_TYPE • CFG_IFC_TE
5	RCW configuration time	Time required varies according to the RCW source and CLKIN frequency.

NOTE

The LS1043ARDB has default DIP switch settings that can manually be repositioned based on the user-selected configuration levels.

3.4.1 Reset configuration signals

The table below describes the reset configuration input signals on the LS1043ARDB.

Table 3-3. Reset configuration input signals

Configuration signal	Pin location	DIP switch preset	Description
CFG_RCW_SRC0	IFC_CLE	SW4[1]	Specifies RCW fetch location
CFG_RCW_SRC1	IFC_AD8	SW4[2]	Specifies RCW fetch location
CFG_RCW_SRC2	IFC_AD9	SW4[3]	Specifies RCW fetch location
CFG_RCW_SRC3	IFC_AD10	SW4[4]	Specifies RCW fetch location
CFG_RCW_SRC4	IFC_AD11	SW4[5]	Specifies RCW fetch location
CFG_RCW_SRC5	IFC_AD12	SW4[6]	Specifies RCW fetch location
CFG_RCW_SRC6	IFC_AD13	SW4[7]	Specifies RCW fetch location

Table continues on the next page...

Table 3-3. Reset configuration input signals (continued)

Configuration signal	Pin location	DIP switch preset	Description
CFG_RCW_SRC7	IFC_AD14	SW4[8]	Specifies RCW fetch location
CFG_RCW_SRC8	IFC_AD15	SW5[1]	Specifies RCW fetch location
CFG_ENG_USE0	IFC_WE_0_B	SW5[2]	Selects differential or single-ended system clock
CFG_ENG_USE1	IFC_OE_B		
CFG_ENG_USE2	IFC_WP_0_B		
CFG_TEST_SEL	TEST_SEL_B	SW5[3]	
CFG_SOC_USE	ASLEEP	Pullup	
CFG_DRAM_TYPE	IFC_A21	Power down by R376	Specifies DRAM type

3.4.2 Reset architecture

The reset signals sent to and received from the LS1043A processor and other devices on the LS1043ARDB are managed by the CPLD controller.

The figure below shows the LS1043ARDB reset architecture.

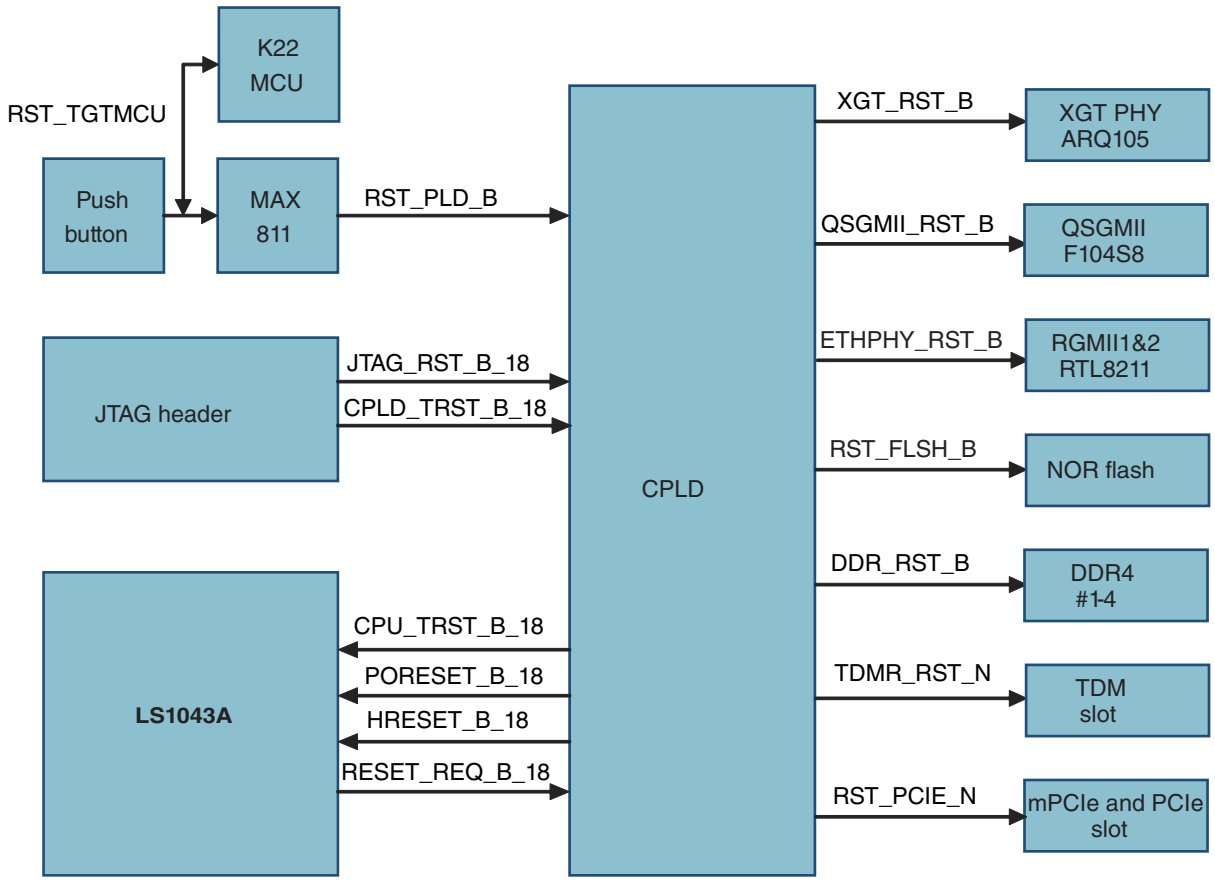

Figure 3-4. Reset architecture

3.5 DDR supply

The LS1043ARDB DDR power supply provides to the DDR4 interface the voltages shown in the table below.

Table 3-4. DDR supply voltages

Voltage name	Voltage	Current	Description
GVDD	1.2 V	<= 2.5 A	DRAM core and I/O voltage
DDR_VREFCA	0.6 V	>= 10 mA	DRAM reference voltage
DDR_VTT	0.6 V	<= 1 A	Bus termination supply
+2V5_VPP	2.5 V	< 200 mA	DRAM activating power supply

The LS1043ARDB uses the VR500 (U33) switching power controller as follows:

- VR500 SW3 generates GVDD up to 2.5 A at a default 1.2 V output for the LS1043A DDR controllers (GVDD) and all SDRAM GVDD supplies.
- VR500 SW4 generates VTT up to 1 A, and it is 50% of SW3 GVDD voltage as VTT. An LDO voltage regulator of VR500 generates 50% of GVDD voltage as VREF.

3.6 POVDD supply

J12 and J13 connectors on the LS1043ARDB connect POVDD power line to LS1043A PROG_MTR and PROG_SFP pins. Otherwise, they are pulled down to the ground plane.

Chapter 4
Clocks, Interrupts, and Temperature Monitoring

This chapter contains the following sections:

4.1 Clocking scheme

The figure below shows the LS1043ARDB clocking scheme.

NOTE

For RDBs, NXP Semiconductors does not support spread spectrum for SerDes clocking.

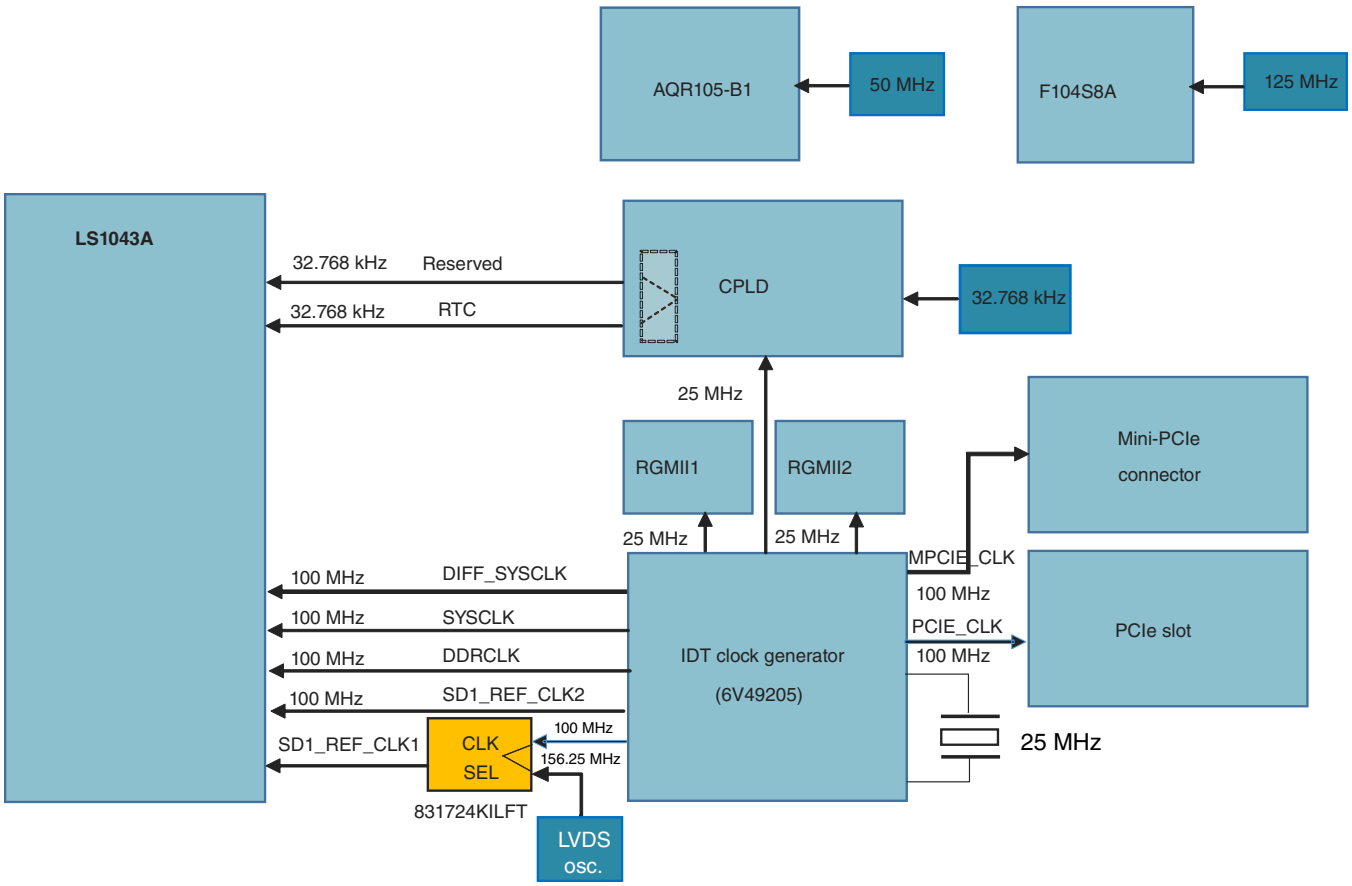

Figure 4-1. Clocking scheme

4.2 Clock frequency selection

In the LS1043ARDB, the default system clock is supplied by the 100 MHz differential system clock. It also supports single-ended clock source for SYSCLK and DDRCLK. Both the differential and single-ended system clocks are provided by an IDT 6V49205BNLGI device, which is a programmable frequency synthesizer with hardware presets. The device is configured such that it generates as output 100 MHz SYSCLK, 100 MHz DDRCLK, and 100 MHz differential system clock.

The table below shows how to select SYSCLK frequency based on the settings of the SW3 switch.

Table 4-1. SYSCLK frequency selection

SW3[1]	SW3[2]	Selected SYSCLK frequency
0	0	66.67 MHz
0	1	100.00 MHz (default value)
1	0	80.00 MHz

Table continues on the next page...

Table 4-1. SYSCLK frequency selection (continued)

SW3[1]	SW3[2]	Selected SYSCLK frequency
1	1	83.33 MHz

4.3 MPIC controller

The MPIC pins of the LS1043A processor are connected to several devices on board. Connection to the Interrupt sources are done through voltage level shifters. LS1043A MPIC assignments are listed in the table below.

Table 4-2. LS1043A interrupt assignments

Signal name	Supported function	Description
IRQ0_B	RGMII1, RGMII2, and QSGMII PHY interrupt	RTL8211FS and F104S8A PHY interrupt
IRQ1_B	10G Ethernet PHY interrupt	AQR105-B1 PHY interrupt
IRQ2_B	Thermal or PMIC interrupt	Thermal warning or fault interrupt or PMIC fault interrupt
IRQ11_B	TDM riser card interrupt	TDMR1 and TDMR2 interrupt

4.4 Temperature anode and cathode

The LS1043ARDB has two pins, TD1_Anode and TD1_Cathode. These pins are connected to a thermal body diode on the die that allows direct temperature measurement. The pins are connected to an SA56004ED device (U45) with dual-channel thermal monitor. This allows you to take direct die temperature readings with an accuracy of ±1 °C.

In addition to triggering the software interrupts in case of thermal problems, the SA56004ED temperature warning and alarm signals are used to drive indicators and are connected to CPLD for monitoring. CPLD uses these signals to power down the system to protect the LS1043ARDB from over-temperature failure.

Chapter 5
Debug and Input/Output

This chapter contains the following sections:

5.1 ARM/JTAG architecture

The ARM/JTAG architecture is shown in the figure below.

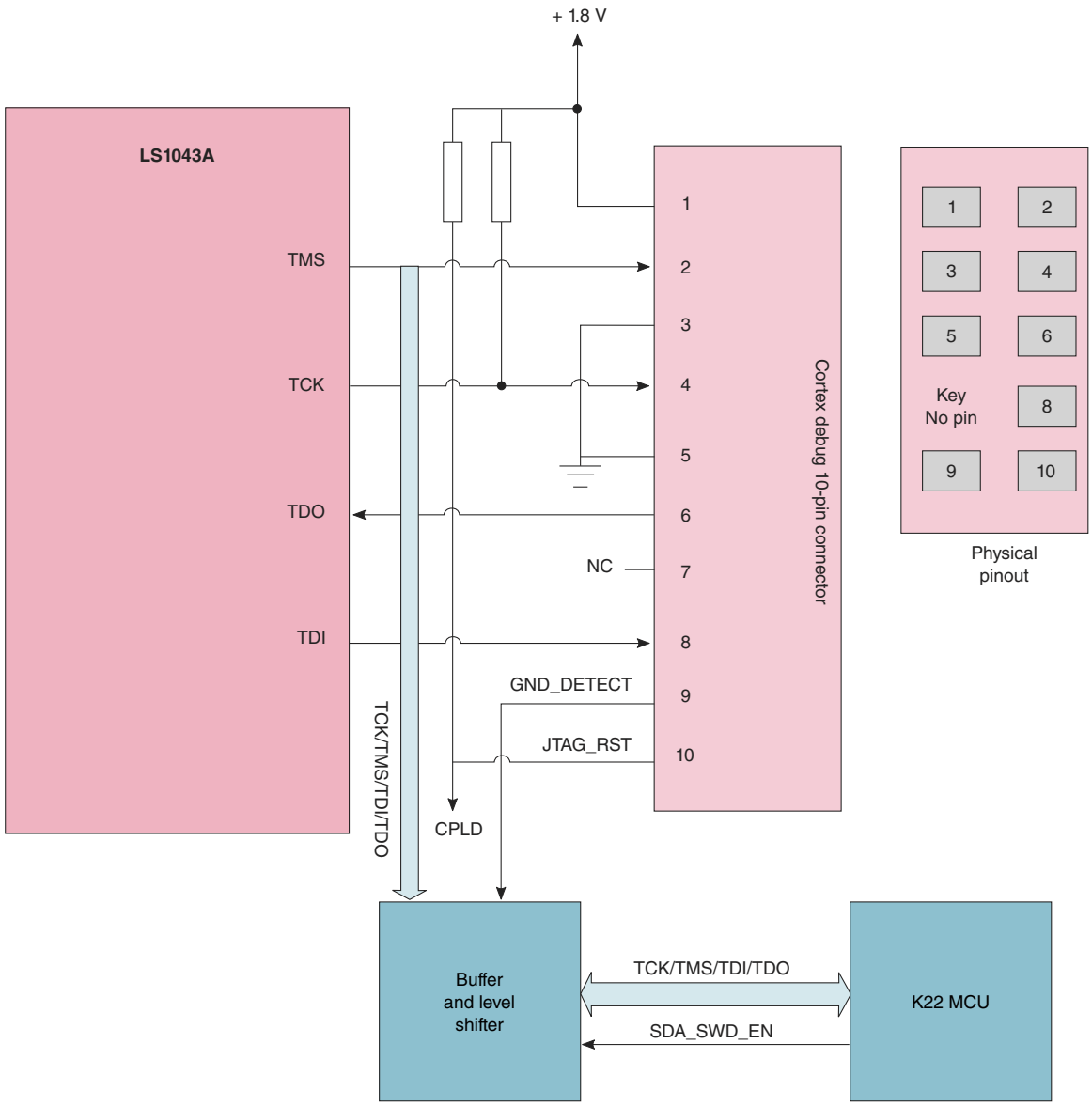

Figure 5-1. ARM/JTAG architecture

The LS1043ARDB has a JTAG header (J16) that helps the LS1043A processor to communicate externally with CodeWarrior TAP.

5.2 CMSIS-DAP

This section describes the MBED circuit on the LS1043ARDB. MBED is an open standard serial and debug adapter. It bridges serial and debug communications between a USB host and an embedded target processor, as shown in the figure below.

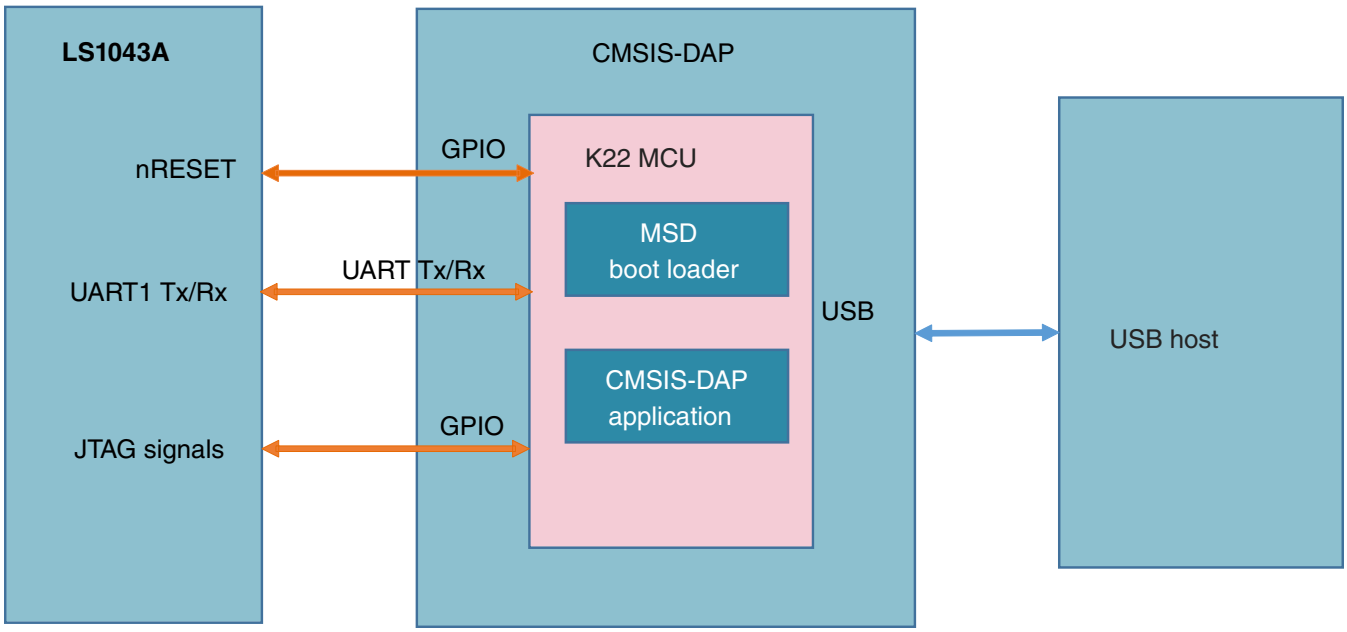

Figure 5-2. CMSIS-DAP

CMSIS-DAP is managed by a Kinetis K22 MCU built on the ARM Cortex-M4 core. The Kinetis K22 includes an integrated USB controller that can operate at clock rates of up to 120 MHz. The CMSIS-DAP circuit includes a status LED and a push button. The push button asserts the reset signal to the target processor. The GPIO signals provide an interface to a JTAG debug port on the target processor. In addition, signal connections are available to implement a UART serial channel.

CMSIS-DAP features a mass storage device (MSD) boot loader, which provides a quick and easy mechanism for loading different CMSIS-DAP applications, such as flash programmers, run control debug interfaces, serial-to-USB converters, and so on.

5.3 GPIOs

The LS1043ARDB has no dedicated general purpose input/output (GPIO) pins. Instead, GPIO functions are multiplexed internally on other signals, which must be disabled before using the GPIO functions. GPIO is not needed for board operation. Most of the GPIO pins are not available for external access because the pins are used for their primary functions. Some GPIO pins are connected to a test point to allow access. The names of the GPIO pins with and without test point access are shown in the table below.

Table 5-1. GPIO mapping

LS1043ARDB primary function	LS1043ARDB GPIO function	Connection	Description
IRQ[3]	GPIO1_23	TDMB_TSYNC	TDM slot
IRQ[4]	GPIO1_24	TDMA_RXD	TDM slot
IRQ[5]	GPIO1_25	TDMA_RSYNC	TDM slot
IRQ[6]	GPIO1_26	TDMA_TXD	TDM slot
IRQ[7]	GPIO1_27	TDMA_TSYNC	TDM slot
IRQ[8]	GPIO1_28	TDMB_RXD	TDM slot
IRQ[9]	GPIO1_29	TDMB_RSYNC	TDM slot
IRQ[10]	GPIO1_30	TDMB_TXD	TDM slot
IRQ[11]	GPIO1_31	CPLD	
ASLEEP	GPIO1_13	ALEEP LED	
RTC	GPIO1_14	RTC CLK	RTC clock

Chapter 6
CPLD Programming

This chapter describes the CPLD register user interface in the LS1043ARDB.

6.1 CPLD memory map / register definitions

The table below shows the memory map for the CPLD registers.

CPLD memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	CPLD major version register (CPLD_VER)	8	R	02h	6.1.1/52
1	CPLD minor version register (CPLD_VER_SUB)	8	R	00h	6.1.2/52
2	PCBA version register (CPLD_PCBA_VER)	8	R	05h	6.1.3/53
3	System reset register (CPLD_SYSTEM_RST)	8	R/W	00h	6.1.4/53
4	CPLD override physical switches enable register (CPLD_SOFT_MUX_ON)	8	R/W	00h	6.1.5/54
5	POR RCW source location register 1 (CPLD_REG_RCW_SRC1)	8	R/W	See section	6.1.6/55
6	POR RCW source location register 2 (CPLD_REG_RCW_SRC2)	8	R/W	See section	6.1.7/56
7	Flash bank selection register (CPLD_REG_BANK)	8	R/W	See section	6.1.8/56
8	System clock single-ended or differential input selection register (CPLD_SYSCLK_SEL)	8	R/W	See section	6.1.9/57
9	UART1 output selection register (CPLD_UART_SEL)	8	R/W	See section	6.1.10/58
A	SerDes PLL1 reference clock input selection register (CPLD_SD1REFCLK_SEL)	8	R/W	See section	6.1.11/58
B	TDM clock or SDHC/USB selection register (CPLD_TDMCLK_MUX_SEL)	8	R/W	See section	6.1.12/59
D	Status LED control register (CPLD_STATUS_LED)	8	R/W	00h	6.1.13/60
E	Global reset register (CPLD_GLOBAL_RST)	8	R/W	00h	6.1.14/60

Table continues on the next page...

CPLD memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
F	TDM riser card presence detection register (CPLD_TDMR_PRS_N)	8	R	01h	6.1.15/61
10	RTC clock assignment register (CPLD_REG_RTC)	8	R/W	00h	6.1.16/61
11	EVDD control register (CPLD_EVDD_SEL)	8	R/W	00h	6.1.17/62
12	CPLD register override physical switch SDHC_VS/SPI_CS0 enable register (CPLD_SOFT_VS_SPICS0)	8	R/W	00h	6.1.18/62
13	SDHC_VS or SPI_CS0 selection register (CPLD_VS_SPICS0_SEL)	8	R/W	See section	6.1.19/63

6.1.1 CPLD major version register (CPLD_VER)

Use this register to specify CPLD major version.

Address: 0h base + 0h offset = 0h

Bit	0	1	2	3	4	5	6	7
Read	VER				Reserved			
Write								
Reset	0	0	0	0	0	0	1	0

CPLD_VER field descriptions

Field	Description
0–3 VER	CPLD major version
4–7 -	This field is reserved.

6.1.2 CPLD minor version register (CPLD_VER_SUB)

Use this register to specify CPLD minor version.

Address: 0h base + 1h offset = 1h

Bit	0	1	2	3	4	5	6	7
Read	VER_SUB				Reserved			
Write								
Reset	0	0	0	0	0	0	0	0

CPLD_VER_SUB field descriptions

Field	Description
0–3 VER_SUB	CPLD minor version
4–7 -	This field is reserved.

6.1.3 PCBA version register (CPLD_PCBA_VER)

Use this register to specify printed circuit board assembly (PCBA) version.

Address: 0h base + 2h offset = 2h

Bit	0	1	2	3	4	5	6	7
Read	PCBA_VER							
Write								
Reset	0	0	0	0	0	1	0	1

CPLD_PCBA_VER field descriptions

Field	Description
0–7 PCBA_VER	PCBA version

6.1.4 System reset register (CPLD_SYSTEM_RST)

Write this register to reset the whole system, maintaining all CPLD registers' current values.

Address: 0h base + 3h offset = 3h

Bit	0	1	2	3	4	5	6	7
Read Write	SYSTEM_ RST	Reserved						
Reset	0	0	0	0	0	0	0	0

CPLD_SYSTEM_RST field descriptions

Field	Description
0 SYSTEM_RST	System reset

Table continues on the next page...

CPLD_SYSTEM_RST field descriptions (continued)

Field	Description
	0 System is running (default value) 1 System is reset
1–7 -	This field is reserved.

6.1.5 CPLD override physical switches enable register (CPLD_SOFT_MUX_ON)

Use this register to specify whether or not a CPLD override physical switch is enabled.

Address: 0h base + 4h offset = 4h

Bit	0	1	2	3
Read Write	RCW_SRC_LOC_CTRL_EN	SYSCLK_IN_CTRL_EN	UART1_OUT_CTRL_EN	SD1REFCLK_IN_CTRL_EN
Reset	0	0	0	0

Bit	4	5	6	7
Read Write	TDMCLK_SDHC_USB_IF_CTRL_EN	SDHC_SPICS_IF_CTRL_EN	FLASH_BANK_CTRL_EN	EVDD_CTRL_EN
Reset	0	0	0	0

CPLD_SOFT_MUX_ON field descriptions

Field	Description
0 RCW_SRC_LOC_CTRL_EN	RCW source location control enable 0 RCW source location control disable (default value) 1 RCW source location control enable
1 SYSCLK_IN_CTRL_EN	System clock single-ended or differential input control enable 0 System clock single-ended or differential input control disable (default value) 1 System clock single-ended or differential input control enable
2 UART1_OUT_CTRL_EN	UART1 output control enable 0 UART1 output control disable (default value) 1 UART1 output control enable
3 SD1REFCLK_IN_CTRL_EN	SerDes PLL1 reference clock input control enable 0 SerDes PLL1 reference clock input control disable (default value) 1 SerDes PLL1 reference clock input control enable

Table continues on the next page...

CPLD_SOFT_MUX_ON field descriptions (continued)

Field	Description
4 TDMCLK_ SDHC_USB_IF_ CTRL_EN	TDM CLK or SDHC/USB interface control enable 0 TDM CLK or SDHC/USB interface control disable (default value) 1 TDM CLK or SDHC/USB interface control enable
5 SDHC_SPICS_ IF_CTRL_EN	SDHC or SPI_CS interface control enable 0 SDHC or SPI_CS interface control disable (default value) 1 SDHC or SPI_CS interface control enable
6 FLASH_BANK_ CTRL_EN	Flash bank control enable 0 Flash bank control disable (default value) 1 Flash bank control enable
7 EVDD_CTRL_EN	EVDD voltage control enable 0 EVDD select disable (default value) 1 EVDD select enable

6.1.6 POR RCW source location register 1 (CPLD_REG_RCW_SRC1)

Use this register to configure RCW source bits 0-7.

Address: 0h base + 5h offset = 5h

Bit	0	1	2	3	4	5	6	7
Read Write	CFG_RCW_SRC[0:7]							
Reset	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW4[1] - SW4[8].

CPLD_REG_RCW_SRC1 field descriptions

Field	Description
0–7 CFG_RCW_ SRC[0:7]	POR RCW source location

6.1.7 POR RCW source location register 2 (CPLD_REG_RCW_SRC2)

Use this register to configure RCW source bit 8.

Address: 0h base + 6h offset = 6h

Bit	0	1	2	3	4	5	6	7
Read / Write	CFG_RCW_SRC[8]	Reserved						
Reset	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW5[1].

CPLD_REG_RCW_SRC2 field descriptions

Field	Description
0 CFG_RCW_SRC[8]	POR RCW source location
1–7 -	This field is reserved.

6.1.8 Flash bank selection register (CPLD_REG_BANK)

Use this register to select flash bank.

Address: 0h base + 7h offset = 7h

Bit	0	1	2	3	4	5	6	7
Read / Write	BANK_CTRL			Reserved				
Reset	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW5[4] - SW5[6].

CPLD_REG_BANK field descriptions

Field	Description
0–2 BANK_CTRL	Bank control bits

Table continues on the next page...

CPLD_REG_BANK field descriptions (continued)

Field	Description
3–7 -	This field is reserved.

6.1.9 System clock single-ended or differential input selection register (CPLD_SYSCLK_SEL)

Use this register to specify whether the system clock has single-ended input or differential input.

Address: 0h base + 8h offset = 8h

Bit	0	1	2	3
Read Write	SYSCLK_IN_SEL	Reserved		
Reset	0*	0*	0*	0*

Bit	4	5	6	7
Read Write	Reserved			
Reset	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW5[2].

CPLD_SYSCLK_SEL field descriptions

Field	Description
0 SYSCLK_IN_ SEL	System clock input selection 0 System clock differential input (default value) 1 System clock single-ended input
1–7 -	This field is reserved.

6.1.10 UART1 output selection register (CPLD_UART_SEL)

Use this register to specify output for UART1.

Address: 0h base + 9h offset = 9h

Bit	0	1	2	3	4	5	6	7
Read / Write	UART1_OUT_SEL	Reserved						
Reset	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW3[3].

CPLD_UART_SEL field descriptions

Field	Description
0 UART1_OUT_SEL	UART1 output selection 0 RJ45 1 CMSIS-DAP (default value)
1–7 -	This field is reserved.

6.1.11 SerDes PLL1 reference clock input selection register (CPLD_SD1REFCLK_SEL)

Use this register to specify input for the SerDes PLL1 reference clock.

Address: 0h base + Ah offset = Ah

Bit	0	1	2	3
Read / Write	SD1REFCLK_SEL	Reserved		
Reset	0*	0*	0*	0*

Bit	4	5	6	7
Read / Write	Reserved			
Reset	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW3[4].

CPLD_SD1REFCLK_SEL field descriptions

Field	Description
0 SD1REFCLK_ SEL	SerDes PLL1 reference clock input selection 0 100 MHz 1 156.25 MHz (default value)
1–7 -	This field is reserved.

6.1.12 TDM clock or SDHC/USB selection register (CPLD_TDMCLK_MUX_SEL)

Use this register to select TDM clock or SDHC/USB.

Address: 0h base + Bh offset = Bh

Bit	0	1	2	3	4	5	6	7
Read Write	TDMCLK_ SDHC_ USB_SEL	Reserved						
Reset	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW3[7].

CPLD_TDMCLK_MUX_SEL field descriptions

Field	Description
0 TDMCLK_ SDHC_USB_SEL	TDM clock or SDHC/USB selection 0 TDM_CLK 1 SDHC/USB (default value)
1–7 -	This field is reserved.

6.1.13 Status LED control register (CPLD_STATUS_LED)

Use this register to specify if status LED is ON or OFF.

Address: 0h base + Dh offset = Dh

Bit	0	1	2	3	4	5	6	7
Read / Write	STATUS_LED_CTRL	Reserved						
Reset	0	0	0	0	0	0	0	0

CPLD_STATUS_LED field descriptions

Field	Description
0 STATUS_LED_CTRL	Status LED control 0 LED OFF (default value) 1 LED ON
1–7 -	This field is reserved.

6.1.14 Global reset register (CPLD_GLOBAL_RST)

Write this register to reset the whole system, initializing all CPLD registers to their default values.

Address: 0h base + Eh offset = Eh

Bit	0	1	2	3	4	5	6	7
Read / Write	GLOBAL_RST	Reserved						
Reset	0	0	0	0	0	0	0	0

CPLD_GLOBAL_RST field descriptions

Field	Description
0 GLOBAL_RST	0 System is running (default value) 1 System is reset
1–7 -	This field is reserved.

6.1.15 TDM riser card presence detection register (CPLD_TDMR_PRS_N)

Use this register to indicate whether or not a TDM riser card is present on the LS1043ARDB board.

Address: 0h base + Fh offset = Fh

Bit	0	1	2	3	4	5	6	7
Read	TDMR_ PRS_N	Reserved						
Write								
Reset	0	0	0	0	0	0	0	1

CPLD_TDMR_PRS_N field descriptions

Field	Description
0 TDMR_PRS_N	TDM riser card presence detection 0 TDM riser card is present 1 TDM riser card is not present (default value)
1–7 -	This field is reserved.

6.1.16 RTC clock assignment register (CPLD_REG_RTC)

Use this register to indicate if the RTC clock is assigned to RTC.

Address: 0h base + 10h offset = 10h

Bit	0	1	2	3	4	5	6	7
Read	RTC_CLK_ ASSGNMT	Reserved						
Write								
Reset	0	0	0	0	0	0	0	0

CPLD_REG_RTC field descriptions

Field	Description
0 RTC_CLK_ ASSGNMT	RTC clock assignment to RTC (only assert from LS1043ARDB Rev. B board) 0 Reserved (default value) 1 To RTC

Table continues on the next page...

CPLD_REG_RTC field descriptions (continued)

Field	Description
1–7 -	This field is reserved.

6.1.17 EVDD control register (CPLD_EVDD_SEL)

Use this register to control the EVDD voltage.

Address: 0h base + 11h offset = 11h

Bit	0	1	2	3	4	5	6	7
Read Write	EVDD_SEL	Reserved						
Reset	0	0	0	0	0	0	0	0

CPLD_EVDD_SEL field descriptions

Field	Description
0 EVDD_SEL	EVDD voltage select register 0 3.3 V (default value) 1 1.8 V
1–7 -	This field is reserved.

6.1.18 CPLD register override physical switch SDHC_VS/ SPI_CS0 enable register (CPLD_SOFT_VS_SPICS0)

Use this register to enable CPLD register value override physical switch to select SDHC_VS or SPI_CS0.

Address: 0h base + 12h offset = 12h

Bit	0	1	2	3
Read Write	VS_SPICS0_EN	Reserved		
Reset	0	0	0	0

Bit	4	5	6	7
Read Write	Reserved			
Reset	0	0	0	0

CPLD_SOFT_VS_SPICS0 field descriptions

Field	Description
0 VS_SPICS0_EN	SDHC_VS or SPI_CS0 CPLD register control enable 0 SDHC_VS or SPI_CS0 CPLD register control disable (default value) 1 SDHC_VS or SPI_CS0 CPLD register control enable
1–7 -	This field is reserved.

6.1.19 SDHC_VS or SPI_CS0 selection register (CPLD_VS_SPICS0_SEL)

Use this register to select SDHC_VS or SPI_CS0.

Address: 0h base + 13h offset = 13h

Bit	0	1	2	3
Read Write	VS_SPICS0_SEL	Reserved		
Reset	0*	0*	0*	0*

Bit	4	5	6	7
Read Write	Reserved			
Reset	0*	0*	0*	0*

* Notes:
- The register reset value is controlled by SW3[8].

CPLD_VS_SPICS0_SEL field descriptions

Field	Description
0 VS_SPICS0_SEL	SDHC_VS or SPI_CS0 CPLD selection 0 SDHC_VS (default value) 1 SPI_CS0
1–7 -	This field is reserved.

Appendix A
Board Revision History

The table below provides the revision history of the board (LS1043ARDB).

Table A-1. Board revision history

Manufacturing part number	Major changes	Silicon revision	Schematic revision	Layout revision
LS1043ARDB-PB	Changed silicon to 1.6 GHz	V1.0, 1.6 GHz	SCH-28529 Rev. C, C1	LAY-28529 Rev. C
LS1043ARDB-PC	Changed silicon to version 1.1	V1.1, 1.6 GHz	SCH-28529 Rev. C2	LAY-28529 Rev. C
LS1043ARDB-PD	Replaced SIP components (buffer, USB switch, level shifter, temperature sensor, and so on) from other vendors with components from NXP	V1.1, 1.6 GHz	SCH-28529 Rev. D , D1, E	LAY-28529 Rev. D, E

Appendix B
Document Revision History

The table below provides the revision history of this document.

Revision number	Date	Topic cross-reference	Change description
Rev. 4	11/2017	Introduction	Changed the LS1043ARDB part number from LS1043ARDB-PB to LS1043ARDB-PD
		Block diagrams	Updated processor block diagram
		eSDHC interface	• Updated second item in the eSDHC features list • Updated Figure 2-4
		DSPI interface	• Updated DSPI features list • Updated Figure 2-5 • Updated Table 2-4
		USB interface	Replaced MAX1588 devices with NX5P3090UK devices from NXP
		I2C interface	Updated information related to thermal monitor and RTC
		MPIC controller	Updated first row in Table 4-2
		CPLD memory map / register definitions	• Removed the CPLD_SDHC_SPICS_SEL register • Added two new registers, CPLD_SOFT_VS_SPICS0 and CPLD_VS_SPICS0_SEL • Updated reset values for CPLD_VER, CPLD_VER_SUB, and CPLD_PCBA_VER registers
		Board Revision History	Added as a new appendix
Rev. 3	12/2016	Board features	Updated the section
		Figure 1-2	Updated the figure
		Ethernet management interfaces	Updated the section
			Removed TA_BB_RTC instances from the document as TA_BB_RTC has been defeatured
			Removed CFG_SVR instances from the document
Rev. 2	08/2016	eSDHC interface	Updated the section

Table continues on the next page...

Revision number	Date	Topic cross-reference	Change description
		GPIOs	Updated the section
		CPLD Programming	• Updated the reset value of the CPLD_VER_SUB register • Updated details of bit 7 of the CPLD_SOFT_MUX_ON register • Added a new register, CPLD_EVDD_SEL
Rev. 1	11/2015	Introduction	Changed the LS1043ARDB part number from LS1043ARDB-PA to LS1043ARDB-PB
		Board features	Changed core clock frequency from 1.5 GHz to 1.6 GHz in Table 1-3
		CPLD memory map / register definitions	• Changed the reset value of the CPLD_VER_SUB register to 04h • Changed the reset value of the CPLD_PCBA_VER register to 03h
Rev. 0	08/2015		Initial public release

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