



N-Channel 25 V (D-S) MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	25			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00265			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.00390			
Q _g typ. (nC)	13.2			
I _D (A)	60 ^{a, g}			
Configuration	Single			

FEATURES

TrenchFET® Gen IV power MOSFET



 \bullet Optimized $Q_g,\ Q_{gd},\ and\ Q_{gd}/Q_{gs}$ ratio reduces switching related power loss

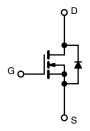
COMPLIANT HALOGEN **FREE**

100 % R_a and UIS tested

· Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Synchronous buck converter
- · Load switching



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8 Single
Lead (Pb)-free and halogen-free	SiSA26DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	25	V	
Gate-source voltage		V _{GS}	+16 / -12		
	T _C = 25 °C		60 ^a		
Continuous drain current (T _J = 150 °C)	T _C = 70 °C	1 . [60 ^a		
	T _A = 25 °C	I _D	29.1 ^{b, c}		
	T _A = 70 °C	1 [23.3 b, c	Δ.	
Pulsed drain current (t = 100 µs)		I _{DM}	150	A	
Continuous source-drain diode current	T _C = 25 °C		35.4		
	T _A = 25 °C	ls l	3.2 b, c		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	25		
Single pulse avalanche energy	L = U. I MIH	E _{AS}	31.2	mJ	
Maximum power dissipation	T _C = 25 °C		39		
	T _C = 70 °C	1 . [25	W	
	T _A = 25 °C	I _P	3.6 ^{b, c}	VV	
	T _A = 70 °C	1 [2.3 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^c			260	-0	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	26	34	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJF}	2.5	3.2	C/VV

Notes

- Package limited.
 Surface mounted on 1" x 1" FR4 board.
- c. 1-105.
 d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
 e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
 f. Maximum under steady state conditions is 81 °C/W.

- $T_C = 25$ °C.



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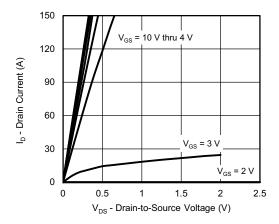
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	19	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4.5	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	2.5	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +16 \text{ / } -12 \text{ V}$	-	-	100	nA	
		V _{DS} = 25 V, V _{GS} = 0 V	-	-	1		
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$	-	-	15	μA	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α	
Delice and a selection of the selection		V _{GS} = 10 V, I _D = 15 A	-	0.00215	0.00265	- Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.00315	0.00390		
Forward transconductance a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	-	88	-	S	
Dynamic ^b					•		
Input capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	2247	-	pF	
Output capacitance	C _{oss}		-	730	-		
Reverse transfer capacitance	C _{rss}		-	105	-		
Tatal mate about	0	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	29	44	nC	
Total gate charge	Q_g		-	13.2	20		
Gate-source charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	5.4	-		
Gate-drain charge	Q_{gd}		-	3.2	-		
Gate resistance	R_g	f = 1 MHz	0.2	0.8	1.5	Ω	
Turn-on delay time	t _{d(on)}		-	9	18		
Rise time	t _r	$V_{DD} = 10 \text{ V}, R_L = 1 \Omega, I_D \cong 10 \text{ A},$	-	23	46		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	16	32		
Fall time	t _f		-	8	16		
Turn-on delay time	t _{d(on)}		-	17	34	ns	
Rise time	t _r	$V_{DD} = 10 \text{ V}, \text{ R}_{L} = 1 \Omega, \text{ I}_{D} \cong 10 \text{ A},$	-	48	96	-	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	13	26		
Fall time	t _f		-	13	26		
Drain-Source Body Diode Characteristi	cs				•		
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	35.4	^	
Pulse diode forward current	I _{SM}		-	-	150	A	
Body diode voltage	V_{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.75	1.1	V	
Body diode reverse recovery time	t _{rr}		-	29	58	ns	
Body diode reverse recovery charge	Q _{rr}	1 10 A 41/44 100 A/ T 05 00	-	16	32	nC	
Reverse recovery fall time	t _a	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	-	12	-	ns	
Reverse recovery rise time	t _b		-	17	-		

Notes

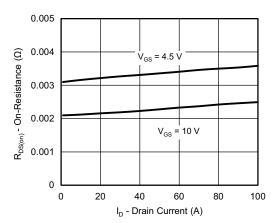
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

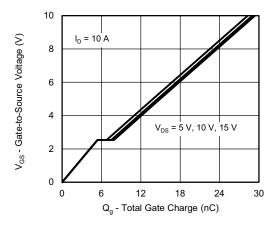




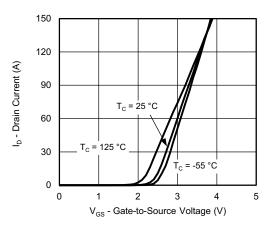
Output Characteristics



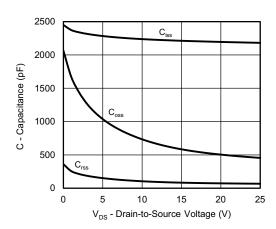
On-Resistance vs. Drain Current and Gate Voltage



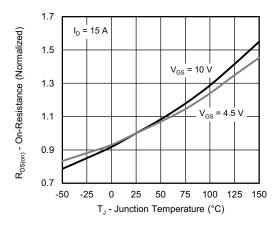
Gate Charge



Transfer Characteristics

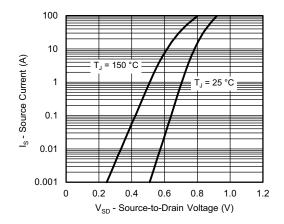


Capacitance

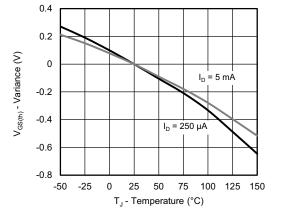


On-Resistance vs. Junction Temperature

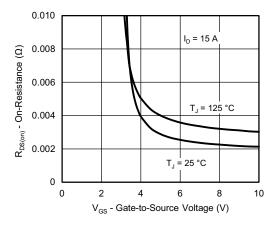




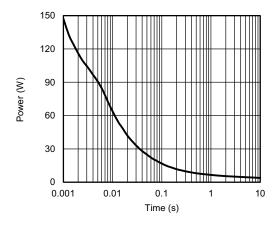
Source-Drain Diode Forward Voltage



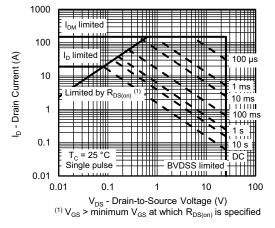
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

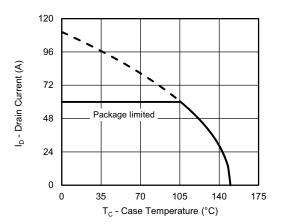


Single Pulse Power, Junction-to-Ambient

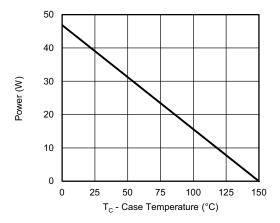


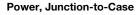
Safe Operating Area, Junction-to-Ambient

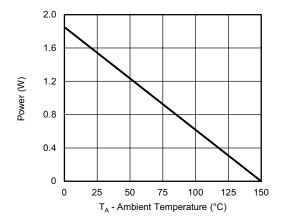




Current Derating a





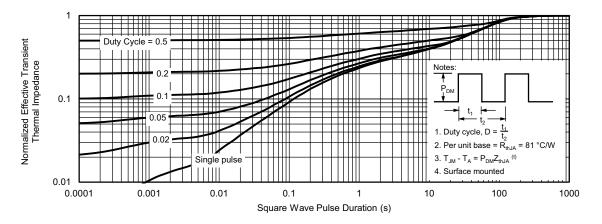


Power, Junction-to-Ambient

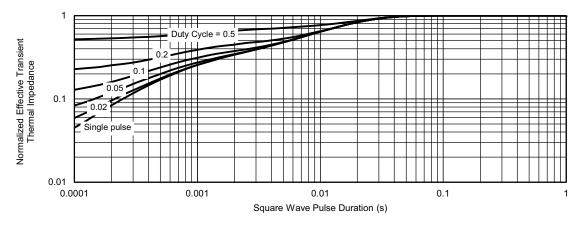
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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