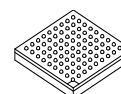




MIMXRT1064DVL6A

i.MX RT1064 Crossover Processors for Consumer Products



Package Information

Plastic Package

196-pin MAPBGA, 10 x 10 mm, 0.65 mm pitch

Ordering Information

See [Table 1 on page 5](#)

1 i.MX RT1064 Introduction

The i.MX RT1064 is a new processor family featuring NXP's advanced implementation of the Arm Cortex®-M7 core, which operates at speeds up to 600 MHz to provide high CPU performance and best real-time response.

The i.MX RT1064 processor has 4 MB on chip Flash and 1 MB on-chip RAM. 512 KB SRAM can be flexibly configured as TCM or general-purpose on-chip RAM, while the other 512 KB SRAM is general-purpose on-chip RAM. The i.MX RT1064 integrates advanced power management module with DCDC and LDO that reduces complexity of external power supply and simplifies power sequencing. The i.MX RT1064 also provides various memory interfaces, including SDRAM, RAW NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. The i.MX RT1064 has rich audio and video features, including LCD display, basic 2D graphics, camera interface, SPDIF, and I2S audio

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interface. The i.MX RT1064 has analog interfaces, such as ADC, ACMP, and TSC.

The i.MX RT1064 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance

1.1 Features

The i.MX RT1064 processors are based on Arm Cortex-M7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-M7 MPCore with:
 - 32 KB L1 Instruction Cache
 - 32 KB L1 Data Cache
 - Full featured Floating Point Unit (FPU) with support of the VFPv5 architecture
 - Support the Armv7-M Thumb instruction set
- Integrated MPU, up to 16 individual protection regions
- Tightly coupled GPIOs, operating at the same frequency as Arm
- Up to 512 KB I-TCM and D-TCM in total
- Frequency of 600/528 MHz
- Cortex M7 CoreSight™ components integration for debug
- Frequency of the core, as per [Table 9, "Operating ranges," on page 19](#).

The SoC-level memory system consists of the following additional components:

- Boot ROM (128 KB)
- On-chip Flash (4 MB)
- On-chip RAM (1 MB)
 - 512 KB OCRAM shared between ITCM/DTCM and OCRAM
 - Dedicate 512 KB OCRAM
- External memory interfaces:
 - 8/16-bit SDRAM, up to SDRAM-133/SDRAM-166
 - 8/16-bit SLC NAND FLASH, with ECC handled in software
 - SD/eMMC
 - SPI NOR FLASH
 - Parallel NOR FLASH with XIP support
 - Two single/dual channel Quad SPI FLASH with XIP support
- Timers and PWMs:
 - Two General Programmable Timers (GPT)
 - 4-channel generic 32-bit resolution timer
 - Each support standard capture and compare operation

- Four Periodical Interrupt Timers (PIT)
 - Generic 32-bit resolution timer
 - Periodical interrupt generation
- Four Quad Timers (QTimer)
 - 4-channel generic 16-bit resolution timer for each
 - Each support standard capture and compare operation
 - Quadrature decoder integrated
- Four FlexPWMs
 - Up to 8 individual PWM channels per each
 - 16-bit resolution PWM suitable for Motor Control applications
- Four Quadrature Encoder/Decoders

Each i.MX RT1064 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display Interface:
 - Parallel RGB LCD interface
 - Support 8/16/24 bit interface
 - Support up to WXGA resolution
 - Support Index color with 256 entry x 24 bit color LUT
 - Smart LCD display with 8/16-bit MPU/8080 interface
- Audio:
 - S/PDIF input and output
 - Three synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
 - MQS interface for medium quality audio via GPIO pads
- Generic 2D graphics engine:
 - BitBlit
 - Flexible image composition options—alpha, chroma key
 - Porter-duff blending
 - Image rotation (90°, 180°, 270°)
 - Image size
 - Color space conversion
 - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
 - Standard 2D-DMA operation
- Camera sensors:
 - Support 24-bit, 16-bit, and 8-bit CSI input
- Connectivity:
 - Two USB 2.0 HS OTG controllers with integrated PHY interfaces

- Two Ultra Secure Digital Host Controller (uSDHC) interfaces
 - MMC 4.5 compliance with HS200 support up to 200 MB/sec
 - SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec
 - Support for SDXC (extended capacity)
- Two 10/100M Ethernet controller with support for IEEE1588
- Eight universal asynchronous receiver/transmitter (UARTs) modules
- Four I2C modules
- Four SPI modules
- Two FlexCAN modules
- FlexCAN (with Flexible Data-Rate supported)
- Three FlexIO modules
- GPIO and Pin Multiplexing:
 - General-purpose input/output (GPIO) modules with interrupt capability
 - Input/output multiplexing controller (IOMUXC) to provide centralized pad control

The i.MX RT1064 processors integrate advanced power management unit and controllers:

- Full PMIC integration, including on-chip DCDC and LDO
- Temperature sensor with programmable trim points
- GPC hardware power management controller

The i.MX RT1064 processors support the following system debug:

- Arm CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) and SWD debug interfaces

The i.MX RT1064 processors support the following analog interfaces:

- Three Analog-Digital-Converters (ADC), one of which supports differential inputs
- Two Digital-Analog-Converters (DAC)
- Four Analog Comparators (ACMP)

Security functions are enabled and accelerated by the following hardware:

- High Assurance Boot (HAB)
- Data Co-Processor (DCP):
 - AES-128, ECB, and CBC mode
 - SHA-1 and SHA-256
 - CRC-32
- Bus Encryption Engine (BEE)
 - AES-128, ECB, and CTR mode
 - On-the-fly QSPI Flash decryption
- True random number generation (TRNG)

- Secure Non-Volatile Storage (SNVS)
 - Secure real-time clock (RTC)
 - Zero Master Key (ZMK)
- Secure JTAG Controller (SJC)

NOTE

The actual feature set depends on the part numbers as described in [Table 1](#). Functions such as display and camera interfaces, connectivity interfaces, and security features are not offered on all derivatives.

1.2 Ordering information

[Table 1](#) provides examples of orderable part numbers covered by this Data Sheet.

Table 1. Ordering information

| Part Number | Feature | | Package | Junction Temperature T _j (°C) |
|-----------------|--|---|---|--|
| MIMXRT1064DVL6A | Features supports: <ul style="list-style-type: none"> • 600 MHz, commercial grade for general purpose, with MPU/FPU • 4 MB Flash • eDMA • Boot ROM (128 KB) • On-chip RAM (1 MB) • SEMC • GPT x2 • 4-channel PIT • Qtimer x4 • PWM x4 • ENC x4 • WDOG x4 • No LCD/CSI/PXP • SPDIF x1 • SAI x3 • MQS x1 • USB OTG x2 • eMMC 4.5/SD 3.0 x2 | <ul style="list-style-type: none"> • Ethernet x2 • UART x8 • I2C x4 • FlexSPI x2 • CAN x2 • FlexCAN (with Flexible Data-Rate supported) • FlexIO x3 • 127 GPIOs (124 tightly coupled) • HAB/DCP/BEE • TRNG • SNVS • SJC • ADC x2 • ACMP x4 • TSC • DCDC • Temperature sensor • GPC hardware power management controller | 10 x 10 mm, 0.65 mm pitch, 196-pin MAPBGA | 0 to +85 |

[Figure 1](#) describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/IMX-RT_SERIES or contact an NXP representative for details.

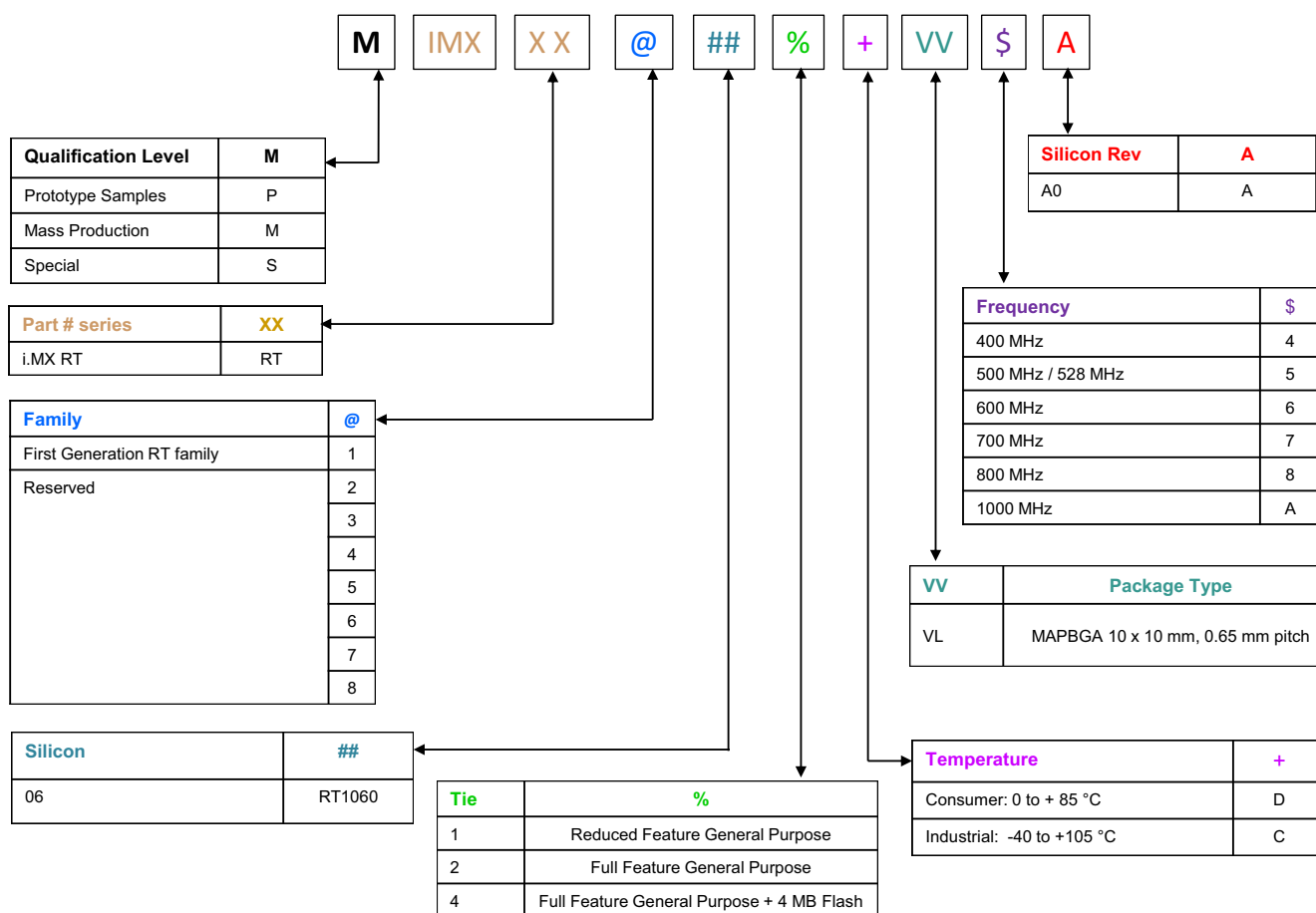


Figure 1. Part number nomenclature—i.MX RT1064

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX RT1064 processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX RT1064 processor system.

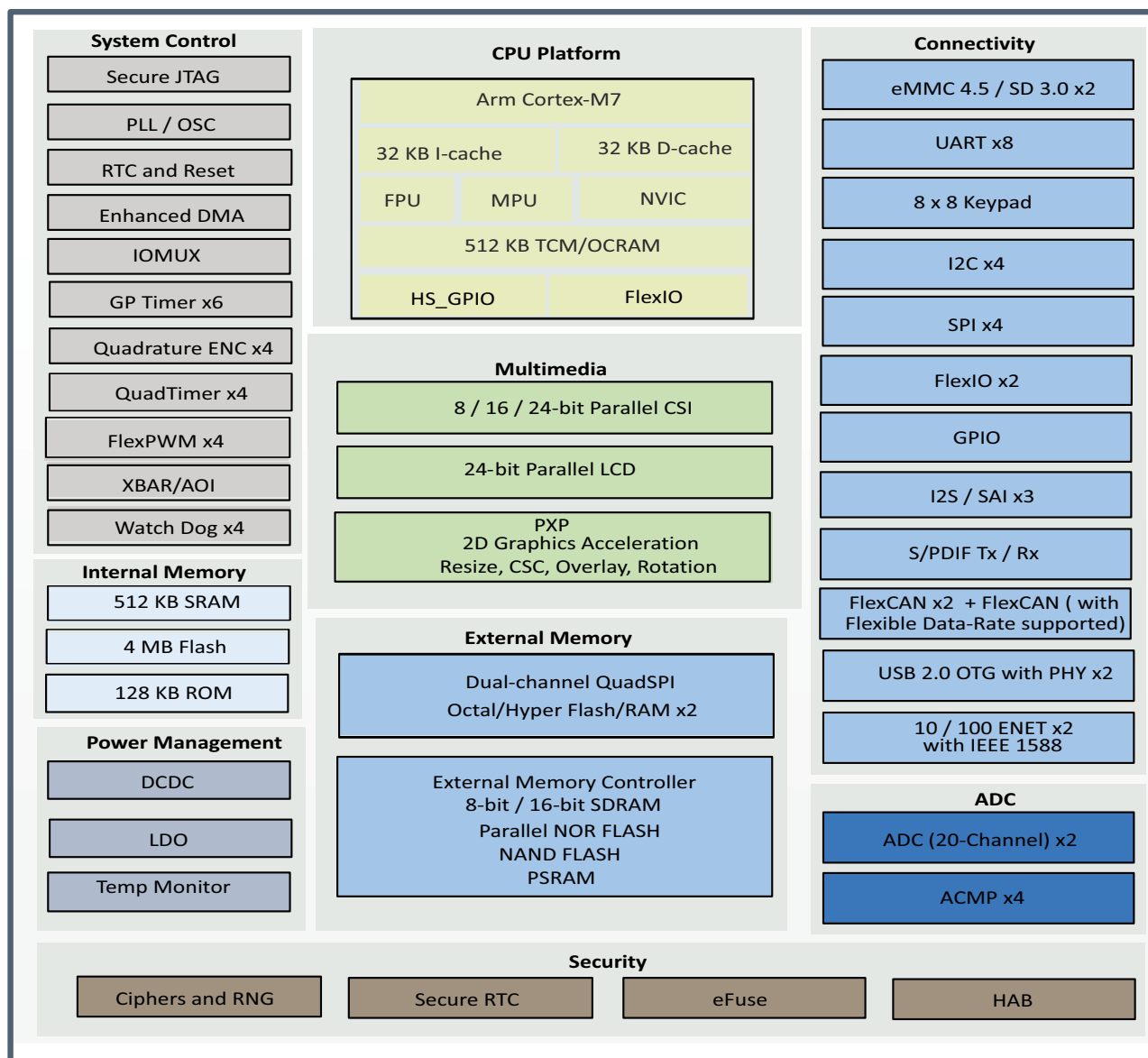


Figure 2. i.MX RT1064 system block diagram

3 Modules List

The i.MX RT1064 processors contain a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

Table 2. i.MX RT1064 modules list

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------------------------|---|-----------------------------------|---|
| ACMP1 ACMP2 ACMP3 ACMP4 | Analog Comparator | Analog | The comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation). |
| ADC1 ADC2 | Analog to Digital Converter | Analog | The ADC is a 12-bit general purpose analog to digital converter. |
| AOI | And-Or-Inverter | Cross Trigger | The AOI provides a universal boolean function generator using a four term sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D). |
| Arm | Arm Platform | Arm | The Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), and CoreSight debug modules. |
| BEE | Bus Encryption Engine | Security | On-The-Fly FlexSPI Flash Decryption |
| CCM GPC SRC | Clock Control Module, General Power Controller, System Reset Controller | Clocks, Resets, and Power Control | These modules are responsible for clock and reset distribution in the system, and also for the system power management. |
| CSI | Parallel CSI | Multimedia Peripherals | The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input. |
| CSU | Central Security Unit | Security | The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX RT1064 platform. |
| DAP | Debug Access Port | System Control Peripherals | The DAP provides real-time access for the debugger without halting the core to: <ul style="list-style-type: none"> • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform. |

Table 2. i.MX RT1064 modules list (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------------|----------------------------------|----------------------------|--|
| DCDC | DCDC Converter | Analog | The DCDC module is used for generating power supply for core logic. Main features are: <ul style="list-style-type: none"> Adjustable high efficiency regulator Supports 3.3 V input voltage Supports nominal run and low power standby modes Supports at 0.9 ~ 1.3 V output in run mode Supports at 0.9 ~ 1.0 V output in standby mode Over current and over voltage detection |
| eDMA | enhanced Direct Memory Access | System Control Peripherals | There is an enhanced DMA (eDMA) engine and two DMA_MUX. <ul style="list-style-type: none"> The eDMA is a 32 channel DMA engine, which is capable of performing complex data transfers with minimal intervention from a host processor. The DMA_MUX is capable of multiplexing up to 128 DMA request sources to the 32 DMA channels of eDMA. |
| ENC | Quadrature Encoder/Decoder | Timer Peripherals | The enhanced quadrature encoder/decoder module provides interfacing capability to position/speed sensors. There are five input signals: PHASEA, PHASEB, INDEX, TRIGGER, and HOME. This module is used to decode shaft position, revolution count, and speed. |
| ENET1 ENET2 | Ethernet Controller | Connectivity Peripherals | The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details. |
| EWM | External Watchdog Monitor | Timer Peripherals | The EWM modules is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode. |
| FLEXCAN1 FLEXCAN2 | Flexible Controller Area Network | Connectivity Peripherals | The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames. |

Table 2. i.MX RT1064 modules list (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|----------------------------------|---------------------------------|---|
| FLEXCAN (FD) | Flexible Controller Area Network | Connectivity Peripherals | The CAN with Flexible Data-Rate protocol and the CAN 2.0 version B protocol supports both standard and extended message frames, both of them have long payloads up to 64 bytes transferred at faster rates up to 8 Mbps. |
| FlexIO1 FlexIO2 FlexIO3 | Flexible Input/output | Connectivity and Communications | The FlexIO is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc. The module can remain functional when the chip is in a low power mode provided the clock it is using remain active. |
| FlexPWM1 FlexPWM2 FlexPWM3 FlexPWM4 | Pulse Width Modulation | Timer Peripherals | The pulse-width modulator (PWM) contains four PWM sub-modules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. The PWM module can generate various switching patterns, including highly sophisticated waveforms. |
| FlexRAM | RAM | Memories | The i.MX RT1064 has 1 MB of on-chip RAM which could be flexible allocated to I-TCM, D-TCM, and on-chip RAM (OCRAM) in a 32 KB granularity. The FlexRAM is the manager of the on-chip RAM array. Major functions of this blocks are: interfacing to I-TCM and D-TCM of Arm core and OCRAM controller; dynamic RAM arrays allocation for I-TCM, D-TCM, and OCRAM. |
| FlexSPI | Quad Serial Peripheral Interface | Connectivity and Communications | FlexSPI acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines. |
| GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 | General Purpose I/O Modules | System Control Peripherals | Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O. |
| GPT1 GPT2 | General Purpose Timer | Timer Peripherals | Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |

Table 2. i.MX RT1064 modules list (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|---------------------------------------|---------------------------------|---|
| KPP | Keypad Port | Human Machine Interfaces | The KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as general purpose input/output (I/O). It supports 8 x 8 external key pad matrix. Main features are: <ul style="list-style-type: none"> • Multiple-key detection • Long key-press detection • Standby key-press detection • Supports a 2-point and 3-point contact key matrix |
| LCDIF | LCD interface | Multimedia Peripherals | The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capabilities. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices. |
| LPI2C1 LPI2C2 LPI2C3 LPI2C4 | Low Power Inter-integrated Circuit | Connectivity and Communications | The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master. The I2C provides a method of communication between a number of external devices. More detailed information, see Section 4.9.2, LPI2C module timing parameters . |
| LPSP11 LPSP12 LPSP13 LPSP14 | Low Power Serial Peripheral Interface | Connectivity and Communications | The LPSP1 is a low power Serial Peripheral Interface (SPI) module that support an efficient interface to an SPI bus as a master and/or a slave. <ul style="list-style-type: none"> • It can continue operating while the chip is in stop modes, if an appropriate clock is available • Designed for low CPU overhead, with DMA off loading of FIFO register access |
| LPUART1 LPUART2 LPUART3 LPUART4 LPUART5 LPUART6 LPUART7 LPUART8 | UART Interface | Connectivity Peripherals | Each of the UART modules support the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. |
| MQS | Medium Quality Sound | Multimedia Peripherals | MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins. |
| PXP | Pixel Processing Pipeline | Multimedia Peripherals | A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications. |

Table 2. i.MX RT1064 modules list (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|---|---------------------------------|--|
| QuadTimer1 QuadTimer2 QuadTimer3 QuadTimer4 | QuadTimer | Timer Peripherals | The quad-timer provides four time channels with a variety of controls affecting both individual and multi-channel features. Specific features include up/down count, cascading of counters, programmable module, count once/repeated, counter preload, compare registers with preload, shared use of input signals, prescaler controls, independent capture/compare, fault input control, programmable input filters, and multi-channel synchronization. |
| ROMCP | ROM Controller with Patch | Memories and Memory Controllers | The ROMCP acts as an interface between the Arm advanced high-performance bus and the ROM. The on-chip ROM is only used by the Cortex-M7 core during boot up. Size of the ROM is 96 KB. |
| RTC OSC | Real Time Clock Oscillator | Clock Sources and Control | The RTC OSC provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.678 kHz reference clock for the RTC. |
| RTWDOG | Watch Dog | Timer Peripherals | The RTWDG module is a high reliability independent timer that is available for system to use. It provides a safety feature to ensure software is executing as planned and the CPU is not stuck in an infinite loop or executing unintended code. If the WDOG module is not serviced (refreshed) within a certain period, it resets the MCU. Windowed refresh mode is supported as well. |
| SAI1 SAI2 SAI3 | Synchronous Audio Interface | Multimedia Peripherals | The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. |
| SA-TRNG | Standalone True Random Number Generator | Security | The SA-TRNG is hardware accelerator that generates a 512-bit entropy as needed by an entropy consuming module or by other post processing functions. |
| SEMC | Smart External Memory Controller | Memory and Memory Controller | The SEMC is a multi-standard memory controller optimized for both high-performance and low pin-count. It can support multiple external memories in the same application with shared address and data pins. The interface supported includes SDRAM, NOR Flash, SRAM, and NAND Flash, as well as 8080 display interface. |

Table 2. i.MX RT1064 modules list (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|--|-------------------------------|---|
| SJC | System JTAG Controller | System Control Peripherals | <p>The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX RT1064 processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE 1149.1 and IEEE 1149.6 standards.</p> <p>The JTAG port is accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX RT1064 SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.</p> |
| SNVS | Secure Non-Volatile Storage | Security | Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting. |
| SPDIF | Sony Philips Digital Interconnect Format | Multimedia Peripherals | A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality. |
| Temp Monitor | Temperature Monitor | Analog | The temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion. |
| TSC | Touch Screen | Human Machine Interfaces | With touch controller to support 4-wire and 5-wire resistive touch panel. |
| USBO2 | Universal Serial Bus 2.0 | Connectivity Peripherals | <p>USBO2 (USB OTG1 and USB OTG2) contains:</p> <ul style="list-style-type: none"> • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0 |

Table 2. i.MX RT1064 modules list (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|------------------|---|-----------------------------|--|
| uSDHC1 uSDHC2 | SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller | Connectivity Peripherals | <p>i.MX RT1064 specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 <p>Two ports support:</p> <ul style="list-style-type: none"> 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max) |
| WDOG1 WDOG2 | Watch Dog | Timer Peripherals | The watchdog (WDOG) Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line. |
| XBAR | Cross BAR | Cross Trigger | Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output. |

3.1 Special signal considerations

Table 3 lists special signal considerations for the i.MX RT1064 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in [Section 7, Package information and contact assignments.](#) Signal descriptions are provided in the *i.MX RT1064 Reference Manual (IMXRT1064RM)*.

Table 3. Special signal considerations

| Signal Name | Remarks |
|---------------------------|---|
| CCM_CLK1_P/ CCM_CLK1_N | <p>One general purpose differential high speed clock Input/output (LVDS I/O) is provided. It can be used:</p> <ul style="list-style-type: none"> To feed external reference clock to the PLLs and further to the modules inside SoC. To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. <p>See the <i>i.MX RT1064 Reference Manual (IMXRT1064RM)</i> for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.</p> |
| DCDC_PSWITCH | <p>PAD is in DCDC_IN domain and connected the ground to bypass DCDC. To enable DCDC function, assert to DCDC_IN with at least 1ms delay for DCDC_IN rising edge.</p> |
| RTC_XTALI/RTC_XTALO | <p>If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤ 100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (> 100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be < 100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.</p> |
| XTALI/XTALO | <p>A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.</p> |
| GPANAIO | <p>This signal is reserved for NXP manufacturing use only. This output must remain unconnected.</p> |

Table 3. Special signal considerations (continued)

| Signal Name | Remarks |
|-------------|--|
| JTAG_#### | <p>The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.</p> <p>JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.</p> <p>JTAG_MOD is referenced as SJC_MOD in the i.MX RT1064 reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.</p> |
| NC | These signals are No Connect (NC) and should be disconnected by the user. |
| POR_B | <p>This cold reset negative logic input resets all modules and logic in the IC.</p> <p>May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).</p> |
| ONOFF | <p>ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.</p> |
| TEST_MODE | TEST_MODE is for NXP factory use. The user must tie this pin directly to GND. |
| WAKEUP | A GPIO powered by SNVS domain power supply which can be configured as wakeup source in SNVS mode. |

Table 4. JTAG Controller interface summary

| JTAG | I/O Type | On-chip Termination |
|------------|----------------|------------------------|
| JTAG_TCK | Input | 47 k Ω pull-up |
| JTAG_TMS | Input | 47 k Ω pull-up |
| JTAG_TDI | Input | 47 k Ω pull-up |
| JTAG_TDO | 3-state output | Keeper |
| JTAG_TRSTB | Input | 47 k Ω pull-up |
| JTAG_MOD | Input | 100 k Ω pull-up |

3.2 Recommended connections for unused analog interfaces

[Table 5](#) shows the recommended connections for unused analog interfaces.

Table 5. Recommended connections for unused analog interfaces

| Module | Pad Name | Recommendations if Unused |
|---------------|---|---|
| CCM | CCM_CLK1_N, CCM_CLK1_P | Not connected |
| USB | USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS | Not connected |
| ADC | VDDA_ADC_3P3 | VDDA_ADC_3P3 must be powered even if the ADC is not used. |

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX RT1064 processors.

4.1 Chip-Level conditions

This section provides the device-level electrical characteristics for the IC. See [Table 6](#) for a quick reference to the individual tables and sections.

Table 6. i.MX RT1064 chip-Level conditions

| For these characteristics | Topic appears |
|--|----------------------------|
| Absolute maximum ratings | on page 18 |
| 10 x 10 MM thermal resistance | on page 19 |
| Operating ranges | on page 19 |
| External clock sources | on page 21 |
| Maximum supply currents | on page 22 |
| Low power mode supply currents | on page 23 |
| USB PHY current consumption | on page 23 |

4.1.1 Absolute maximum ratings

CAUTION

Stress beyond those listed under [Table 7](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[Table 7](#) shows the absolute maximum operating ratings.

Table 7. Absolute maximum ratings

| Parameter Description | Symbol | Min | Max | Unit |
|---|--------------------------------|------|-----|------|
| Core supplies input voltage | VDD_SOC_IN | -0.3 | 1.6 | V |
| VDD_HIGH_IN supply voltage | VDD_HIGH_IN | -0.3 | 3.7 | V |
| Power for DCDC | DCDC_IN | -0.3 | 3.6 | V |
| Supply input voltage to Secure Non-Volatile Storage and Real Time Clock | VDD_SNVS_IN | -0.3 | 3.6 | V |
| USB VBUS supply | USB_OTG1_VBUS USB_OTG2_VBUS | — | 5.5 | V |
| Supply for 12-bit ADC | VDDA_ADC | -0.3 | 3.6 | V |

Table 7. Absolute maximum ratings (continued)

| | | | | |
|---|-----------------------------------|--------|-------------------------|----|
| IO supply for GPIO in SDIO1 bank (3.3 V mode) | NVCC_SD0 | -0.3 | 3.6 | V |
| IO supply for GPIO in SDIO1 bank (1.8 V mode) | | -0.3 | 1.95 | V |
| IO supply for GPIO in SDIO2 bank (3.3 V mode) | NVCC_SD1 | -0.3 | 3.6 | V |
| IO supply for GPIO in SDIO2 bank (1.8 V mode) | | -0.3 | 1.95 | V |
| IO supply for GPIO in EMC bank (3.3 V mode) | NVCC_EMC | -0.3 | 3.6 | V |
| IO supply for GPIO in EMC bank (1.8 V mode) | | -0.3 | 1.95 | V |
| ESD damage Immunity: | Vesd | | | |
| Human Body Model (HBM) Charge Device Model (CDM) | | — — | 1000 500 | V |
| Input/Output Voltage range | V _{in} /V _{out} | -0.5 | OVDD + 0.3 ¹ | V |
| Storage Temperature range | T _{STORAGE} | -40 | 150 | °C |

¹ OVDD is the I/O supply voltage.

4.1.2 10 x 10 MM thermal resistance

Table 8 shows the 10 x 10 MM package thermal resistance data.

Table 8. 10 x 10 MM thermal resistance data

| Rating | Board type ¹ | Symbol | Value | Unit |
|--|-------------------------|------------------|-------|------|
| Junction to Ambient Thermal resistance ² | JESD51-9, 2S2P | R _{θJA} | 40.8 | °C/W |
| Junction to Package Top Thermal resistance ² | JESD51-9, 2S2P | Ψ _{JT} | 0.5 | °C/W |
| Junction to Case Thermal Resistance ³ | JESD51-9, 1S | R _{θJC} | 16.8 | °C/W |

¹ Thermal test board meets JEDEC specification for this package (JESD51-9).

² Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

³ Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead centre.

4.1.3 Operating ranges

Table 9 provides the operating ranges of the i.MX RT1064 processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX RT1064 Reference Manual* (IMXRT1064RM).

Table 9. Operating ranges

| Parameter Description | Symbol | Operating Conditions | Min | Typ | Max ¹ | Unit | Comment |
|-----------------------|--------|----------------------|-----|-----|------------------|------|---------|
|-----------------------|--------|----------------------|-----|-----|------------------|------|---------|

Table 9. Operating ranges (continued)

| | | | | | | | |
|-----------------------------|--------------------------|---------------------------------------|-------|-----|------|---|---|
| Run Mode | VDD_SOC_IN | Overdrive | 1.25 | — | 1.3 | V | — |
| | VDD_SOC_IN | M7 core at 528 MHz | 1.15 | — | 1.3 | V | — |
| | | M7 core at 132 MHz | 1.15 | — | 1.3 | | |
| | | M7 core at 24 MHz | 0.925 | — | 1.3 | | |
| IDLE Mode | VDD_SOC_IN | M7 core operation at 528 MHz or below | 1.15 | — | 1.3 | V | — |
| SUSPEND (DSM) Mode | VDD_SOC_IN | — | 0.925 | — | 1.3 | V | Refer to Table 12 Low power mode current and power consumption |
| SNVS Mode | VDD_SOC_IN | — | 0 | — | 1.3 | V | — |
| Power for DCDC | DCDC_IN | — | 3.0 | — | 3.6 | V | — |
| VDD_HIGH internal Regulator | VDD_HIGH_IN ² | — | 3.0 | — | 3.6 | V | Must match the range of voltages that the rechargeable backup battery supports. |
| Backup battery supply range | VDD_SNVS_IN ³ | — | 2.40 | — | 3.6 | V | Can be combined with VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state. |
| USB supply voltages | USB_OTG1_VBUS | — | 4.40 | — | 5.5 | V | — |
| | USB_OTG2_VBUS | — | 4.40 | — | 5.5 | V | — |
| GPIO supplies | NVCC_GPIO | — | 3.0 | 3.3 | 3.6 | V | All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not. |
| | | | 1.65 | 1.8 | 1.95 | V | |
| | NVCC_SD0 | — | 3.0 | 3.3 | 3.6 | V | |
| | | | 1.65 | 1.8 | 1.95 | V | |
| | NVCC_SD1 | — | 3.0 | 3.3 | 3.6 | V | |
| | | | 1.65 | 1.8 | 1.95 | V | |
| A/D converter | VDDA_ADC_3P3 | — | 3.0 | 3.3 | 3.6 | V | VDDA_ADC_3P3 must be powered even if the ADC is not used. VDDA_ADC_3P3 cannot be powered when the other SoC supplies (except VDD_SNVS_IN) are off. |
| | | | 3.0 | 3.3 | 3.6 | V | |

Table 9. Operating ranges (continued)

| Temperature Operating Ranges | | | | | | | See the application note, i.MX RT1064 Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor. |
|------------------------------|----------------|---------------------|---|---|----|----|---|
| Junction temperature | T _j | Standard Commercial | 0 | — | 85 | °C | |

¹ Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

² Applying the maximum voltage results in shorten lifetime. 3.6 V usage limited to < 1% of the use profile. Reset of profile limited to below 3.49 V.

³ In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX RT1064 Hardware Development Guide* (IMXRT1064HDG).

4.1.4 External clock sources

Each i.MX RT1064 processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 10 shows the interface frequency requirements.

Table 10. External input clock frequency

| Parameter Description | Symbol | Min | Typ | Max | Unit |
|-------------------------------------|-------------------|-----|---------------------------|-----|------|
| RTC_XTALI Oscillator ^{1,2} | f _{ckil} | — | 32.768 ³ /32.0 | — | kHz |
| XTALI Oscillator ^{2,4} | f _{xtal} | — | 24 | — | MHz |

¹ External oscillator or a crystal with internal oscillator amplifier.

² The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX RT1064 Crossover Processors* (IMXRT1064HDG).

³ Recommended nominal frequency 32.768 kHz.

⁴ External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with NXP SDK to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
 - Approximately 25 μ A more I_{dd} than crystal oscillator
 - Approximately $\pm 50\%$ tolerance
 - No external component required

- Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
 - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
 - Higher accuracy than ring oscillator
 - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in [Table 11](#) represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

See the *i.MX RT1064 Power Consumption Measurement Application Note* for more details on typical power consumption under various use case definitions.

Table 11. Maximum supply currents

| Power Rail | Conditions | Max Current | Unit |
|---|--|-------------|------|
| DCDC_IN | Max power for FF chip at 85 °C | 100 | mA |
| VDD_HIGH_IN | Include internal loading in analog | 50 | mA |
| VDD_SNVS_IN | — | 250 | μA |
| USB_OTG1_VBUS USB_OTG2_VBUS | 25 mA for each active USB interface | 50 | mA |
| VDDA_ADC_3P3 | 3.3 V power supply for 12-bit ADC, 600 μA typical, 750 μA max, for each ADC. 100 Ohm max loading for touch panel, cause 33 mA current. | 40 | mA |
| NVCC_GPIO NVCC_SD0 NVCC_SD1 NVCC EMC | $I_{max} = N \times C \times V \times (0.5 \times F)$ Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F) In this equation, I _{max} is in Amps, C in Farads, V in Volts, and F in Hertz. | | |

4.1.6 Low power mode supply currents

Table 12 shows the current core consumption (not including I/O) of i.MX RT1064 processors in selected low power modes.

Table 12. Low power mode current and power consumption

| Mode | Test Conditions | Supply | Typical ¹ | Units |
|----------------|--|---------------------|----------------------|-------|
| SYSTEM IDLE | <ul style="list-style-type: none"> LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V CPU in WFI, CPU clock gated 24 MHz XTAL is ON System PLL is active, other PLLs are power down Peripheral clock gated, but remain powered | DCDC_IN (3.3 V) | 4.04 | mA |
| | | VDD_HIGH_IN (3.3 V) | 7.66 | |
| | | VDD_SNVS_IN (3.3 V) | 0.032 | |
| | | Total | 38.72 | mW |
| LOW POWER IDLE | <ul style="list-style-type: none"> LDO_2P5 and LDO_1P1 are set to Weak mode WFI, half FlexRAM power down in power gate mode All PLLs are power down 24 MHz XTAL is off, 24 MHz RCOSC used as clock source Peripheral clock gated, but remain powered | DCDC_IN (3.3 V) | 1.11 | mA |
| | | VDD_HIGH_IN (3.3 V) | 0.309 | |
| | | VDD_SNVS_IN (3.3 V) | 0.048 | |
| | | Total | 4.84 | mW |
| SUSPEND (DSM) | <ul style="list-style-type: none"> LDO_2P5 and LDO_1P1 are shut off CPU in Power Gate mode All PLLs are power down 24 MHz XTAL is off, 24 MHz RCOSC is off All clocks are shut off, except 32 kHz RTC Peripheral clock gated, but remain powered | DCDC_IN (3.3 V) | 0.19 | mA |
| | | VDD_HIGH_IN (3.3 V) | 0.029 | |
| | | VDD_SNVS_IN (3.3 V) | 0.020 | |
| | | Total | 0.789 | mW |
| SNVS (RTC) | <ul style="list-style-type: none"> All SOC digital logic, analog module are shut off 32 kHz RTC is alive | DCDC_IN (0 V) | 0 | mA |
| | | VDD_HIGH_IN (0 V) | 0 | |
| | | VDD_SNVS_IN (3.3 V) | 0.02 | |
| | | Total | 0.066 | mW |

¹ The typical values shown here are for information only and are not guaranteed. These values are average values measured on a typical process wafer at 25°C.

4.1.7 USB PHY current consumption

4.1.7.1 Power down mode

In power down mode, everything is powered down, including the USB VBUS valid detectors in typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY current consumption in power down mode

| | VDD_USB_CAP (3.0 V) | VDD_HIGH_CAP (2.5 V) | NVCC_PLL (1.1 V) |
|---------|---------------------|----------------------|------------------|
| Current | 5.1 μ A | 1.7 μ A | < 0.5 μ A |

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 System power and clocks

This section provide the information about the system power and clocks.

4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- When internal DCDC is enabled, external delay circuit is required to delay the “DCDC_PSWITCH” signal 1 ms after DCDC_IN is stable.
- POR_B should be held low during the entire power up sequence.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX RT1064 Reference Manual* ([IMXRT1064RM](#)) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS, USB_OTG2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

4.2.1.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_XXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of [Section 7, Package information and contact assignments](#).”

4.2.2 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The on-board LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

4.2.2.1 Digital regulators (LDO_SNVS)

There are one digital LDO regulator (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulator is to reduce the input supply variation because of its input supply ripple rejection and its on-die trimming. This translates into more stable voltage for the on-chip logics.

The regulator has two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the target voltage.

For additional information, see the *i.MX RT1064 Reference Manual (IMXRT1064RM)*.

4.2.2.2 Regulators for analog modules

4.2.2.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see [Table 9](#) for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V

to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX RT1064 Crossover Processors* (IMXRT1064HDG).

For additional information, see the *i.MX RT1064 Reference Manual* ([IMXRT1064RM](#)).

4.2.2.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see [Table 9](#) for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB PHY, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω .

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX RT1064 Crossover Processors* (IMXRT1064HDG).

For additional information, see the *i.MX RT1064 Reference Manual* ([IMXRT1064RM](#)).

4.2.2.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VUSB voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX RT1064 Crossover Processors* (IMXRT1064HDG).

For additional information, see the *i.MX RT1064 Reference Manual* ([IMXRT1064RM](#)).

4.2.2.2.4 DCDC

DCDC can be configured to operate on power-save mode when the load current is less than 50 mA. During the power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

DCDC can detect the peak current in the P-channel switch. When the peak current exceeds the threshold, DCDC will give an alert signal, and the threshold can be configured. By this way, DCDC can roughly detect the current loading.

DCDC also includes the following protection functions:

- Over current protection. In run mode, DCDC shuts down when detecting abnormal large current in the P-type power switch.
- Over voltage protection. DCDC shuts down when detecting the output voltage is too high.
- Low voltage detection. DCDC shuts down when detecting the input voltage is too low.

For additional information, see the *i.MX RT1064 Reference Manual* ([IMXRT1064RM](#)).

4.2.3 PLL's electrical characteristics

This section provides PLL electrical characteristics.

4.2.3.1 Audio/Video PLL's electrical parameters

Table 14. Audio/Video PLL's electrical parameters

| Parameter | Value |
|--------------------|--------------------------|
| Clock output range | 650 MHz ~1.3 GHz |
| Reference clock | 24 MHz |
| Lock time | < 11250 reference cycles |

4.2.3.2 528 MHz PLL

Table 15. 528 MHz PLL's electrical parameters

| Parameter | Value |
|--------------------|--------------------------|
| Clock output range | 528 MHz PLL output |
| Reference clock | 24 MHz |
| Lock time | < 11250 reference cycles |

4.2.3.3 Ethernet PLL

Table 16. Ethernet PLL's electrical parameters

| Parameter | Value |
|--------------------|--------------------------|
| Clock output range | 1 GHz |
| Reference clock | 24 MHz |
| Lock time | < 11250 reference cycles |

4.2.3.4 480 MHz PLL

Table 17. 480 MHz PLL's electrical parameters

| Parameter | Value |
|--------------------|------------------------|
| Clock output range | 480 MHz PLL output |
| Reference clock | 24 MHz |
| Lock time | < 383 reference cycles |

4.2.3.5 Arm PLL

Table 18. Arm PLL's electrical parameters

| Parameter | Value |
|--------------------|-------------------------|
| Clock output range | 648 MHz ~ 1296 MHz |
| Reference clock | 24 MHz |
| Lock time | < 2250 reference cycles |

4.2.4 On-chip oscillators

4.2.4.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement an oscillator. The oscillator is powered from NVCC_PLL.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.2.4.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes

power from VDD_HIGH_IN when that supply is available and transitions to the backup battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from the VDD_HIGH_IN/VDD_SNVS_IN. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, $R_s = (3.2 - 2.5) / 0.6 \text{ m} = 1.17 \text{ k}$.

Table 19. OSC32K main characteristics

| | Min | Typ | Max | Comments |
|---------------------------|-----|-----------------|----------------|---|
| Fosc | — | 32.768 KHz | — | This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well. |
| Current consumption | — | 4 μA | — | The 4 μA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μA when ring oscillator is inactive, 20 μA when the ring oscillator is running. Another 1.5 μA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 μA on vdd_rtc when the ring oscillator is not running. |
| Bias resistor | — | 14 M Ω | — | This integrated bias resistor sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations. |
| Crystal Properties | | | | |
| Cload | — | 10 pF | — | Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal. |
| ESR | — | 50 k Ω | 100 k Ω | Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin. |

4.3 I/O parameters

This section provide parameters on I/O interfaces.

4.3.1 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (Clock Inputs) DC Parameters
- General Purpose I/O (GPIO)
- LVDS I/O DC Parameters

NOTE

The term 'NVCC_XXXX' in this section refers to the associated supply rail of an input or output.

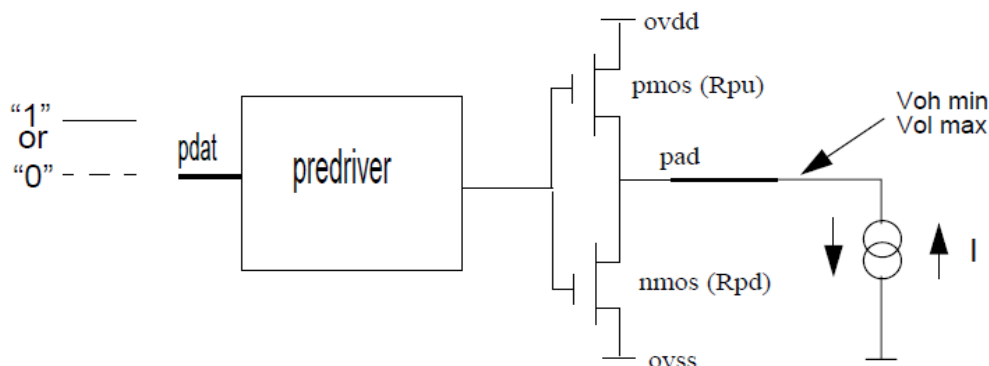


Figure 3. Circuit for parameters Voh and Vol for I/O cells

4.3.1.1 XTALI and RTC_XTALI (clock inputs) DC parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC parameters¹

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---------------------------------------|--------|-----------------|----------------|----------|------|
| XTALI high-level DC input voltage | Vih | — | 0.8 x NVCC_PLL | NVCC_PLL | V |
| XTALI low-level DC input voltage | Vil | — | 0 | 0.2 | V |
| RTC_XTALI high-level DC input voltage | Vih | — | 0.8 | 1.1 | V |
| RTC_XTALI low-level DC input voltage | Vil | — | 0 | 0.2 | V |

¹ The DC parameters are for external clock input only.

4.3.1.2 Single voltage general purpose I/O (GPIO) DC parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 21. Single voltage GPIO DC parameters

| Parameter | Symbol | Test Conditions | Min | Max | Units |
|---|-----------------|---|--------------------|--------------------|-------|
| High-level output voltage ¹ | V _{OH} | I _{oh} = -0.1mA (ipp_dse=001,010) I _{oh} = -1mA (ipp_dse=011,100,101,110,111) | NVCC_XXXX-0.15 | — | V |
| Low-level output voltage ¹ | V _{OL} | I _{ol} = 0.1mA (ipp_dse=001,010) I _{ol} = 1mA (ipp_dse=011,100,101,110,111) | — | 0.15 | V |
| High-Level input voltage ^{1,2} | V _{IH} | — | 0.7 x NVCC_XXXX | NVCC_XXXX | V |
| Low-Level input voltage ^{1,2} | V _{IL} | — | 0 | 0.3 x NVCC_XXXX | V |
| Input Hysteresis (NVCC_XXXX = 1.8V) | VHYS_LowVDD | NVCC_XXXX = 1.8V | 250 | — | mV |
| Input Hysteresis (NVCC_XXXX = 3.3V) | VHYS_HighVDD | NVCC_XXXX = 3.3V | 250 | — | mV |
| Schmitt trigger VT ^{+2,3} | VTH+ | — | 0.5 x NVCC_XXXX | — | mV |
| Schmitt trigger VT ^{-2,3} | VTH- | — | — | 0.5 x NVCC_XXXX | mV |
| Pull-up resistor (22_kΩ PU) | RPU_22K | V _{in} = 0V | — | 212 | μA |
| Pull-up resistor (22_kΩ PU) | RPU_22K | V _{in} = NVCC_XXXX | — | 1 | μA |
| Pull-up resistor (47_kΩ PU) | RPU_47K | V _{in} = 0V | — | 100 | μA |
| Pull-up resistor (47_kΩ PU) | RPU_47K | V _{in} = NVCC_XXXX | — | 1 | μA |
| Pull-up resistor (100_kΩ PU) | RPU_100K | V _{in} = 0V | — | 48 | μA |
| Pull-up resistor (100_kΩ PU) | RPU_100K | V _{in} = NVCC_XXXX | — | 1 | μA |
| Pull-down resistor (100_kΩ PD) | RPD_100K | V _{in} = NVCC_XXXX | — | 48 | μA |
| Pull-down resistor (100_kΩ PD) | RPD_100K | V _{in} = 0V | — | 1 | μA |
| Input current (no PU/PD) | I _{IN} | V _I = 0, V _I = NVCC_XXXX | -1 | 1 | μA |
| Keeper Circuit Resistance | R_Keeper | V _I = 0.3 x NVCC_XXXX, V _I = 0.7 x NVCC_XXXX | 105 | 175 | kΩ |

¹ Overshoot and undershoot conditions (transitions above NVCC_XXXX and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{il} or V_{ih}. Monotonic input transition time is from 0.1 ns to 1 s.

³ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.3.1.3 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 22 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 22. LVDS I/O DC characteristics¹

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------------------------|--------|-------------------------|-------|-------|-------|------|
| Output Differential Voltage | VOD | Rload=100 Ω Diff | 250 | 350 | 450 | mV |
| Output High Voltage | VOH | IOH = 0 mA | 1.25 | 1.375 | 1.6 | V |
| Output Low Voltage | VOL | IOL = 0 mA | 0.9 | 1.025 | 1.25 | V |
| Offset Voltage | VOS | — | 1.125 | 1.2 | 1.375 | V |

¹ Note: The LVDS interface is limited to CCM_CLK1_P and CCM_CLK1_N.

4.3.2 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)

Figure 4 shows load circuit for output, and Figure 5 show the output transition time waveform.

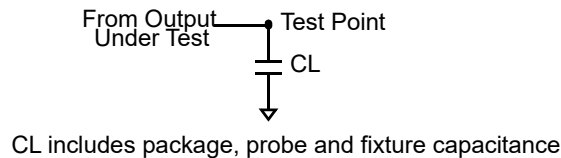


Figure 4. Load circuit for output

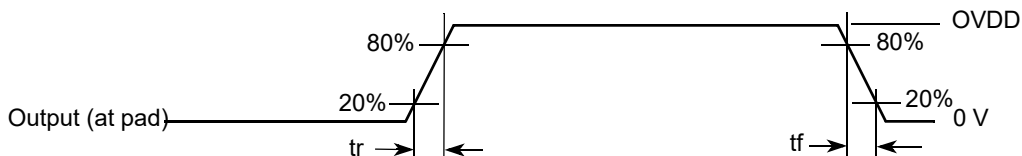


Figure 5. Output transition time waveform

4.3.2.1 General purpose I/O AC parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 23 and Table 24, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 23. General purpose I/O AC parameters 1.8 V mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|--|-----|-----|------------------------|------|
| Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 2.72/2.79 1.51/1.54 | ns |
| Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 3.20/3.36 1.96/2.07 | |
| Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 3.64/3.88 2.27/2.53 | |
| Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=011) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 4.32/4.50 3.16/3.17 | |
| Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 24. General purpose I/O AC parameters 3.3 V mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|--|-----|-----|------------------------|------|
| Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 1.70/1.79 1.06/1.15 | ns |
| Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 2.35/2.43 1.74/1.77 | |
| Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 3.13/3.29 2.46/2.60 | |
| Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=001) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 5.14/5.57 4.77/5.15 | ns |
| Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.3.3 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX RT1064 processors for the following I/O types:

- Single Voltage General Purpose I/O (GPIO)

NOTE

GPIO I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to NVCC_XXXX. Output driver impedance is calculated from this voltage divider (see [Figure 6](#)).

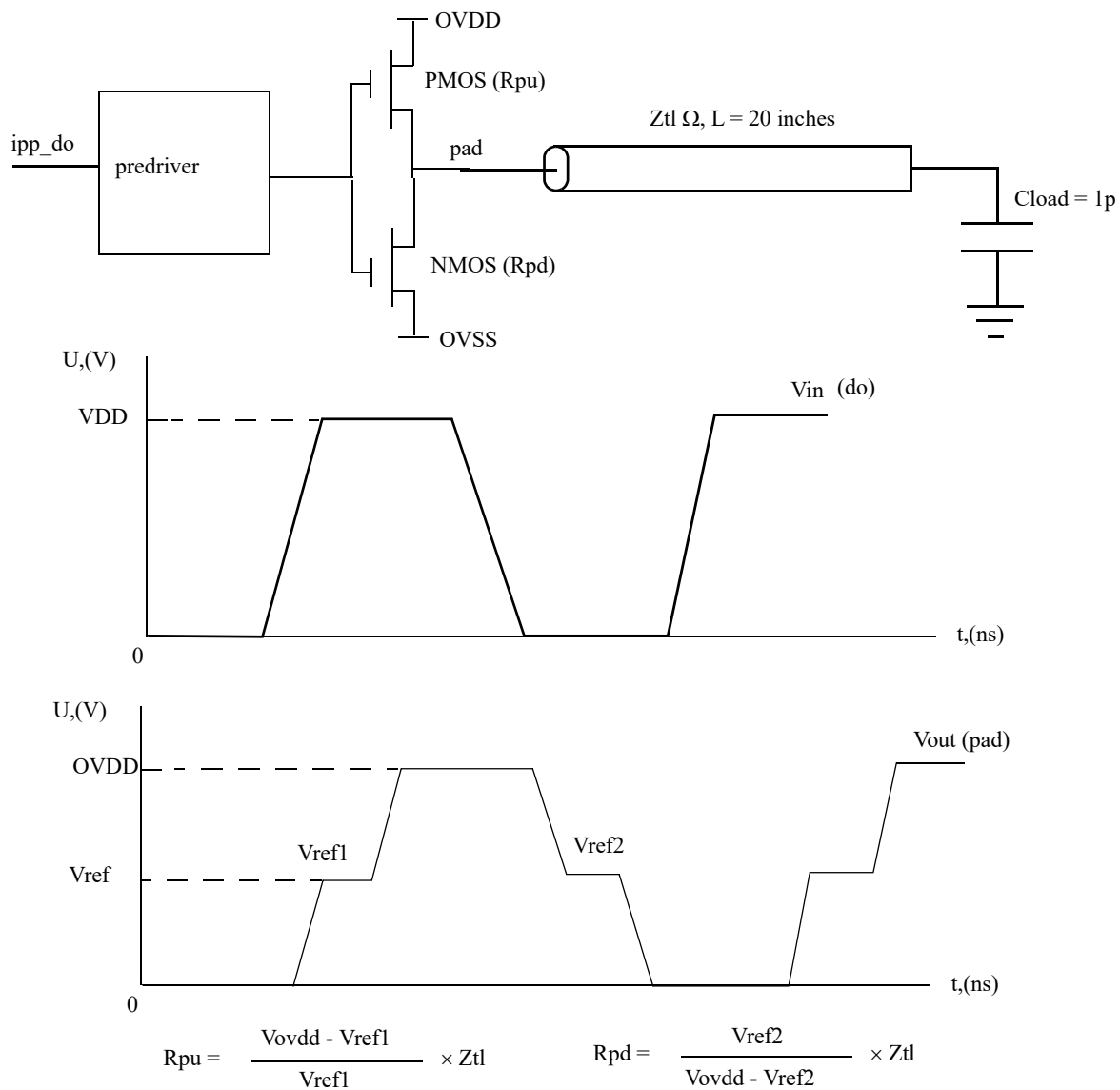


Figure 6. Impedance matching load for measurement

4.3.3.1 Single voltage GPIO output buffer impedance

Table 25 shows the GPIO output buffer impedance (NVCC_XXXX 1.8 V).

Table 25. GPIO output buffer average impedance (NVCC_XXXX 1.8 V)

| Parameter | Symbol | Drive Strength (DSE) | Typ Value | Unit |
|-------------------------|--------|----------------------|-----------|----------|
| Output Driver Impedance | Rdrv | 001 | 260 | Ω |
| | | 010 | 130 | |
| | | 011 | 88 | |
| | | 100 | 65 | |
| | | 101 | 52 | |
| | | 110 | 43 | |
| | | 111 | 37 | |

Table 26 shows the GPIO output buffer impedance (NVCC_XXXX 3.3 V).

Table 26. GPIO output buffer average impedance (NVCC_XXXX 3.3 V)

| Parameter | Symbol | Drive Strength (DSE) | Typ Value | Unit |
|-------------------------|--------|----------------------|-----------|----------|
| Output Driver Impedance | Rdrv | 001 | 157 | Ω |
| | | 010 | 78 | |
| | | 011 | 53 | |
| | | 100 | 39 | |
| | | 101 | 32 | |
| | | 110 | 26 | |
| | | 111 | 23 | |

4.4 System modules

This section contains the timing and electrical parameters for the modules in the i.MX RT1064 processor.

4.4.1 Reset timings parameters

Figure 7 shows the reset timing and Table 27 lists the timing parameters.

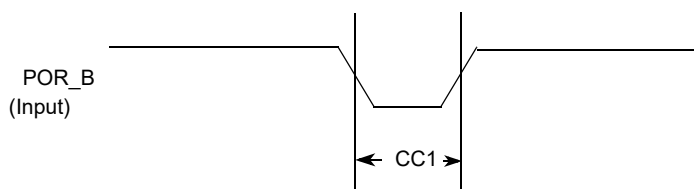


Figure 7. Reset timing diagram

Table 27. Reset timing parameters

| ID | Parameter | Min | Max | Unit |
|-----|---|-----|-----|-----------------|
| CC1 | Duration of POR_B to be qualified as valid. | 1 | — | RTC_XTALI cycle |

4.4.2 WDOG reset timing parameters

Figure 8 shows the WDOG reset timing and Table 28 lists the timing parameters.

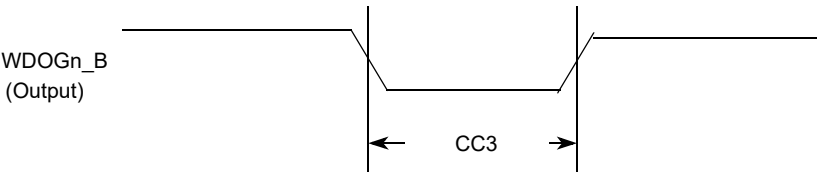


Figure 8. WDOGn_B timing diagram

Table 28. WDOGn_B timing parameters

| ID | Parameter | Min | Max | Unit |
|-----|-------------------------------|-----|-----|-----------------|
| CC3 | Duration of WDOGn_B Assertion | 1 | — | RTC_XTALI cycle |

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μ s.

NOTE

WDOGn_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.4.3 SCAN JTAG Controller (SJC) timing parameters

Figure 9 depicts the SJC test clock input timing. Figure 10 depicts the SJC boundary scan timing. Figure 11 depicts the SJC test access port. Signal parameters are listed in Table 29.

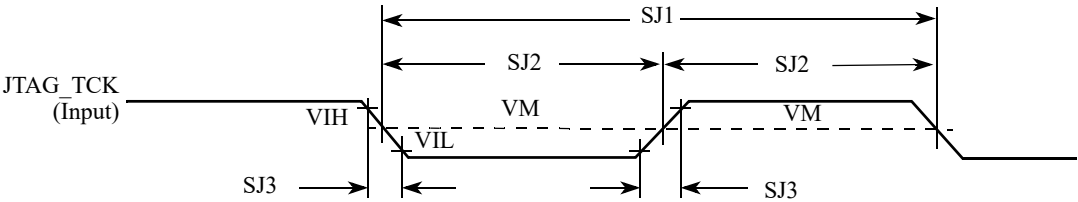


Figure 9. Test clock input timing diagram

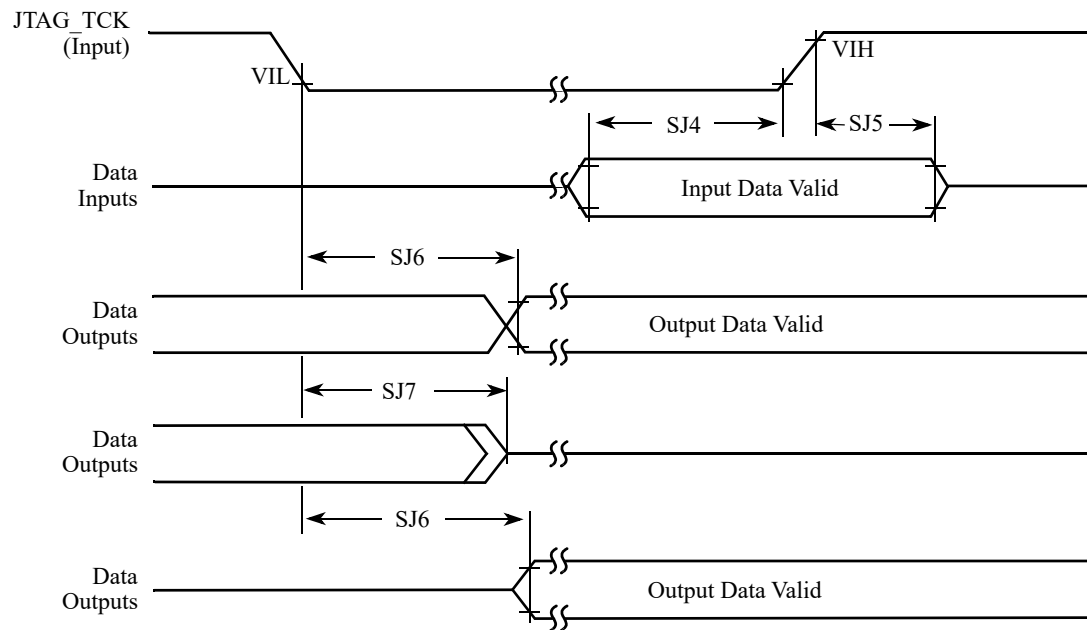


Figure 10. Boundary Scan (JTAG) timing diagram

Electrical Characteristics

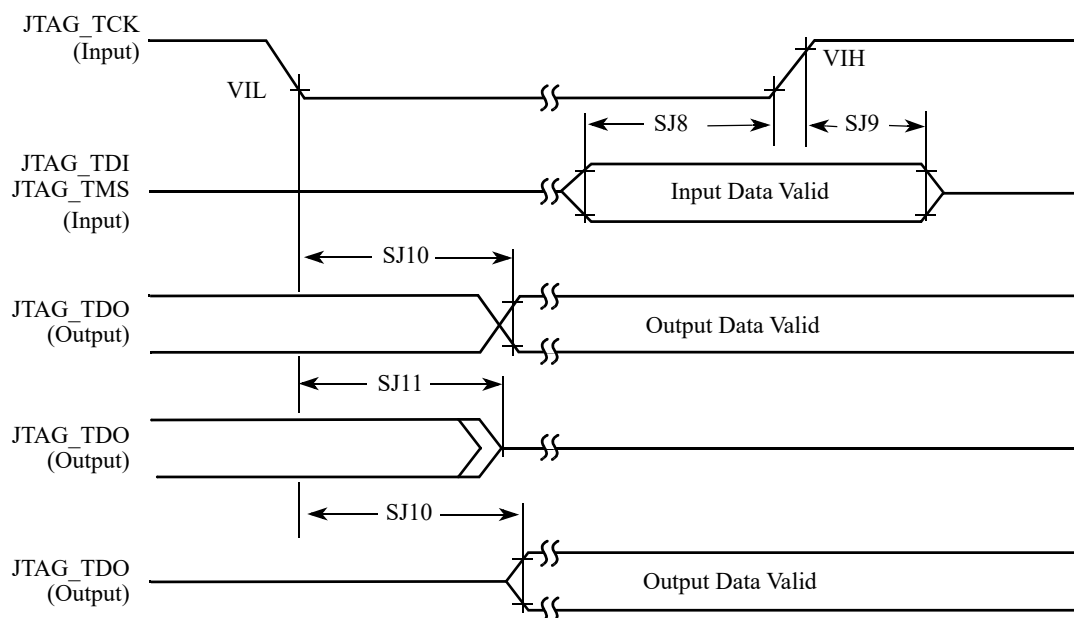


Figure 11. Test access port timing diagram

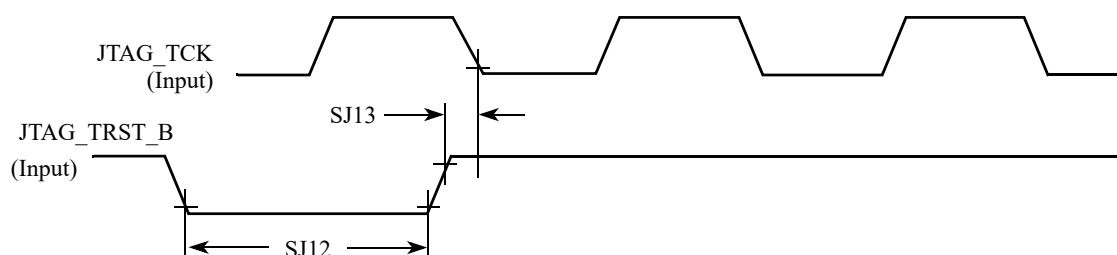


Figure 12. JTAG_TRST_B timing diagram

Table 29. JTAG timing

| ID | Parameter ^{1,2} | All Frequencies | | Unit |
|-----|---|-----------------|-----|------|
| | | Min | Max | |
| SJ0 | JTAG_TCK frequency of operation $1/(3 \cdot T_{DC})^1$ | 0.001 | 22 | MHz |
| SJ1 | JTAG_TCK cycle time in crystal mode | 45 | — | ns |
| SJ2 | JTAG_TCK clock pulse width measured at V_M ² | 22.5 | — | ns |
| SJ3 | JTAG_TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 5 | — | ns |
| SJ5 | Boundary scan input data hold time | 24 | — | ns |
| SJ6 | JTAG_TCK low to output data valid | — | 40 | ns |
| SJ7 | JTAG_TCK low to output high impedance | — | 40 | ns |
| SJ8 | JTAG_TMS, JTAG_TDI data set-up time | 5 | — | ns |

Table 29. JTAG timing (continued)

| ID | Parameter ^{1,2} | All Frequencies | | Unit |
|------|---|-----------------|-----|------|
| | | Min | Max | |
| SJ9 | JTAG_TMS, JTAG_TDI data hold time | 25 | — | ns |
| SJ10 | JTAG_TCK low to JTAG_TDO data valid | — | 44 | ns |
| SJ11 | JTAG_TCK low to JTAG_TDO high impedance | — | 44 | ns |
| SJ12 | JTAG_TRST_B assert time | 100 | — | ns |
| SJ13 | JTAG_TRST_B set-up time to JTAG_TCK low | 40 | — | ns |

¹ T_{DC} = target frequency of SJC² V_M = mid-point voltage

4.4.4 Debug trace timing specifications

Table 30. Debug trace operating behaviors

| Symbol | Description | Min | Max | Unit |
|--------|--------------------------------------|------|-----|------|
| T1 | ARM_TRACE_CLK frequency of operation | — | 70 | MHz |
| T2 | ARM_TRACE_CLK period | 1/T1 | — | MHz |
| T3 | Low pulse width | 6 | — | ns |
| T4 | High pulse width | 6 | — | ns |
| T5 | Clock and data rise time | — | 1 | ns |
| T6 | Clock and data fall time | — | 1 | ns |
| T7 | Data setup | 2 | — | ns |
| T8 | Data hold | 0.7 | — | ns |

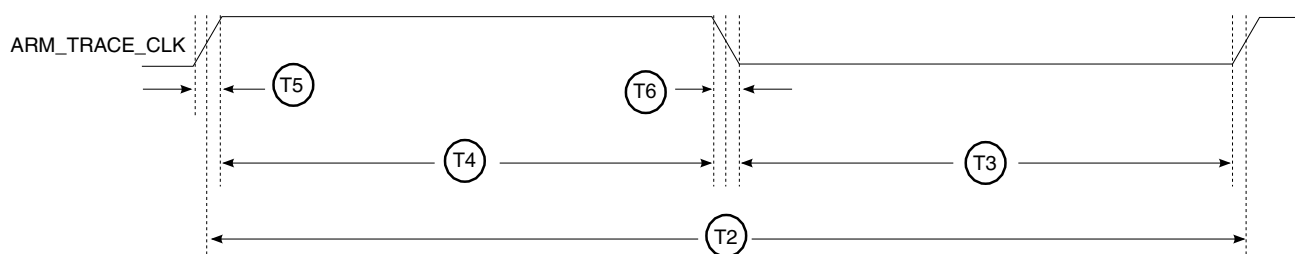


Figure 13. ARM_TRACE_CLK specifications

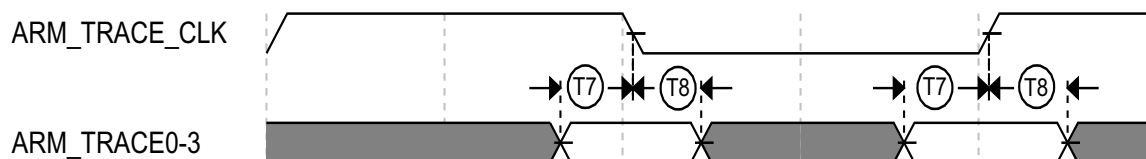


Figure 14. Trace data specifications

4.5 External memory interface

The following sections provide information about external memory interfaces.

4.5.1 SEMC specifications

The following sections provide information on SEMC interface.

Measurements are with a load of 15 pF and an input slew rate of 1 V/ns.

4.5.1.1 SEMC output timing

There are ASYNC and SYNC mode for SEMC output timing.

4.5.1.1.1 SEMC output timing in ASYNC mode

Table 31 shows SEMC output timing in ASYNC mode.

Table 31. SEMC output timing in ASYNC mode

| Symbol | Parameter | Min. | Max. | Unit | Comment |
|------------|---------------------------|------------------|------|------|--|
| | Frequency of operation | — | 166 | MHz | |
| T_{CK} | Internal clock period | 6 | — | ns | |
| T_{AVO} | Address output valid time | — | 2 | ns | These timing parameters apply to Address and ADV# for NOR/PSRAM in ASYNC mode. |
| T_{AHO} | Address output hold time | $(T_{CK} - 2)^1$ | — | ns | |
| T_{ADVL} | ADV# low time | $(T_{CK} - 1)^2$ | | | |
| T_{DVO} | Data output valid time | — | 2 | ns | These timing parameters apply to Data/CLE/ALE and WE# for NAND, apply to Data/DM/CRE for NOR/PSRAM, apply to Data/DCX and WRX for DBI interface. |
| T_{DHO} | Data output hold time | $(T_{CK} - 2)^3$ | — | ns | |
| T_{WEL} | WE# low time | $(T_{CK} - 1)^4$ | | ns | |

¹ Address output hold time is configurable by SEMC_CR0.AH. AH field setting value is 0x0 in above table. When AH is set with value N, T_{AHO} min time should be $((N + 1) \times T_{CK})$. See the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for more detail about SEMC_CR0.AH register field.

- ² ADV# low time is configurable by SEMC_*CR0.AS. AS field setting value is 0x0 in above table. When AS is set with value N, T_{ADL} min time should be $((N + 1) \times T_{CK} - 1)$. See the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for more detail about SEMC_*CR0.AS register field.
- ³ Data output hold time is configurable by SEMC_*CR0.WEH. WEH field setting value is 0x0 in above table. When WEH is set with value N, T_{DHO} min time should be $((N + 1) \times T_{CK})$. See the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for more detail about SEMC_*CR0.WEH register field.
- ⁴ WE# low time is configurable by SEMC_*CR0.WEL. WEL field setting value is 0x0 in above table. When WEL is set with value N, T_{WEL} min time should be $((N + 1) \times T_{CK} - 1)$. See the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for more detail about SEMC_*CR0.WEL register field.

Figure 15 shows the output timing in ASYNC mode.

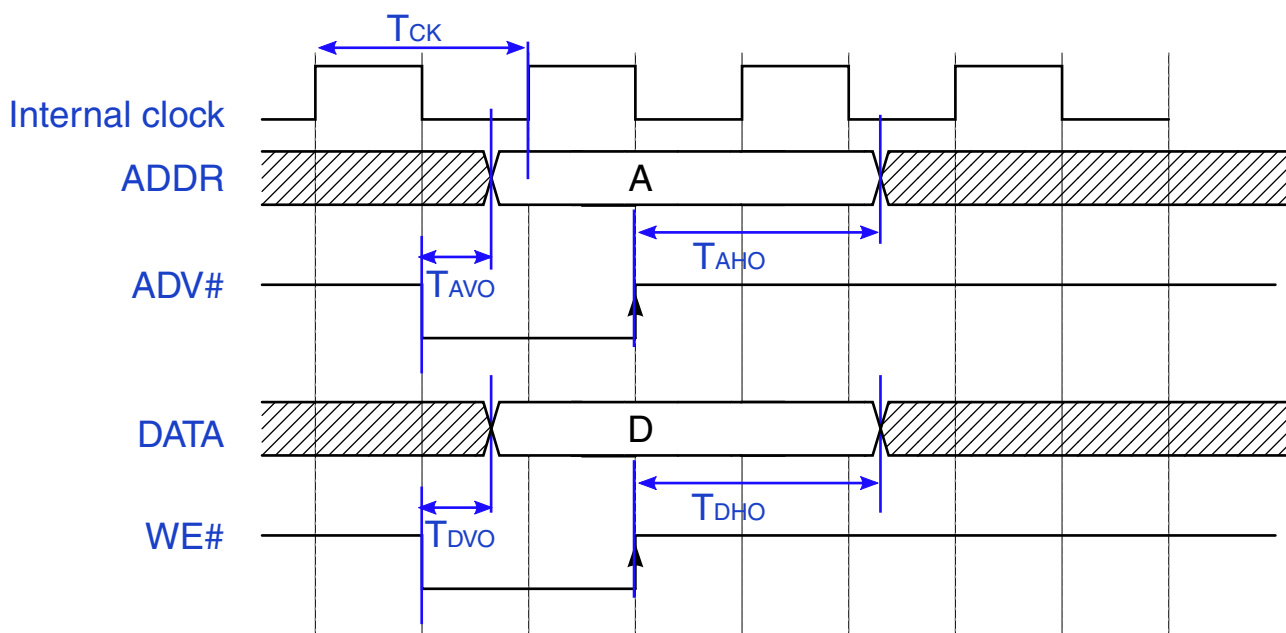


Figure 15. SEMC output timing in ASYNC mode

4.5.1.1.2 SEMC output timing in SYNC mode

Table 32 shows SEMC output timing in SYNC mode.

Table 32. SEMC output timing in SYNC mode

| Symbol | Parameter | Min. | Max. | Unit | Comment |
|-----------|------------------------|------|------|------|---|
| | Frequency of operation | — | 166 | MHz | — |
| T_{CK} | Internal clock period | 6 | — | ns | — |
| T_{DVO} | Data output valid time | 1 | — | ns | These timing parameters apply to Address/Data/DM/CKE/control signals with SEMC_CLK for SDRAM. |
| T_{DHO} | Data output hold time | -1 | — | ns | |

Figure 16 shows the output timing in SYNC mode.

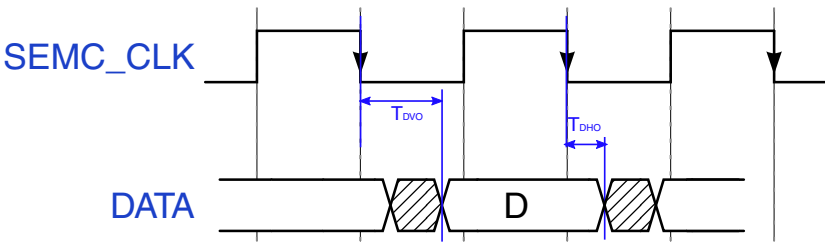


Figure 16. SEMC output timing in SYNC mode

4.5.1.2 SEMC input timing

There are ASYNC and SYNC mode for SEMC input timing.

4.5.1.2.1 SEMC input timing in ASYNC mode

Table 33 shows SEMC output timing in ASYNC mode.

Table 33. SEMC output timing in ASYNC mode

| Symbol | Parameter | Min. | Max. | Unit | Comment |
|-----------------|------------------|------|------|------|---|
| T _{IS} | Data input setup | 8.67 | — | ns | For NAND/NOR/PSRAM/DBI, these timing parameters apply to RE# and Read Data. |
| T _{IH} | Data input hold | 0 | — | ns | |

Figure 17 shows the input timing in ASYNC mode.

NAND non-EDO mode and NOR/PSRAM/8080 timing

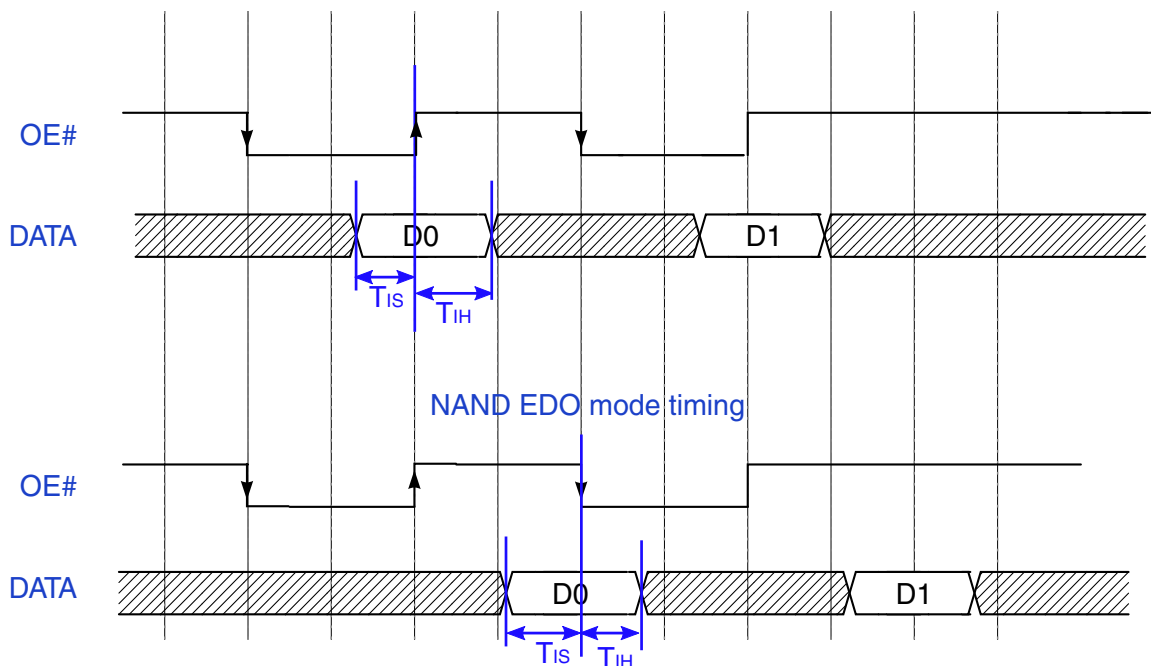


Figure 17. SEMC input timing in ASYNC mode

4.5.1.2.2 SEMC input timing in SYNC mode

Table 34 and Table 35 show SEMC input timing in SYNC mode.

Table 34. SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x0)

| Symbol | Parameter | Min. | Max. | Unit | Comment |
|----------|------------------|------|------|------|---------|
| T_{IS} | Data input setup | 8.67 | — | ns | — |
| T_{IH} | Data input hold | 0 | — | ns | |

Table 35. SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x1)

| Symbol | Parameter | Min. | Max. | Unit | Comment |
|----------|------------------|------|------|------|---------|
| T_{IS} | Data input setup | 0.6 | — | ns | — |
| T_{IH} | Data input hold | 1 | — | ns | |

Figure 18 shows the input timing in SYNC mode.

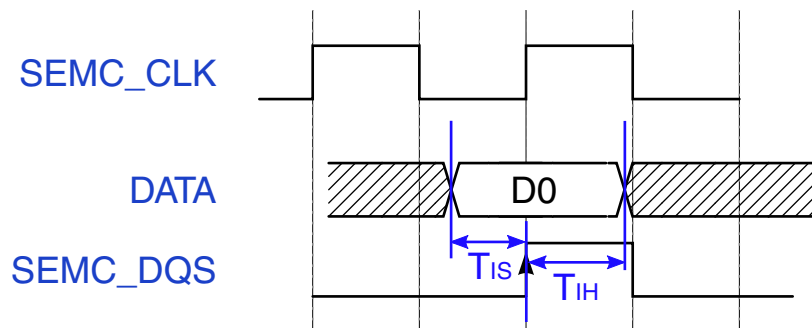


Figure 18. SEMC input timing in SYNC mode

4.5.2 FlexSPI parameters

Measurements are with a load 15 pf and input slew rate of 1 V/ns.

4.5.2.1 FlexSPI input/read timing

There are four sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI_{in}_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI_{in}_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI_{in}_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these four internal sample clock sources.

4.5.2.1.1 SDR mode with FlexSPI_{in}_MCR0[RXCLKSRC] = 0x0, 0x1

Table 36. FlexSPI input timing in SDR mode where FlexSPI_{in}_MCR0[RXCLKSRC] = 0X0

| Symbol | Parameter | Min | Max | Unit |
|-----------------|------------------------------|------|-----|------|
| | Frequency of operation | — | 60 | MHz |
| T _{IS} | Setup time for incoming data | 8.67 | — | ns |
| T _{IH} | Hold time for incoming data | 0 | — | ns |

Table 37. FlexSPI input timing in SDR mode where FlexSPI_{in}_MCR0[RXCLKSRC] = 0X1

| Symbol | Parameter | Min | Max | Unit |
|-----------------|------------------------------|-----|-----|------|
| | Frequency of operation | — | 133 | MHz |
| T _{IS} | Setup time for incoming data | 2 | — | ns |
| T _{IH} | Hold time for incoming data | 1 | — | ns |

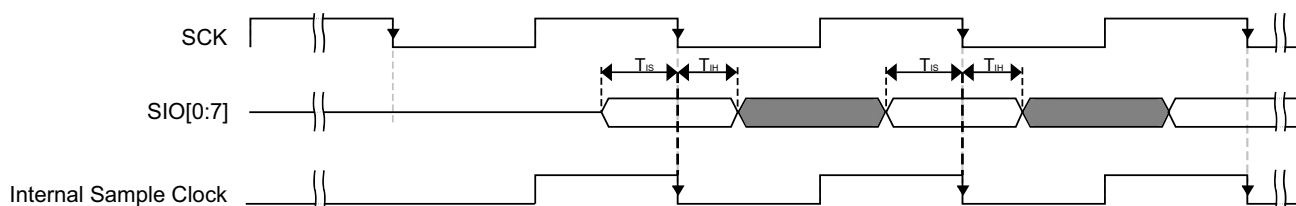


Figure 19. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X0, 0X1

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.5.2.1.2 SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 38. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (case A1)

| Symbol | Parameter | Value | | Unit |
|-------------------------|--|-------|-----|------|
| | | Min | Max | |
| | Frequency of operation | — | 166 | MHz |
| T_{SCKD} | Time from SCK to data valid | — | — | ns |
| T_{SCKDQS} | Time from SCK to DQS | — | — | ns |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between T_{SCKD} and T_{SCKDQS} | -2 | 2 | ns |

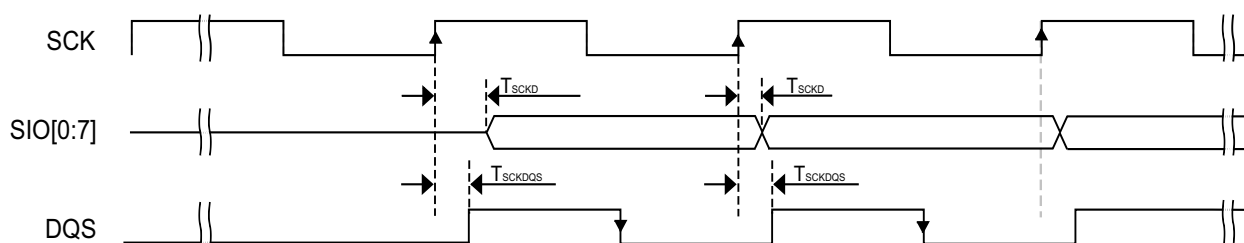


Figure 20. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X3 (case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 39. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (case A2)

| Symbol | Parameter | Value | | Unit |
|-------------------------|--|-------|-----|------|
| | | Min | Max | |
| | Frequency of operation | — | 166 | MHz |
| T_{SCKD} | Time from SCK to data valid | — | — | ns |
| T_{SCKDQS} | Time from SCK to DQS | — | — | ns |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between T_{SCKD} and T_{SCKDQS} | -2 | 2 | ns |

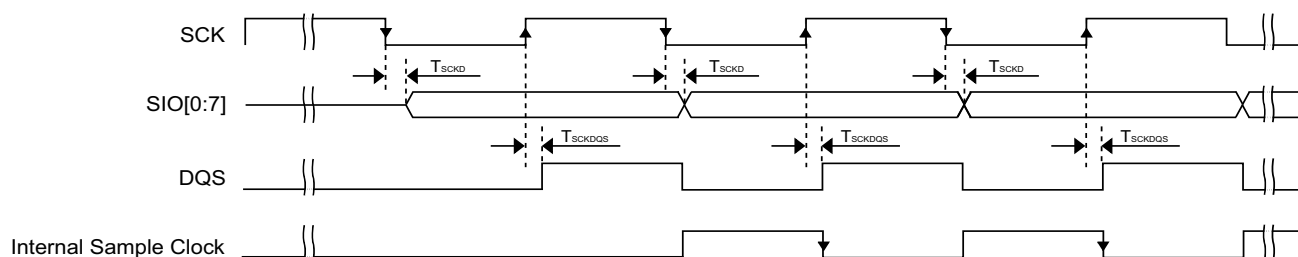


Figure 21. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (case A2)

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half cycle delayed DQS falling edge.

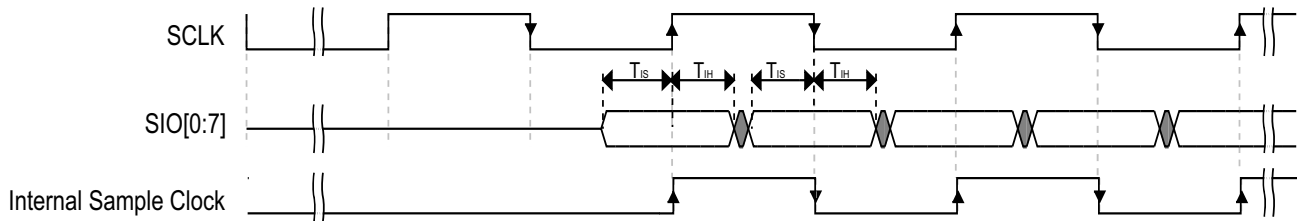
4.5.2.1.3 DDR mode with FlexSPI_n_MCR0[RXCLKSRC] = 0x0, 0x1

Table 40. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x0

| Symbol | Parameter | Min | Max | Unit |
|----------|------------------------------|------|-----|------|
| | Frequency of operation | — | 30 | MHz |
| T_{IS} | Setup time for incoming data | 8.67 | — | ns |
| T_{IH} | Hold time for incoming data | 0 | — | ns |

Table 41. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x1

| Symbol | Parameter | Min | Max | Unit |
|----------|------------------------------|-----|-----|------|
| | Frequency of operation | — | 66 | MHz |
| T_{IS} | Setup time for incoming data | 2 | — | ns |
| T_{IH} | Hold time for incoming data | 1 | — | ns |

**Figure 22. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x0, 0x1**

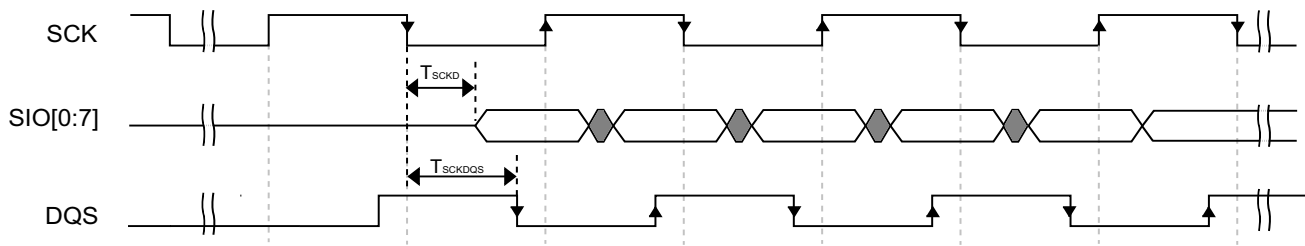
4.5.2.1.4 DDR mode with FlexSPI_n_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in DDR mode:

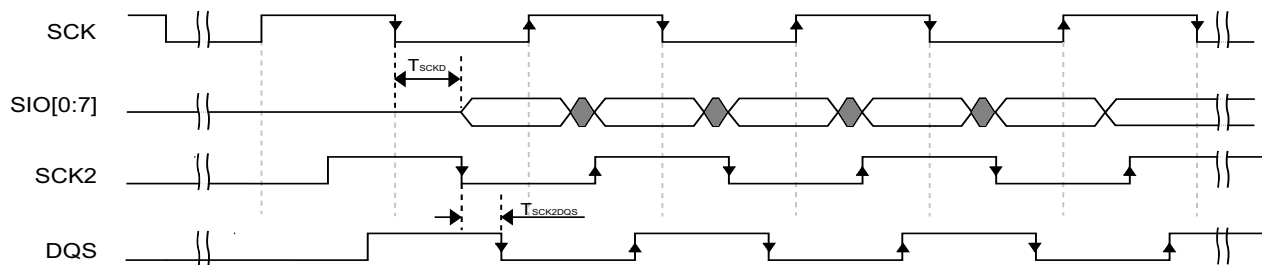
- B1—Memory generates both read data and read strobe on SCK edge
- B2—Memory generates read data on SCK edge and generates read strobe on SCK2 edge

Table 42. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (case B1)

| Symbol | Parameter | Min | Max | Unit |
|-------------------------|--|-----|-----|------|
| | Frequency of operation | — | 166 | MHz |
| T_{SCKD} | Time from SCK to data valid | — | — | ns |
| T_{SCKDQS} | Time from SCK to DQS | — | — | ns |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between T_{SCKD} and T_{SCKDQS} | -1 | 1 | ns |

Figure 23. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (case B1)Table 43. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (case B2)

| Symbol | Parameter | Min | Max | Unit |
|---|--|-----|-----|------|
| | Frequency of operation | — | 166 | MHz |
| T _{SCKD} | Time from SCK to data valid | — | — | ns |
| T _{SCKD} - T _{SCKDQS} | Time delta between T _{SCKD} and T _{SCKDQS} | -1 | 1 | ns |

Figure 24. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (case B2)

4.5.2.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.5.2.2.1 SDR mode

Table 44. FlexSPI output timing in SDR mode

| Symbol | Parameter | Min | Max | Unit |
|------------------|------------------------|-----|------------------|------|
| | Frequency of operation | — | 166 ¹ | MHz |
| T _{ck} | SCK clock period | 6.0 | — | ns |
| T _{DVO} | Output data valid time | — | 1 | ns |
| T _{DHO} | Output data hold time | -1 | — | ns |

Table 44. FlexSPI output timing in SDR mode (continued)

| Symbol | Parameter | Min | Max | Unit |
|-----------|-------------------------------|-----------------------|-----|------|
| T_{CSS} | Chip select output setup time | $3 \times T_{CK} - 1$ | — | ns |
| T_{CSH} | Chip select output hold time | $3 \times T_{CK} + 2$ | — | ns |

¹ The actual maximum frequency supported is limited by the FlexSPI_n_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI_n_FLSHAxCR1 register, the default values are shown above. Please refer to the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for more details.

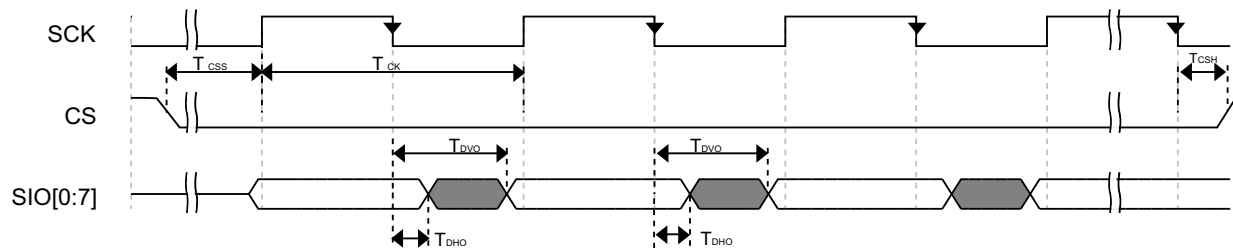


Figure 25. FlexSPI output timing in SDR mode

4.5.2.2.2 SDR mode

Table 45. FlexSPI output timing in SDR mode

| Symbol | Parameter | Min | Max | Unit |
|-----------|---|-----------------------------|-----|------|
| | Frequency of operation ¹ | — | 166 | MHz |
| T_{ck} | SCK clock period (FlexSPI _n _MCR0[RXCLKSRC] = 0x0) | 6.0 | — | ns |
| T_{DVO} | Output data valid time | — | 2.2 | ns |
| T_{DHO} | Output data hold time | 0.8 | — | ns |
| T_{CSS} | Chip select output setup time | $3 \times T_{CK} / 2 - 0.7$ | — | ns |
| T_{CSH} | Chip select output hold time | $3 \times T_{CK} / 2 + 0.8$ | — | ns |

¹ The actual maximum frequency supported is limited by the FlexSPI_n_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI_n_FLSHAxCR1 register, the default values are shown above. Please refer to the *i.MX RT1064 Reference Manual (IMXRT1064RM)* for more details.

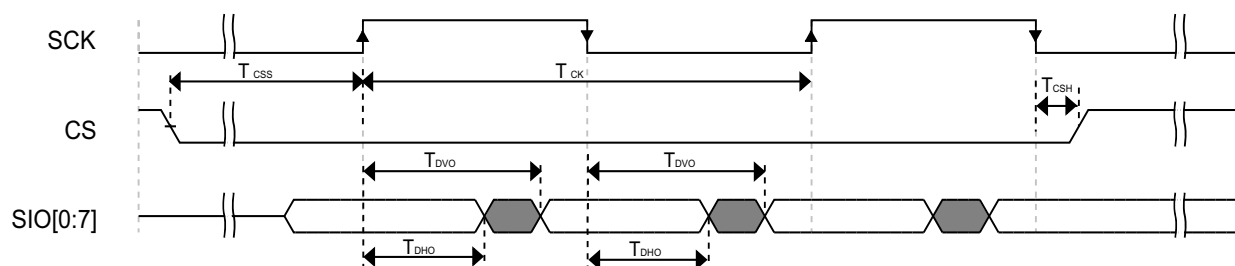


Figure 26. FlexSPI output timing in DDR mode

4.6 Display and graphics

The following sections provide information on display and graphic interfaces.

4.6.1 CMOS Sensor Interface (CSI) timing parameters

The following sections describe the CSI timing in gated and ungated clock modes.

4.6.1.0.1 Gated clock mode timing

Figure 27 and Figure 28 shows the gated clock mode timings for CSI, and Table 46 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC (VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

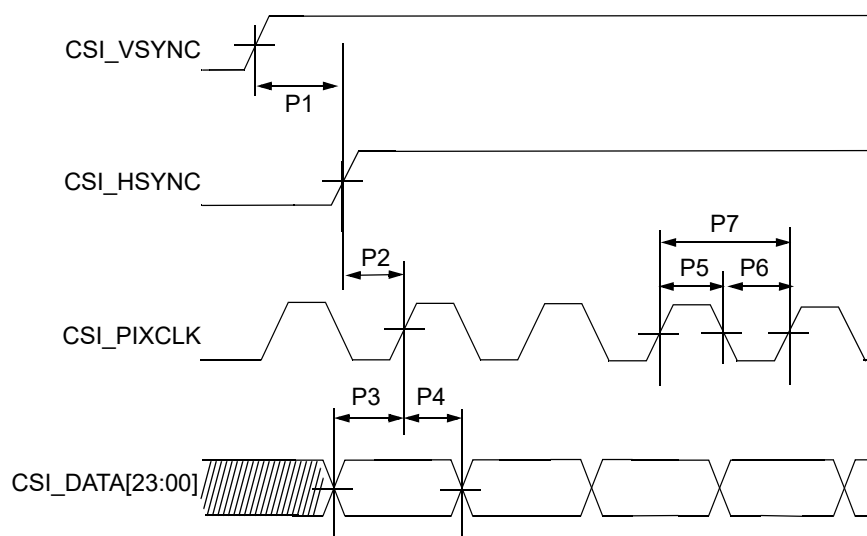


Figure 27. CSI Gated clock mode—sensor data at falling edge, latch data at rising edge

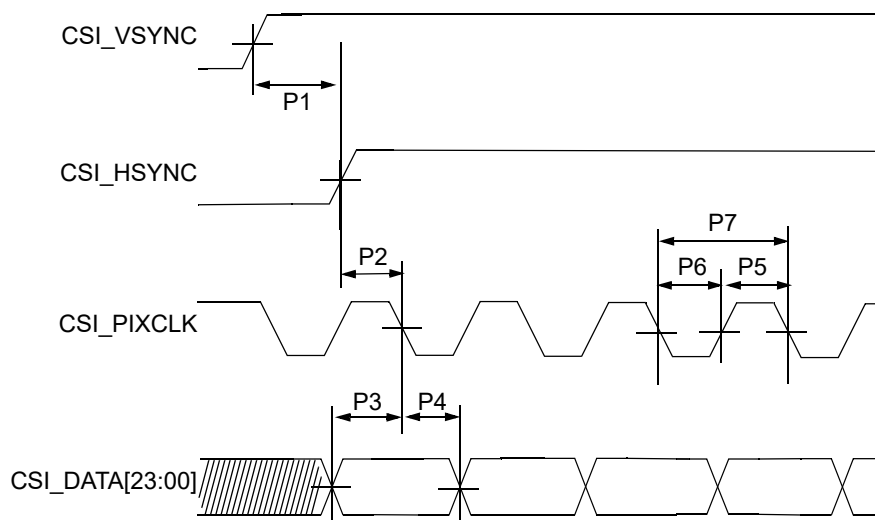


Figure 28. CSI Gated clock mode—sensor data at rising edge, latch data at falling edge

Table 46. CSI gated clock mode timing parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|----|-----------------------------|--------|------|------|-------|
| P1 | CSI_VSYNC to CSI_HSYNC time | tV2H | 33.5 | — | ns |
| P2 | CSI_HSYNC setup time | tHsu | 1 | — | ns |
| P3 | CSI DATA setup time | tDsu | 1 | — | ns |
| P4 | CSI DATA hold time | tDh | 1 | — | ns |
| P5 | CSI pixel clock high time | tCLKh | 3.75 | — | ns |
| P6 | CSI pixel clock low time | tCLKl | 3.75 | — | ns |
| P7 | CSI pixel clock frequency | fCLK | — | 80 | MHz |

4.6.1.0.2 Ungated clock mode timing

Figure 29 shows the ungated clock mode timings of CSI, and Table 47 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

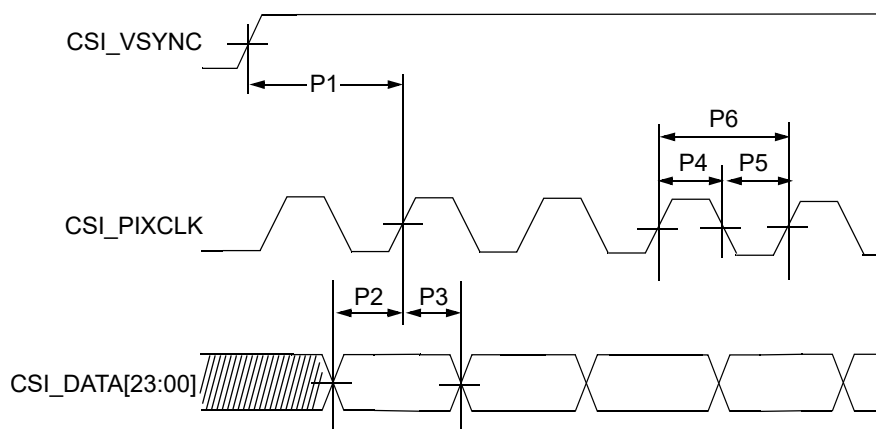


Figure 29. CSI ungated clock mode—sensor data at falling edge, latch data at rising edge

Table 47. CSI ungated clock mode timing parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|----|-------------------------------|--------|------|------|-------|
| P1 | CSI_VSYNC to pixel clock time | tVSYNC | 33.5 | — | ns |
| P2 | CSI DATA setup time | tDsu | 1 | — | ns |
| P3 | CSI DATA hold time | tDh | 1 | — | ns |
| P4 | CSI pixel clock high time | tCLKh | 3.75 | — | ns |
| P5 | CSI pixel clock low time | tCLKl | 3.75 | — | ns |
| P6 | CSI pixel clock frequency | fCLK | — | 80 | MHz |

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

4.6.2 LCD Controller (LCDIF) timing parameters

Figure 30 shows the LCDIF timing and Table 48 lists the timing parameters.

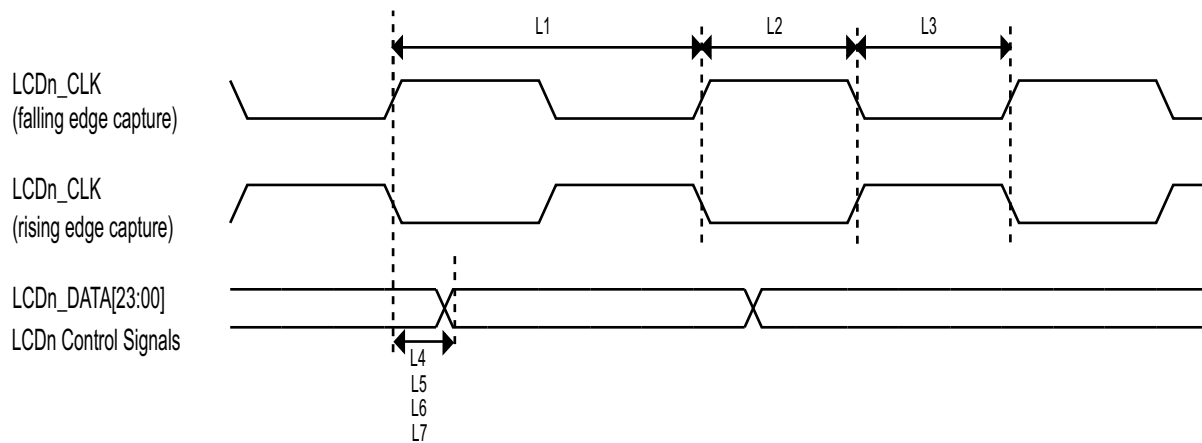


Figure 30. LCD timing

Table 48. LCD timing parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|----|---|----------------|-----|-----|------|
| L1 | LCD pixel clock frequency | tCLK(LCD) | — | 75 | MHz |
| L2 | LCD pixel clock high (falling edge capture) | tCLKH(LCD) | 3 | — | ns |
| L3 | LCD pixel clock low (rising edge capture) | tCLKL(LCD) | 3 | — | ns |
| L4 | LCD pixel clock high to data valid (falling edge capture) | td(CLKH-DV) | -1 | 1 | ns |
| L5 | LCD pixel clock low to data valid (rising edge capture) | td(CLKL-DV) | -1 | 1 | ns |
| L6 | LCD pixel clock high to control signal valid (falling edge capture) | td(CLKH-CTRLV) | -1 | 1 | ns |
| L7 | LCD pixel clock low to control signal valid (rising edge capture) | td(CLKL-CTRLV) | -1 | 1 | ns |

4.7 Audio

This section provide information about SAI/I2S and SPDIF.

4.7.1 SAI/I2S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 49. Master mode SAI timing

| Num | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|-------------|
| S1 | SAI_MCLK cycle time | 15 | — | ns |
| S2 | SAI_MCLK pulse width high/low | 40% | 60% | MCLK period |
| S3 | SAI_BCLK cycle time | 40 | — | ns |
| S4 | SAI_BCLK pulse width high/low | 40% | 60% | BCLK period |
| S5 | SAI_BCLK to SAI_FS output valid | — | 15 | ns |
| S6 | SAI_BCLK to SAI_FS output invalid | 0 | — | ns |
| S7 | SAI_BCLK to SAI_TXD valid | — | 15 | ns |
| S8 | SAI_BCLK to SAI_TXD invalid | 0 | — | ns |
| S9 | SAI_RXD/SAI_FS input setup before SAI_BCLK | 15 | — | ns |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK | 0 | — | ns |

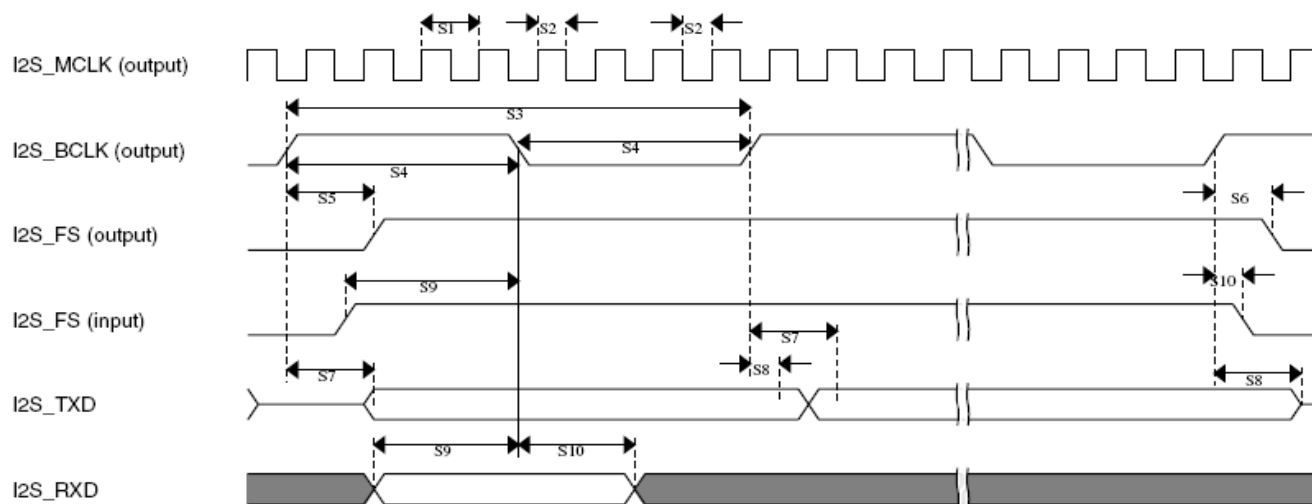


Figure 31. SAI timing—Master modes

Table 50. Slave mode SAI timing

| Num | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|-------------|
| S11 | SAI_BCLK cycle time (input) | 40 | — | ns |
| S12 | SAI_BCLK pulse width high/low (input) | 40% | 60% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK | 10 | — | ns |
| S14 | SAI_FS input hold after SAI_BCLK | 2 | — | ns |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid | — | 20 | ns |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0 | — | ns |

Table 50. Slave mode SAI timing

| Num | Characteristic | Min | Max | Unit |
|-----|-------------------------------|-----|-----|------|
| S17 | SAI_RXD setup before SAI_BCLK | 10 | — | ns |
| S18 | SAI_RXD hold after SAI_BCLK | 2 | — | ns |

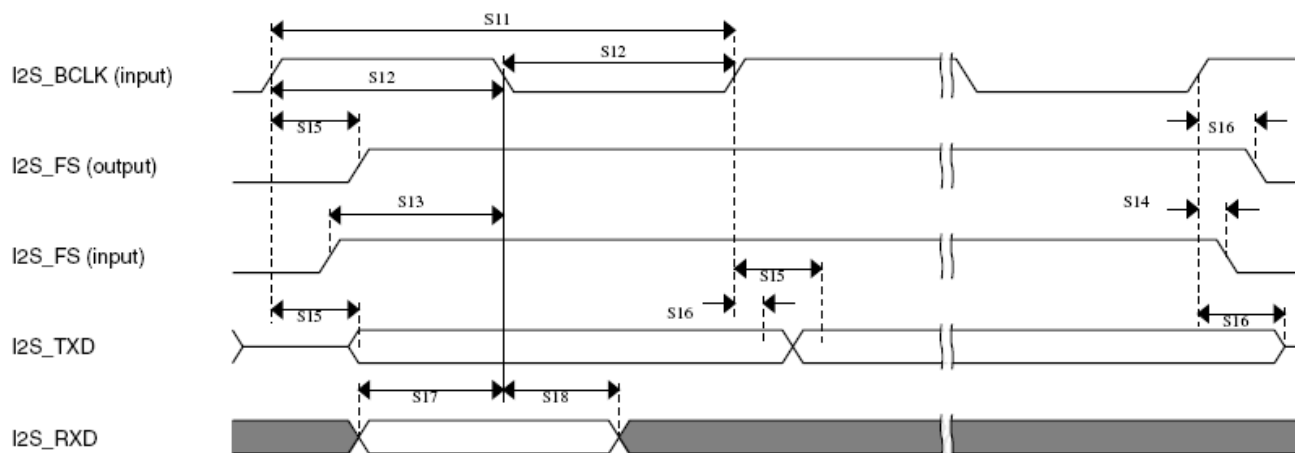


Figure 32. SAI timing—Slave mode

4.7.2 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 51 and Figure 33 and Figure 34 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 51. SPDIF timing parameters

| Characteristics | Symbol | Timing Parameter Range | | Unit |
|--|--------|------------------------|------|------|
| | | Min | Max | |
| SPDIF_IN Skew: asynchronous inputs, no specs apply | — | — | 0.7 | ns |
| SPDIF_OUT output (Load = 50pf) | — | — | 1.5 | ns |
| • Skew | — | — | 24.2 | |
| • Transition rising | — | — | 31.3 | |
| SPDIF_OUT1 output (Load = 30pf) | — | — | 1.5 | ns |
| • Skew | — | — | 13.6 | |
| • Transition rising | — | — | 18.0 | |
| Modulating Rx clock (SPDIF_SR_CLK) period | srckp | 40.0 | — | ns |

Table 51. SPDIF timing parameters (continued)

| Characteristics | Symbol | Timing Parameter Range | | Unit |
|---|---------|------------------------|-----|------|
| | | Min | Max | |
| SPDIF_SR_CLK high period | srckph | 16.0 | — | ns |
| SPDIF_SR_CLK low period | srckpl | 16.0 | — | ns |
| Modulating Tx clock (SPDIF_ST_CLK) period | stclkp | 40.0 | — | ns |
| SPDIF_ST_CLK high period | stclkph | 16.0 | — | ns |
| SPDIF_ST_CLK low period | stckpl | 16.0 | — | ns |

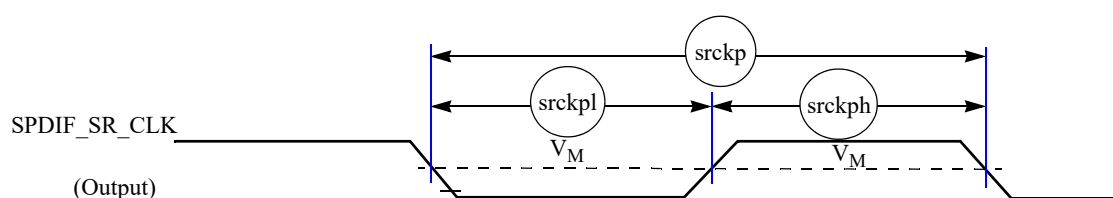


Figure 33. SPDIF_SR_CLK timing diagram

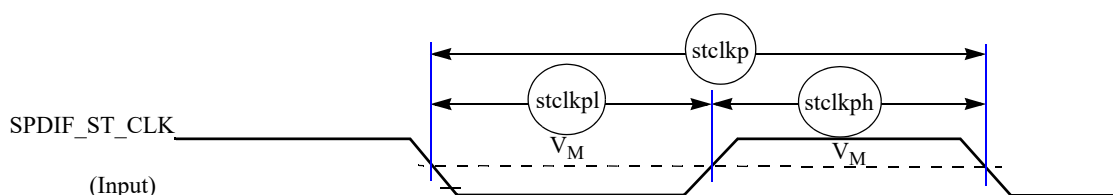


Figure 34. SPDIF_ST_CLK timing diagram

4.8 Analog

The following sections provide information about analog interfaces.

4.8.1 DCDC

Table 52 introduces the DCDC electrical specifications.

Table 52. DCDC electrical specifications

| Mode | Buck mode, one output | Notes |
|----------------------------|-----------------------|--|
| Input voltage | 3.3 V | Min = 2.8 V, Max = 3.6 V |
| Output voltage | 1.1 V | Configurable 0.8 - 1.575 with 25 mV one step in Run mode |
| Max loading | 500 mA | — |
| Loading in low power modes | 200 μ A ~ 30 mA | — |

Table 52. DCDC electrical specifications (continued)

| Mode | Buck mode, one output | Notes |
|-------------------------|--|---|
| Efficiency | 90% max | @150 mA |
| Low power mode | Open loop mode | Ripple is about 15 mV in Run mode |
| Run mode | <ul style="list-style-type: none"> Always continuous mode Support discontinuous mode | Configurable by register |
| Inductor | 4.7 μ H | — |
| Capacitor | 33 μ F | — |
| Over voltage protection | 1.55 V | Detect VDDSOC, when the voltage is higher than 1.6 V, shutdown DCDC. |
| Over Current protection | 1 A | Detect the peak current <ul style="list-style-type: none"> Run mode: when the current is larger than 1 A, shutdown DCDC. |
| Low DCDC_IN detection | 2.6 V | Detect the DCDC_IN, when battery is lower than 2.6 V, shutdown DCDC. |

4.8.2 A/D converter

This section introduces information about A/D converter.

4.8.2.1 12-bit ADC electrical characteristics

The section provide information about 12-bit ADC electrical characteristics.

4.8.2.1.1 12-bit ADC operating conditions

Table 53. 12-bit ADC operating conditions

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|-------------------|--------------------------------------|-------------------|-----------------|------------------|------------------|-------|---------|
| Supply voltage | Absolute | V _{DDA} | 3.0 | - | 3.6 | V | — |
| | Delta to VDD (VDD-VDDA) ² | ΔV_{DDA} | -100 | 0 | 100 | mV | — |
| Ground voltage | Delta to VSS (VSS-VSSAD) | ΔV_{SSAD} | -100 | 0 | 100 | mV | — |
| Ref Voltage High | — | V _{DDA} | 1.13 | V _{DDA} | V _{DDA} | V | — |
| Ref Voltage Low | — | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V | — |
| Input Voltage | — | V _{ADIN} | V _{SS} | — | V _{DDA} | V | — |
| Input Capacitance | 8/10/12 bit modes | C _{ADIN} | — | 1.5 | 2 | pF | — |
| Input Resistance | ADLPC=0, ADHSC=1 | R _{ADIN} | — | 5 | 7 | kohms | — |
| | ADLPC=0, ADHSC=0 | | — | 12.5 | 15 | kohms | — |
| | ADLPC=1, ADHSC=0 | | — | 25 | 30 | kohms | — |

Table 53. 12-bit ADC operating conditions (continued)

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|---|---|------------|-----|------------------|-----|-------|--------------------------------|
| Analog Source Resistance | 12 bit mode $f_{ADCK} = 40\text{MHz}$ ADLSMP=0, ADSTS=10, ADHSC=1 | R_{AS} | — | — | 1 | kohms | $T_{\text{samp}}=150\text{ns}$ |
| R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS} | | | | | | | |
| ADC Conversion Clock Frequency | ADLPC=0, ADHSC=1 12 bit mode | f_{ADCK} | 4 | — | 40 | MHz | — |
| | ADLPC=0, ADHSC=0 12 bit mode | | 4 | — | 30 | MHz | — |
| | ADLPC=1, ADHSC=0 12 bit mode | | 4 | — | 20 | MHz | — |

¹ Typical values assume $V_{DDAD} = 3.0\text{V}$, $\text{Temp} = 25^\circ\text{C}$, $f_{ADCK}=20\text{MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential differences

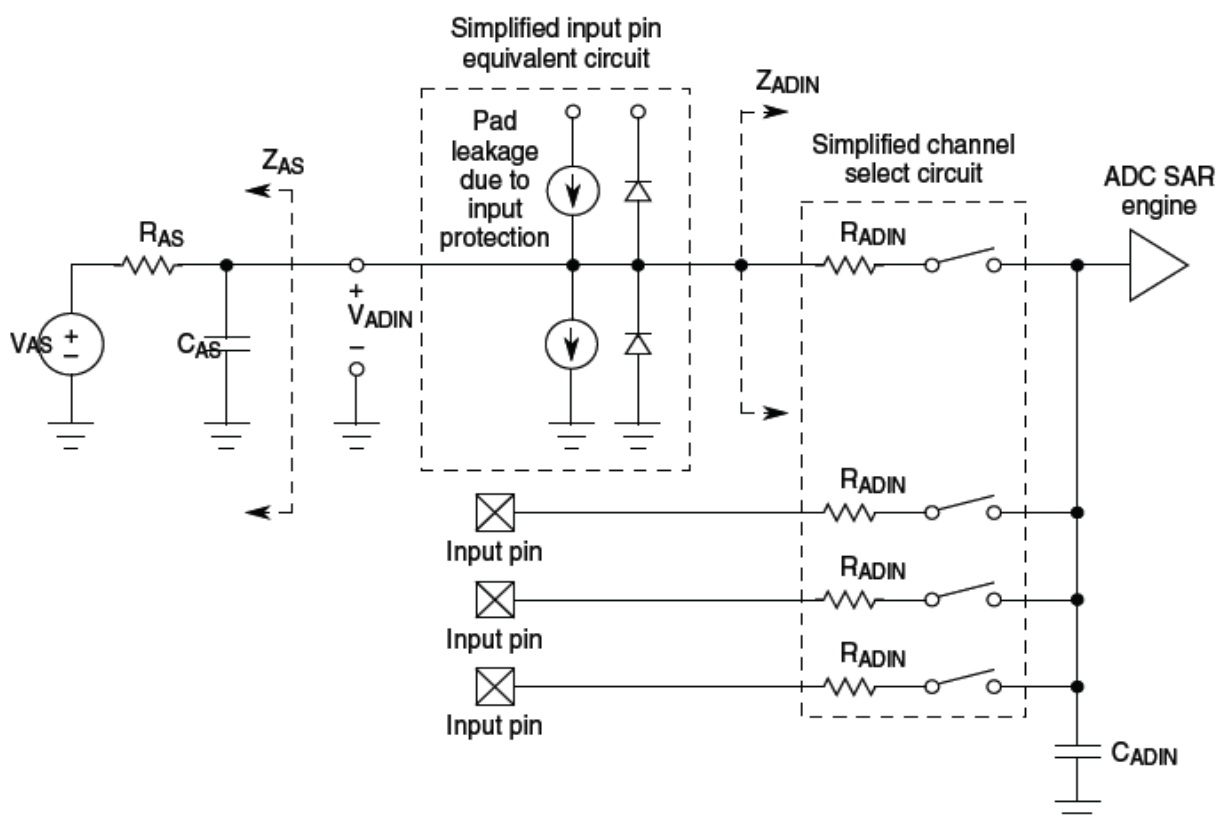


Figure 35. 12-bit ADC input impedance equivalency diagram

12-bit ADC characteristics

Table 54. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSAD}$)

| Characteristic | Conditions ¹ | Symb | Min | Typ ² | Max | Unit | Comment |
|----------------------------------|----------------------------|-------------|-----|------------------|-----|---------|-----------------------------|
| Supply Current | ADLPC=1, ADHSC=0 | I_{DDA} | — | 350 | — | μA | ADLSMP=0 ADSTS=10 ADCO=1 |
| | ADLPC=0, ADHSC=0 | | | 460 | | | |
| | ADLPC=0, ADHSC=1 | | | 750 | | | |
| Supply Current | Stop, Reset, Module Off | I_{DDA} | — | 1.4 | 2 | μA | — |
| ADC Asynchronous Clock Source | ADHSC=0 | f_{ADACK} | — | 10 | — | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | ADHSC=1 | | — | 20 | — | | |
| Sample Cycles | ADLSMP=0, ADSTS=00 | Csamp | — | 2 | — | cycles | — |
| | ADLSMP=0, ADSTS=01 | | | 4 | | | |
| | ADLSMP=0, ADSTS=10 | | | 6 | | | |
| | ADLSMP=0, ADSTS=11 | | | 8 | | | |
| | ADLSMP=1, ADSTS=00 | | | 12 | | | |
| | ADLSMP=1, ADSTS=01 | | | 16 | | | |
| | ADLSMP=1, ADSTS=10 | | | 20 | | | |
| | ADLSMP=1, ADSTS=11 | | | 24 | | | |

Table 54. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSAD}$) (continued)

| Characteristic | Conditions ¹ | Symb | Min | Typ ² | Max | Unit | Comment |
|----------------------------|-------------------------|-------|-----|------------------|-----|--|---------------------|
| Conversion Cycles | ADLSMP=0 ADSTS=00 | Cconv | — | 28 | — | cycles | — |
| | ADLSMP=0 ADSTS=01 | | | 30 | | | |
| | ADLSMP=0 ADSTS=10 | | | 32 | | | |
| | ADLSMP=0 ADSTS=11 | | | 34 | | | |
| | ADLSMP=1 ADSTS=00 | | | 38 | | | |
| | ADLSMP=1 ADSTS=01 | | | 42 | | | |
| | ADLSMP=1 ADSTS=10 | | | 46 | | | |
| | ADLSMP=1, ADSTS=11 | | | 50 | | | |
| Conversion Time | ADLSMP=0 ADSTS=00 | Tconv | — | 0.7 | — | μ s | Fadc=40 MHz |
| | ADLSMP=0 ADSTS=01 | | | 0.75 | | | |
| | ADLSMP=0 ADSTS=10 | | | 0.8 | | | |
| | ADLSMP=0 ADSTS=11 | | | 0.85 | | | |
| | ADLSMP=1 ADSTS=00 | | | 0.95 | | | |
| | ADLSMP=1 ADSTS=01 | | | 1.05 | | | |
| | ADLSMP=1 ADSTS=10 | | | 1.15 | | | |
| | ADLSMP=1, ADSTS=11 | | | 1.25 | | | |
| Total Unadjusted Error | 12 bit mode | TUE | — | 3.4 | — | LSB 1 LSB = $(V_{REFH} - V_{REFL})/2$ N | AVGE = 1, AVGS = 11 |
| | 10 bit mode | | — | 1.5 | — | | |
| | 8 bit mode | | — | 1.2 | — | | |
| Differential Non-Linearity | 12 bit mode | DNL | — | 0.76 | — | LSB | AVGE = 1, AVGS = 11 |
| | 10bit mode | | — | 0.36 | — | | |
| | 8 bit mode | | — | 0.14 | — | | |

Table 54. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSAD}$) (continued)

| Characteristic | Conditions ¹ | Symb | Min | Typ ² | Max | Unit | Comment |
|---------------------------------|-------------------------|-----------------|----------------------------|------------------|-----|------|---------------------|
| Integral Non-Linearity | 12 bit mode | INL | — | 2.78 | — | LSB | AVGE = 1, AVGS = 11 |
| | 10bit mode | | — | 0.61 | — | | |
| | 8 bit mode | | — | 0.14 | — | | |
| Zero-Scale Error | 12 bit mode | E _{ZS} | — | -1.14 | — | LSB | AVGE = 1, AVGS = 11 |
| | 10bit mode | | — | -0.25 | — | | |
| | 8 bit mode | | — | -0.19 | — | | |
| Full-Scale Error | 12 bit mode | E _{FS} | — | -1.06 | — | LSB | AVGE = 1, AVGS = 11 |
| | 10bit mode | | — | -0.03 | — | | |
| | 8 bit mode | | — | -0.02 | — | | |
| Effective Number of Bits | 12 bit mode | ENOB | 10.1 | 10.7 | — | Bits | AVGE = 1, AVGS = 11 |
| Signal to Noise plus Distortion | See ENOB | SINAD | SINAD = 6.02 x ENOB + 1.76 | | | dB | AVGE = 1, AVGS = 11 |

¹ All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

² Typical values assume $V_{DDAD} = 3.0$ V, Temp = 25°C, $F_{adck} = 20$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

4.8.3 ACMP

Table 55 lists the ACMP electrical specifications.

Table 55. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|---|----------|------|----------|------|
| V_{DD} | Supply voltage | 3.0 | — | 3.6 | V |
| I_{DDHS} | Supply current, High-speed mode (EN = 1, PMODE = 1) | — | 347 | — | μA |
| $I_{DDL S}$ | Supply current, Low-speed mode (EN = 1, PMODE = 0) | — | 42 | — | μA |
| V_{AIN} | Analog input voltage | V_{SS} | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 21 | mV |

Table 55. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------|---|----------------|----------|------|------------------|
| V_H | Analog comparator hysteresis ¹ | | | | mV |
| | • CR0[HYSTCTR] = 00 | — | 1 | 2 | |
| | • CR0[HYSTCTR] = 01 | — | 21 | 54 | |
| | • CR0[HYSTCTR] = 10 | — | 42 | 108 | |
| | • CR0[HYSTCTR] = 11 | — | 64 | 184 | |
| V_{CMPOH} | Output high | $V_{DD} - 0.5$ | — | — | V |
| V_{CMPOI} | Output low | — | — | 0.5 | V |
| t_{DHS} | Propagation delay, high-speed mode (EN = 1, PMODE = 1) ² | — | 25 | 40 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN = 1, PMODE = 0) ² | — | 50 | 90 | ns |
| t_{DInit} | Analog comparator initialization delay ³ | — | 1.5 | — | μs |
| I_{DAC6b} | 6-bit DAC current adder (enabled) | — | 5 | — | μA |
| R_{DAC6b} | 6-bit DAC reference inputs | — | V_{DD} | — | V |
| INL_{DAC6b} | 6-bit DAC integral non-linearity | -0.3 | — | 0.3 | LSB ⁴ |
| DNL_{DAC6b} | 6-bit DAC differential non-linearity | -0.15 | — | 0.15 | LSB ⁴ |

¹ Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD} - 0.7$ V in high speed mode.

² Signal swing is 100 mV.

³ Comparator initialization delay is defined as the time between software writes to the enable comparator module and the comparator output setting to a stable level.

⁴ 1 LSB = $V_{reference} / 64$

4.9 Communication interfaces

The following sections provide the information about communication interfaces.

4.9.1 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

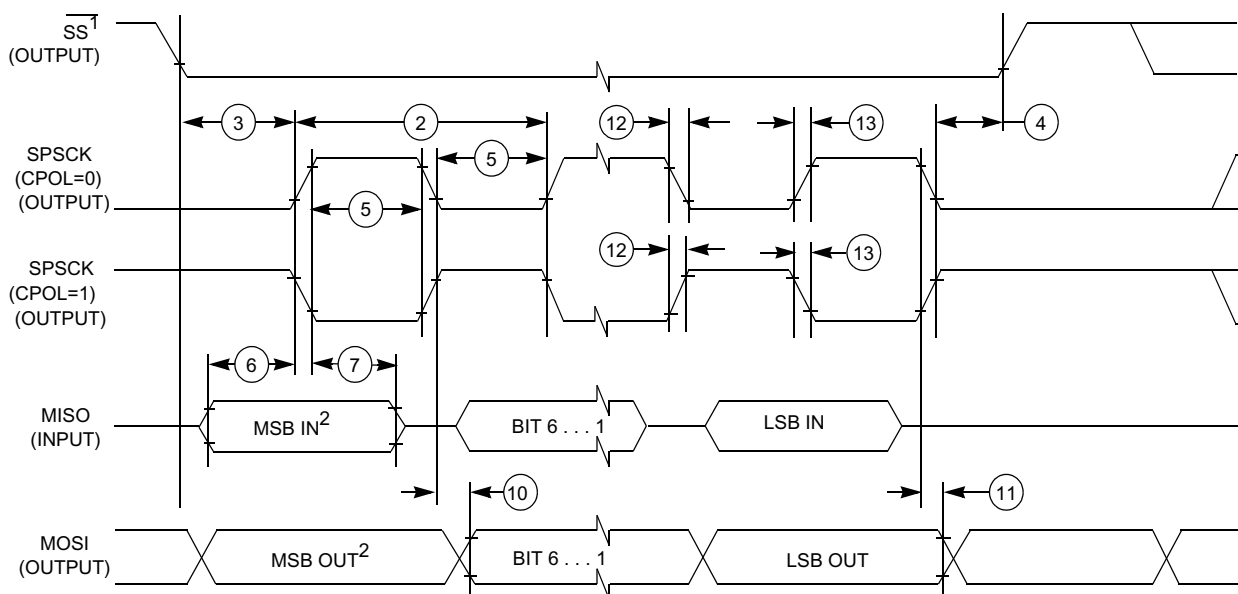
All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 56. LPSPI Master mode timing

| Number | Symbol | Description | Min. | Max. | Units | Note |
|--------|----------------------|--------------------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{OP} | Frequency of operation | $f_{periph} / 2048$ | $f_{periph} / 2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 18 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |
| 8 | t_V | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} t_{FI} | Rise time input Fall time input | — | $t_{periph} - 25$ | ns | — |
| 11 | t_{RO} t_{FO} | Rise time output Fall time output | — | 25 | ns | — |

¹ Absolute maximum frequency of operation (f_{op}) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must be guaranteed this limit is not exceeded.

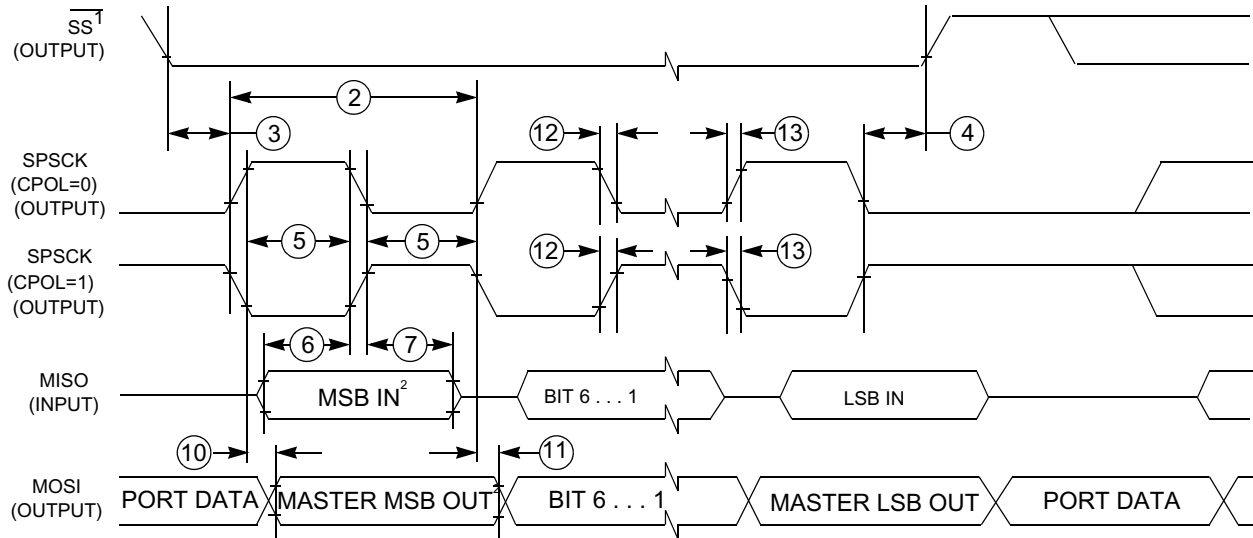
² $t_{periph} = 1 / f_{periph}$



1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 36. LPSPI Master mode timing (CPHA = 0)



1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 37. LPSPI Master mode timing (CPHA = 1)

Table 57. LPSPI Slave mode timing

| Number | Symbol | Description | Min. | Max. | Units | Note |
|--------|----------------------|------------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{OP} | Frequency of operation | 0 | $f_{periph} / 2$ | Hz | 1 |
| 2 | t_{SPSCCK} | SPSCCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | $t_{WSPSCCK}$ | Clock (SPSCCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_V | Data valid (after SPSCCK edge) | — | 31 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} t_{FI} | Rise time input Fall time input | — | $t_{periph} - 25$ | ns | — |
| 13 | t_{RO} t_{FO} | Rise time input Fall time input | — | 25 | ns | — |

¹ Absolute maximum frequency of operation (f_{op}) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must be guaranteed this limit is not exceeded.

² $t_{periph} = 1 / f_{periph}$

³ Time to data active from high-impedance state

⁴ Hold time to high-impedance state

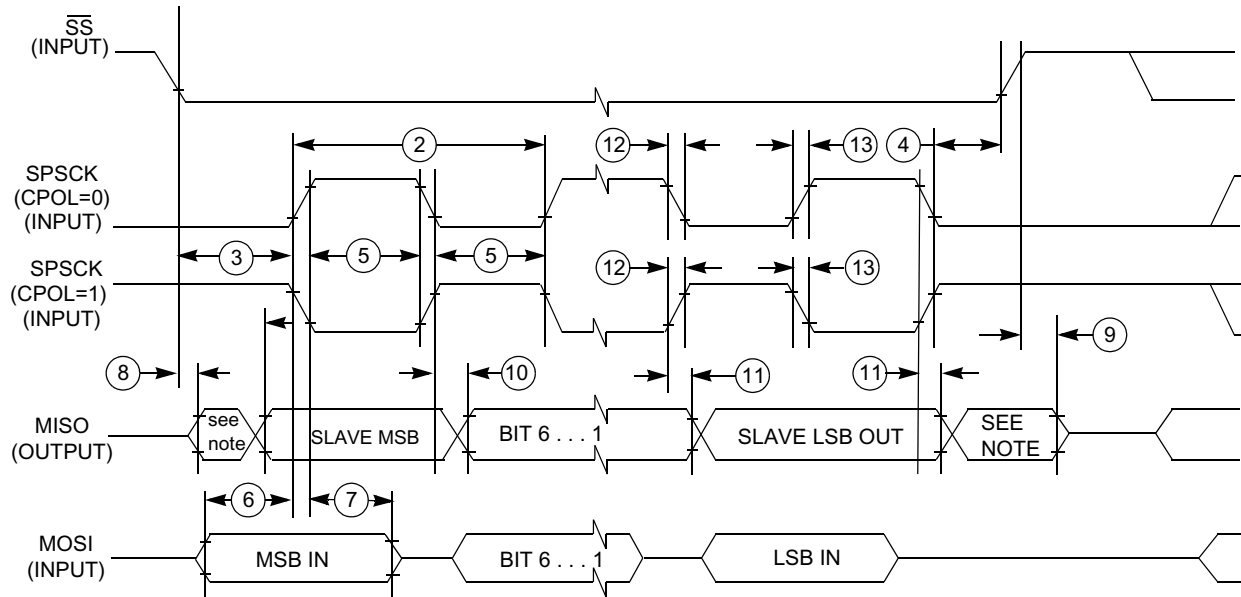


Figure 38. LPSPI Slave mode timing (CPHA = 0)

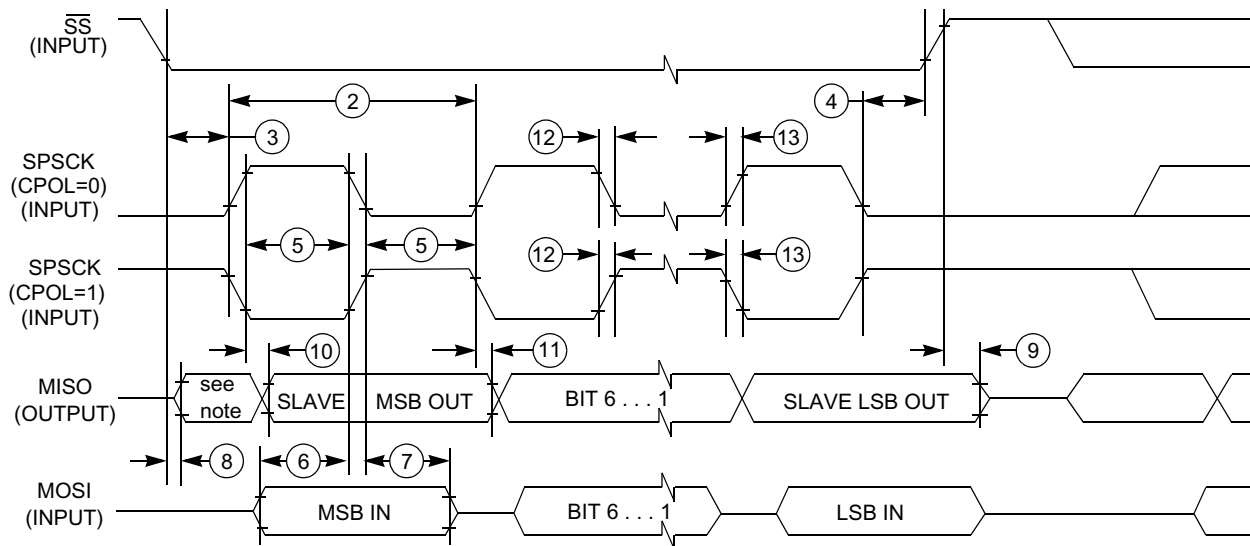


Figure 39. LPSPI Slave mode timing (CPHA = 1)

4.9.2 LPI2C module timing parameters

This section describes the timing parameters of the LPI2C module.

Table 58. LPI2C module timing parameters

| Symbol | Description | | Min | Max | Unit | Notes |
|-----------|---------------------|---------------------------|-----|------|------|-------|
| f_{SCL} | SCL clock frequency | Standard mode (Sm) | 0 | 100 | kHz | 1, 2 |
| | | Fast mode (Fm) | 0 | 400 | | |
| | | Fast mode Plus (Fm+) | 0 | 1000 | | |
| | | Ultra Fast mode (UFm) | 0 | 5000 | | |
| | | High speed mode (Hs-mode) | 0 | 3400 | | |

¹ Hs-mode is only supported in slave mode.

² See General switching specifications.

4.9.3 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41/4.5 (Dual Data Rate) timing and SDR104/50(SD3.0) timing.

4.9.3.1 SD/eMMC4.3 (single data rate) AC timing

Figure 40 depicts the timing of SD/eMMC4.3, and Table 59 lists the SD/eMMC4.3 timing characteristics.

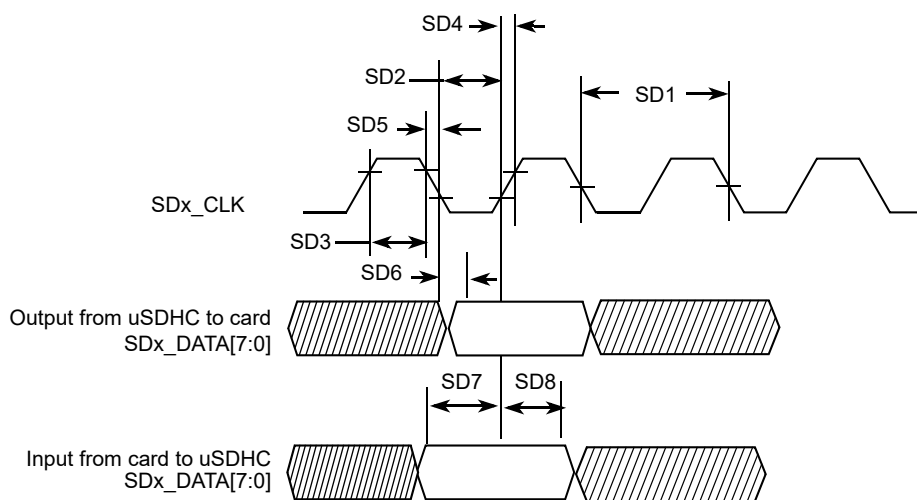


Figure 40. SD/eMMC4.3 timing

Table 59. SD/eMMC4.3 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|---|------------|------|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed/High Speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock Frequency (MMC Full Speed/High Speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock Frequency (Identification Mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock Low Time | t_{WL} | 7 | — | ns |
| SD3 | Clock High Time | t_{WH} | 7 | — | ns |
| SD4 | Clock Rise Time | t_{TLH} | — | 3 | ns |
| SD5 | Clock Fall Time | t_{THL} | — | 3 | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD6 | uSDHC Output Delay | t_{OD} | -6.6 | 3.6 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD7 | uSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD8 | uSDHC Input Hold Time ⁴ | t_{IH} | 1.5 | — | ns |

¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

³ In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.3.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 41 depicts the timing of eMMC4.4/4.41. Table 60 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

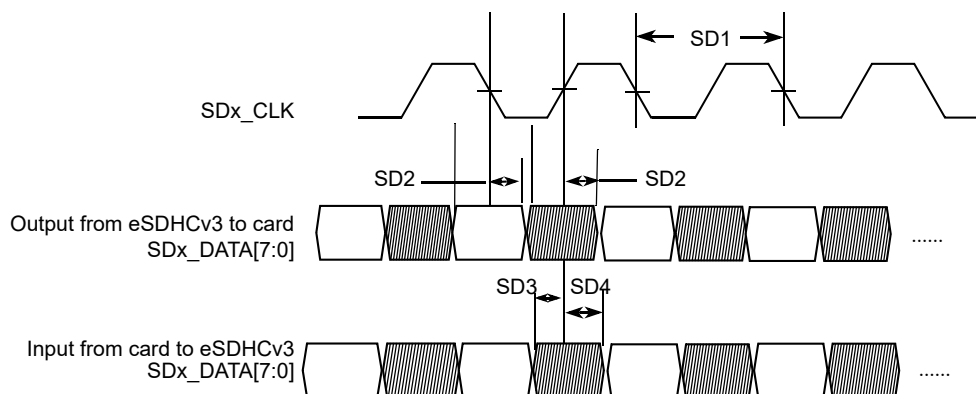


Figure 41. eMMC4.4/4.41 timing

Table 60. eMMC4.4/4.41 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|------------------------------------|-----------|-----|-----|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (eMMC4.4/4.41 DDR) | f_{PP} | 0 | 52 | MHz |
| SD1 | Clock Frequency (SD3.0 DDR) | f_{PP} | 0 | 50 | MHz |
| uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD2 | uSDHC Output Delay | t_{OD} | 2.5 | 7.1 | ns |
| uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD3 | uSDHC Input Setup Time | t_{ISU} | 1.7 | — | ns |
| SD4 | uSDHC Input Hold Time | t_{IH} | 1.5 | — | ns |

4.9.3.3 SDR50/SDR104 AC timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 61 lists the SDR50/SDR104 timing characteristics.

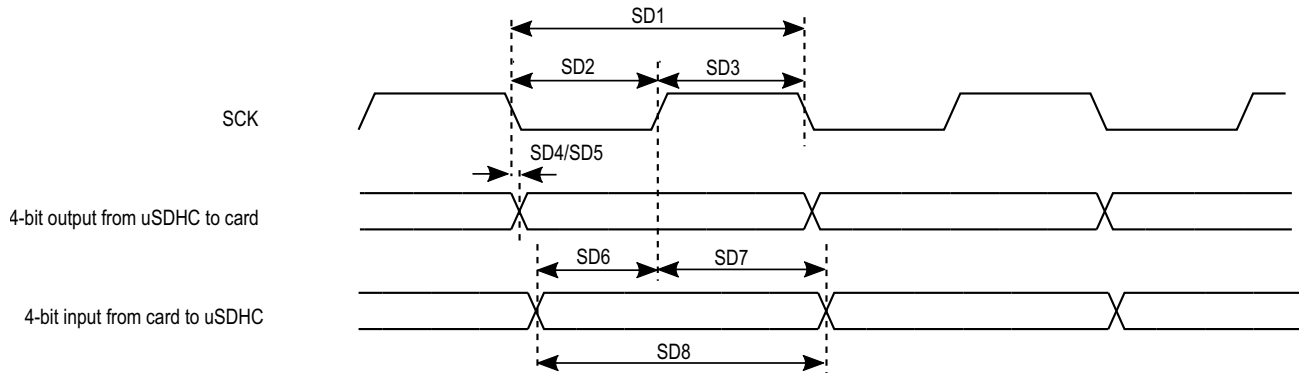


Figure 42. SDR50/SDR104 timing

Table 61. SDR50/SDR104 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|-------------------------|-----------|-----------------------|-----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency Period | t_{CLK} | 5.0 | — | ns |
| SD2 | Clock Low Time | t_{CL} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| SD3 | Clock High Time | t_{CH} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK) | | | | | |
| SD4 | uSDHC Output Delay | t_{OD} | -3 | 1 | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK) | | | | | |
| SD5 | uSDHC Output Delay | t_{OD} | -1.6 | 1 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK) | | | | | |
| SD6 | uSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD7 | uSDHC Input Hold Time | t_{IH} | 1.5 | — | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)¹ | | | | | |
| SD8 | Card Output Data Window | t_{ODW} | $0.5 \times t_{CLK}$ | — | ns |

¹Data window in SDR104 mode is variable.

4.9.3.4 HS200 mode timing

Figure 43 depicts the timing of HS200 mode, and Table 62 lists the HS200 timing characteristics.

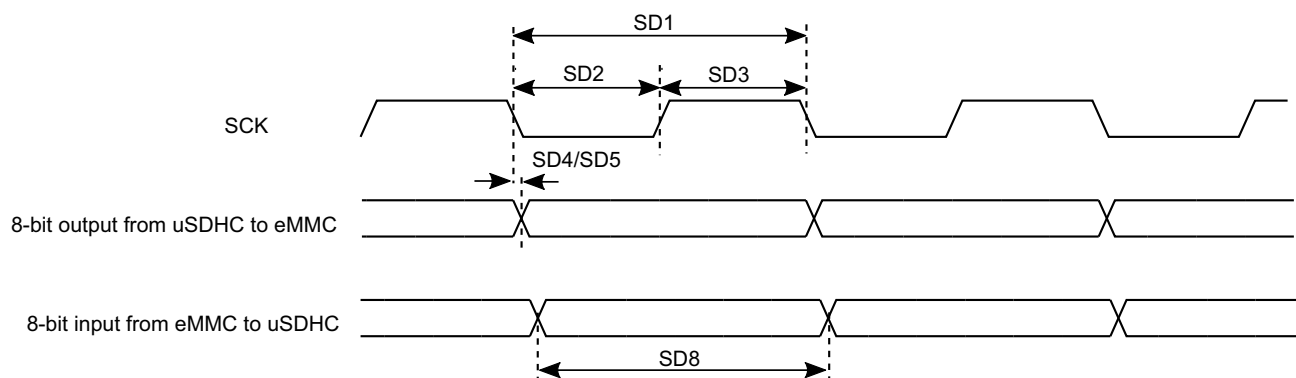


Figure 43. HS200 mode timing

Table 62. HS200 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|-------------------------|-----------|-----------------------|-----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency Period | t_{CLK} | 5.0 | — | ns |
| SD2 | Clock Low Time | t_{CL} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| SD3 | Clock High Time | t_{CH} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK) | | | | | |
| SD5 | uSDHC Output Delay | t_{OD} | -1.6 | 0.74 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)¹ | | | | | |
| SD8 | Card Output Data Window | t_{ODW} | $0.5 \times t_{CLK}$ | — | ns |

¹HS200 is for 8 bits while SDR104 is for 4 bits.

4.9.3.5 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1 supply are identical to those shown in Table 21, "Single voltage GPIO DC parameters," on page 31.

4.9.4 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.9.4.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.9.4.1.1 MII receive signal timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 44 shows MII receive signal timings. Table 63 describes the timing parameters (M1–M4) shown in the figure.

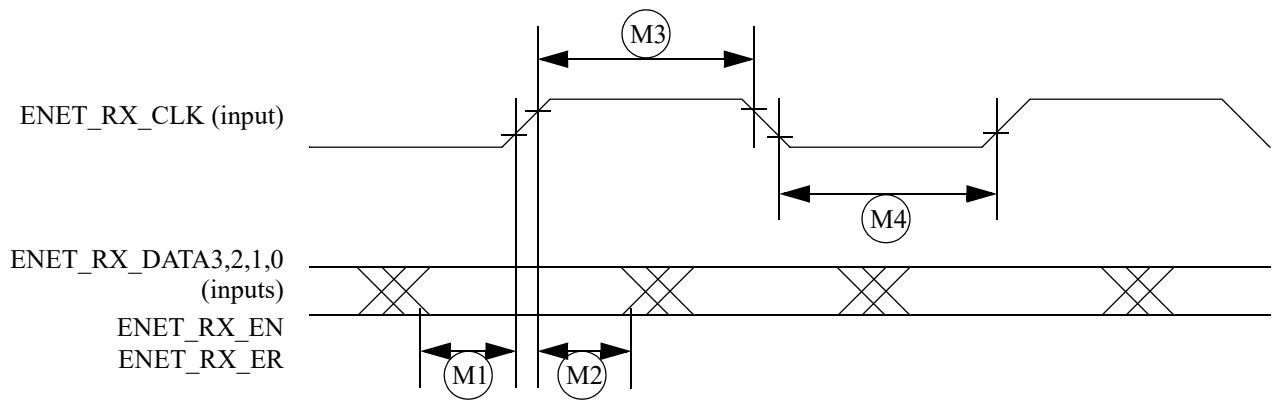


Figure 44. MII receive signal timing diagram

Table 63. MII receive signal timing

| ID | Characteristic ¹ | Min. | Max. | Unit |
|----|--|------|------|--------------------|
| M1 | ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup | 5 | — | ns |
| M2 | ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold | 5 | — | ns |
| M3 | ENET_RX_CLK pulse width high | 35% | 65% | ENET_RX_CLK period |
| M4 | ENET_RX_CLK pulse width low | 35% | 65% | ENET_RX_CLK period |

¹ ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.9.4.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 45 shows MII transmit signal timings. Table 64 describes the timing parameters (M5–M8) shown in the figure.

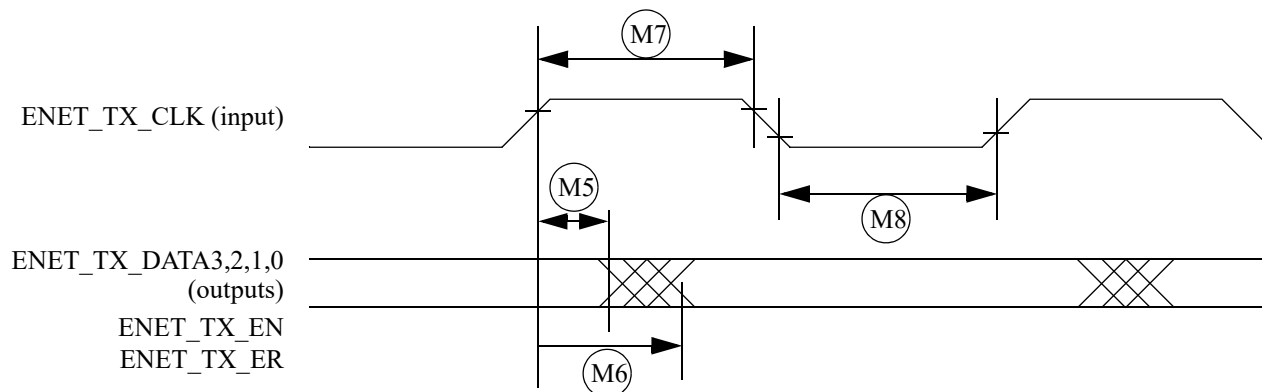


Figure 45. MII transmit signal timing diagram

Table 64. MII transmit signal timing

| ID | Characteristic ¹ | Min. | Max. | Unit |
|----|--|------|------|--------------------|
| M5 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid | 5 | — | ns |
| M6 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid | — | 20 | ns |
| M7 | ENET_TX_CLK pulse width high | 35% | 65% | ENET_TX_CLK period |
| M8 | ENET_TX_CLK pulse width low | 35% | 65% | ENET_TX_CLK period |

¹ ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.9.4.1.3 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

Figure 46 shows MII asynchronous input timings. Table 65 describes the timing parameter (M9) shown in the figure.

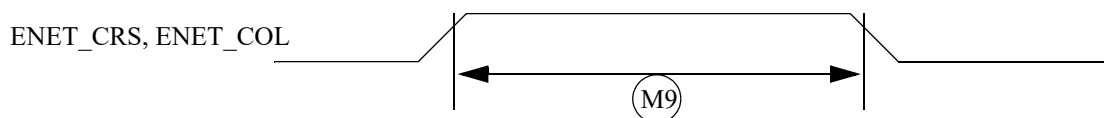


Figure 46. MII asynchronous inputs timing diagram

Table 65. MII asynchronous inputs signal timing

| ID | Characteristic | Min. | Max. | Unit |
|-----------------|--|------|------|--------------------|
| M9 ¹ | ENET_CRS to ENET_COL minimum pulse width | 1.5 | — | ENET_TX_CLK period |

¹ ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.9.4.1.4 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 47 shows MII asynchronous input timings. Table 66 describes the timing parameters (M10–M15) shown in the figure.

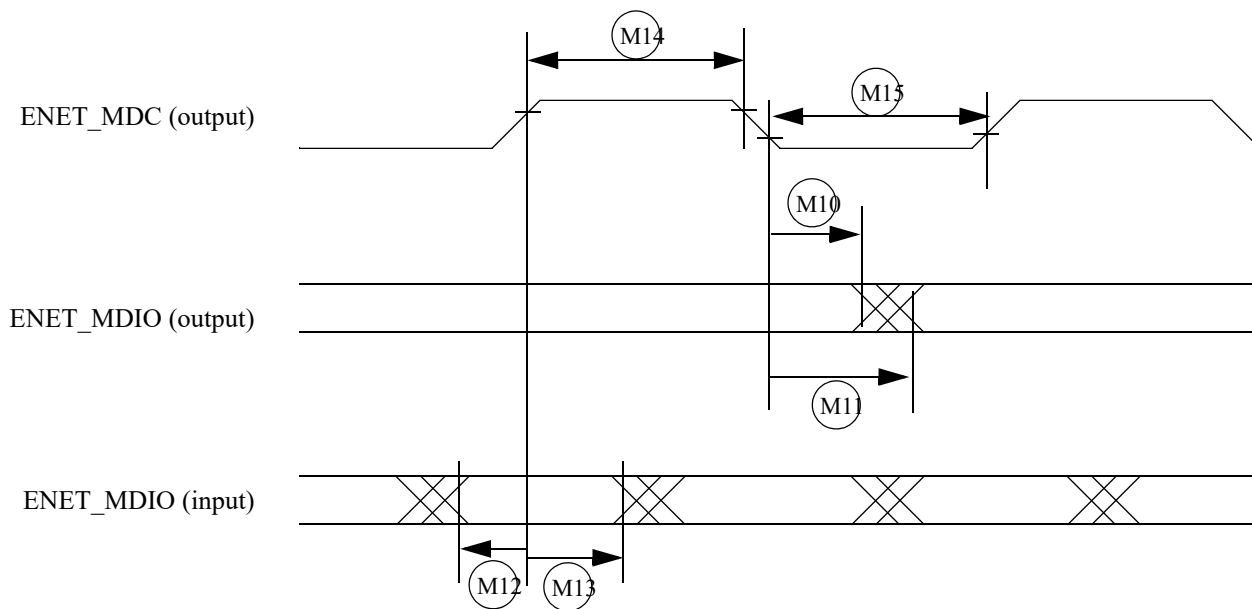


Figure 47. MII serial management channel timing diagram

Table 66. MII serial management channel timing

| ID | Characteristic | Min. | Max. | Unit |
|-----|--|------|------|-----------------|
| M10 | ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay) | 0 | — | ns |
| M11 | ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay) | — | 5 | ns |
| M12 | ENET_MDIO (input) to ENET_MDC rising edge setup | 18 | — | ns |
| M13 | ENET_MDIO (input) to ENET_MDC rising edge hold | 0 | — | ns |
| M14 | ENET_MDC pulse width high | 40% | 60% | ENET_MDC period |
| M15 | ENET_MDC pulse width low | 40% | 60% | ENET_MDC period |

4.9.4.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz \pm 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 48 shows RMI mode timings. Table 67 describes the timing parameters (M16–M21) shown in the figure.

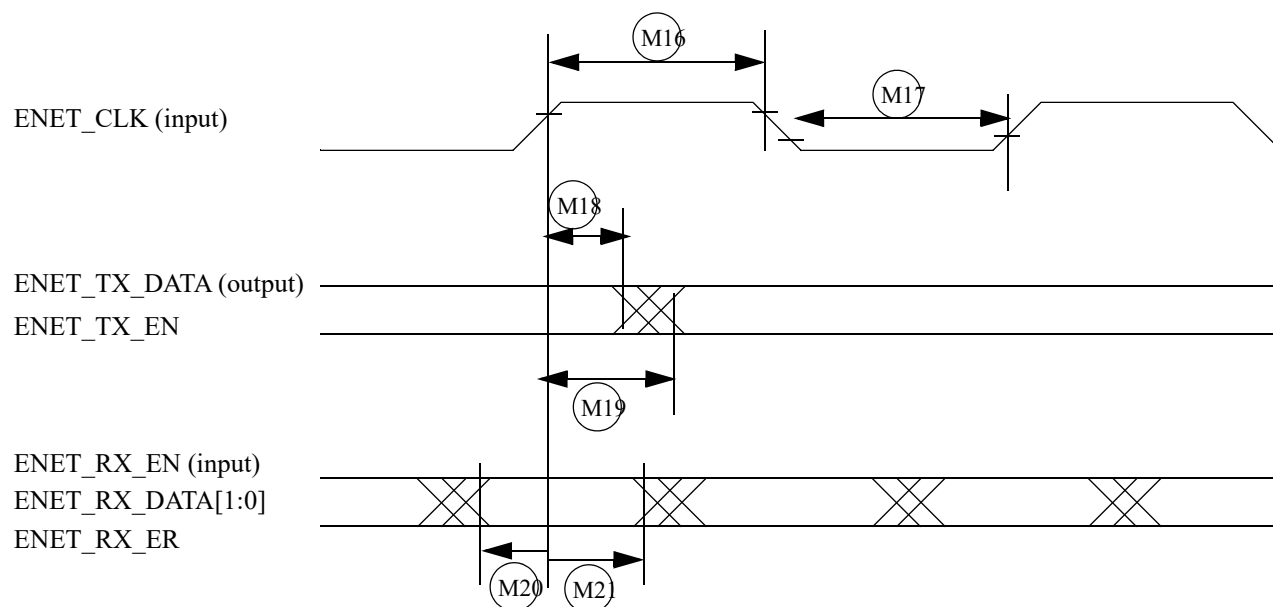


Figure 48. RMI mode signal timing diagram

Table 67. RMI signal timing

| ID | Characteristic | Min. | Max. | Unit |
|-----|---|------|------|-----------------|
| M16 | ENET_CLK pulse width high | 35% | 65% | ENET_CLK period |
| M17 | ENET_CLK pulse width low | 35% | 65% | ENET_CLK period |
| M18 | ENET_CLK to ENET_TXD[1:0], ENET_TX_DATA invalid | 4 | — | ns |
| M19 | ENET_CLK to ENET_TXD[1:0], ENET_TX_DATA valid | — | 13 | ns |
| M20 | ENET_RX_DATA[1:0], ENET_RX_EN, ENET_RX_ER to ENET_CLK setup | 2 | — | ns |
| M21 | ENET_CLK to ENET_RX_DATA[1:0], ENET_RX_EN, ENET_RX_ER hold | 2 | — | ns |

4.9.5 Flexible Controller Area Network (FLEXCAN) AC electrical specifications

Please refer to [Section 4.3.2.1, General purpose I/O AC parameters](#).

4.9.6 LPUART electrical specifications

Please refer to [Section 4.3.2.1, General purpose I/O AC parameters](#).

4.9.7 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
 - Title: 5V Short Circuit Withstand Requirement Change
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
 - Title: Pull-up/Pull-down resistors
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: Suspend Current Limit Changes
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: USB 2.0 Phase Locked SOFs
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
 - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
 - Revision 1.2, December 7, 2010
 - Portable device only

4.10 Timers

This section provide information on timers.

4.10.1 Pulse Width Modulator (PWM) characteristics

This section describes the electrical information of the PWM.

Table 68. PWM timing parameters

| Parameter | Symbo | Min | Typ | Max | Unit |
|---------------------|-------|-----|-----|-----|------|
| PWM Clock Frequency | — | — | — | 150 | MHz |

4.10.2 Quad timer timing

[Table 69](#) listed the timing parameters.

Table 69. Quad timer timing

| Characteristic | Symbol | Min ¹ | Max | Unit | See Figure |
|------------------------------|-------------|------------------|-----|------|------------|
| Timer input period | T_{IN} | $2T + 6$ | — | ns | |
| Timer input high/low period | T_{INHL} | $1T + 3$ | — | ns | |
| Timer output period | T_{OUT} | 33 | — | ns | |
| Timer output high/low period | T_{OUTHL} | 16.7 | — | ns | |

¹ T = clock cycle. For 60 MHz operation, T = 16.7 ns.

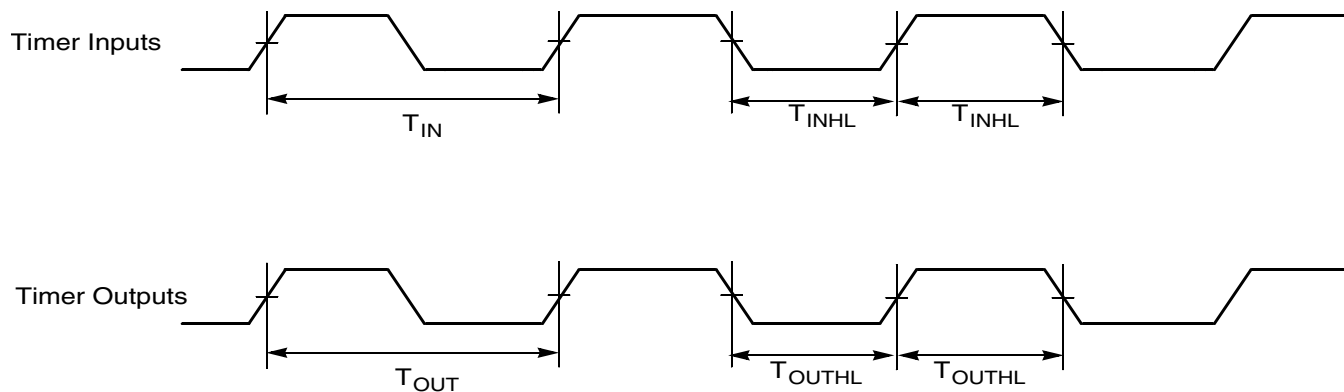


Figure 49. Quad timer timing

5 Flash

This section introduces the on-chip flash electrical parameters.

[Table 70](#) shows the operating ranges of on-chip flash power supply by NVCC_GPIO.

Table 70. Operating ranges

| Parameter | Symbol | Conditions | Spec. | | Unit |
|----------------|-----------|--|-------|-----|------|
| | | | Min | Max | |
| Supply voltage | NVCC_GPIO | $F_R = 133 \text{ MHz}$, $f_R = 50 \text{ MHz}$ | 3.0 | 3.6 | V |

For details about the flash AC parameters, refer to the following [link](#).

6 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

6.1 Boot mode configuration pins

Table 71 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX RT1064 Fuse Map document and the System Boot chapter in *i.MX RT1064 Reference Manual (IMXRT1064RM)*.

Table 71. Fuses and associated pins used for boot

| Pad | Default setting on reset | eFuse name | Details |
|---------------|--------------------------|------------|--|
| GPIO_AD_B0_04 | 100 K pull-down | BOOT_MODE0 | Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses. |
| GPIO_AD_B0_05 | 100 K pull-down | BOOT_MODE1 | |
| GPIO_B0_04 | 100 K pull-down | BT_CFG[0] | |
| GPIO_B0_05 | 100 K pull-down | BT_CFG[1] | |
| GPIO_B0_06 | 100 K pull-down | BT_CFG[2] | |
| GPIO_B0_07 | 100 K pull-down | BT_CFG[3] | |
| GPIO_B0_08 | 100 K pull-down | BT_CFG[4] | |
| GPIO_B0_09 | 100 K pull-down | BT_CFG[5] | |
| GPIO_B0_10 | 100 K pull-down | BT_CFG[6] | |
| GPIO_B0_11 | 100 K pull-down | BT_CFG[7] | |
| GPIO_B0_12 | 100 K pull-down | BT_CFG[8] | |
| GPIO_B0_13 | 100 K pull-down | BT_CFG[9] | |
| GPIO_B0_14 | 100 K pull-down | BT_CFG[10] | |
| GPIO_B0_15 | 100 K pull-down | BT_CFG[11] | |

6.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 72. Boot trough NAND

| PAD Name | IO Function | ALT | Comments |
|-------------|--------------|-------|----------|
| GPIO_EMC_00 | semc.DATA[0] | ALT 0 | — |
| GPIO_EMC_01 | semc.DATA[1] | ALT 0 | — |
| GPIO_EMC_02 | semc.DATA[2] | ALT 0 | — |

Table 72. Boot trough NAND

| | | | |
|-------------|---------------|-------|---|
| GPIO_EMC_03 | semc.DATA[3] | ALT 0 | — |
| GPIO_EMC_04 | semc.DATA[4] | ALT 0 | — |
| GPIO_EMC_05 | semc.DATA[5] | ALT 0 | — |
| GPIO_EMC_06 | semc.DATA[6] | ALT 0 | — |
| GPIO_EMC_07 | semc.DATA[7] | ALT 0 | — |
| GPIO_EMC_30 | semc.DATA[8] | ALT 0 | — |
| GPIO_EMC_31 | semc.DATA[9] | ALT 0 | — |
| GPIO_EMC_32 | semc.DATA[10] | ALT 0 | — |
| GPIO_EMC_33 | semc.DATA[11] | ALT 0 | — |
| GPIO_EMC_34 | semc.DATA[12] | ALT 0 | — |
| GPIO_EMC_35 | semc.DATA[13] | ALT 0 | — |
| GPIO_EMC_36 | semc.DATA[14] | ALT 0 | — |
| GPIO_EMC_37 | semc.DATA[15] | ALT 0 | — |
| GPIO_EMC_18 | semc.ADDR[9] | ALT 0 | — |
| GPIO_EMC_19 | semc.ADDR[11] | ALT 0 | — |
| GPIO_EMC_20 | semc.ADDR[12] | ALT 0 | — |
| GPIO_EMC_22 | semc.BA1 | ALT 0 | — |
| GPIO_EMC_41 | semc.CSX[0] | ALT 0 | — |

Table 73. Boot trough NOR

| PAD Name | IO Function | ALT | Comments |
|-------------|---------------|-------|----------|
| GPIO_EMC_00 | semc.DATA[0] | ALT 0 | — |
| GPIO_EMC_01 | semc.DATA[1] | ALT 0 | — |
| GPIO_EMC_02 | semc.DATA[2] | ALT 0 | — |
| GPIO_EMC_03 | semc.DATA[3] | ALT 0 | — |
| GPIO_EMC_04 | semc.DATA[4] | ALT 0 | — |
| GPIO_EMC_05 | semc.DATA[5] | ALT 0 | — |
| GPIO_EMC_06 | semc.DATA[6] | ALT 0 | — |
| GPIO_EMC_07 | semc.DATA[7] | ALT 0 | — |
| GPIO_EMC_30 | semc.DATA[8] | ALT 0 | — |
| GPIO_EMC_31 | semc.DATA[9] | ALT 0 | — |
| GPIO_EMC_32 | semc.DATA[10] | ALT 0 | — |
| GPIO_EMC_33 | semc.DATA[11] | ALT 0 | — |

Table 73. Boot trough NOR

| | | | |
|-------------|---------------|-------|---|
| GPIO_EMC_34 | semc.DATA[12] | ALT 0 | — |
| GPIO_EMC_35 | semc.DATA[13] | ALT 0 | — |
| GPIO_EMC_36 | semc.DATA[14] | ALT 0 | — |
| GPIO_EMC_37 | semc.DATA[15] | ALT 0 | — |
| GPIO_EMC_09 | semc.ADDR[0] | ALT 0 | — |
| GPIO_EMC_10 | semc.ADDR[1] | ALT 0 | — |
| GPIO_EMC_11 | semc.ADDR[2] | ALT 0 | — |
| GPIO_EMC_12 | semc.ADDR[3] | ALT 0 | — |
| GPIO_EMC_13 | semc.ADDR[4] | ALT 0 | — |
| GPIO_EMC_14 | semc.ADDR[5] | ALT 0 | — |
| GPIO_EMC_15 | semc.ADDR[6] | ALT 0 | — |
| GPIO_EMC_16 | semc.ADDR[7] | ALT 0 | — |
| GPIO_EMC_19 | semc.ADDR[11] | ALT 0 | — |
| GPIO_EMC_20 | semc.ADDR[12] | ALT 0 | — |
| GPIO_EMC_21 | semc.BA0 | ALT 0 | — |
| GPIO_EMC_22 | semc.BA1 | ALT 0 | — |
| GPIO_EMC_41 | semc.CSX[0] | ALT 0 | — |

Table 74. Boot through FlexSPI

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|-------------------|----------|----------|
| GPIO_SD_B1_00 | flexspi.B_DATA[3] | ALT 1 | — |
| GPIO_SD_B1_01 | flexspi.B_DATA[2] | ALT 1 | — |
| GPIO_SD_B1_02 | flexspi.B_DATA[1] | ALT 1 | — |
| GPIO_SD_B1_03 | flexspi.B_DATA[0] | ALT 1 | — |
| GPIO_SD_B1_04 | flexspi.B_SCLK | ALT 1 | — |
| GPIO_SD_B0_05 | flexspi.B_DQS | ALT 4 | — |
| GPIO_SD_B0_04 | flexspi.B_SS0_B | ALT 4 | — |
| GPIO_SD_B0_01 | flexspi.B_SS1_B | ALT 6 | — |
| GPIO_SD_B1_05 | flexspi.A_DQS | ALT 1 | — |
| GPIO_SD_B1_06 | flexspi.A_SS0_B | ALT 1 | — |
| GPIO_SD_B0_00 | flexspi.A_SS1_B | ALT 6 | — |
| GPIO_SD_B1_07 | flexspi.A_SCLK | ALT 1 | — |
| GPIO_SD_B1_08 | flexspi.A_DATA[0] | ALT 1 | — |
| GPIO_SD_B1_09 | flexspi.A_DATA[1] | ALT 1 | — |

Table 74. Boot through FlexSPI (continued)

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|-------------------|----------|----------|
| GPIO_SD_B1_10 | flexspi.A_DATA[2] | ALT 1 | — |
| GPIO_SD_B1_11 | flexspi.A_DATA[3] | ALT 1 | — |

Table 75. Boot through SD1

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|--------------|----------|----------|
| GPIO_SD_B0_00 | usdhc1.CMD | ALT 0 | — |
| GPIO_SD_B0_01 | usdhc1.CLK | ALT 0 | — |
| GPIO_SD_B0_02 | usdhc1.DATA0 | ALT 0 | — |
| GPIO_SD_B0_03 | usdhc1.DATA1 | ALT 0 | — |
| GPIO_SD_B0_04 | usdhc1.DATA2 | ALT 0 | — |
| GPIO_SD_B0_05 | usdhc1.DATA3 | ALT 0 | — |

Table 76. Boot through SD2

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|----------------|----------|----------|
| GPIO_SD_B1_00 | usdhc2.DATA3 | ALT 0 | — |
| GPIO_SD_B1_01 | usdhc2.DATA2 | ALT 0 | — |
| GPIO_SD_B1_02 | usdhc2.DATA1 | ALT 0 | — |
| GPIO_SD_B1_03 | usdhc2.DATA0 | ALT 0 | — |
| GPIO_SD_B1_04 | usdhc2.CLK | ALT 0 | — |
| GPIO_SD_B1_05 | usdhc2.CMD | ALT 0 | — |
| GPIO_SD_B1_06 | usdhc2.RESET_B | ALT 0 | — |
| GPIO_SD_B1_08 | usdhc2.DATA4 | ALT 0 | — |
| GPIO_SD_B1_09 | usdhc2.DATA5 | ALT 0 | — |
| GPIO_SD_B1_10 | usdhc2.DATA6 | ALT 0 | — |
| GPIO_SD_B1_11 | usdhc2.DATA7 | ALT 0 | — |

Table 77. Boot through SPI-1

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|-------------|----------|----------|
| GPIO_SD_B0_00 | lpspi1.SCK | ALT 4 | — |
| GPIO_SD_B0_02 | lpspi1.SDO | ALT 4 | — |
| GPIO_SD_B0_03 | lpspi1.SDI | ALT 4 | — |
| GPIO_SD_B0_01 | lpspi1.PCS0 | ALT 4 | — |

Table 78. Boot through SPI-2

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|-------------|----------|----------|
| GPIO_SD_B1_07 | lpspi2.SCK | ALT 4 | — |
| GPIO_SD_B1_08 | lpspi2.SDO | ALT 4 | — |
| GPIO_SD_B1_09 | lpspi2.SDI | ALT 4 | — |
| GPIO_SD_B1_06 | lpspi2.PCS0 | ALT 4 | — |

Table 79. Boot through SPI-3

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|-------------|----------|----------|
| GPIO_AD_B0_00 | lpspi3.SCK | ALT 7 | — |
| GPIO_AD_B0_01 | lpspi3.SDO | ALT 7 | — |
| GPIO_AD_B0_02 | lpspi3.SDI | ALT 7 | — |
| GPIO_SD_B0_03 | lpspi3.PCS0 | ALT 7 | — |

Table 80. Boot through SPI-4

| PAD Name | IO Function | Mux Mode | Comments |
|------------|-------------|----------|----------|
| GPIO_B0_03 | lpspi4.SCK | ALT 3 | — |
| GPIO_B0_02 | lpspi4.SDO | ALT 3 | — |
| GPIO_B0_01 | lpspi4.SDI | ALT 3 | — |
| GPIO_B0_00 | lpspi4.PCS0 | ALT 3 | — |

Table 81. Boot through UART1

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|---------------|----------|----------|
| GPIO_AD_B0_12 | lpuart1.TX | ALT 2 | — |
| GPIO_AD_B0_13 | lpuart1.RX | ALT 2 | — |
| GPIO_AD_B0_14 | lpuart1.CTS_B | ALT 2 | — |
| GPIO_AD_B0_15 | lpuart1.RTS_B | ALT 2 | — |

Table 82. Boot through UART2

| PAD Name | IO Function | Mux Mode | Comments |
|---------------|---------------|----------|----------|
| GPIO_AD_B1_00 | lpuart2.CTS_B | ALT 2 | — |
| GPIO_AD_B1_01 | lpuart2.RTS_B | ALT 2 | — |
| GPIO_AD_B1_02 | lpuart2.TX | ALT 2 | — |
| GPIO_AD_B1_03 | lpuart2.RX | ALT 2 | — |

7 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

7.1 10 x 10 mm package information

7.1.1 10 x 10 mm, 0.65 mm pitch, ball matrix

[Figure 50](#) shows the top, bottom, and side views of the 10 x 10 mm MAPBGA package.



7.1.2 10 x 10 mm supplies contact assignments and functional contact assignments

Table 83 shows the device connection list for ground, sense, and reference contact signals.

Table 83. 10 x 10 mm supplies contact assignment

| Supply Rail Name | Ball(s) Position(s) | Remark |
|------------------|---|--------|
| DCDC_IN | L1, L2 | — |
| DCDC_IN_Q | K4 | — |
| DCDC_GND | N1, N2 | — |
| DCDC_LP | M1, M2 | — |
| DCDC_PSWITCH | K3 | — |
| DCDC_SENSE | J5 | — |
| GPANAIO | N10 | — |
| NGND_KEL0 | K9 | — |
| NVCC EMC | E6, F5 | — |
| NVCC_GPIO | E9, F10, J10 | — |
| NVCC_PLL | P10 | — |
| NVCC_SD0 | J6 | — |
| NVCC_SD1 | K5 | — |
| VDDA_ADC_3P3 | N14 | — |
| VDD_HIGH_CAP | P8 | — |
| VDD_HIGH_IN | P12 | — |
| VDD_SNVS_CAP | M10 | — |
| VDD_SNVS_IN | M9 | — |
| VDD_SOC_IN | F6, F7, F8, F9, G6, G9, H6, H9, J9 | — |
| VDD_USB_CAP | K8 | — |
| VSS | A1, A14, B5, B10, E2, E13, G7, G8, H7, H8, J7, J8, K2, K13, L9, N5, N8, P1, P14 | — |

Table 84 shows an alpha-sorted list of functional contact assignments for the 10 x 10 mm package.

Table 84. 10 x 10 mm functional contact assignments

| Ball Name | 10 x 10 Ball | Power Group | Ball Type | Default Setting | | | |
|------------|--------------|-------------|-----------|-----------------|------------------|--------------|-------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| CCM_CLK1_N | P13 | — | — | — | CCM_CLK1_N | — | — |
| CCM_CLK1_P | N13 | — | — | — | CCM_CLK1_P | — | — |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|---------------|-----|-----------|--------------|------|------------------|-------|----------|
| GPIO_AD_B0_00 | M14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[0] | Input | Keeper |
| GPIO_AD_B0_01 | H10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[1] | Input | Keeper |
| GPIO_AD_B0_02 | M11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[2] | Input | Keeper |
| GPIO_AD_B0_03 | G11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[3] | Input | Keeper |
| GPIO_AD_B0_04 | F11 | NVCC_GPIO | Digital GPIO | ALT0 | SRC.BOOT.MODE[0] | Input | 100 K PD |
| GPIO_AD_B0_05 | G14 | NVCC_GPIO | Digital GPIO | ALT0 | SRC.BOOT.MODE[1] | Input | 100 K PD |
| GPIO_AD_B0_06 | E14 | NVCC_GPIO | Digital GPIO | ALT0 | JTAG.MUX.TMS | Input | 47 K PU |
| GPIO_AD_B0_07 | F12 | NVCC_GPIO | Digital GPIO | ALT0 | JTAG.MUX.TCK | Input | 47 K PU |
| GPIO_AD_B0_08 | F13 | NVCC_GPIO | Digital GPIO | ALT0 | JTAG.MUX.MOD | Input | 100 K PU |
| GPIO_AD_B0_09 | F14 | NVCC_GPIO | Digital GPIO | ALT0 | JTAG.MUX.TDI | Input | 47 K PU |
| GPIO_AD_B0_10 | G13 | NVCC_GPIO | Digital GPIO | ALT0 | JTAG.MUX.TDO | Input | Keeper |
| GPIO_AD_B0_11 | G10 | NVCC_GPIO | Digital GPIO | ALT0 | JTAG.MUX.TRSTB | Input | 47 K PU |
| GPIO_AD_B0_12 | K14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[12] | Input | Keeper |
| GPIO_AD_B0_13 | L14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[13] | Input | Keeper |
| GPIO_AD_B0_14 | H14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[14] | Input | Keeper |
| GPIO_AD_B0_15 | L10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[15] | Input | Keeper |
| GPIO_AD_B1_00 | J11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[16] | Input | Keeper |
| GPIO_AD_B1_01 | K11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[17] | Input | Keeper |
| GPIO_AD_B1_02 | L11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[18] | Input | Keeper |
| GPIO_AD_B1_03 | M12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[19] | Input | Keeper |
| GPIO_AD_B1_04 | L12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[20] | Input | Keeper |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|---------------|-----|-----------|--------------|------|--------------|-------|--------|
| GPIO_AD_B1_05 | K12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[21] | Input | Keeper |
| GPIO_AD_B1_06 | J12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[22] | Input | Keeper |
| GPIO_AD_B1_07 | K10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[23] | Input | Keeper |
| GPIO_AD_B1_08 | H13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[24] | Input | Keeper |
| GPIO_AD_B1_09 | M13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[25] | Input | Keeper |
| GPIO_AD_B1_10 | L13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[26] | Input | Keeper |
| GPIO_AD_B1_11 | J13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[27] | Input | Keeper |
| GPIO_AD_B1_12 | H12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[28] | Input | Keeper |
| GPIO_AD_B1_13 | H11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[29] | Input | Keeper |
| GPIO_AD_B1_14 | G12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[30] | Input | Keeper |
| GPIO_AD_B1_15 | J14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO1.IO[31] | Input | Keeper |
| GPIO_B0_00 | D7 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[0] | Input | Keeper |
| GPIO_B0_01 | E7 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[1] | Input | Keeper |
| GPIO_B0_02 | E8 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[2] | Input | Keeper |
| GPIO_B0_03 | D8 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[3] | Input | Keeper |
| GPIO_B0_04 | C8 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[4] | Input | Keeper |
| GPIO_B0_05 | B8 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[5] | Input | Keeper |
| GPIO_B0_06 | A8 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[6] | Input | Keeper |
| GPIO_B0_07 | A9 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[7] | Input | Keeper |
| GPIO_B0_08 | B9 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[8] | Input | Keeper |
| GPIO_B0_09 | C9 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[9] | Input | Keeper |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|------------|-----|-----------|--------------|------|--------------|-------|--------|
| GPIO_B0_10 | D9 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[10] | Input | Keeper |
| GPIO_B0_11 | A10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[11] | Input | Keeper |
| GPIO_B0_12 | C10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[12] | Input | Keeper |
| GPIO_B0_13 | D10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[13] | Input | Keeper |
| GPIO_B0_14 | E10 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[14] | Input | Keeper |
| GPIO_B0_15 | E11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[15] | Input | Keeper |
| GPIO_B1_00 | A11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[16] | Input | Keeper |
| GPIO_B1_01 | B11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[17] | Input | Keeper |
| GPIO_B1_02 | C11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[18] | Input | Keeper |
| GPIO_B1_03 | D11 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[19] | Input | Keeper |
| GPIO_B1_04 | E12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[20] | Input | Keeper |
| GPIO_B1_05 | D12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[21] | Input | Keeper |
| GPIO_B1_06 | C12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[22] | Input | Keeper |
| GPIO_B1_07 | B12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[23] | Input | Keeper |
| GPIO_B1_08 | A12 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[24] | Input | Keeper |
| GPIO_B1_09 | A13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[25] | Input | Keeper |
| GPIO_B1_10 | B13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[26] | Input | Keeper |
| GPIO_B1_11 | C13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[27] | Input | Keeper |
| GPIO_B1_12 | D13 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[28] | Input | Keeper |
| GPIO_B1_13 | D14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[29] | Input | Keeper |
| GPIO_B1_14 | C14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[30] | Input | Keeper |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|-------------|-----|-----------|--------------|------|--------------|-------|--------|
| GPIO_B1_15 | B14 | NVCC_GPIO | Digital GPIO | ALT5 | GPIO2.IO[31] | Input | Keeper |
| GPIO_EMC_00 | E3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[0] | Input | Keeper |
| GPIO_EMC_01 | F3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[1] | Input | Keeper |
| GPIO_EMC_02 | F4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[2] | Input | Keeper |
| GPIO_EMC_03 | G4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[3] | Input | Keeper |
| GPIO_EMC_04 | F2 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[4] | Input | Keeper |
| GPIO_EMC_05 | G5 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[5] | Input | Keeper |
| GPIO_EMC_06 | H5 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[6] | Input | Keeper |
| GPIO_EMC_07 | H4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[7] | Input | Keeper |
| GPIO_EMC_08 | H3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[8] | Input | Keeper |
| GPIO_EMC_09 | C2 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[9] | Input | Keeper |
| GPIO_EMC_10 | G1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[10] | Input | Keeper |
| GPIO_EMC_11 | G3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[11] | Input | Keeper |
| GPIO_EMC_12 | H1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[12] | Input | Keeper |
| GPIO_EMC_13 | A6 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[13] | Input | Keeper |
| GPIO_EMC_14 | B6 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[14] | Input | Keeper |
| GPIO_EMC_15 | B1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[15] | Input | Keeper |
| GPIO_EMC_16 | A5 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[16] | Input | Keeper |
| GPIO_EMC_17 | A4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[17] | Input | Keeper |
| GPIO_EMC_18 | B2 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[18] | Input | Keeper |
| GPIO_EMC_19 | B4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[19] | Input | Keeper |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|-------------|----|----------|--------------|------|--------------|-------|----------|
| GPIO_EMC_20 | A3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[20] | Input | Keeper |
| GPIO_EMC_21 | C1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[21] | Input | Keeper |
| GPIO_EMC_22 | F1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[22] | Input | Keeper |
| GPIO_EMC_23 | G2 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[23] | Input | Keeper |
| GPIO_EMC_24 | D3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[24] | Input | Keeper |
| GPIO_EMC_25 | D2 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[25] | Input | Keeper |
| GPIO_EMC_26 | B3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[26] | Input | Keeper |
| GPIO_EMC_27 | A2 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[27] | Input | 100 K PD |
| GPIO_EMC_28 | D1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[28] | Input | Keeper |
| GPIO_EMC_29 | E1 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[29] | Input | Keeper |
| GPIO_EMC_30 | C6 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[30] | Input | Keeper |
| GPIO_EMC_31 | C5 | NVCC_EMC | Digital GPIO | ALT5 | GPIO4.IO[31] | Input | Keeper |
| GPIO_EMC_32 | D5 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[18] | Input | Keeper |
| GPIO_EMC_33 | C4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[19] | Input | Keeper |
| GPIO_EMC_34 | D4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[20] | Input | Keeper |
| GPIO_EMC_35 | E5 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[21] | Input | Keeper |
| GPIO_EMC_36 | C3 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[22] | Input | Keeper |
| GPIO_EMC_37 | E4 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[23] | Input | Keeper |
| GPIO_EMC_38 | D6 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[24] | Input | Keeper |
| GPIO_EMC_39 | B7 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[25] | Input | Keeper |
| GPIO_EMC_40 | A7 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[26] | Input | Keeper |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|---------------|----|-------------|--------------|------|---------------------|--------|----------|
| GPIO_EMC_41 | C7 | NVCC_EMC | Digital GPIO | ALT5 | GPIO3.IO[27] | Input | Keeper |
| GPIO_SD_B0_00 | J4 | NVCC_SD0 | Digital GPIO | ALT5 | GPIO3.IO[12] | Input | Keeper |
| GPIO_SD_B0_01 | J3 | NVCC_SD0 | Digital GPIO | ALT5 | GPIO3.IO[13] | Input | Keeper |
| GPIO_SD_B0_02 | J1 | NVCC_SD0 | Digital GPIO | ALT5 | GPIO3.IO[14] | Input | Keeper |
| GPIO_SD_B0_03 | K1 | NVCC_SD0 | Digital GPIO | ALT5 | GPIO3.IO[15] | Input | Keeper |
| GPIO_SD_B0_04 | H2 | NVCC_SD0 | Digital GPIO | ALT5 | GPIO3.IO[16] | Input | Keeper |
| GPIO_SD_B0_05 | J2 | NVCC_SD0 | Digital GPIO | ALT5 | GPIO3.IO[17] | Input | Keeper |
| GPIO_SD_B1_00 | L5 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[0] | Input | Keeper |
| GPIO_SD_B1_01 | M5 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[1] | Input | Keeper |
| GPIO_SD_B1_02 | M3 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[2] | Input | Keeper |
| GPIO_SD_B1_03 | M4 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[3] | Input | Keeper |
| GPIO_SD_B1_04 | P2 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[4] | Input | Keeper |
| GPIO_SD_B1_05 | N3 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[5] | Input | Keeper |
| GPIO_SD_B1_06 | L3 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[6] | Input | Keeper |
| GPIO_SD_B1_07 | L4 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[7] | Input | Keeper |
| GPIO_SD_B1_08 | P3 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[8] | Input | Keeper |
| GPIO_SD_B1_09 | N4 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[9] | Input | Keeper |
| GPIO_SD_B1_10 | P4 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[01] | Input | Keeper |
| GPIO_SD_B1_11 | P5 | NVCC_SD1 | Digital GPIO | ALT5 | GPIO3.IO[11] | Input | Keeper |
| ONOFF | M6 | VDD_SNVS_IN | Digital GPIO | ALT0 | ONOFF | Input | 100 K PU |
| PMIC_ON_REQ | K7 | VDD_SNVS_IN | Digital GPIO | ALT0 | SNVS_LP.PMIC_ON_REQ | Output | 100 K PU |

Table 84. 10 x 10 mm functional contact assignments (continued)

| | | | | | | | |
|----------------|-----|--------------|--------------|------|------------------------|--------|----------------------------|
| PMIC_STBY_REQ | L7 | VDD_SNVIS_IN | Digital GPIO | ALT0 | CCM.PMIC_VSTBY_RE Q | Output | 100 K PU (PKE disabled) |
| POR_B | M7 | VDD_SNVIS_IN | Digital GPIO | ALT0 | SRC.POR_B | Input | 100 K PU |
| RTC_XTALI | N9 | — | — | — | — | — | — |
| RTC_XTALO | P9 | — | — | — | — | — | — |
| TEST_MODE | K6 | VDD_SNVIS_IN | Digital GPIO | ALT0 | TCU.TEST_MODE | Input | 100 K PU |
| USB_OTG1_CHD_B | N12 | — | — | — | — | — | — |
| USB_OTG1_DN | M8 | — | — | — | — | — | — |
| USB_OTG1_DP | L8 | — | — | — | — | — | — |
| USB_OTG1_VBUS | N6 | — | — | — | — | — | — |
| USB_OTG2_DN | N7 | — | — | — | — | — | — |
| USB_OTG2_DP | P7 | — | — | — | — | — | — |
| USB_OTG2_VBUS | P6 | — | — | — | — | — | — |
| XTALI | P11 | — | — | — | — | — | — |
| XTALO | N11 | — | — | — | — | — | — |
| WAKEUP | L6 | VDD_SNVIS_IN | Digital GPIO | ALT5 | GPIO5.IO[0] | Input | 100 K PU |

7.1.3 10 x 10 mm, 0.65 mm pitch, ball map

Table 85 shows the 10 x 10 mm, 0.65 mm pitch ball map for the i.MX RT1064.

Table 85. 10x10 mm, 0.65 mm pitch, ball map

| G | F | E | D | C | B | A |
|---------------|---------------|---------------|-------------|-------------|-------------|-------------|
| GPIO_EMC_10 | GPIO_EMC_22 | GPIO_EMC_29 | GPIO_EMC_28 | GPIO_EMC_21 | GPIO_EMC_15 | VSS |
| GPIO_EMC_23 | GPIO_EMC_04 | VSS | GPIO_EMC_25 | GPIO_EMC_09 | GPIO_EMC_18 | GPIO_EMC_27 |
| GPIO_EMC_11 | GPIO_EMC_01 | GPIO_EMC_00 | GPIO_EMC_24 | GPIO_EMC_36 | GPIO_EMC_26 | GPIO_EMC_20 |
| GPIO_EMC_03 | GPIO_EMC_02 | GPIO_EMC_37 | GPIO_EMC_34 | GPIO_EMC_33 | GPIO_EMC_19 | GPIO_EMC_17 |
| GPIO_EMC_05 | NVCC_EMC | GPIO_EMC_35 | GPIO_EMC_32 | GPIO_EMC_31 | VSS | GPIO_EMC_16 |
| VDD_SOC_IN | VDD_SOC_IN | NVCC_EMC | GPIO_EMC_38 | GPIO_EMC_30 | GPIO_EMC_14 | GPIO_EMC_13 |
| VSS | VDD_SOC_IN | GPIO_B0_01 | GPIO_B0_00 | GPIO_EMC_41 | GPIO_EMC_39 | GPIO_EMC_40 |
| VSS | VDD_SOC_IN | GPIO_B0_02 | GPIO_B0_03 | GPIO_B0_04 | GPIO_B0_05 | GPIO_B0_06 |
| VDD_SOC_IN | VDD_SOC_IN | NVCC_GPIO | GPIO_B0_10 | GPIO_B0_09 | GPIO_B0_08 | GPIO_B0_07 |
| GPIO_AD_B0_11 | NVCC_GPIO | GPIO_B0_14 | GPIO_B0_13 | GPIO_B0_12 | VSS | GPIO_B0_11 |
| GPIO_AD_B0_03 | GPIO_AD_B0_04 | GPIO_B0_15 | GPIO_B1_03 | GPIO_B1_02 | GPIO_B1_01 | GPIO_B1_00 |
| GPIO_AD_B1_14 | GPIO_AD_B0_07 | GPIO_B1_04 | GPIO_B1_05 | GPIO_B1_06 | GPIO_B1_07 | GPIO_B1_08 |
| GPIO_AD_B0_10 | GPIO_AD_B0_08 | VSS | GPIO_B1_12 | GPIO_B1_11 | GPIO_B1_10 | GPIO_B1_09 |
| GPIO_AD_B0_05 | GPIO_AD_B0_09 | GPIO_AD_B0_06 | GPIO_B1_13 | GPIO_B1_14 | GPIO_B1_15 | VSS |
| G | F | E | D | C | B | A |

Table 85. 10x10 mm, 0.65 mm pitch, ball map (continued)

| | P | N | M | L | K | J | H |
|----|---------------|----------------|---------------|---------------|---------------|---------------|---------------|
| 1 | VSS | DCDC_GND | DCDC_LP | DCDC_IN | GPIO_SD_B0_03 | GPIO_SD_B0_02 | GPIO_EMC_12 |
| 2 | GPIO_SD_B1_04 | DCDC_GND | DCDC_LP | DCDC_IN | VSS | GPIO_SD_B0_05 | GPIO_SD_B0_04 |
| 3 | GPIO_SD_B1_08 | GPIO_SD_B1_05 | GPIO_SD_B1_02 | GPIO_SD_B1_06 | DCDC_PSWITCH | GPIO_SD_B0_01 | GPIO_EMC_08 |
| 4 | GPIO_SD_B1_10 | GPIO_SD_B1_09 | GPIO_SD_B1_03 | GPIO_SD_B1_07 | DCDC_IN_Q | GPIO_SD_B0_00 | GPIO_EMC_07 |
| 5 | GPIO_SD_B1_11 | VSS | GPIO_SD_B1_01 | GPIO_SD_B1_00 | NVCC_SD1 | DCDC_SENSE | GPIO_EMC_06 |
| 6 | USB_OTG2_VBUS | USB_OTG1_VBUS | ONOFF | WAKEUP | TEST_MODE | NVCC_SD0 | VDD_SOC_IN |
| 7 | USB_OTG2_DP | USB_OTG2_DN | POR_B | PMIC_STBY_REQ | PMIC_ON_REQ | VSS | VSS |
| 8 | VDD_HIGH_CAP | VSS | USB_OTG1_DN | USB_OTG1_DP | VDD_USB_CAP | VSS | VSS |
| 9 | RTC_XTALO | RTC_XTALI | VDD_SNVIS_IN | VSS | NGND_KEL0 | VDD_SOC_IN | VDD_SOC_IN |
| 10 | NVCC_PLL | GPANAIO | VDD_SNVIS_CAP | GPIO_AD_B0_15 | GPIO_AD_B1_07 | NVCC_GPIO | GPIO_AD_B0_01 |
| 11 | XTALI | XTALO | GPIO_AD_B0_02 | GPIO_AD_B1_02 | GPIO_AD_B1_01 | GPIO_AD_B1_00 | GPIO_AD_B1_13 |
| 12 | VDD_HIGH_IN | USB_OTG1_CHD_B | GPIO_AD_B1_03 | GPIO_AD_B1_04 | GPIO_AD_B1_05 | GPIO_AD_B1_06 | GPIO_AD_B1_12 |
| 13 | CCM_CLK1_N | CCM_CLK1_P | GPIO_AD_B1_09 | GPIO_AD_B1_10 | VSS | GPIO_AD_B1_11 | GPIO_AD_B1_08 |
| 14 | VSS | VDDA_ADC_3P3 | GPIO_AD_B0_00 | GPIO_AD_B0_13 | GPIO_AD_B0_12 | GPIO_AD_B1_15 | GPIO_AD_B0_14 |
| | P | N | M | L | K | J | H |

8 Revision history

Table 86 provides a revision history for this data sheet.

Table 86. i.MX RT1064 Data Sheet document revision history

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|-----------------------|
| Rev. 0 | 10/2018 | • Initial version |

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