TW2968

8-Channel WD1 (960H)/D1 Compatible Video Decoders and Audio Codecs

FN8394
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Features

Video Decoder

- WD1 (960H) and D1 compatible video decoding operation and each channel is programmable
- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60) support with automatic format detection
- Built-in analog anti-alias filter
- Eight 10-bit ADCs and analog clamping circuit for CVBS input
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for CVBS channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with peaking and CTI
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, sharpness
- Automatic color control and color killer
- ITU-R 656 like YCbCr (4:2:2) output or time multiplexed output with 36/72/144MHz for WD1 or 27/54/108MHz for D1 format

Audio Codec

- Ten integrated audio ADCs processing and one audio DAC
- Provides multi-channel audio mixed analog output
- Supports I2S/DSP Master/Slave interface for record output and playback input
- PCM 8/16-bit and u-Law/A-Law 8-bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz

Miscellaneous

- Embedded PTZ Tx pulse generation
- Two-wire MPU serial bus interface
- Integrated clock PLL for 144/108MHz clock output
- Power save and Power down mode
- Low power consumption
- Single 27MHz crystal for all standards and both WD1 and D1 format
- 3.3V tolerant I/O
- 1.0V/3.3V power supply
- 128-pin LQFP package (pin compatible with TW2964 128-LQFP version)

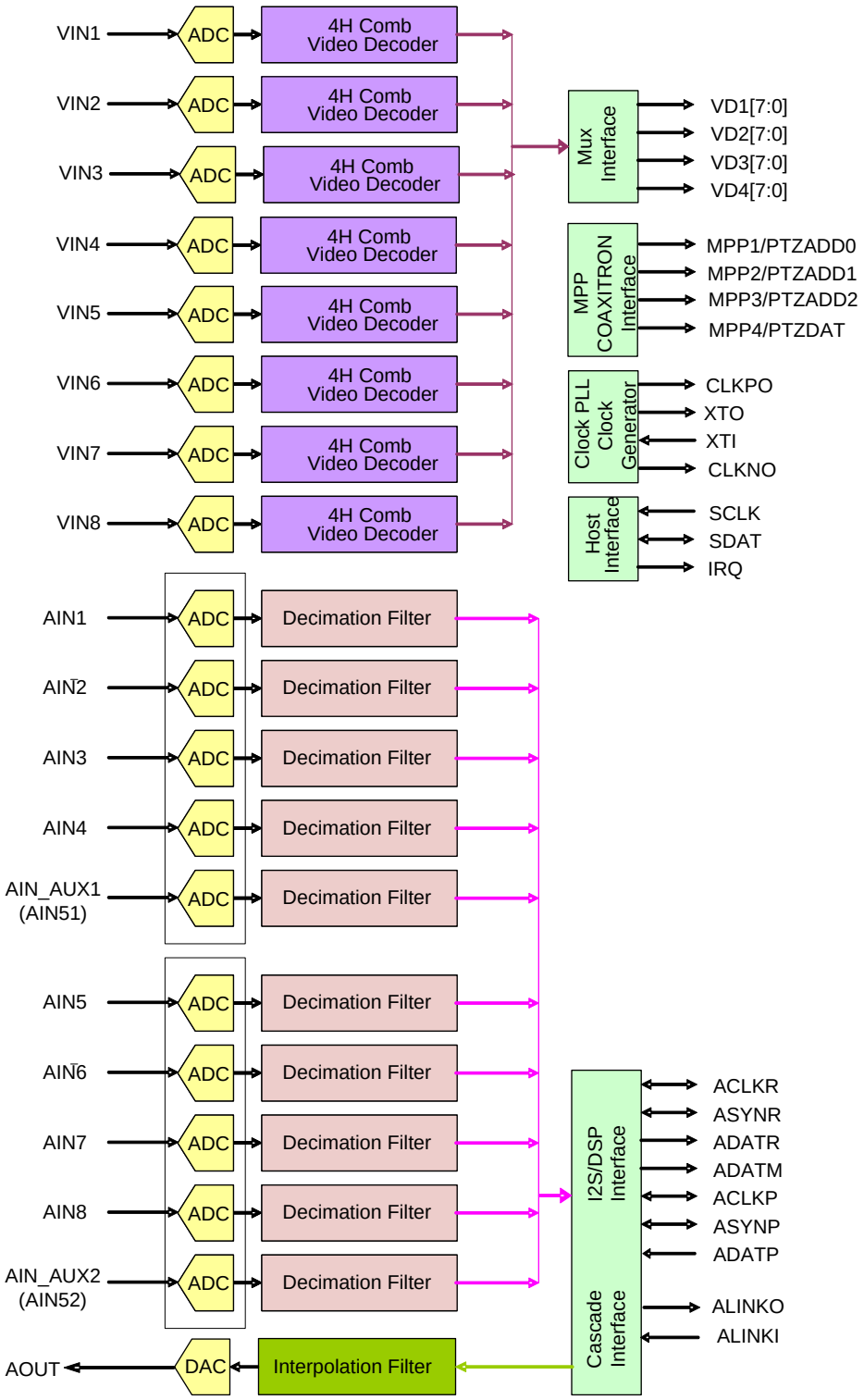

FIGURE 1. TW2968 VIDEO BLOCK DIAGRAM

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW2968-LA1-CR (Note 1)	TW2968 LA1-CR	128 Lead LQFP (14mmx14mm)	Q128.14X14
TW2968-LA1-CR-EVAL	Evaluation Board		

NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Video Decoder

VIDEO DECODER OVERVIEW

The TW2968 is a low power NTSC/PAL video decoder chip that is designed for video surveillance applications. It consumes very low power in a typical composite input application. The available power down mode further reduces the power consumption. It uses the 1.0V for digital supply voltage and 3.3V for I/O and analog power. A single 27MHz crystal is all that needed to decode all analog video standards.

The video decoder decodes the base-band analog CVBS into digital 8-bit 4:2:2 YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43) and synchronization circuitry. The Y/C separation is done with high quality adaptive 4H (5-line) comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal.

Analog Front End

The analog front-end prepares and digitizes the AC coupled analog signal for further processing. Each channel has built-in anti-aliasing filter and 10-bit over-sampling ADCs. The characteristic of the filter is available in the filter curve section. The Y channel has additional 2-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). It can support a maximum input voltage range of 1.4V without attenuation. Software selectable analog inputs allow two selectable composite video inputs.

Sync Processor

The sync processor of TW2968 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward. It allows the sampling of the video signal in line-locked fashion.

Y/C Separation

For NTSC and PAL standard signals, the luma/chroma separation can be done either by adaptive comb filtering or notch/band-pass filter combination. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

TW2968 employs high quality 4-H (5-line) adaptive comb filter to reduce artifacts like hanging dots and crawling dots. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color Demodulation

The color demodulation of NTSC and PAL signal is done by first quadrature down mixing and then low-pass filtering. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

AUTOMATIC CHROMA GAIN CONTROL

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC control is –6db to +26db.

COLOR KILLER

For low color amplitude signals, black and white video or very noisy signals, the color will be suppressed or killed. The color killer uses the burst amplitude measurement as well as sub-carrier PLL status to switch-off the color.

AUTOMATIC STANDARD DETECTION

The TW2968 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC or PAL color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM. Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection. The SECAM standard can be recognized but not properly decoded.

TW2968 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW2968

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (Note 1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding
NTSC 50	625	50	3.579545 MHz	

NOTE:

1. NTSC-Japan has 0 IRE setup.

Component Processing

The TW2968 supports the brightness, contrast, color saturation and Hue adjustment for changing the video characteristic. The Cb and Cr gain can be adjusted independently for flexibility.

SHARPNESS

The TW2968 also provides a sharpness control function through control registers. It provides the control up to +9db. The center frequency of the enhancement curve is selectable. A coring function is provided to prevent noise enhancement.

COLOR TRANSIENT IMPROVEMENT

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

Video Output Format

The TW2968 supports ITU-R BT.656 like format. All video data and timing signal of four channels are synchronous with the pins CLKPO or CLKNO output. Therefore, CLKPO or CLKNO can be connected to four channel interfaces for synchronizing data.

TOTAL PIXEL PER HORIZONTAL LINE

The number of total pixel per horizontal line depends on Horizontal line frequency of video input signal incoming in VINn pin. As standard, if 27MHz/54MHz/108MHz output mode(036Mn=0),60Hz video has 858x2 27MHz clocks,50Hz video has 864x2 27MHz clocks.If 36MHz/72MHz/144MHz output mode(036Mn=1),60Hz video has 1144x2 36MHz clocks,50Hz video has 1152x2 36MHz clocks.

CHANNEL ID

The channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Each ITU-R BT.656 like data stream in 4x output data, 2x output data can have this Sync Code and Blanking Code. Table 2 shows this Channel ID format. Nibble data value m shows Video Decoder number to be output in this video stream.

TABLE 2. THE CHANNEL ID FORMAT FOR 4X960H, 2X960H TIME-MULTIPLEXED FORMAT

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE			
Field	Vtime	Htime	F	V	H	First	Second	Third	Fourth
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xFm
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEm
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDm
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xCm
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xBm
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAm
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9m
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x8m

(a) ITU-R BT.656 Sync Code with Channel ID

VIDEO	H BLANKING CODE WITH CHANNEL ID		
	Y	CB	CR
VINn	8'h1m	8'h8m	8'h8m

(b) Horizontal Blanking Code with Channel ID

As default, m = 0 VIN1 656 data, m = 1 VIN2 656 data, m = 2 VIN3 656 data, m = 3 VIN4 656 data,m=4 VIN5 656 data,m=5 VIN6 656 data,m=6 VIN7 656 data,m=7 VIN8 656 data.CH1NUM, CH2NUM, CH3NUM, CH4NUM ,CH5NUM,CH6NUM,CH7NUM and CH8NUM registers can change this m value in each video channel output data if necessary.

VIDEO LOSS OUTPUT

When NOVID_656 register is set to 1, bit7 of Fourth byte of SAV/EAV code will be 0 when video signal is lost. This can be an optional set of 656 SAV/EAV code for no-video (video lost) specific application.

ITU-R BT.656 LIKE FORMAT

In ITU-R BT.656 like format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 2. The SAV and EAV sequences are shown in Table 3. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

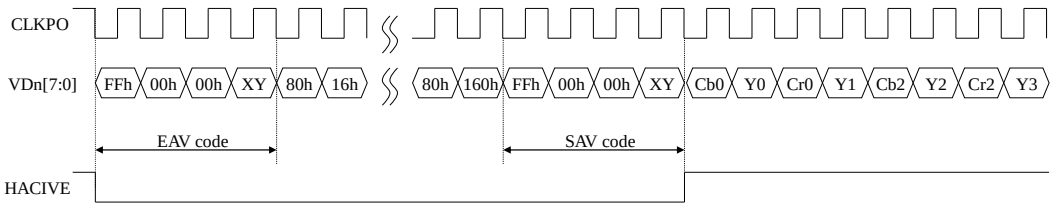


FIGURE 2. TIMING DIAGRAM OF ITU-R BT.656 LIKE FORMAT

TABLE 3. ITU-R BT.656 LIKE SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
									FOURTH	
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	NORMAL	OPTION (NOTE NOTE:1)
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE:

1. Option includes video loss information in ITU-R BT.656 like format.

TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED FORMAT WITH 54/72MHZ

The TW2968 supports two channels ITU-R BT.656 time-multiplexed format with 54MHz/72MHz that is useful to security application requiring two channel outputs through one channel video port. When VDnMD register is set to 1,the dual ITU-R BT.656 time-multiplexed format is enable on VDn[7:0] output pins.VDnO1SEL/VDnO2SEL register select CH1/CH2 data to be output on VDn pin from 8 Video Decoder BT.656 data. Fig9 and Fig10 illustrate VDn[7:0]/CLKPO/CLKNO pin timing with 54MHz/27MHz,72MHz/36MHz clock output mode.

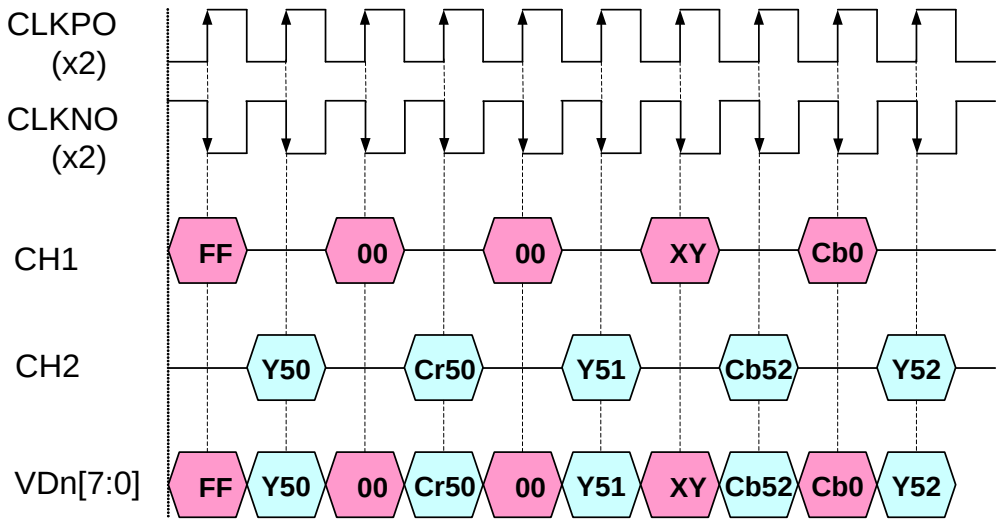


FIGURE 3. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH X2 CLOCK

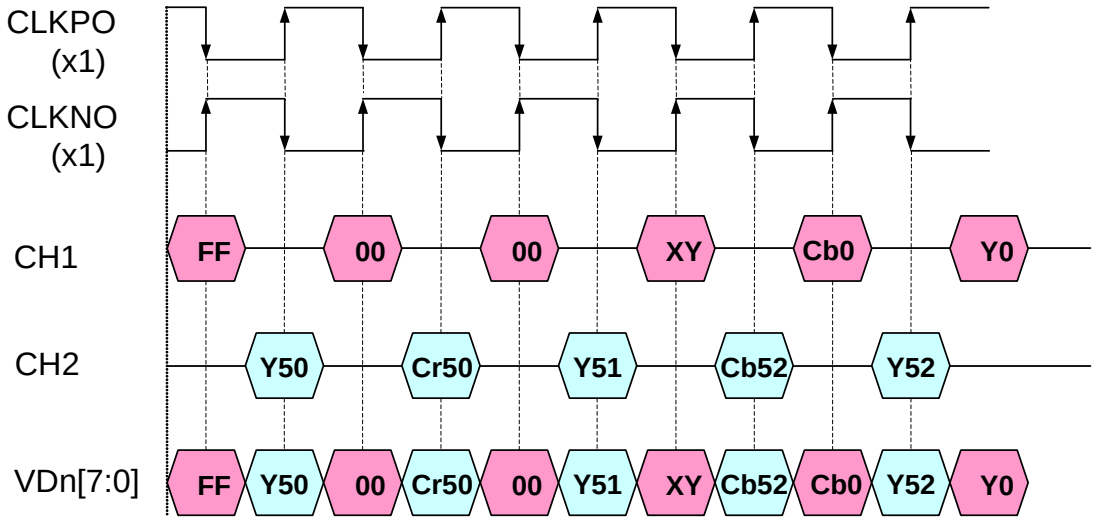


FIGURE 4. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH X1 CLOCK.

FOUR CHANNEL 960H TIME-DIVISION-MULTIPLEXED FORMAT WITH 108/144MHZ

Four channel of 960H/720H at 36MHz/27MHz video stream that are time-division-multiplexed at x4(144MHz/108MHz) data rate format is implemented in TW2968 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, TW2968 implements single 8-bit bus at 4 times the base band pixel clock rate of x1(36MHz/27MHz). While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band x1(36MHz/27MHz) ITU-R BT.656 like specification. For interface that can accept the new x4(144MHz/108MHz) clock bus, only one single clock at x4(144MHz/108MHz) is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

Figure 5 depicts the temporal arrangement of the video data in x4(144MHz/108MHz) data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is x4(144MHz/108MHz) clock

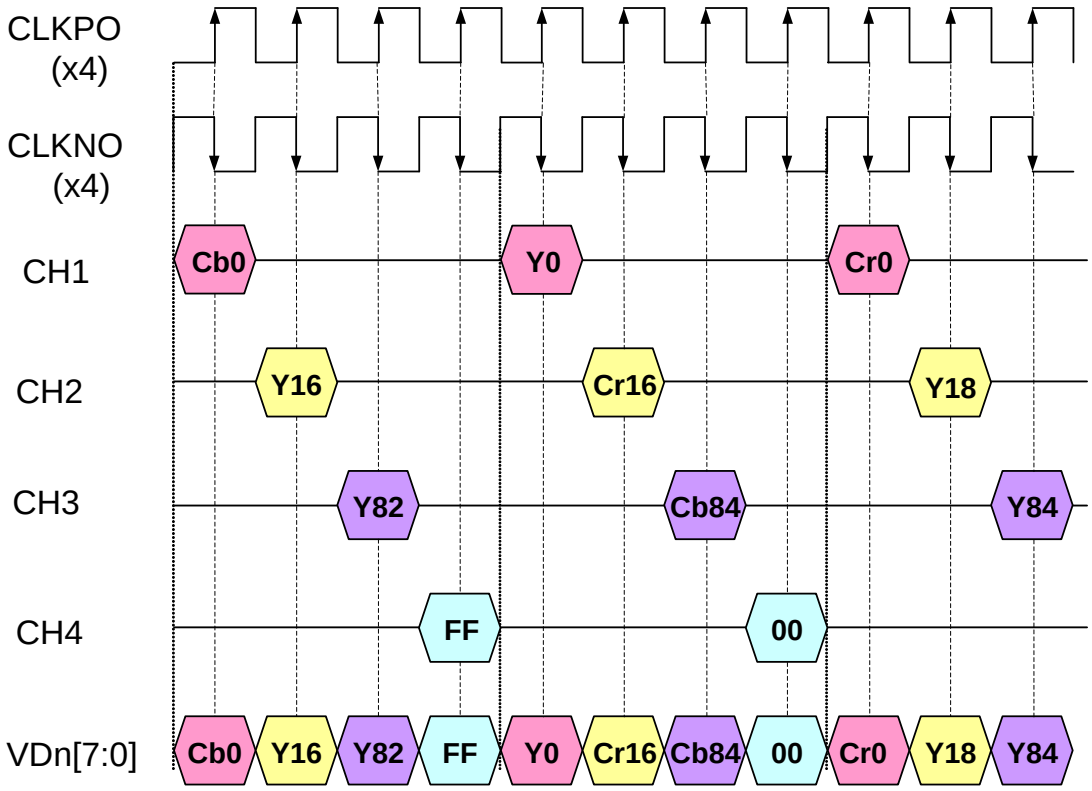


FIGURE 5. PIN OUTPUT TIMING OF 4 CH TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH X4 CLOCK

TABLE 4. SHOWS THE SPECIAL FORMAT OF ITU-R BT. 656 LIKE EMBEDDED TIMING CODE AND CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									Fourth			
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xFp	0xFq	0xFr	0xFs
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xEp	0xEq	0xEr	0xEs
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xDp	0xDq	0xDr	0xDs
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xCp	0xCq	0xCr	0xCs
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xBp	0xBq	0xBr	0xBs
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xAp	0xAq	0xAr	0xAs
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x9p	0x9q	0x9r	0x9s
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x8p	0x8q	0x8r	0x8s

Note : The nibble value of p,q,r and s are setup by combinations of CH1NUM,CH2NUM,CH3NUM,CH4NUM,CH5NUM,CH6NUM,CH7NUM,CH8NUM,VD101SEL,VD102SEL,VD103SEL,VD104SEL,VD201SEL,VD202SEL,VD203SEL,VD204SEL,VD301SEL,VD302SEL,VD303SEL,VD304SEL,VD401SEL,VD402SEL,VD403SEL,VD404SEL registers.

OUTPUT ENABLING ACT

After power-up, the TW2968 registers have the default values. After RSTB pin is asserted and released, all registers have the default values. After reset, the TW2968 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

VIDEO OUTPUT CHANNEL SELECTION

If VDnMD]register is set to 0hex,VDnO1SEL register selects one number of VIN1-8 to be output on VDn[7:0] pin as Single Channel ITU-R BT.656 like Format output. If VDnMD register is set to 1hex, VDnO1SEL register and VDnO2SEL register select two numbers of VIN1-8 to be output on VDn[7:0] pin as Two Channel ITU-R BT.656 like Time-multiplexed Format output. If VDnMD register is set to 2hex, Four Channel ITU-R BT.656 like x4 Time-multiplexed Format is output on VDn[7:0] pin and output CH1/CH2/CH3/CH4 data for each VDn[7:0] pin are selected by VDnO1SEL,VDnO2SEL,VDnO3SEL,VDnO4SEL registers.

EXTRA SYNC OUTPUT

The additional timing information such as sync and field flag are also supported up to VIN1,VIN2,VIN3,VIN4 through the MPP pins. The video output timing is illustrated in Figure 6 and Figure 7. TW2968 HS/VS/FLD output function is compatible to TW9907 Video decoder HSYNC/VSYNC/FIELD output function. Start of VS timing is controlled by VSHT register(V timing) and OVSDLY register(H timing).End of VS timing is controlled by OVSEND register(V Timing). Start of FLD timing is controlled by OFDLY register(V timing). Start of HS timing is controlled by HSBEGIN register and End of HS timing is controlled by HSEND register.

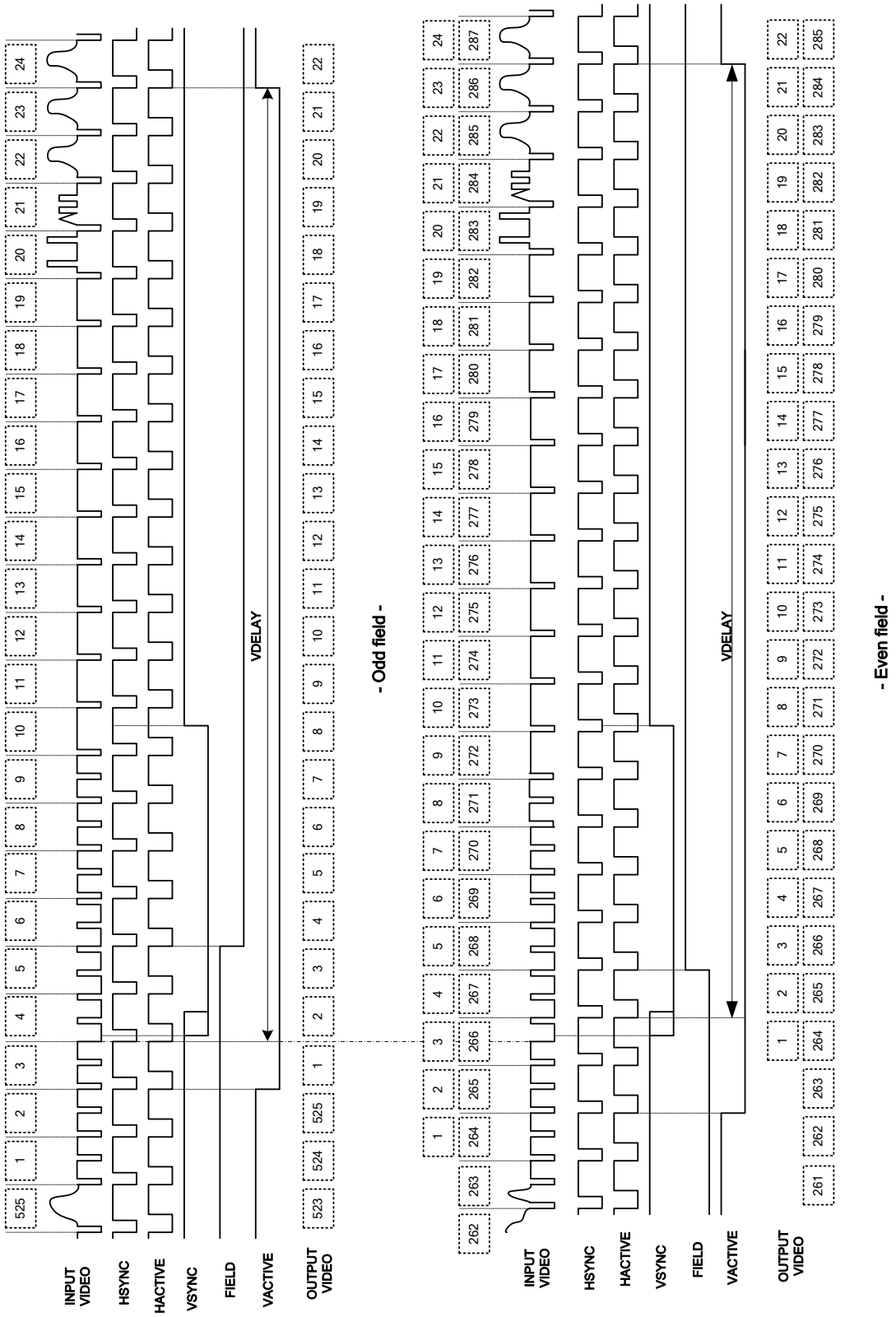


FIGURE 6. VERTICAL TIMING DIAGRAM FOR 60HZ/525 LINE SYSTEM

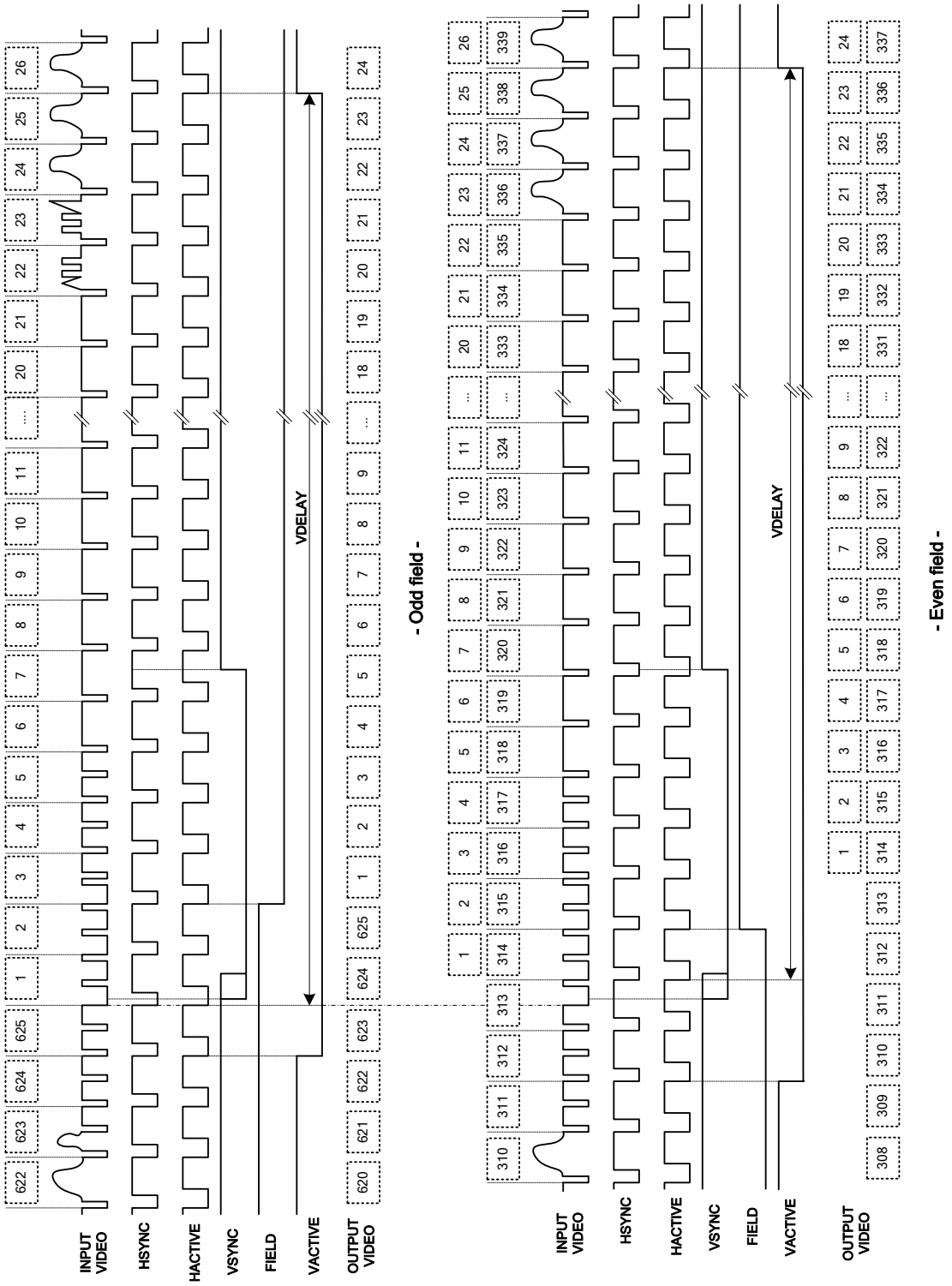


FIGURE 7. VERTICAL TIMING DIAGRAM FOR 50HZ/625 LINE SYSTEM

Audio Codec

Function of AIN_AUX1 and AIN_AUX2 are same as AIN1/2/3/4/5/6/7/8.In this document,
AIN51 naming is used for AIN_AUX1 ,and AIN52 naming is used for AIN_AUX2.
AIN51=AIN_AUX1,AIN52=AIN_AUX2.

The audio codec in the TW2968 is composed of ten audio Analog-to-Digital converter processes, one Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as Figure 8. The TW2968 can accept 10 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

The level of analog audio input signal AIN1/2/3/4/51/5/6/7/8/52 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1/2/3/4/51/5/6/7/8/52 registers and then sampled by each Analog-to-Digital converters. The digital serial audio input data through the ACLKP, ASYNP and ADATP pin are used for playback function. To record audio data, the TW2968 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pin.

The TW2968 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1/2/3/4/51/5/6/7/8/52/P registers.
This mixing audio output can be provided through the analog and digital interfaces. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The embedded audio Digital-to-Analog converter supports the analog audio output.

The main purpose of AIN51/52 is to make the standard I2S/DSP digital audio output for AIN51/AIN52 data on ADATM pin for special application.Usually,8 AIN1/AIN2/AIN3/AIN4/AIN5/AIN6/AIN7/AIN8 audio data are used on ADATR pin output.

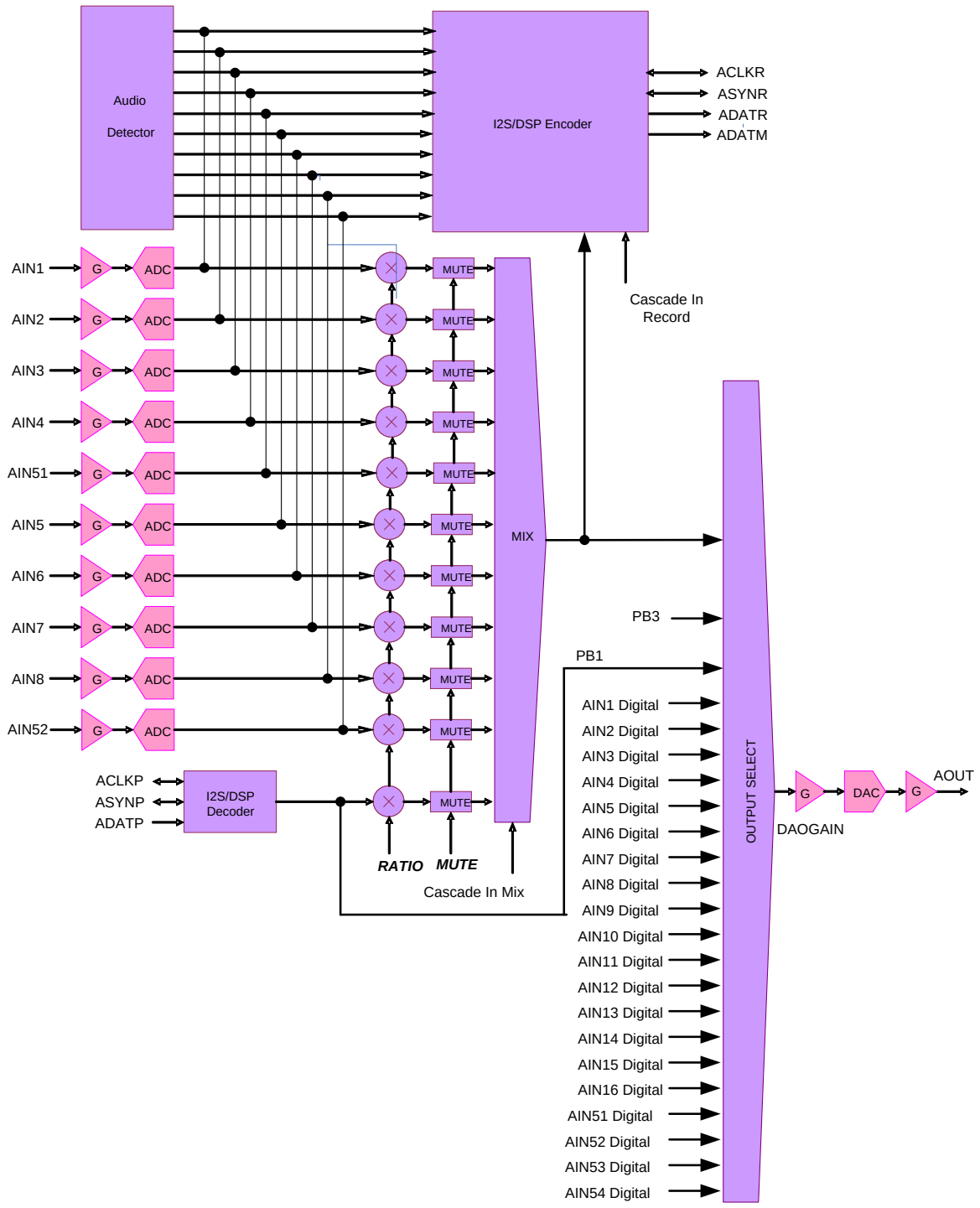


FIGURE 8. BLOCK DIAGRAM OF AUDIO CODEC

AUDIO CLOCK MASTER/SLAVE MODE

The TW2968 has two types of Audio Clock modes. If ACLKRMASTER register is set to 1, fs audio sample date is processed from audio clock internal ACKG (Audio Clock Generator) generates. In this master mode, ACLKR/ASYNR pins are output mode. ASYNROEN register for ASYNR pin should be set to 0 (output enable mode). If ACLKRMASTER register is set to 0, fs audio sample rate is processed from audio clock on ACLKR pin input. 256xfs, 320xfs or 384xfs audio clock should be connected to ACLKR pin from external master clock source in this slave mode. ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode. AIN5MD and AFS384 register set up Audio fs mode by following table.

REGISTER		FS MODE
AIN5MD	AFS384	
0	0	256xfs
1	0	320xfs
0	1	384xfs

AUDIO DETECTION

The TW2968 has an audio detector for individual 10 channels. Those are detection of differential amplitude from audio data The accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1/2/3/4/51/5/6/7/8/52 registers. The status for audio detection are read by the AVDET1_STATE/AVDET2_STATE/
A51DET_STATE/A52DET_STATE register and those also make the interrupt request through the IRQ pin with the combination of the status for video loss detection.

MULTI-CHIP OPERATION

TW2968 can output 16 channel audio data on ACLKR/ASYNR/ADATR output simultaneously. Therefore, up to 2 chips should be connected on most Multi-Chip application cases. SMD register selects Audio cascade serial interface mode. If SMD register is set to 2, ALINKI pin is audio cascade serial input and ALINKO pin is audio cascade serial output mode.

Each stage chip can accept 10 analog audio signals so that two cascaded chips will be 16-channel audio controller as default {AFS384, AIN5MD} = 00. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW2968 can generate 16 channel data simultaneously using multi-channel method. In addition, each stage chip can support 8 channel record outputs that are corresponding with analog audio inputs. This first stage chip can also output 16 channel mixing audio data by the digital serial audio data and analog audio signal. The first stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog converter in the first stage chip.

Several Master/Slave mode configurations are available. Figure 10 is the most recommended and demanded system with Clock Master mode (ACLKRMASTER = 1). Figure 11 is the most recommended system with Clock Slave Sync Slave mode (ACLKRMASTER=0, ASYNROEN=1) . Other system combinations are also available if application need different type specific system. Figure 10 and Figure 11 show the most typical system.

In the following FIGUREs, Mix1-16-51-54/Pb1 means Mix output of AIN1-16, AIN51-54 and Playback1. AIN1-16-51-54/Pb1 means one selected Audio output in AIN1-16-51-54/Pb1.

If one of TW2968s uses {AFS384, AIN5MD} = 01 or {AFS384, AIN5MD} = 10, all other cascaded TW2968 chips must set up same {AFS384 AIN5MD} mode together.

In Multi-Chip Audio operation mode, one same Oscillator clock source need to be connected to all TW2968 XTI pins.

If special application needs 108MHz XTI input, the RSTB pin input control needs to be considered. RSTB input controlled by MPP4 or MPP3 GPO output is one of the solutions. Another way needs XTI/RSTB timing control, as shown in Figure 9.RSTB/XTI timing control is not required in 27MHz XTI mode.

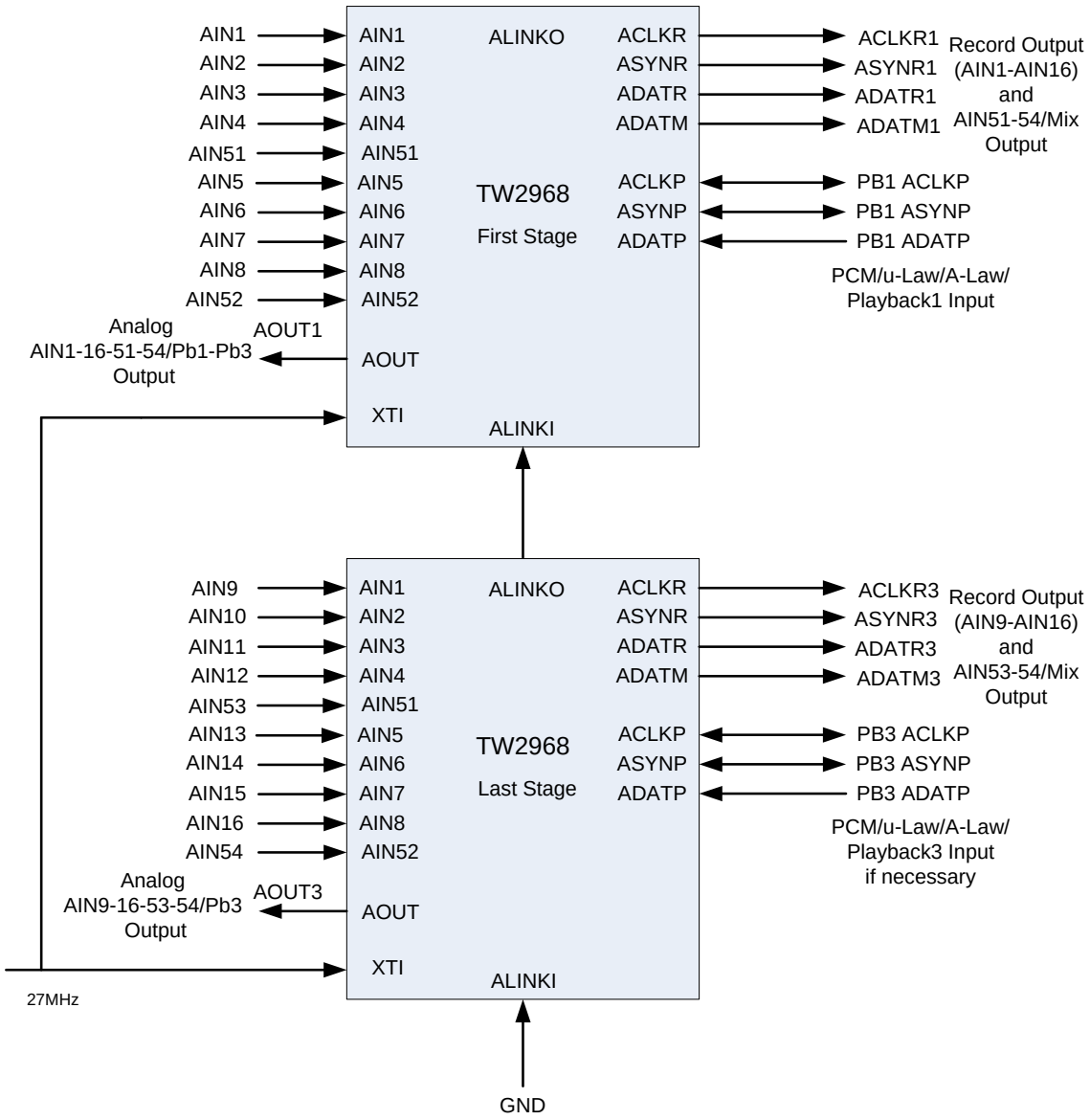


FIGURE 10. RECOMMENDED CLOCK MASTER CASCADE MODE SYSTEM

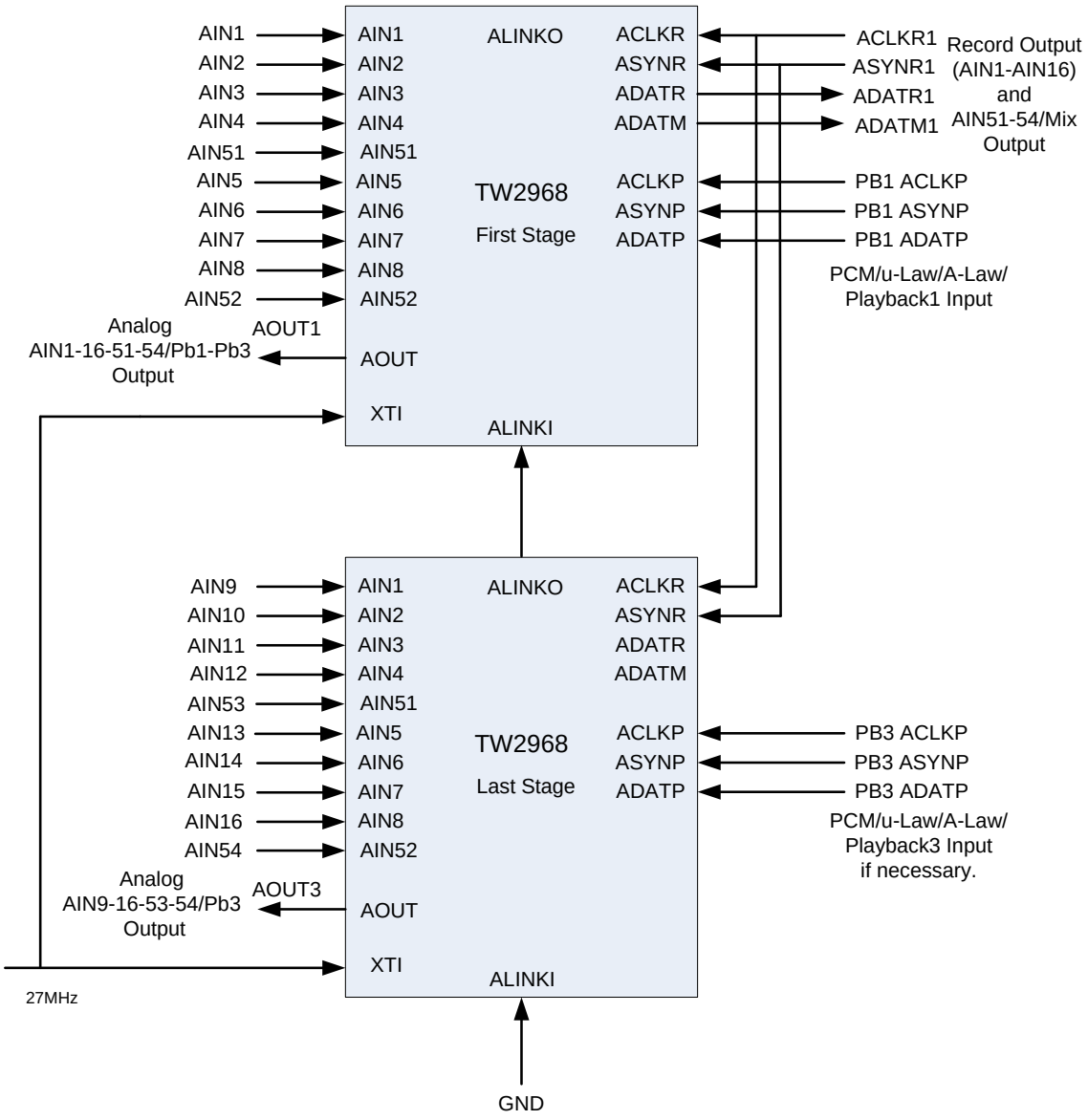


FIGURE 11. RECOMMENDED CLOCK SLAVE SYNC SLAVE CASCADE MODE SYSTEM

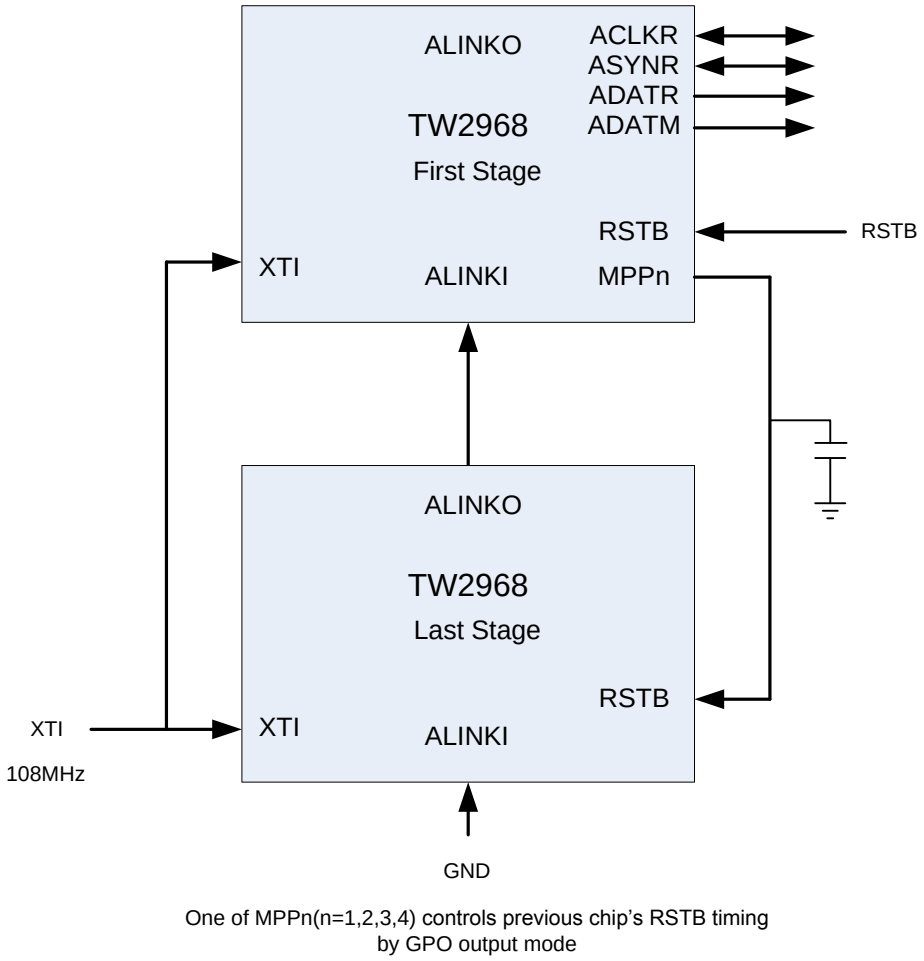


FIGURE 12. RSTB CONTROL BY MPP4GPO OUTPUT FOR 108MHZ XTI INPUT

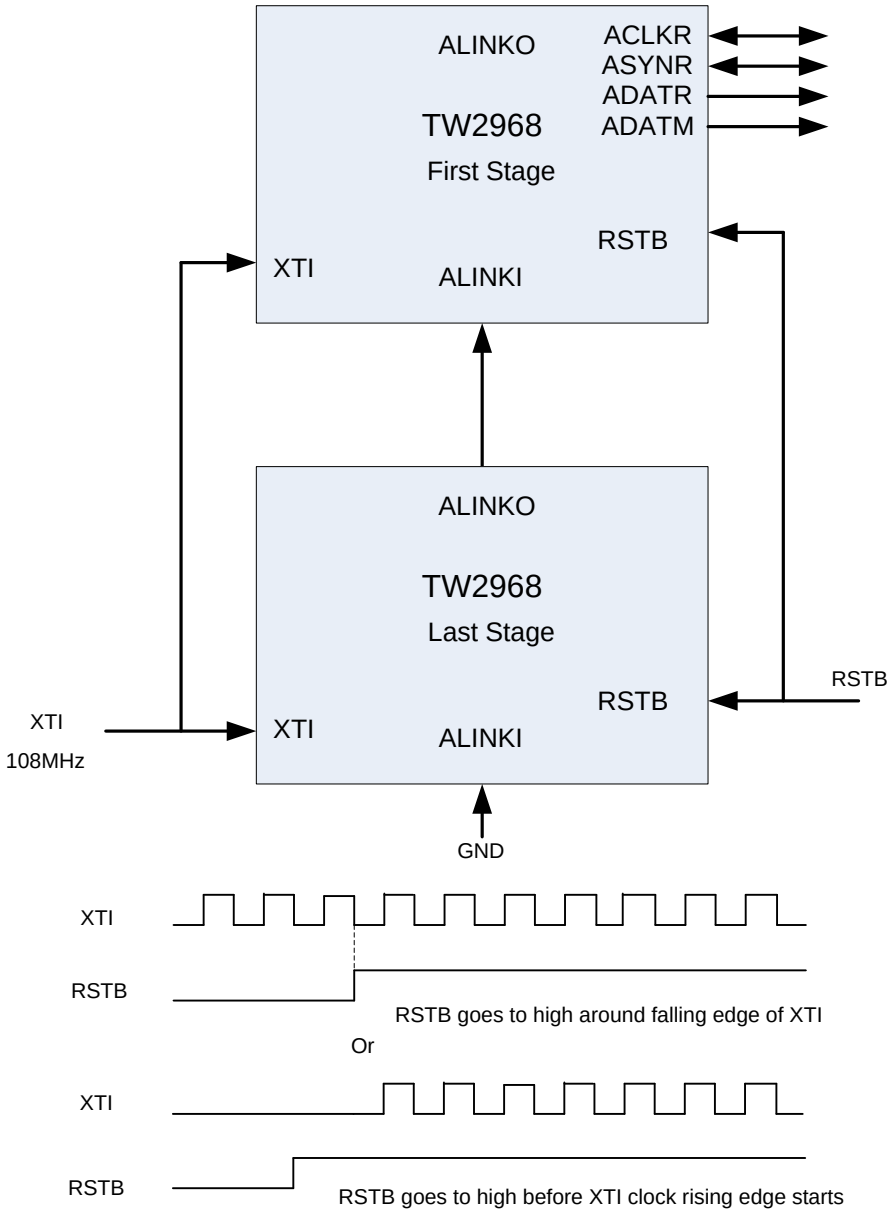
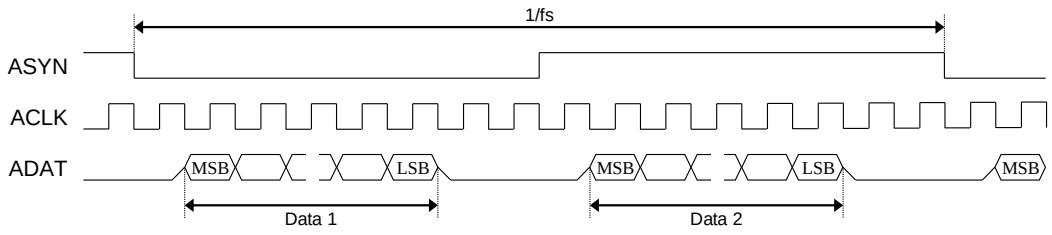


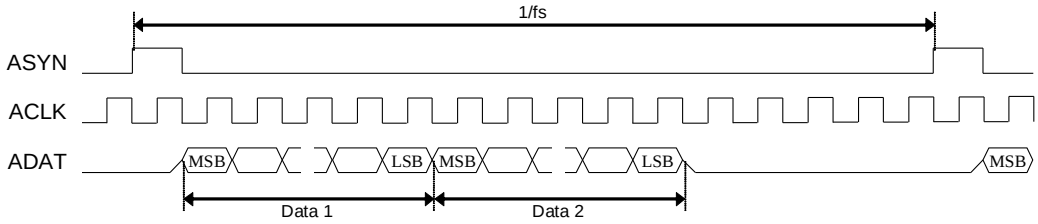
FIGURE 13. RSTB CONTROL FOR 108MHZ XTI INPUT

SERIAL AUDIO INTERFACE

There are 3 kinds of digital serial audio interfaces in the TW2968; the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in Figure 143.



(a) I2S Format



(b) DSP Format

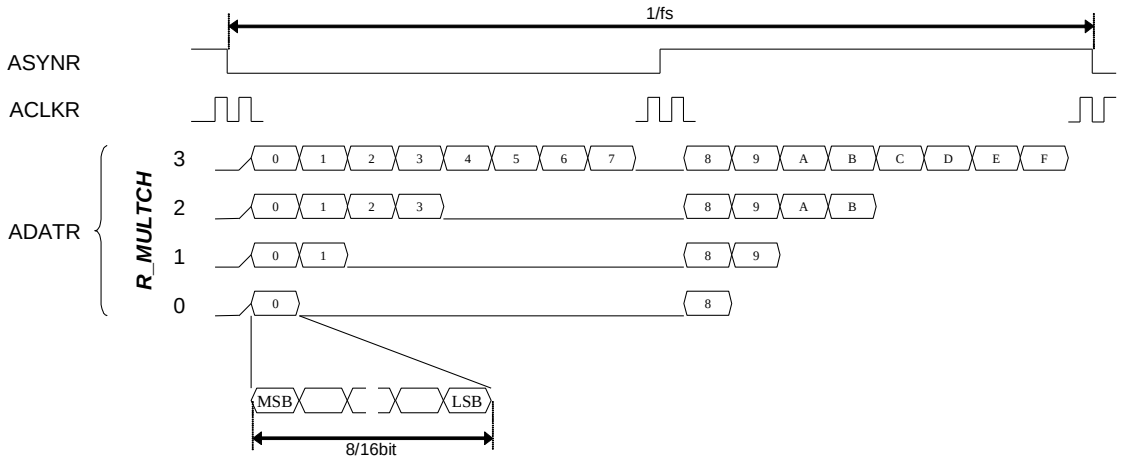
FIGURE 14. TIMING CHART OF SERIAL AUDIO INTERFACE

Playback Input

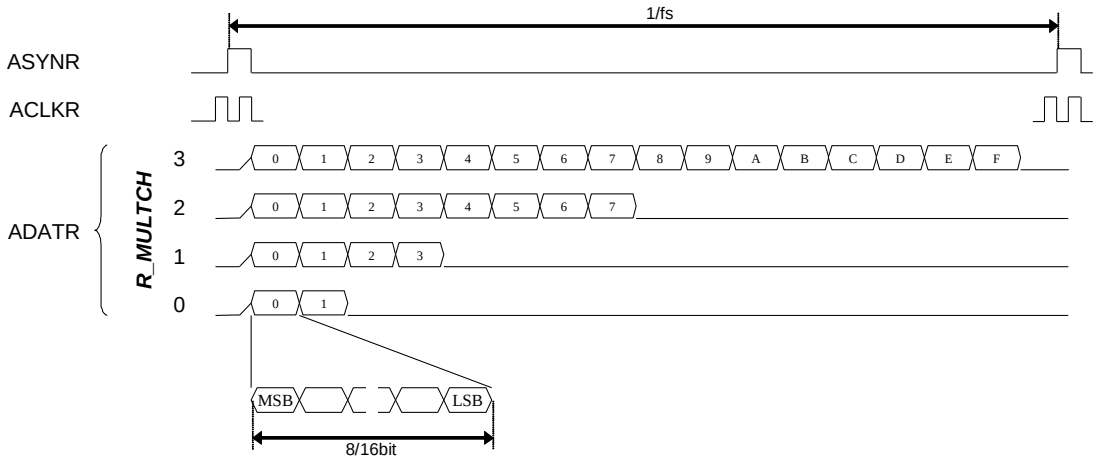
The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW2968 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from 256xfs, 320xfs or 384xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW2968 can provide an extended I2S and DSP format which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256xACLKR clock length with AIN5MD=0. Figure 15 shows the digital serial audio data organization for multi-channel audio.



(a) I2S Format



(b) DSP Format

FIGURE 15. TIMING CHART OF MULTI-CHANNEL AUDIO RECORD

Table 5 shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is also shown in Table 5.

TABLE 5. SEQUENCE OF MULTI-CHANNEL AUDIO RECORD

(a) I2S Format

R_MULTCH	PIN	LEFT CHANNEL								RIGHT CHANNEL							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(b) DSP Format

R_MULTCH	PIN	LEFT/RIGHT CHANNEL															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data, which are mixing audio, and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

AUDIO CLOCK SLAVE MODE DATA OUTPUT TIMING

TW2968 always output ASYNR/ADATR/ADATM by ACLKR falling edge triggered timing. ADATR/ADATM output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR/ADATM output are always fixed to one ACLKR falling edge timing. However, if ASYNR is input, ADATR/ADATM output timing changes by ASYNR input timing.

ASYNR is ACLKR falling edge triggered input/output

If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge, or if ASYNR is output, TW2968 output ADATR/ADATM by ACLKR falling edge triggered timing as shown in the following FIGUREs. ASYNR signal is changing during ACLKR = 0. TW2968 output ADATR/ADATM data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

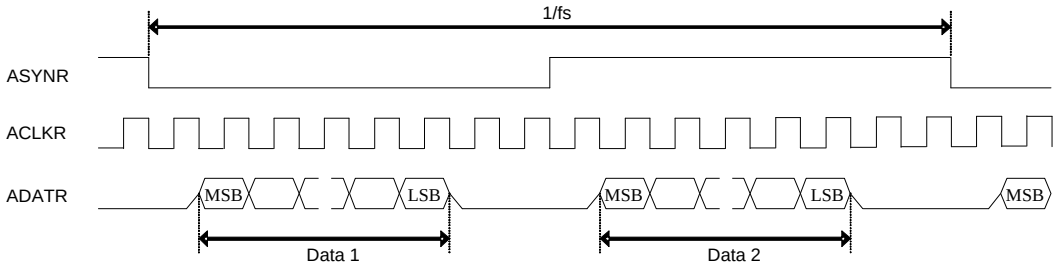


FIGURE 16. ACLKMASTER=0, RM_SYNC=0

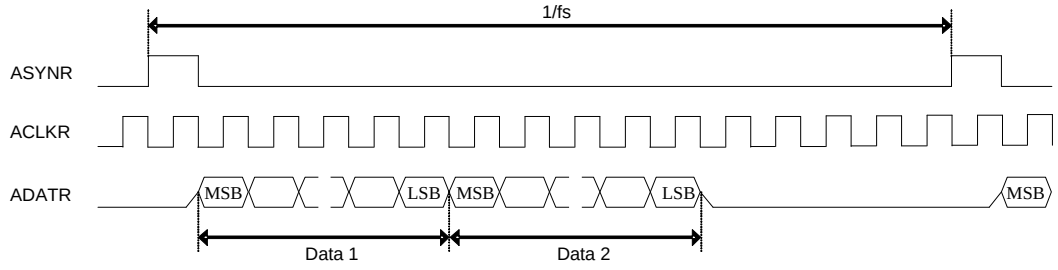


FIGURE 17. ACLKMASTER=0, RM_SYNC=1

ASYNR is ACLKR rising edge triggered input

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge, TW2968 output ADATR/ADATM by ACLKR falling edge triggered timing as shown in the following FIGUREs. ASYNR signal is changing during ACLKR = 1. TW2968 output ADATR/ADATM data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

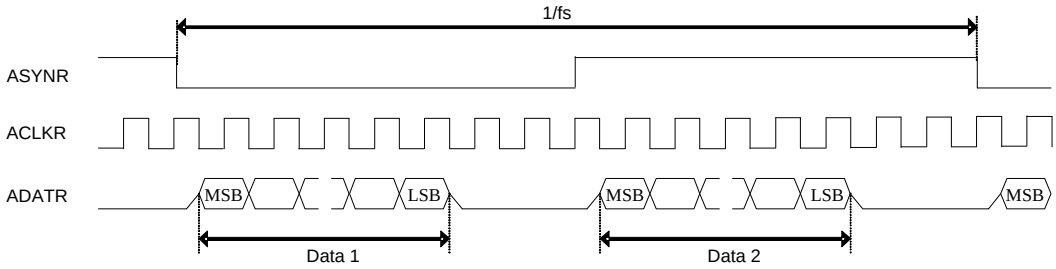


FIGURE 18. ACLKMASTER=0, RM_SYNC=0, ASYNROEN=1

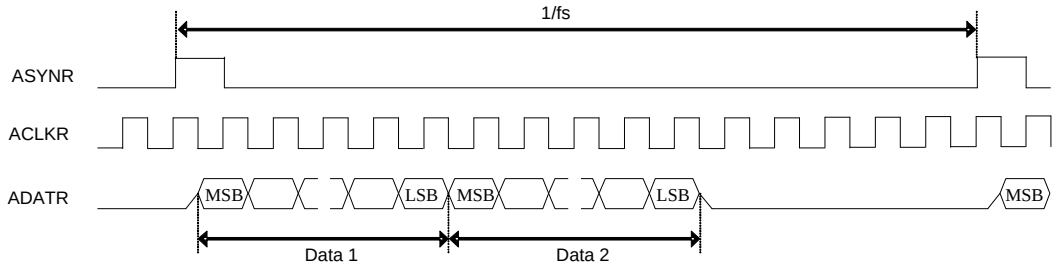


FIGURE 19. ACLKMASTER=0, RM_SYNC=1, ASYNROEN=1

ACLKP/ASYNP SLAVE MODE DATA INPUT TIMING

The following 8 data input timings are supported. ADATPDLY register needs to be set up according to the difference of ADATP data input timings. Data1 is only used as default. The MSB bit is the first input bit as default PBINSWAP = 0.If PBINSWAP = 1, LSB bit is the first input bit.

ASYNP is ACLKP falling edge triggered input.

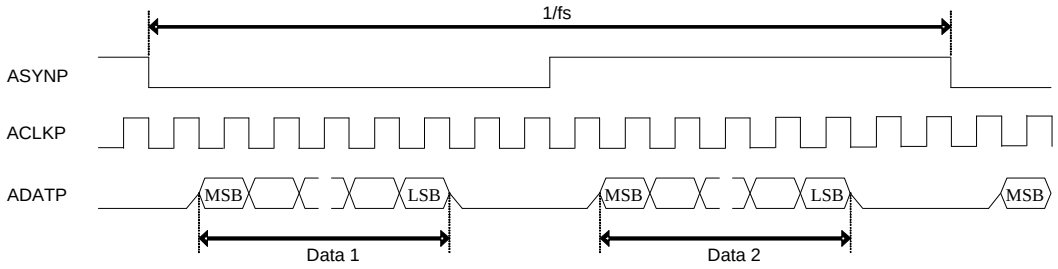


FIGURE 20. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

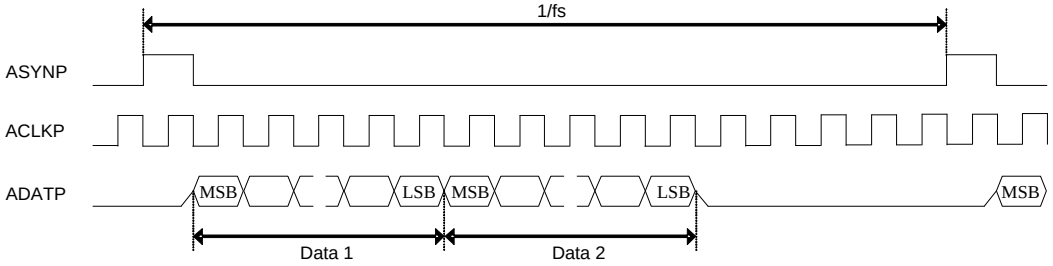


FIGURE 21. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

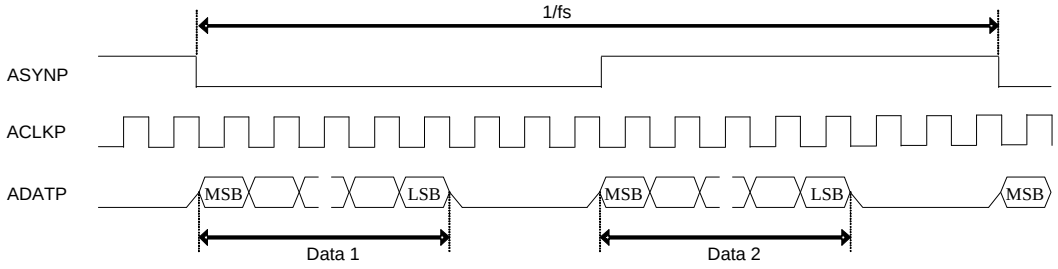


FIGURE 22. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

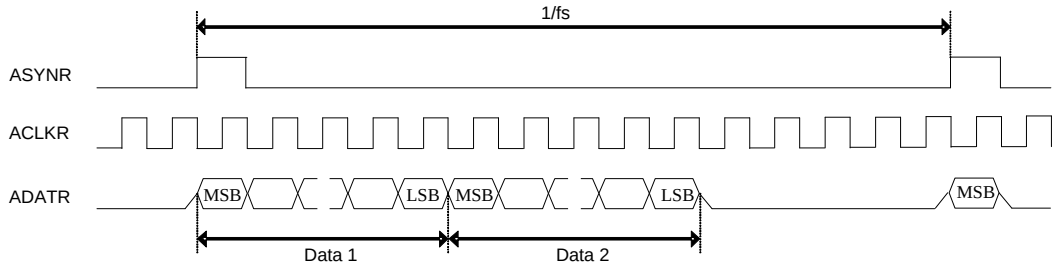


FIGURE 23. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

ASYNP is ACLKP rising edge triggered input.

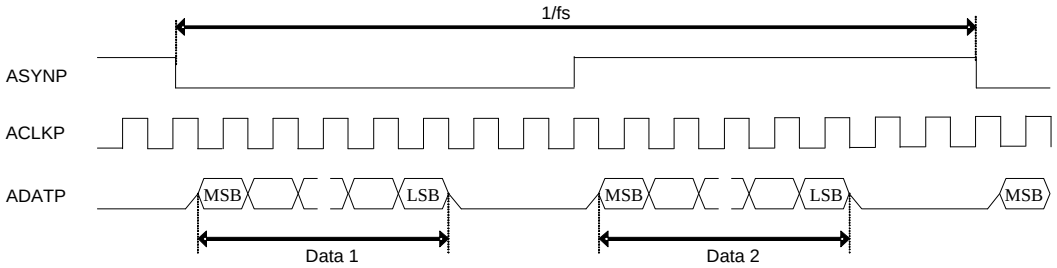


FIGURE 24. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

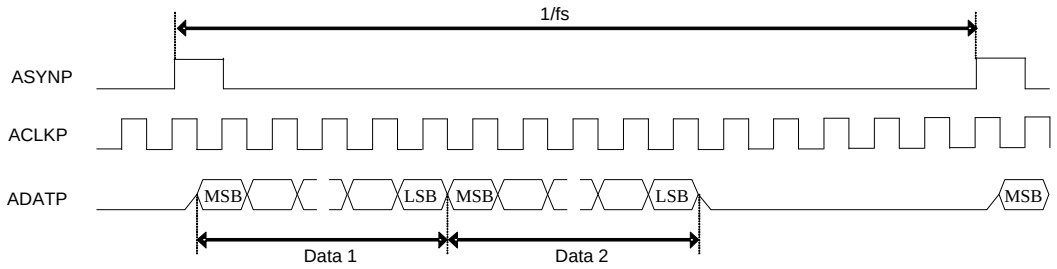


FIGURE 25. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

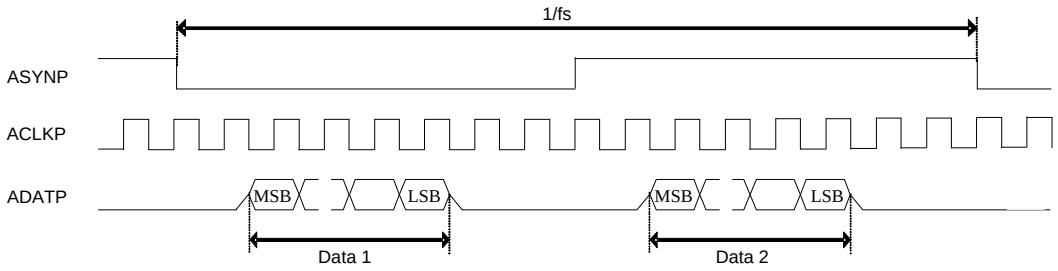


FIGURE 26. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

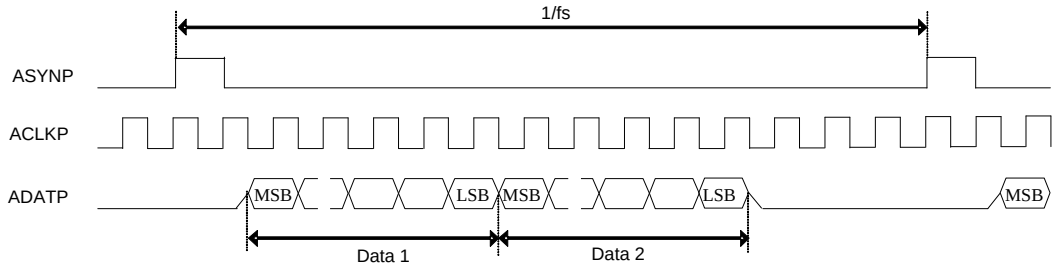


FIGURE 276. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

AUDIO CLOCK GENERATION

TW2968 has built-in audio clock generator. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKI register based following two equations.

ACKI = round (F AMCLK / F 27MHz * 2^23), it gives the Audio master Clock Nominal increment.

ACKI registers make audio_source _clock by 27MHz clock.
If MASCKMD=0, AMCLK=audio_source_clock.If MASCKMD=1, AMCLK=audio_source_clock/2.
AMCLK is used as audio system clock and audio ADC clock in Master clock mode.If 44.1kHz or 48kHz Fs mode is used,MASCKMD must be set up to 0.

The following table provides setting example of some common used audio frequency assuming XTI clock frequency of 27MHz.If ACLKRMASTER register bit is set to 1, following AMCLK is used as audio system clock with MASCKMD inside TW2968.

ACPL=1(Loop open) should be used in TW2968 system.

256xfs mode: AFS384 = 0, AIN5MD = 0,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
256 X 16 KHZ		
4.096	2545166	26-D6-0E
256 x 8 KHz		
2.048	1272583	13-6B-07

320xfs mode: AFS384 = 0, AIN5MD = 1,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
320 x 16 KHz		
5.12	3181457	30-8B-91
320 x 8 KHz		
2.56	1590729	18-45-C9

384xfs mode: AFS384 = 1, AIN5MD=0,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
384 x 16 KHz		
6.144	3817749	3A-41-15
384 x 8 KHz		
3.072	1908874	1D-20-8A

256xfs mode: AFS384=0,AIN5MD=0,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
256 x 48 KHz		
12.288	3817749	3A-41-15
256 x 44.1KHz		
11.2896	3507556	35-85-65
256 x 32 KHz		
8.192	2545166	26-D6-0E
256 x 16 KHz		
4.096	1272583	13-6B-07
256 x 8 KHz		
2.048	636291	9-B5-83

320xfs mode: AFS384=0,AIN5MD=1,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
320 x 32 KHz		
10.24	3181457	30-8B-91
320 x 16 KHz		
5.12	1590729	18-45-C9
320 x 8 KHz		
2.56	795364	C-22-E4

384xfs mode: AFS384=1,AIN5MD=0,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
384 x 32 KHz		
12.288	3817749	3A-41-15
384 x 16 KHz		
6.144	1908874	1D-20-8A
384 x 8 KHz		
3.072	954437	E-90-45

AUDIO CLOCK AUTO SETUP

If ACLKRMASTER = 1 audio clock master mode is selected, and AFAUTO register is set to “1”,TW2968 set up ACKI register by AFMD register value automatically.ACKI control input in ACKG module block is automatically set up to the required value by the condition of AFS384 and AFS384 register value.

AFAUTO	AFMD	ACKG MODULE ACKI CONTROL INPUT VALUE
1	0	8kHz mode value by each AFS384/AIN5MD case.
1	1	16kHz mode value by each AFS384/AIN5MD case.
1	2	32kHz mode value by each AFS384/AIN5MD case.
1	3	44.1kHz mode value by eachAFS384/AIN5MD case.
1	4	48kHz mode value by each AFS384/AIN5MD case.
0	X	ACKI register set up ACKI control input value.

Two-wire Serial Bus Interface

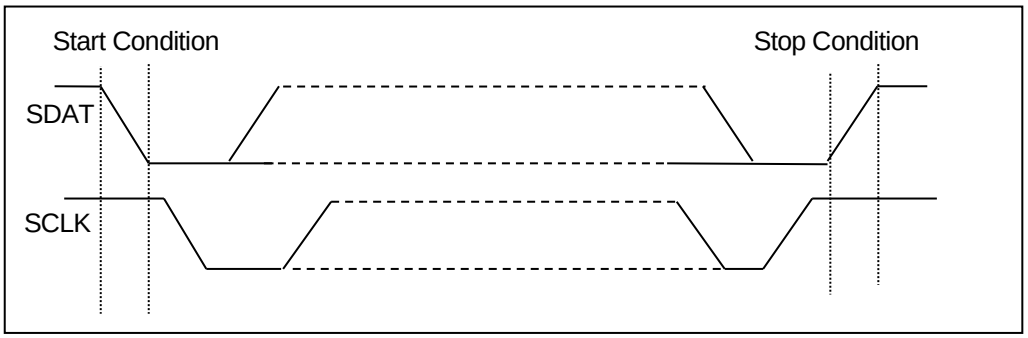


FIGURE 28. DEFINITION OF THE SERIAL BUS INTERFACE BUS START AND STOP

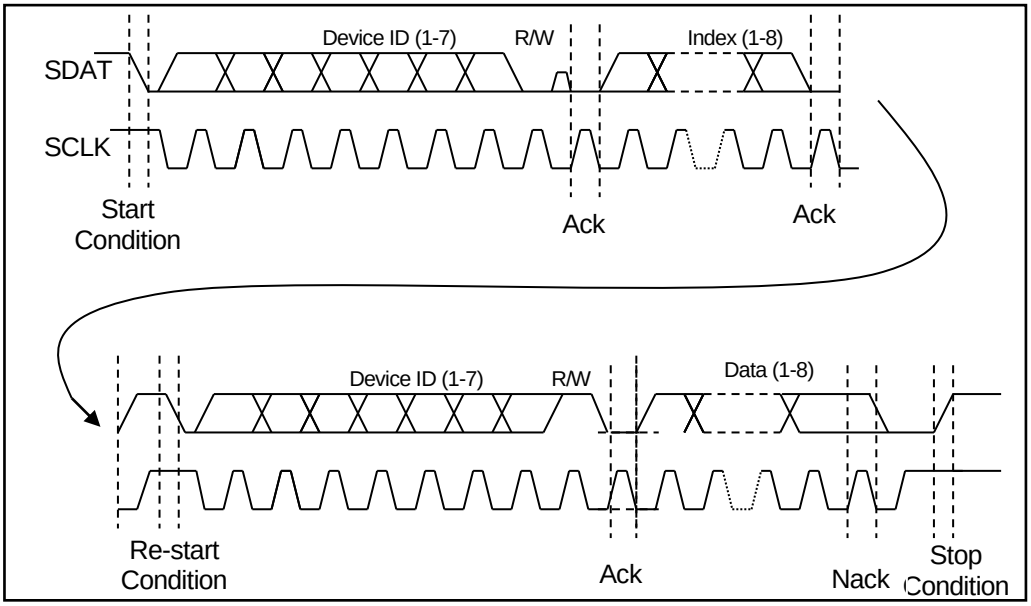


FIGURE 29. ONE COMPLETE REGISTER READ SEQUENCE VIA THE SERIAL BUS INTERFACE

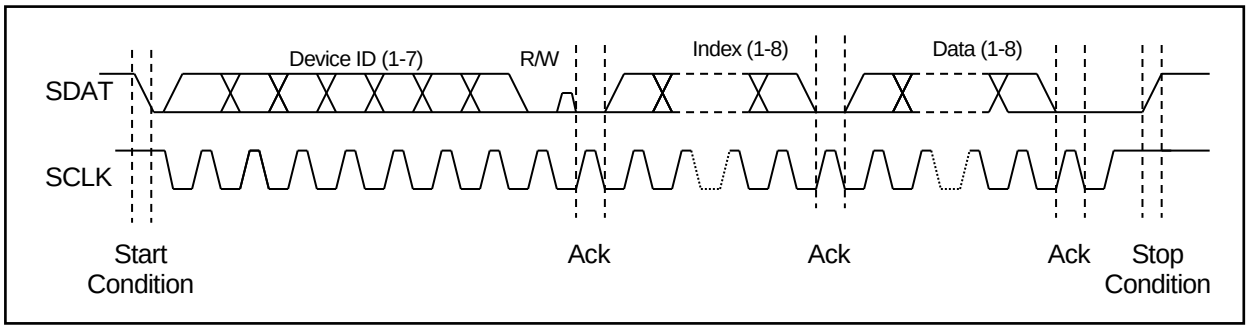


FIGURE 30. ONE COMPLETE REGISTER WRITE SEQUENCE VIA THE SERIAL BUS INTERFACE

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW2968 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDDO. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW2968 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD[1:0] (Serial Interface Address) pins to either VDDO or VSS (See below Table) through a pull-up or pull-down resister. The SIAD[1:0] pins are multi-purpose pins and must not tied to supply voltage or ground directly. If the SIAD[1:0] pins are tied to VDDO, then the least significant 2-bit of the 7-bit address is a “11”. If the SIAD[1:0] pins are tied to VSS then the least significant 2-bit of the 7-bit address is a “00”. The most significant 5-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDAT from high to low, while SCLK is high, this is defined to be a start condition (See FIGURE 27.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in FIGURE 29. (For the TW2968, the next byte is normally the index to the TW2968 registers and is a write to the TW2968 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

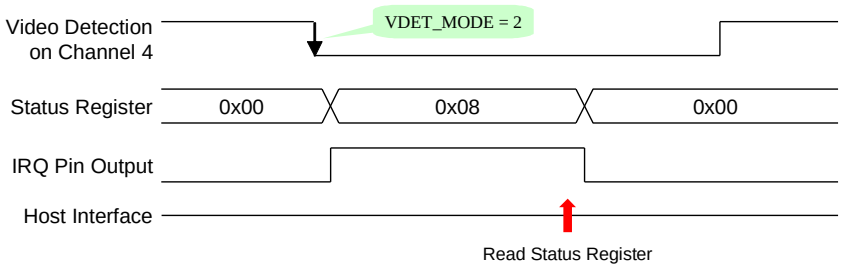
To write to the internal register of the TW2968, the master sends another 8-bits of data, the TW2968 loads this to the register pointed by the internal index register. The TW2968 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW2968 if they are in ascending sequential order. After each 8-bit transfer,the TW2968 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW2968 the host will issue a stop condition.

SERIAL BUS INTERFACE 7-BIT SLAVE ADDRESS							READ/WRITE BIT
0	1	0	1	0	SIAD[1]	SIAD[0]	1 = Read 0 = Write

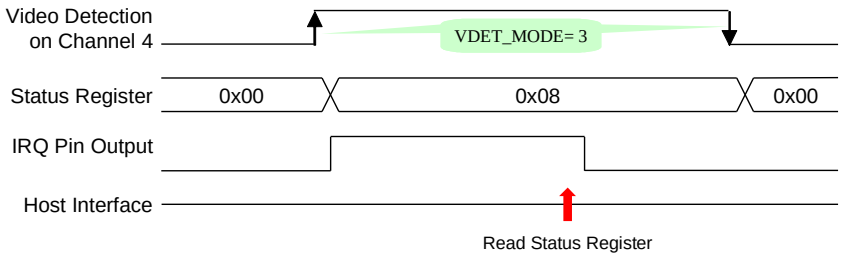
A TW2968 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See FIGURE 28). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Interrupt Interface

The TW2968 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video or audio signal from TW2968. To use interrupt request function, the interrupt request should be enabled by the IRQENA and polarity of the IRQ pin should be selected by the IRQPOL. Also, each channel of video and audio detection should be enabled by the AVDET1_ENA,A51DET_ENA, AVDET2_ENA,A52DET_ENA.Then,the interrupt mode should be defined by the VDET_MODE and ADET_MODE that control the time to request interrupt and set the status register AVDET1_STATE,A51DET_STATE, AVDET2_STATE,A52DET_STATE. FIGURE 31 shows operation of interrupt when the VDET_MODE and/or ADET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading all enabled bits in AVDET1_STATE, A51DET_STATE,AVDET2_STATE,A52DET_STATE.If some bits are not enabled for interrupt requests in AVDET1_ENA,A51DET_ENA,AVDET2_ENA,A52DET_ENA,those bits in AVDET1_STATE,A51DET_STATE, AVDET2_STATE,A52DET_STATE are not needed to be read to clear interrupt.When the VDET_MODE and/or ADET_MODE is 1 or 2, the status register AVDET1_STATE,A51DET_STATE,AVDET2_STATE,A52DET_STATE will also be cleared automatically by reading AVDET_STATE,A51DET_STATE,AVDET2_STATE,A52DET_STATE. However, when the VDET_MODE and/or ADET_MODE are 3, the status register AVDET1_STATE, A51DET_STATE,AVDET2_STATE,A52DET_STATE will not be cleared automatically, but has the same value as actual status of video and audio detection flag.



(a) Status Register of Automatic Cleared Mode



(b) Status Register same as Video and Audio Detection Flag Mode

FIGURE 32. TIMING DIAGRAM OF INTERRUPT INTERFACE

Clock PLL

The TW2968 has built-in clock PLL.It generates 108MHz clock and 144MHz clock from 27MHz input reference clock.

XTI Clock Input

If XTI input needs special x2(54MHz or 72MHz),x4(108MHz or 144MHz) frequency, IRQ pin pull-down setting during RSTB = 0 period support up to 400kbps two wire serial bus speed at X1/X4 XTI input mode.

IRQ	TWO WIRE SERIAL BUS SPEED	SYSTEM CLOCK OF TWO WIRE SERIAL BUS INTERFACE	REQUIRED XTI INPUT FREQUENCY
NC	400kbps	XTI	X1(27MHz or 36MHz)
NC	350kbps	XTI/2	X2(54MHz or 72MHz)
Pull-down	400kbps	XTI/4	X4(108MHz or 144MHz)

In this special mode,if XTI=36MHz/72MHz/144MHz,WD1 960H video output is only supported,and if XTI=54MHz/108MHz,D1 720H video output is only supported.
Some normal functions are not available when XTI=27MHz is not used.

PTZ Tx Pulse Generation

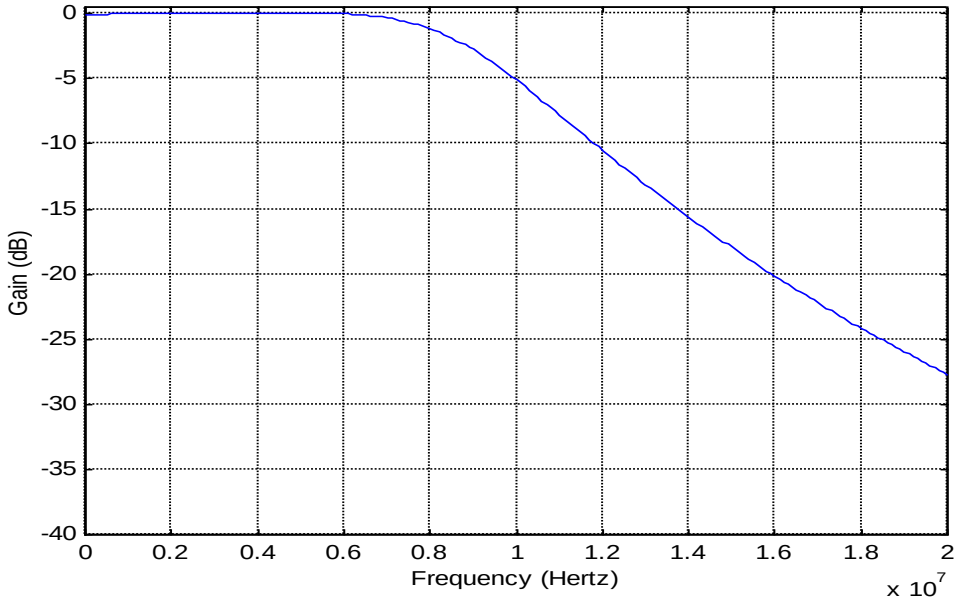
TW2968 has a PTZ Tx pulse generation function. This technology is used to share single coaxial cable for CVBS downstream image transmission and PTZ control command pulse upstream transmission. When the camera module receives PTZ control command pulse, it operates Pan, Tilt or Zoom depending on the command encoded in the PTZ pulse.

The bit stream protocols (such as Pelco-C, etc.) are specified in a standard document separately. This feature is used to provide flexible, fundamental and general purpose bit sequence generation features, while remaining independent from the individual PTZ communication protocol standards. Please refer to the example application schematic for the external circuit to inject PTZ control pulse to coaxial cable.

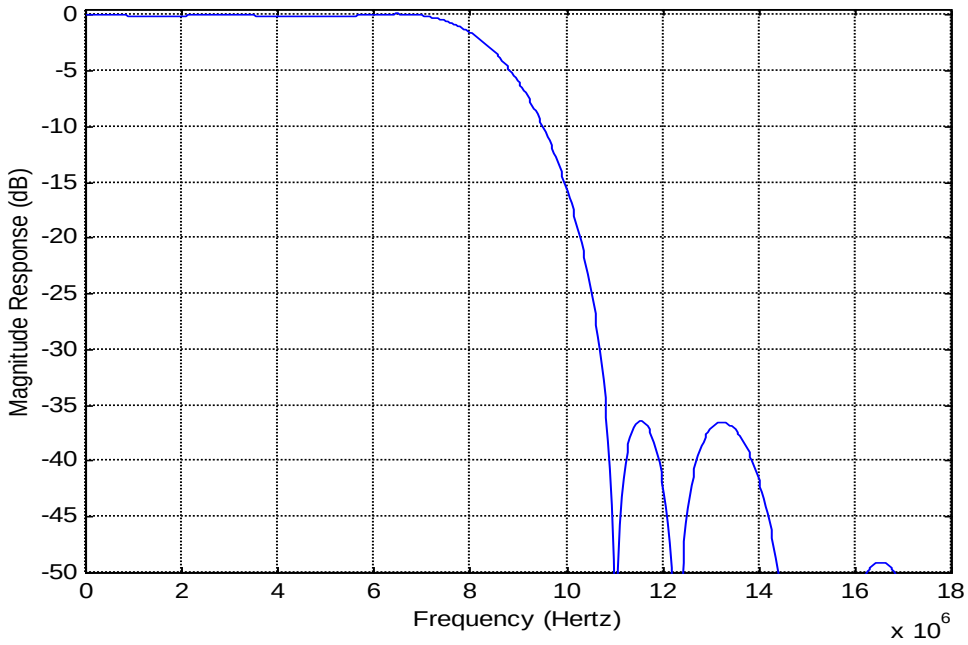
When using this function, please make sure to change related registers, except enable or disable register of this function, while PTZ Tx pulse generation is disabled.

Video Decoder Filter Curves

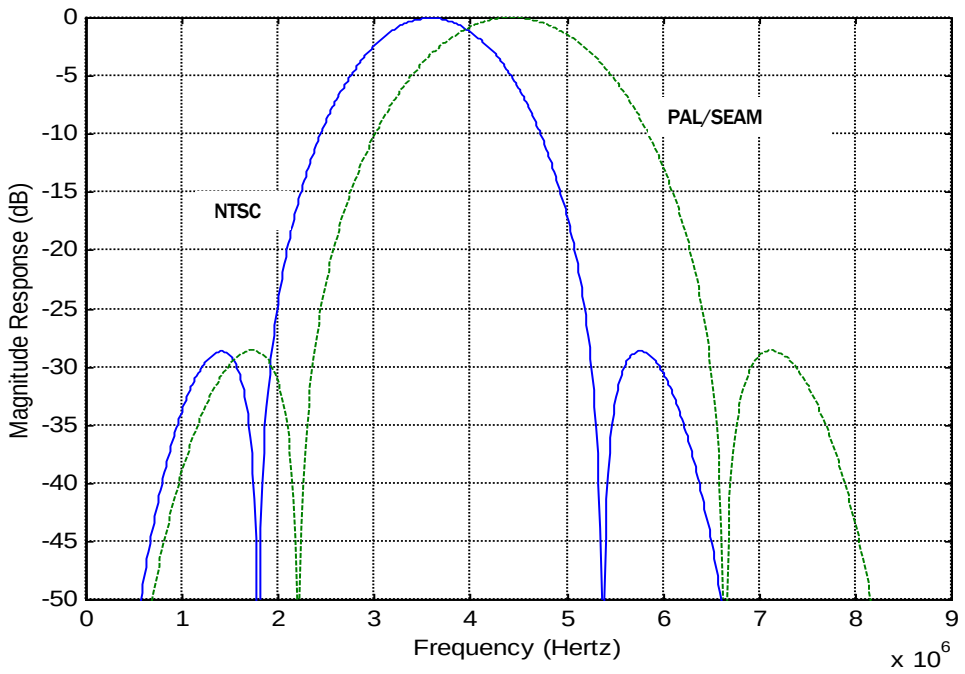
ANTI-ALIAS FILTER



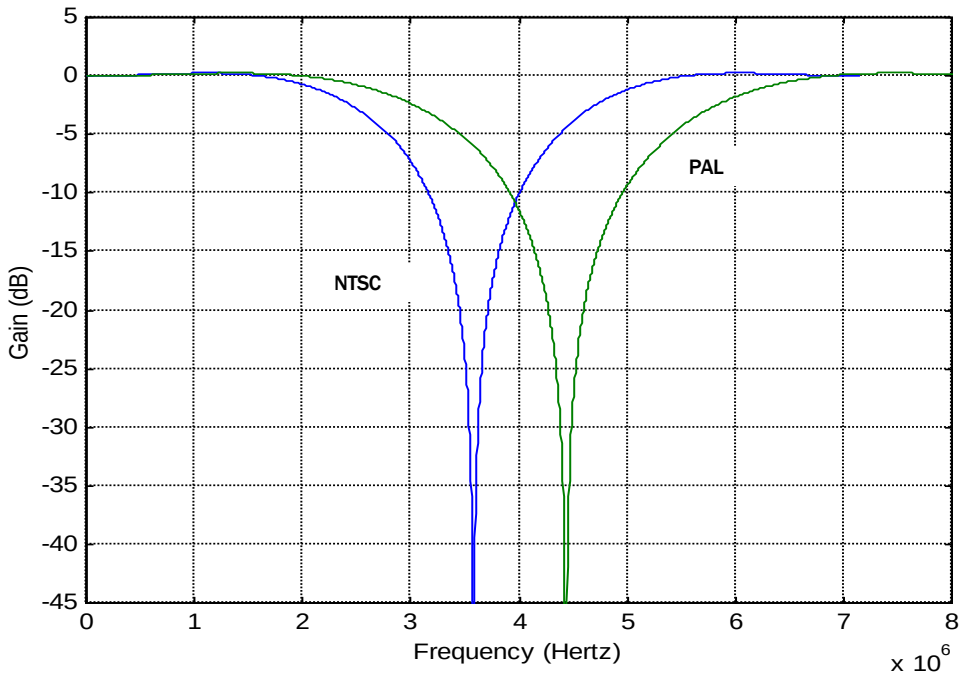
DECIMATION FILTER



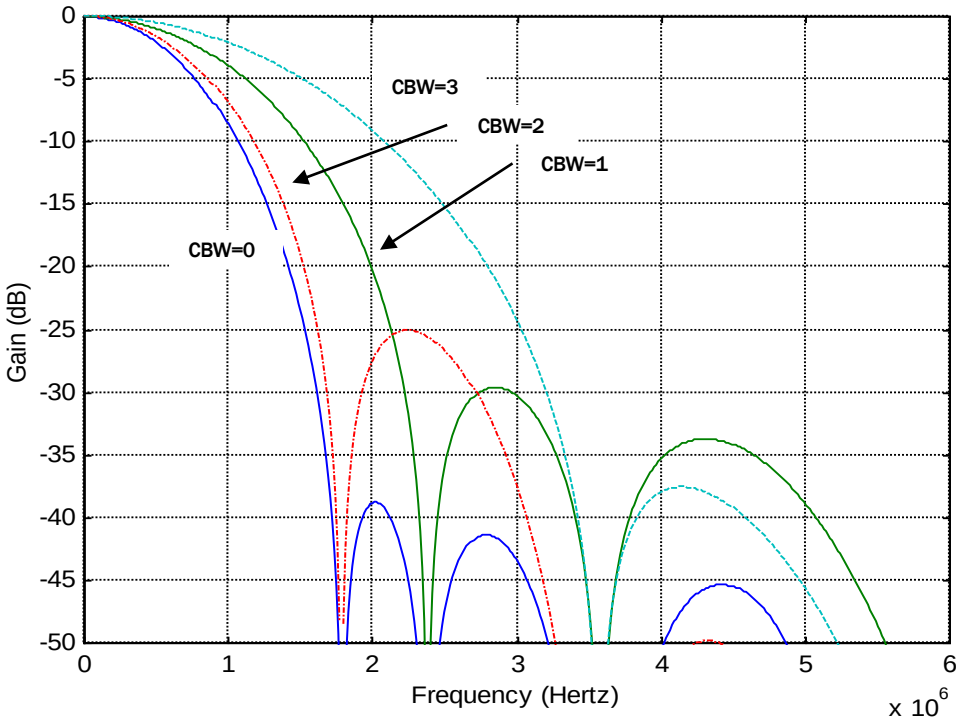
CHROMA BAND PASS FILTER CURVES



LUMA NOTCH FILTER CURVE FOR NTSC AND PAL

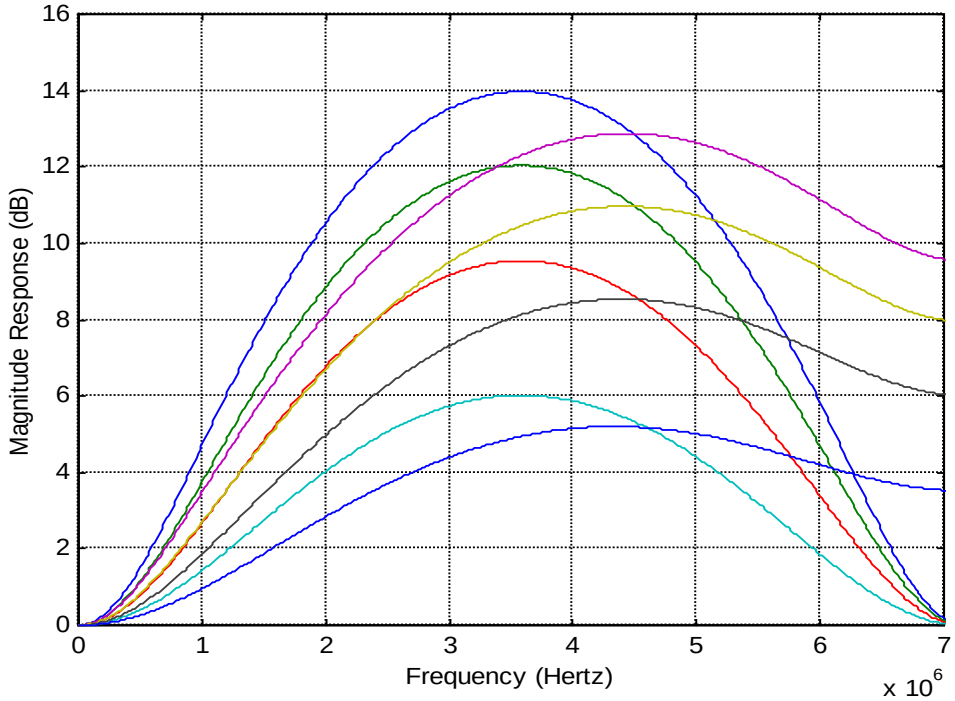


CHROMINANCE LOW-PASS FILTER CURVE

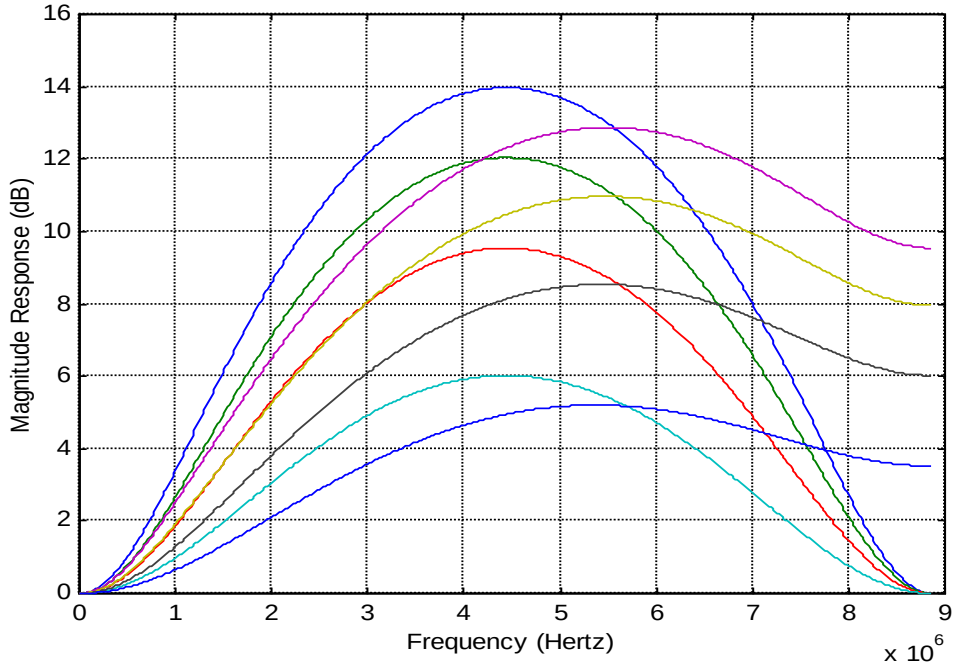


PEAKING FILTER CURVES

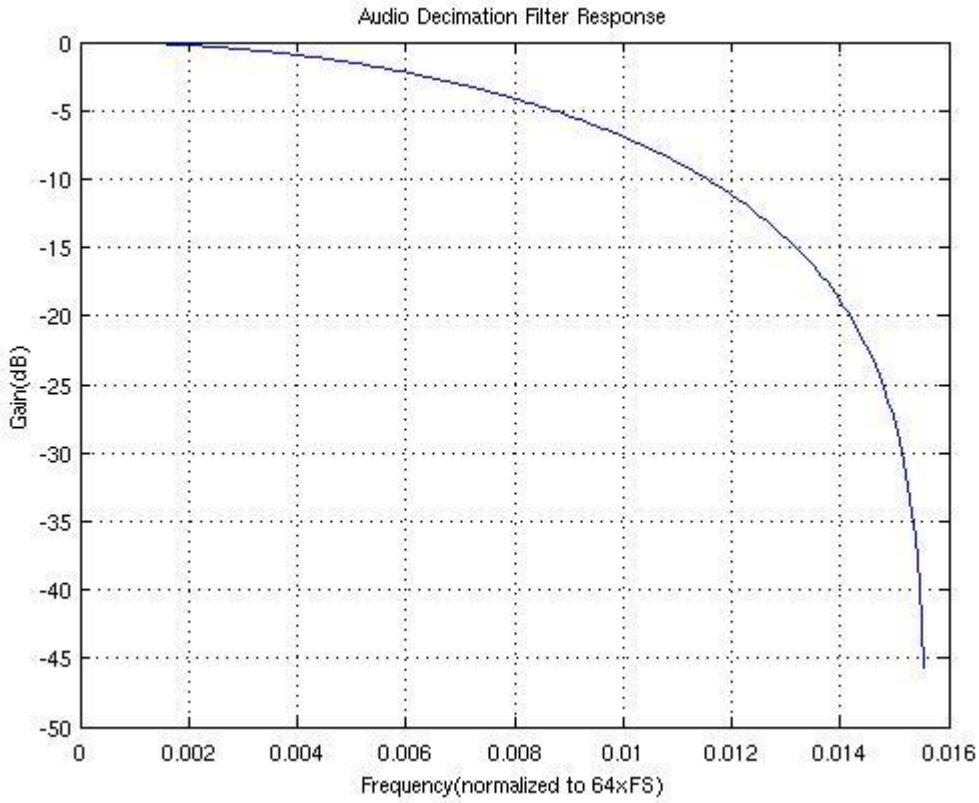
NTSC



PAL



Audio Decimation Filter Response



(*) 0.016 line = 0.016x64xFs

Control Register

PAGE MODE REGISTER MAP

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x40	PAGE	0	0	0	0	0	0	PAGE	

PAGE0 REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN1	VIN2	VIN3	VIN4									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xA0	0xA1	0xA2	0xA3	NT50	NT50	CVSTD*			CVFMT			
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF*							

Note: * Read only registers

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x4F	TESTOUTSEL	0	0	OETESTOUTSEL	TEST_OUTSEL				
0x51	FBITINV	FBITINV8	FBITINV7	FBITINV6	FBITINV5	FBITINV4	FBITINV3	FBITINV2	FBITINV1
0x52	ANADACTEST	VCM_SEL	LPF_SEL			BIAS_SEL	AN_ADACTEST		
0x53	VADCCKPOL	VADCCKPOL							
0x54	ASAVE1	0	ADACLK_INV	DOUT_RST	DIV_RST	ACALEN	ASAVE1		
0x55	AAFLPF1234	AAFLPF4		AAFLPF3		AAFLPF2		AAFLPF1	
0x56	HASYNC1234	HASYNC4	HASYNC3	HASYNC2	HASYNC1	HBLEN4[8]	HBLEM3[8]	HBLEN2[8]	HBLEN1[8]
0x57	HBLEN1	HBLEM1[7:0]							
0x58	HBLEN2	HBLEN2[7:0]							
0x59	HBLEN3	HBLEN3[7:0]							
0x5A	HBLEN4	HBLEN4[7:0]							
0x5B	CKDS	0	0	0	0	PLLCKOUT	XTI36	CKN_DS	CLP_DS
0x5C	BGCTL	0	0	BGCTL	0	0	0	0	0
0x5D	CH2MISC2	NKILL_2	PKILL_2	SKILL_2	CBAL_2	FCS_2	LCS_2	CCS_2	BST_2
0x5E	CH3MISC2	NKILL_3	PKILL_3	SKILL_3	CBAL_3	FCS_3	LCS_3	CCS_3	BST_3
0x5F	CH4MISC2	NKILL_4	PKILL_4	SKILL_4	CBAL_4	FCS_4	LCS_4	ICCS_4	BST_4
0x60	VCO	CLK_DIFF	CP_SEL			LP_X8		VCO	
0x61	XTIMD	PLLRST	PLL_PD	PLL_IREF	DECOSC	SEL_144_72	SEL_108_54	XTIMD	
0x62	MPPOE	0	0	0	0	MPP4OE	MPP3OE	MPP2OE	MPP1OE
0x63	CH12NUM	CH2NUM				CH1NUM			
0x64	CH34NUM	CH4NUM				CH3NUM			
0x65	CH56NUM	CH6NUM				CH5NUM			
0x66	CH78NUM	CH8NUM				CH7NUM			
0x67	HZST	HZST							
0x68	HZOOM_HI1234	HZOOM4[9:8]		HZOOM3[9:8]		HZOOM2[9:8]		HZOOM1[9:8]	
0x69	HZOOM1_LOW	HZOOM1[7:0]							
0x6A	HZOOM2_LOW	HZOOM2[7:0]							
0x6B	HZOOM3_LOW	HZOOM3[7:0]							
0x6C	HZOOM4_LOW	HZOOM4[7:0]							
0x6D	D1 NMGAIN	NMGAIN720				SHCOR720			
0x6E	PCLAMP720	PCLAMP720							
0x6F	VDFREQ	VD4FREQ	VD3FREQ	VD2FREQ	VD1FREQ	VD4_OEB	VD3_OEB	VD2_OEB	VD1_OEB
0x70	ACLKPOL	ACK36MD	S2I_8BIT	ACLKRPOL	ACLKPPOL	AFAUTO	AFMD		
0x71	AINCTL	I2S8MODE	MASCKMD	PBINSWAP	ASYNRDLY	ASYNPDLY	ADATPDLY	INLAWMD	
0x72	MRATIOMD	MRATIOMD	ADACTEST	AOFFCORE	DAORATIO	DAOGAIN			
0x73	A51NUM	0	0	0	MUTEADATR	MUTEADATM	AIN51FORM	AINTPOFF	A51DET_ENA
0x74	A51DETST	0	0	0	0	0	0	0	A51DET_STATE*

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x75	AADC51OFS_H	0	0	0	0	0	0	AADC51OFS[9:8]	
0x76	AADC51OFS_L	AADC51OFS[7:0]							
0x77	AUD51ADC_H	0	0	0	0	0	0	AUD5A1DC[9:8]	
0x78	AUD51ADC_L	AUD51ADC[7:0]							
0x79	ADJAADC51_H	0	0	0	0	0	0	ADJAADC51[9:8]	
0x7A	ADJAADC51_L	ADJAADC51[7:0]							
0x7B	I2SO_RSEL	0	0	0	I2SO_RSEL				
0x7C	I2SO_LSEL	0	0	0	I2SO_LSEL				
0x7D	RECSEL5	I2SRECSEL54		I2SRECSEL53		I2SRECSEL52		I2SRECSEL51	
0x7E	ADATMI2S	A51OUTOFF	ADATM_I2SOEN	MIX_MUTE_A51	ADET_TH51[4:0]				
0x7F	AIGAIN51	AIGAIN51				MIX_RATIO51			
0x80	SRST	COAXRST	0	AUDIORST	VOUTRST	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST
0x81	ACNTL	0	0	0	0	CLKPDN	YCLEN2	YFLEN1	YFLEN2
0x82	ACNTL2	CTEST	YCLEN1	CKIPOL27	CKIPOL36	GTEST	VLPF	CKLY	CKLC
0x83	CNTRL1	PBW	DEM	IDSNS	SET7	COMB	HCOMP	YCOMB	PDLY
0x84	CKHY	GMEN	CKHY		HSDLY				
0x85	SHCOR960	SHCOR960				0	0	0	0
0x86	CORING	CTCOR		CCOR		VCOR		CIF	
0x87	CLMPG	CLPEND				CLPST			
0x88	IAGC	NMGAIN960				WPGAIN			0
0x89	AIN5MD	ATHROUGH	ASYNSERIAL	ACLKR128	ACLKR64	AFS384	AIN5MD	0	0
0x8A	PEAKWT	PEAKWT							
0x8B	CLMPL	CLMPLD	CLMPL						
0x8C	SYNCT	SYNCTD	SYNCT						
0x8D	MISSCNT	MISSCNT				HSWIN			
0x8E	PCLAMP960	PCLAMP960							
0x8F	VCNTL1	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT
0x90	VCNTL2	BSHT			VSHT				
0x91	CKILL	CKILMAX		CKILMIN					
0x92	VTL	HTL				VTL			
0x93	LDLY	CKLM	YDLY			PD_BIAS	VSAVE1		
0x94	MISC1	HPLC	EVCNT	PALC	SDET	0	BYPASS	0	
0x95	CBW	HPM		ACCT		SPM		CBW	
0x96	MISC2	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST
0x97	CLMD	FRM		YNR		CLMD		PSP	
0x98	HSLOWCTL	HSBEGIN[3:0]				HSEND[3:0]			
0x99	HSBEGIN	HSBEGIN[11:4]							
0x9A	HSEND	HSEND[11:4]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x9B	OVSDLY	OVSDLY							
0x9C	OVSEND	0	OFDLY			VSMODE	OVSEND		
0x9E	NOVID	VDELAYMD	FC27	CHID_MD		NOVID_656	EAVSWAP	VIPCFG	NTSC656
0x9F	CLKODEL	CLKNO_DEL				CLKPO_DEL			
0xA8	HFLT12	HFLT2				HFLT1			
0xA9	HFLT34	HFLT4				HFLT3			
0xAA	AGCEN1234	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0xAB	AGCGAIN1	AGCGAIN1[7:0]							
0xAC	AGCGAIN2	AGCGAIN2[7:0]							
0xAD	AGCGAIN3	AGCGAIN3[7:0]							
0xAE	AGCGAIN4	AGCGAIN4[7:0]							
0xAF	VSHP12	0	VSHP2			0	VSHP1		
0xB0	VSHP34	0	VSHP4			0	VSHP3		
0xB1	TESTVNUM	0	0	0	0	CLPOE	TESTVNUM		
0xB2	VDLOSSOE	VDLOSSOE8	VDLOSSOE7	VDLOSSOE6	VDLOSSOE5	VDLOSSOE4	VDLOSSOE3	VDLOSSOE2	VDLOSSOE1
0xB3	AADC0FS_H	AADC4OFS[9:8]		AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]	
0xB4	AADC1OFS_L	AADC1OFS[7:0]							
0xB5	AADC2OFS_L	AADC2OFS[7:0]							
0xB6	AADC3OFS_L	AADC3OFS[7:0]							
0xB7	AADC4OFS_L	AADC4OFS[7:0]							
0xB8	AUDADC_H*	AUD4ADC[9:8]		AUD3ADC[9:8]		AUD2ADC[9:8]		AUD1ADC[9:8]	
0xB9	AUD1ADC_L*	AUD1ADC[7:0]							
0xBA	AUD2ADC_L*	AUD2ADC[7:0]							
0xBB	AUD3ADC_L*	AUD3ADC[7:0]							
0xBC	AUD4ADC_L*	AUD4ADC[7:0]							
0xBD	ADJAADC_H*	ADJAADC4[9:8]		ADJAADC3[9:8]		ADJAADC2[9:8]		ADJAADC1[9:8]	
0xBE	ADJAADC1_L*	ADJAADC1[7:0]							
0xBF	ADJAADC2_L*	ADJAADC2[7:0]							
0xC0	ADJAADC3_L*	ADJAADC3[7:0]							
0xC1	ADJAADC4_L*	ADJAADC4[7:0]							
0xC8	MPP12	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0xC9	MPP34	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		
0xCB	POLMPP	POLMPP8	POLMPP7	POLMPP6	POLMPP5	POLMPP4	POLMPP3	POLMPP2	POLMPP1
0xCC	H960EN	H960EN8	H960EN7	H960EN6	H960EN5	H960EN4	H960EN3	H960EN2	H960EN1
0xCD	O36M	O36M8	O36M7	O36M6	O36M5	O36M4	O36M3	O36M2	O36M1
0xCE	ANAPWDN	AAUTOMUTE	0	A_DAC_PWDN	A_ADC_PWDN	VADC_PWDN			
0xCF	SMD	SMD		0	0	0	0	0	0
0xD0	AIGAIN21	AIGAIN2				AIGAIN1			

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xD1	AIGAIN43	AIGAIN4				AIGAIN3			
0xD2	R_MULTCH	M_RLSWAP	RM_SYNC	RM_PBSEL		R_ADATM		R_MULTCH	
0xD3	R_SEQ10	R_SEQ_1				R_SEQ_0			
0xD4	R_SEQ32	R_SEQ_3				R_SEQ_2			
0xD5	R_SEQ54	R_SEQ_5				R_SEQ_4			
0xD6	R_SEQ76	R_SEQ_7				R_SEQ_6			
0xD7	R_SEQ98	R_SEQ_9				R_SEQ_8			
0xD8	R_SEQBA	R_SEQ_B				R_SEQ_A			
0xD9	R_SEQDC	R_SEQ_D				R_SEQ_C			
0xDA	R_SEQFE	R_SEQ_F				R_SEQ_E			
0XDB	AMASTER	ADACEN	AADCEN	PB_MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER
0xDC	MIX_MUTE	LAWMD		MIX_DERATIO	MIX_MUTE				
0xDD	MIX_RATIO21	MIX_RATIO2				MIX_RATIO1			
0xDE	MIX_RATIO43	MIX_RATIO4				MIX_RATIO3			
0xDF	MIX_RATIOP	AOGAIN				MIX_RATIOP			
0xE0	MIX_OUTSEL	0	AADCCKPOL	ADACCKPOL	MIX_OUTSEL				
0xE1	ADET	AAMPMD	ADET_FILT			ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]
0xE2	ADET_TH12	ADET_TH2[3:0]				ADET_TH1[3:0]			
0xE3	ADET_TH34	ADET_TH4[3:0]				ADET_TH3[3:0]			
0xE4	YDLY12	0	YDLY2			0	YDLY1		
0xE5	YDLY34	0	YDLY4			0	YDLY3		
0xE7	VDMD	VD4MD		VD3MD		VD2MD		VD1MD	
0xE8	VD1012SEL	VD102SEL				VD101SEL			
0xE9	VD1034SEL	VD104SEL				VD103SEL			
0XEA	VD2012SEL	VD202SEL				VD201SEL			
0xEB	VD2034SEL	VD204SEL				VD203SEL			
0xEC	VD3012SEL	VD302SEL				VD301SEL			
0xED	VD3034SEL	VD304SEL				VD303SEL			
0xEE	VD4012SEL	VD402SEL				VD401SEL			
0xEF	VD4034SEL	VD404SEL				VD403SEL			
0xF0	ACKI_L	ACKI[7:0]							
0xF1	ACKI_M	ACKI[15:8]							
0xF2	ACKI_H	0	0	ACKI[21:16]					
0xF3	ACKN_L	ACKN[7:0]							
0xF4	ACKN_M	ACKN[15:8]							
0xF5	ACKN_H	0	0	0	0	0	0	ACKN[17:16]	
0xF6	SDIV	0	0	SDIV					
0xF7	LRDIV	0	0	LRDIV					

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xF8	ACCNTL	APZ	APG			Reserved	ACPL	SRPH	LRPH
0xF9	VMISC	LIM16	PBREFEN	YCBCR422	MPPMD	VBI_FRAM	CNTL656	CLKNF	CLKPF
0xFA	CLKOCTL	0	OE	CLKNO_OEB	CLKPO_OEB	CLKNO_MD		CLKPO_MD	
0xFB	AVDET_MODE	CLKNO_POL	CLKPO_POL	IRQENA	IRQPOL	ADET_MODE		VDET_MODE	
0xFC	AVDET1_ENA	AVDET1_ENA							
0xFD	AVDET1_STATE*	AVDET1_STATE							
0xFE	TEST	DEV_ID[6:5]*		0	0	0	TEST		
0xFF	DEV_ID*	DEV_ID[4:0]*					REV_ID		

Note: * Read only registers

PAGE1 REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN5	VIN6	VIN7	VIN8									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xA0	0xA1	0xA2	0xA3	NT50	NT50	CVSTD*			CVFMT			
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF*							

Note: * Read only registers

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x54	ASAVE2	0	0	0	0	0	ASAVE2		
0x55	AAFLPF5678	AAFLPF8		AAFLPF7		AAFLPF6		AAFLPF5	
0x56	HASYNC5678	HASYNC8	HASYNC7	HASYNC6	HASYNC5	HBLEN8[8]	HBLEM7[8]	HBLEN6[8]	HBLEN5[8]
0x57	HBLEN5	HBLEM5[7:0]							
0x58	HBLEN6	HBLEN6[7:0]							
0x59	HBLEN7	HBLEN7[7:0]							
0x5A	HBLEN8	HBLEN8[7:0]							
0x5D	CH6MISC2	NKILL_6	PKILL_6	SKILL_6	CBAL_6	FCS_6	LCS_6	CCS_6	BST_6
0x5E	CH7MISC2	NKILL_7	PKILL_7	SKILL_7	CBAL_7	FCS_7	LCS_7	CCS_7	BST_7
0x5F	CH8MISC2	NKILL_8	PKILL_8	SKILL_8	CBAL_8	FCS_8	LCS_8	ICCS_8	BST_8
0x68	HZOOM_HI5678	HZOOM8[9:8]		HZOOM7[9:8]		HZOOM6[9:8]		HZOOM5[9:8]	
0x69	HZOOM5_LOW	HZOOM5[7:0]							
0x6A	HZOOM6_LOW	HZOOM6[7:0]							
0x6B	HZOOM7_LOW	HZOOM7[7:0]							
0x6C	HZOOM4_LOW	HZOOM8[7:0]							
0x73	A52NUM	0	0	0	0	0	0	0	A52DET_ENA
0x74	A52DETST	0	0	0	0	0	0	0	A52DET_STATE*
0x75	AADC52OFS_H	0	0	0	0	0	0	AADC52OFS[9:8]	
0x76	AADC52OFS_L	AADC52OFS[7:0]							
0x77	AUD52ADC_H	0	0	0	0	0	0	AUD5A2DC[9:8]	
0x78	AUD52ADC_L	AUD52ADC[7:0]							
0x79	ADJAADC52_H	0	0	0	0	0	0	ADJAADC52[9:8]	
0x7A	ADJAADC52_L	ADJAADC52[7:0]							
0x7E	ADET_TH52	0	0	MIX_MUTE_A52	ADET_TH52[4:0]				
0x7F	AIGAIN52	AIGAIN52				MIX_RATIO52			
0x80	SRST	0	0	0	0	VDEC8RST	VDEC7RST	VDEC6RST	VDEC5RST
0x93	VSAVE2	0	0	0	0	PD_BIAS2	VSAVE2		
0x96	MISC2_5	NKILL_5	PKILL_5	SKILL)5	CBAL_5	FCS_5	LCS_5	CCS_5	BST_5
0xA8	HFLT56	HFLT6				HFLT5			
0xA9	HFLT78	HFLT8				HFLT7			
0xAA	AGCEN5678	AGCEN8	AGCEN7	AGCEN6	AGCEN5	AGCGAIN8[8]	AGCGAIN7[8]	AGCGAIN6[8]	AGCGAIN5[8]
0xAB	AGCGAIN5	AGCGAIN5[7:0]							
0xAC	AGCGAIN6	AGCGAIN6[7:0]							
0xAD	AGCGAIN7	AGCGAIN7[7:0]							
0xAE	AGCGAIN8	AGCGAIN8[7:0]							
0xAF	VSHP65	0	VSHP6			0	VSHP5		
0xB0	VSHP87	0	VSHP8			0	VSHP7		
0xB3	AADC0FS_H	AADC8OFS[9:8]		AADC7OFS[9:8]		AADC6OFS[9:8]		AADC5OFS[9:8]	

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xB4	AADC5OFS_L	AADC5OFS[7:0]							
0xB5	AADC6OFS_L	AADC6OFS[7:0]							
0xB6	AADC7OFS_L	AADC7OFS[7:0]							
0xB7	AADC8OFS_L	AADC8OFS[7:0]							
0xB8	AUDADC_H*	AUD8ADC[9:8]		AUD7ADC[9:8]		AUD6ADC[9:8]		AUD5ADC[9:8]	
0xB9	AUD5ADC_L*	AUD5ADC[7:0]							
0xBA	AUD6ADC_L*	AUD6ADC[7:0]							
0xBB	AUD7ADC_L*	AUD7ADC[7:0]							
0xBC	AUD8ADC_L*	AUD8ADC[7:0]							
0xBD	ADJAADC_H*	ADJAADC8[9:8]		ADJAADC7[9:8]		ADJAADC6[9:8]		ADJAADC5[9:8]	
0xBE	ADJAADC5_L*	ADJAADC5[7:0]							
0xBF	ADJAADC6_L*	ADJAADC6[7:0]							
0xC0	ADJAADC7_L*	ADJAADC7[7:0]							
0xC1	ADJAADC8_L*	ADJAADC8[7:0]							
0xC8	MPP56	GPP_VAL6	MPP_MODE6			GPP_VAL5	MPP_MODE5		
0xC9	MPP78	GPP_VAL8	MPP_MODE8			GPP_VAL7	MPP_MODE7		
0xD0	AIGAIN65	AIGAIN6				AIGAIN5			
0xD1	AIGAIN87	AIGAIN8				AIGAIN7			
0xDD	MIX_RATIO56	MIX_RATIO6				MIX_RATIO5			
0xDE	MIX_RATIO78	MIX_RATIO8				MIX_RATIO7			
0xE1	ADET5678	0	0	0	0	ADET_TH8[4]	ADET_TH7[4]	ADET_TH6[4]	ADET_TH5[4]
0xE2	ADET_TH56	ADET_TH6[3:0]				ADET_TH5[3:0]			
0xE3	ADET_TH78	ADET_TH8[3:0]				ADET_TH7[3:0]			
0xE4	YDLY56	0	YDLY6			0		YDLY5	
0xFC	AVDET2_ENA	AVDET2_ENA							
0xFD	AVDET2_STATE*	AVDET2_STATE							

Note: * Read only registers

PAGE2 REGISTER MAP

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x01	COAX_CH	COAX_LINE_NUM		COAX_FLD_MD		COAX_TX_WEN	COAX_CH		
0x02	COAX_TX_EN	COAX_VSTR		0	COAX_FLD_POL	COAX_DEF_D	COAX_TX_MODE	COAX_TX_EN	0
0x03	COAX_VSTRT	COAX_VSTRT							
0x04	COAX_DATALEN	COAX_DATALEN							
0x05	COAX_BITCLK_H	COAX_BITCLK[15:8]							
0x06	COAX_BITCLK_L	COAX_BITCLK[7:0]							
0x07	COAX_HSTART_H	COAX_HSTART[15:8]							
0x08	COAX_HSTART_L	COAX_HSTART[7:0]							
0x09	COAX_L0_70	COAX_L0[7:0]							
0x0A	COAX_L0_158	COAX_L0[15:8]							
0x0B	COAX_L0_2316	COAX_L0[23:16]							
0x0C	COAX_L0_3124	COAX_L0[31:24]							
0x0D	COAX_L0_3932	COAX_L0[39:32]							
0x0E	COAX_L0_4740	COAX_L0[47:40]							
0x0F	COAX_L0_5548	COAX_L0[55:48]							
0x10	COAX_L0_6356	COAX_L0[63:56]							
0x11	COAX_L0_7164	COAX_L0[71:64]							
0x12	COAX_L0_7972	COAX_L0[79:72]							
0x13	COAX_L0_8780	COAX_L0[87:80]							
0x14	COAX_L0_9588	COAX_L0[95:88]							
0x15	COAX_L1_70	COAX_L1[7:0]							
0x16	COAX_L1_158	COAX_L1[15:8]							
0x17	COAX_L1_2316	COAX_L1[23:16]							
0x18	COAX_L1_3124	COAX_L1[31:24]							
0x19	COAX_L1_3932	COAX_L1[39:32]							
0x1A	COAX_L1_4740	COAX_L1[47:40]							
0x1B	COAX_L1_5548	COAX_L1[55:48]							
0x1C	COAX_L1_6356	COAX_L1[63:56]							
0x1D	COAX_L1_7164	COAX_L1[71:64]							
0x1E	COAX_L1_7972	COAX_L1[79:72]							
0x1F	COAX_L1_8780	COAX_L1[87:80]							
0x20	COAX_L1_9588	COAX_L1[95:88]							
0x21	COAX_L2_70	COAX_L2[7:0]							
0x22	COAX_L2_158	COAX_L2[15:8]							
0x23	COAX_L2_2316	COAX_L2[23:16]							
0x24	COAX_L2_3124	COAX_L2[31:24]							
0x25	COAX_L2_3932	COAX_L2[39:32]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x26	COAX_L2_4740	COAX_L2[47:40]							
0x27	COAX_L2_5548	COAX_L2[55:48]							
0x28	COAX_L2_6356	COAX_L2[63:56]							
0x29	COAX_L2_7164	COAX_L2[71:64]							
0x2A	COAX_L2_7972	COAX_L2[79:72]							
0x2B	COAX_L2_8780	COAX_L2[87:80]							
0x2C	COAX_L2_9588	COAX_L2[95:88]							
0x2D	COAX_L3_70	COAX_L3[7:0]							
0x2E	COAX_L3_158	COAX_L3[15:8]							
0x2F	COAX_L3_2316	COAX_L3[23:16]							
0x30	COAX_L3_3124	COAX_L3[31:24]							
0x31	COAX_L3_3932	COAX_L3[39:32]							
0x32	COAX_L3_4740	COAX_L3[47:40]							
0x33	COAX_L3_5548	COAX_L3[55:48]							
0x34	COAX_L3_6356	COAX_L3[63:56]							
0x35	COAX_L3_7164	COAX_L3[71:64]							
0x36	COAX_L3_7972	COAX_L3[79:72]							
0x37	COAX_L3_8780	COAX_L3[87:80]							
0x38	COAX_L3_9588	COAX_L3[95:88]							
0x39	IRQMD	IRQMD		FIELDDET_ENA	DONEDET_ENA	FIELDET_MODE		DONEDT_MODE	
0x3A	COAX_STATE*	0	0	0	0	0	0	COAX_FLD_STA*	COAX_STATE*

Note: * Read only registers

Register Descriptions

Page Access

0X40 – PAGE MODE REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00
1-0	PAGE	R/W	0 = page0 access mode.page0 registers can be read/written. 1 = page1 access mode.page1 registers can be read/written. 2 = page2 access mode.page2 registers can be read/written.	0

Page0 Registers

Followings show page0 registers.These registers can be accessed when 0X40 is 0.

0X00(VIN1)/0X10(VIN2)/0X20(VIN3)/0X30(VIN4) – VIDEO STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0X01(VIN1)/0X11(VIN2)/0X21(VIN3)/0X31(VIN4) – BRIGHTNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(VIN1)/0X12(VIN2)/0X22(VIN3)/0X32(VIN4) – CONTRAST CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h

0X03(VIN1)/0X13(VIN2)/0X23(VIN3)/0X33(VIN4) – SHARPNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with ‘0’ having no effect on the output image. 1 through 15 provides sharpness enhancement with ‘F’ being the strongest.	1

0X04(VIN1)/0X14(VIN2)/0X24(VIN3)/0X34(VIN4) – CHROMA (U) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X05(VIN1)/0X15(VIN2)/0X25(VIN3)/0X35(VIN4) – CHROMA (V) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(VIN1)/0X16(VIN2)/0X26(VIN3)/0X36(VIN4) – HUE CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(VIN1)/0X17(VIN2)/0X27(VIN3)/0X37(VIN4) – CROPPING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08(VIN1)/0X18(VIN2)/0X28(VIN3)/0X38(VIN4) – VERTICAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(VIN1)/0X19(VIN2)/0X29(VIN3)/0X39(VIN4) – VERTICAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(VIN1)/0X1A(VIN2)/0X2A(VIN3)/0X3A(VIN4) – HORIZONTAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

0X0B(VIN1)/0X1B(VIN2)/0X2B(VIN3)/0X3B(VIN4) – HORIZONTAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0X0C(VIN1)/0X1C(VIN2)/0X2C(VIN3)/0X3C(VIN4) – MACROVISION DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(VIN1)/0X1D(VIN2)/0X2D(VIN3)/0X3D(VIN4) – CHIP STATUS II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(VIN1)/0X1E(VIN2)/0X2E(VIN3)/0X3E(VIN4) – STANDARD SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM(not supported) 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(VIN1)/0X1F(VIN2)/0X2F(VIN3)/0X3F(VIN4) – STANDARD RECOGNITION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0X56(VIN1/VIN2/VIN3/VIN4) – HASYNC

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HASYNC4	R/W	1: the length of EAV to SAV is set up and fixed by VIN4 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN4 HACTIVE registers.	0
6	HASYNC3	R/W	1: the length of EAV to SAV is set up and fixed by VIN3 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN3 HACTIVE registers.	0
5	HASYNC2	R/W	1: the length of EAV to SAV is set up and fixed by VIN2 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN2 HACTIVE registers.	0
4	HASYNC1	R/W	1: the length of EAV to SAV is set up and fixed by VIN1 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN1 HACTIVE registers.	0
3	HBLEN4[8]	R/W	Bit8 of VIN4 HBLEN[8:0].Please see HBLEN description.	0
2	HBLEN3[8]	R/W	Bit8 of VIN3 HBLEN[8:0]. Please see HBLEN description.	0
1	HBLEN2[8]	R/W	Bit8 of VIN2 HBLEN[8:0]. Please see HBLEN description.	0
0	HBLEN1[8]	R/W	Bit8 of VIN1 HBLEN[8:0]. Please see HBLEN description.	0

0X57(VIN1)/0X58(VIN2)/0X59(VIN3)/0X5A(VIN4) – HBLEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HBLENn[7:0] n=1,2,3,4	R/W	These bits are effective when HASYNC bit is set to 1.These bits set up the length of EAV to SAV code when HASYNC bit is 1.Normal value is (Total pixel per line – HACTIVE) value.HBLENn[8] is 0 normally. HBLENn[8] is optional purpose only. 36MHz WD1 Vdeo Decoder mode. NTSC/PAL-M(60Hz): B8h(184dec)=1144-960 PAL/SECAM(50Hz): C0h(192dec)=1152-960 27MHz D1 Vdeo Decoder mode. NTSC/PAL-M(60Hz): 8Ah(138dec)=858-720 PAL/SECAM(50Hz): 90h(144dec)=864-720	90h

0X68(VIN1/VIN2/VIN3/VIN4) – HZOOM_HI

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HZOOM4 [9:8]	R/W	Bit9-8 of VIN4 HZOOM registers.	0
5-4	HZOOM3 [9:8]	R/W	Bit9-8 of VIN3 HZOOM registers.	0
3-2	HZOOM2 [9:8]	R.W	Bit9-8 of VIN2 HZOOM registers.	0
1-0	HZOOM1 [9:8]	R/W	Bit9-8 of VIN1 HZOOM registers.	0

0X69(VIN1)/0X6A(VIN2)/0X6B(VIN3)/0X6C(VIN4) – HZOOM_LO

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HZOOM [7:0]	R/W	Bit7-0 of Horizontal Zoom Up register.This register has Horizontal Zoom Up fcuntion together HZOOMn[9:8] by following equation. HZOOM[9:0] = 1024 x source H pixel number / output H pixel number. For example, source H pixel numer = 948 Output H pixel number = 960 HZOOM[9:0] = 1024 x 948 / 960 = 1011.2 = 3F3h. If HZOOM=000h is set up,No HZOOM(path through) output.	00h

0XA0(VIN1)/0XA1(VIN2)/0XA2(VIN3)/0XA3(VIN4) – NT50

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register Standard Selection.	0
6-4	VSTD	R/W	Reserved	0h
3-0	CVFMT	R/W	Reserved	8h

0XA4(VIN1)/0XA5(VIN2)/0XA6(VIN3)/0XA7(VIN4) – ID DETECTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0XAA(VIN1/VIN2/VIN3/VIN4) – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AGCEN4	R/W	Select Video AGC loop function on VIN4 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN4	0
6	AGCEN3	R/W	Select Video AGC loop function on VIN3 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN3	0
5	AGCEN2	R/W	Select Video AGC loop function on VIN2 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN2	0
4	AGCEN1	R/W	Select Video AGC loop function on VIN1 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN1	0
3	AGCGAIN4[8]	R/W	AGCGAIN4 MSB bit	0
2	AGCGAIN3[8]	R/W	AGCGAIN3 MSB bit	0
1	AGCGAIN2[8]	R/W	AGCGAIN2 MSB bit	0
0	AGCGAIN1[8]	R/W	AGCGAIN1 MSB bit	0

0XAB(VIN1)/0XAC(VIN2)/0XAD(VIN3)/0XAE(VIN4) – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN bit7-0.	F0h

0XC4(VIN1)/0XC5(VIN2)/0XC6(VIN3)/0XC7(VIN4) – H MONITOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator (Test purpose only)	X

0X4F – TEST_OUTSEL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R	Reserved	00b
5	OE_TEST_ OUTSEL	R/W	Test Purpose function. 1: {MPP4.MPP3,VD4[7:0]} pins are output enable even if other pin output control registers are set up output disable/tri-state. 0: normal function.	0
4-0	TEST_OUTSEL	R/W	When OE_TEST_OUTSEL is 1,{MPP4,MPP3,VD4[7:0]} pins output following 10bit data.MPP4 is MSB bit9.VD4[0] is LSB bit0. 00h : VIN1 10bit video ADC data 01h : VIN2 10bit video ADC data 02h : VIN3 10bit video ADC data 03h : VIN4 10bit video ADC data 04h : AIN1 10bit audio ADC data 05h : AIN2 10bit audio ADC data 06h : AIN3 10bit audio ADC data 07h : AIN4 10bit audio ADC data 08h : AIN_AUX1 10bit audio ADC data 09h : 10bit audio DAC input data 0Bh : VIN1 video ADC Gain control input data 0Ch : VIN2 video ADC Gain control input data 0Dh : VIN3 video ADC Gain control input data 0Eh : VIN4 video ADC Gain control input data 10h : VIN5 10bit video ADC data 11h : VIN6 10bit video ADC data 12h : VIN7 10bit video ADC data 13h : VIN8 10bit video ADC data 14h : AIN5 10bit audio ADC data 15h : AIN6 10bit audio ADC data 16h : AIN7 10bit audio ADC data 17h : AIN8 10bit audio ADC data 18h : AIN_AUX2 10bit audio ADC data 0Bh : VIN5 video ADC Gain control input data 0Ch : VIN6 video ADC Gain control input data 0Dh : VIN7 video ADC Gain control input data 0Eh : VIN8 video ADC Gain control input data	0

0X51 – FBITINV

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	FBITINV8	R/W	VIN8 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
6	FBITINV7	R/W	VIN7 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
5	FBITINV6	R/W	VIN6 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
4	FBITINV5	R/W	VIN5 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
3	FBITINV4	R/W	VIN4 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
2	FBITINV3	R/W	VIN3 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
1	FBITINV2	R/W	VIN2 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0
0	FBITINV1	R/W	VIN1 656 output data EAV/SAV optional control 1 : F-bit in 4th byte of 656 EAV/SAV code is inversed. 0 : normal mode.F-bit is not inversed.	0

0X52 – AUDIO DAC CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCM_SEL	R/W	Reserved.	0
5-4	LPF_SEL	R/W	Audio DAC LPF corner frequency selection. 0h : 15.6kHz 1h : 7.8kHz 2h : Don't use 3h : 3.9kHz 4h,5h,6h : Don't use 7h : 2.6kHz	0
3	BIAS_SEL	R/W	Bias selection. 0 : AVDD33 as the reference voltage. 1 : select bandgap voltage as the reference.	0
2-0	ADACTEST	R/W	Audio DAC Test control. 0h : normal operation 1h : ibias places to the dac_out(Don't use) 2h : din_0 is placed to the dac_out(Don't use) 3h : both ibias and din_0 are placed at the dac_out(Don't use) 4h : disable output driver.Dac_out floating 5h : disable output driver,ibias places to dac_out 6h : disable output driver,din_0 places to dac_out 7h : don't use	0

0X53 – VADC_CKPOL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VADC8CKPOL	R/W	1 : VIN8 ADC clock polarity is inversed. 0 : VIN8 ADC clock polarity is not inversed.	0
6	VADC7CKPOL	R/W	1 : VIN7 ADC clock polarity is inversed. 0 : VIN7 ADC clock polarity is not inversed.	0
5	VADC6CKPOL	R/W	1 : VIN6 ADC clock polarity is inversed. 0 : VIN6 ADC clock polarity is not inversed.	0
4	VADC5CKPOL	R/W	1 : VIN5 ADC clock polarity is inversed. 0 : VIN5 ADC clock polarity is not inversed.	0
3	VADC4CKPOL	R/W	1 : VIN4 ADC clock polarity is inversed. 0 : VIN4 ADC clock polarity is not inversed.	0
2	VADC3CKPOL	R/W	1 : VIN3 ADC clock polarity is inversed. 0 : VIN3 ADC clock polarity is not inversed.	0
1	VADC2CKPOL	R/W	1 : VIN2 ADC clock polarity is inversed. 0 : VIN2 ADC clock polarity is not inversed.	0
0	VADC1CKPOL	R/W	1 : VIN1 ADC clock polarity is inversed. 0 : VIN1 ADC clock polarity is not inversed.	0

0X54 – AUDIO ADC CONTROL 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6	ADACLK_INV	R/W	Audio DAC clock inversion. 0 : not inversed inside audio DAC. 1 : Clock is inversed inside audio DAC.	0
5	DOUT_RST	R/W	Audio ADC digital output reset for all channel. Test purpose only. This bit must be set up to 0 again after 1 value is set up.	0
4	DIV_RST	R/W	Audio ADC divider reset.Test purpose Only. This bit must be set up to 0 again after 1 value is set up.	0
3	ACALEN	RW	Audio ADC Calibration control.Test purpose only. This bit must be set up to 0 again after 1 value is set up.	0
2-0	ASAVE1	R/W	AIN1/AIN2/AIN3/AIN4/AIN51 Audio ADC power save control. 7h : normal mode. Others : test purpose only.	7

0X55 – VIN1/2/3/4 VIDEO INPUT ANTI-ALIASING FILTER SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AAFLPF4	R/W	VIN4 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
5-4	AAFLPF3	R/W	VIN3 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
3-2	AAFLPF2	R/W	VIN2 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
1-0	AAFLPF1	R/W	VIN1 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0

0X5B – CLOCK OUTPU PIN DRIVE SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	PLLCKOUT	R/W	1 : IRQ pin output PLL 36MHz clock. CLKPO pin output PLL 144MHz clock. CLKNO pin output PLL 108MHz clock. Test purpose only. 0 : normal mode.	0
2	XTI36	R/W	0 : XTI pin is normal 27MHz input. 1 : Special WD1 mode.XTI pin is one of 36MHz/72MHz/144MHz input. 27MHz/54MHz/108MHz D1 mode is not supported in this special mode.	0
1	CKN_DS	R/W	0 : CLKNO pin output is 12mA current drive mode. 1 : CLKNO pin output is 16mA current drive mode.	0
0	CKP_DS	R/W	0 : CLKPO pin output is 12mA current drive mode. 1 : CLKPO pin output is 16mA current drive mode.	0

0X5C– BGCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5	BGCTL	R/W	0: Reg96[7:0] control all VIN1/VIN2/VIN3/VIN4/VIN5/VIN6/VIN7 /VIN8 video. 1: Page0 Reg96[7:0] control only VIN1 video. Page0 Reg5D[7:0] control only VIN2 video. Page0 Reg5E[7:0] control only VIN3 video. Page0 Reg5F[7:0] control only VIN4 video. Page1 Reg96[7:0] control only VIN5 video. Page1 Reg5D[7:0] control only VIN6 video. Page1 Reg5E[7:0] control only VIN7 video. Page1 Reg5F[7:0] control only VIN8 video.	0
4-0	Reserved	R/W		00

0X5D – VIN2 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_2	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_2	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_2	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_2	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_2	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_2	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_2	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_2	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5E – VIN3 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_3	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_3	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_3	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_3	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_3	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_3	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_3	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_3	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5F – VIN4 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_4	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_4	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_4	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_4	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_4	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_4	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_4	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_4	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X60 – CLOK PLL CONTROL 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLK_DIFF	R/W	1 : XTI pin to PLL REF clock input is differential input. 0 : XTI pin to PLL REF clock input is non-differential input.	0
6-4	CP_SEL	R/W	Charge-pump current for PLL 0h : 1uA, 1h : 5uA, 2h : 10uA, 3h : 20uA, 4h : 40uA, 5h : 60UA, 6h : 80uA, 7h : 100uA.	2
3-2	LP_X8	R/W	Loop resistor for PLL 0h : 55.7K, 1h : 17.6K, 2h ; 8.81K, 3h : 6.23K	1
1-0	VCO	R/W	Select VCO gain for PLL 0h : 416MHz/V, 1h : 517MHz/V, 2h : 615MHz/V, 3h : 755MHz/V	2

0X61 – VIDEO CLOCK SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PLLRST	R/W	PLL module Reset#.Test purpose only. 1 : PLL module Reset#, 0 : PLL module is in normal mode.	0
6	PLL_PD	R/W	1 : PLL module is in power down mode. 0 : PLL module is in normal mode.	0
5	PLL_IREF	R/W	PLL Current bias reference	0
4	DECOSC	R/W	Video Decoder system clock select. 0: (PLL output clock)/4 is selected for video decoder process. 1: Video decoder system clock is generated by XTI input crystal clock.	1
3	SEL_144_72	R/W	1 : PLL moulde output 144MHz clock for D1 video decoder. 0 : PLL moulde output 72MHz clock.Test purpose only.	1
2	SEL_108_54	R/W	1 : PLL moulde output 108MHz clock for D1 video decoder. 0 : PLL moulde output 54MHz clock.Test purpose only.	1
1-0	XTIMD	R/W	XTI pin input clock process control. If XTIMD=0/1/2, Clock PLL Output clock is not used for internal logic process. 0: XTI clock is directly used for all video decoder clock source. 1: XTI/2 clock is used for all video decoder clock source. 2: XTI/4 clock is used for all video decoder clock source. 3: PLL output clock is used for all video decoder clock source.	3h

0X62 – O36M/MPPOE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	MPP4OE	R/W	0 : MPP4 pin is input 1 : MPP4 pin is output	0
2	MPP3OE	R/W	0 : MPP4 pin is input 1 : MPP3 pin is output	0
1	MPP2OE	R/W	0 : MPP2 pin is input 1 : MPP2 pin is output	0
0	MPP1OE	R/W	0 : MPP1 pin is input 1 : MPP1 pin is output	0

0X63 – CHANNEL ID 12

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CH2NUM	R/W	Set up Channel ID number in VIN2 video decoder data output.	1h
3-0	CH1NUM	R/W	Set up Channel ID number in VIN1 video decoder data output.	0h

0X64 – CHANNEL ID 34

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CH4NUM	R/W	Set up Channel ID number in VIN4 video decoder data output.	3h
3-0	CH3NUM	R/W	Set up Channel ID number in VIN3 video decoder data output.	2h

0X65 – CHANNEL ID 56

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CH6NUM	R/W	Set up Channel ID number in VIN6 video decoder data output.	5h
3-0	CH5NUM	R/W	Set up Channel ID number in VIN5 video decoder data output.	4h

0X66 – CHANNEL ID 78

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CH8NUM	R/W	Set up Channel ID number in VIN8 video decoder data output.	7h
3-0	CH7NUM	R/W	Set up Channel ID number in VIN7 video decoder data output.	6h

0X67 – HZST

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HZST	R/W	HZOOM UP process start control.After this number's pixels passed out data process from internal hsync(pksync),Hzoom Up module starts it's zooming up process.	80h

0X6D – D1 NMGAIN/SHCOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	NMGAIN 720	R/W	These bits control the normal AGC loop maximum correction value in 720H D1 video decoder.	2h
3-0	SHCOR 720	R/W	These bits provide coring function for the sharpness control in 720H WD1 video decoder.	8h

0X6E – D1 CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP 720	R/W	These bits set the clamping position from the PLL sync edge in 720H D1 video decoder.	38h

0X6F – VIDEO BUS TRI-STATE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VD4FREQ	R/W	1 : VD4[7:0] pin output 36MHz video data. 0 : VD4[7:0] pin output 27MHz video data.	0
6	VD3FREQ	R/W	1 : VD3[7:0] pin output 36MHz video data. 0 : VD3[7:0] pin output 27MHz video data.	0
5	VD2FREQ	R/W	1 : VD2[7:0] pin output 36MHz video data. 0 : VD2[7:0] pin output 27MHz video data.	0
4	VD1FREQ	R/W	1 : VD1[7:0] pin output 36MHz video data. 0 : VD1[7:0] pin output 27MHz video data.	0
3	VD4OEB	R/W	VD4[7:0] output tri-state control. 1: tri-state output VD4[7:0]. 0: normal output VD4[7:0].	0
2	VD3OEB	R/W	VD3[7:0] output tri-state control. 1: tri-state output VD3[7:0]. 0: normal output VD3[7:0].	0
1	VD2OEB	R/W	VD2[7:0] output tri-state control. 1: tri-state output VD2[7:0]. 0: normal output VD2[7:0].	0
0	VD1OEB	R/W	VD1[7:0] output tri-state control. 1: tri-state output VD1[7:0]. 0: normal output VD1[7:0].	0

0X70 – AUDIO CLOCK CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ACK36MD	R/W	1 : 36MHz clock source is used for audio system clock. Special purpose only. 0 : 27MHz clock source is usded for audio system clock.	0
6	S2I_8BIT	R/W	0 : ACLKP/ASYNP/ADATP pin input is 16-bit control. 1 : ACLKP/ASYNP/ADATP pin input is 8-bit control.	0
5	ACLKRPOL	R/W	ACLKR input signal polarity inverse. 0 : not inversed. 1 : inverses.	0
4	ACLKPPOL	R/W	ACLKP input signal polarity inverse. 0 : not inversed. 1 : inversed.	0
3	AFAUTO	R/W	ACKI[21:0] control automatic set up with AFMD registers. This mode is only effective when ACLKRMASTER=1. 0 : ACKI[21:0] registers set up ACKI control. 1 : ACKI control is automatically set up by AFMD register values.	1
2-0	AFMD	R/W	AFAUTO control mode. 0 : 8kHz setting (default). 1 : 16kHz setting. 2 : 32kHz setting. 3 : 44.1kHz setting. 4 : 48kHz setting.	0h

0X71 – DIGITAL AUDIO INPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	I2S8MODE	R/W	8-bit I2S Record output mode. 0 : L/R half length separated output. 1 : One continuous packed output equal to DSP output format.	0
6	MASCKMD	R/W	Audio Clock Master ACLKR output wave format.If ACLKRMASTER=1 and 44.1kHs or 48kHz Fs mode is selected,this bit must be 0. 0 : High period is one 27MHz clock period. 1 : Almost duty 50-50% clock output on ACLKR pin. If this mode is selected, two times bigger number value need to be set up ACKI registers. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1. SDIV=00h is used with this function normally.	1
5	PBINSWAP	R/W	Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping. 0 : Not swapping. 1 : Swapping.	0
4	ASYNRDLY	R/W	ASYNR input signal delay. 0 : No delay. 1 : Add one 27MHz period delay in ASYNR signal input.	0
3	ASYNPDLY	R/W	ASYNP input signal delay. 0 : No delay. 1 : Add one 36MHz period delay in ASYNP signal input.	0
2	ADATPDLY	R/W	ADATP input data delay by one ACLKP clock. 0 : No delay. This is for I2S type 1T delay input interface. 1 : Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.	0
1-0	INLAWMD	R/W	Select u-Law/A-Law/PCM/SB data input format on ADATP pin. 0 : PCM input 1 : SB(Signed MSB bit in PCM data is inverted) input 2 : u-Law input 3 : A-Law input	0h

0X72 – MIX RATIO VALUE 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	MRATIOMD	R/W	Audio Mixing ratio value divider control 0 : MIX_RATIOn 0 0.25 (default) 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1 : MIX_RATIO / 64	0
6	ADACTEST	R/W	0 : must be set up 0 in normal mode. 1 : test purpose only	0
5	AOFFCORE	R/W	0: Audio No-input Noise reduction on(Test purpose only) 1: Audio No-input Noise reduction off	1

0X72 – MIX RATIO VALUE 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4	DAORATIO	R/W	Digital Audio Output Gain is controlled by following. 0: DAOGAIN 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00(default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1: DAOGAIN / 64	0
3-0	DAOGAIN	R/W	Digital Audio Output Gain. Gain is controlled with DAORATIO mode.	8h

0X73 – A51DET_ENA

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R	Reserved	0h
4	MUTEADATR	R/W	0 : normal ADATR output 1: ADATR output is always 0.	0
3	MUTEADATM	R/W	0 : normal ADATM output 1: ADATM output is always 0.	0
2	AIN51FORM	R/W	AIN51/52/53/54 record output format selection. This bit is only effective when A51OUTOFF register is set to 0. When AIN1/2/3/4/51 and AIN6/7/8/9/52 are required to be continuous order in record output, 1 is necessary. 0: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat4><dat5> <dat6><dat7><dat51>< dat52> R dat : <dat8><dat9><datA><datB><datC><datD> <datE><datF><dat53><dat54> If DSP mode(RM_SYNC=1) all data are continuous. <dat0><dat1><dat2><dat3><dat4><dat5><dat6> <dat7><dat8><dat9><datA><datB><datC><datD> <datE><datF><dat51><dat52><dat53><dat54> 1: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat51><dat4> <dat5><dat6><dat7><dat52> R dat : <dat8><dat9><datA><datB><dat53><datC> <datD>< datE>< datF><dat54> If DSP mode(RM_SYNC=1) all data continuous. <dat0><dat1><dat2><dat3>< dat51><dat4><dat5> <dat6><dat7><dat52><dat8><dat9><datA><datB> <dat53><datC><datD><datE><datF><dat54>	0
1	AINTPOFF	R/W	0 : must be set up 1 : test purpose only	0
0	A51DET_ENA	R/W	Enable state register updating and interrupt request of audio AIN51 (AIN_AUX1 input in this chip) detection for each input. 0 : Disable state register updating and interrupt request 1 : Enable state register updating and interrupt request	0

0X74 – STATUS OF AUDIO 51 DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-1	Reserved	R		00h
0	A51DET_STATE	R	State of Audio AIN51(AIN_AUX1 input in this chip) detection. This bit is activated according ADET_MODE. 0 : Inactivated 1 : Activated	0

0X7B – ADATM I2S OUTPUT SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4-0	I2SO_RSEL	R/W	Select R-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h

*Note :
Both I2SO_RSEL and I2SO_LSEL select output data by following order.

0	Select record audio of channel 1(AIN1)
1	Select record audio of channel 2(AIN2)
2	Select record audio of channel 3(AIN3)
3	Select record audio of channel 4(AIN4)
4	Select record audio of channel 5(AIN5)
5	Select record audio of channel 6(AIN6)
6	Select record audio of channel 7(AIN7)
7	Select record audio of channel 8(AIN8)
8	Select record audio of channel 9(AIN9)
9	Select record audio of channel 10(AIN10)
10(Ah)	Select record audio of channel 11(AIN11)
11(Bh)	Select record audio of channel 12(AIN12)
12(Ch)	Select record audio of channel 13(AIN13)
13(Dh)	Select record audio of channel 14(AIN14)
14(Eh)	Select record audio of channel 15(AIN15)
15(Fh)	Select record audio of channel 16(AIN16)
16(10h)	Select playback audio of the first stage chip(PB1)
17(11h)	Select playback audio of the second stage chip(PB2)
18(12h)	Select playback audio of the third stage chip(PB3)
19(13h)	Select playback audio of the last stage chip(PB4)
20(14h)	Select mixed audio.
21(15h)	Select record audio of channel 51(AIN51)(default)
22(16h)	Select record audio of channel 52(AIN52)
23(17h)	Select record audio of channel 53(AIN53)
24(18h)	Select record audio of channel 54(AIN54)
Others	no audio output.

0X7C – ADATM I2S OUTPUT SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4-0	I2SO_LSEL	R/W	Select L-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h

* Note : Please read 0x7B Note for detail description.

0X7D – AIN51/52/53/54 RECORD OUTPUT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	I2SRECSEL54	R/W	Select output data in bellow dat54 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	3h
5-4	I2SRECSEL53	R/W	Select output data in bellow dat53 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	2h
3-2	I2SRECSEL52	R/W	Select output data in bellow dat52 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	1h
1-0	I2SRECSEL51	R/W	Select output data in bellow dat51 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	0

These registers are only effective when A51OUTOFF=0.These registers function change under AIN51FORM control at that time as follows.

When AIN51FORM=0:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat51><dat52>

R data : <dat8><dat9><datA><datB><datC><datD><datE><datF><dat53><dat54>

If DSP mode(RM_SYNC=1), all data are continuous.

<dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat8><dat9><datA><datB><datC>

<datD><datE><datF><dat51><dat52><dat53><dat54>

When AIN51FORM=1:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52>

R data : <dat8><dat9><datA><datB><dat53><datC><datD><datE><datF><dat54>

If DSP mode(RM_SYNC=1),all data are continuous.

<dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52><dat8><dat9>
<datA><datB><dat53><datC><datD><datE><datF><dat54>

All other datN(N=0,1,2,,,,F) are selected by R_SEQ_N registers

0X7E – A5OUTOFF

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	A5OUTOFF	R/W	AIN5 data output control on ADATR record signal. 0: output AIN51/AIN52/AIN53/AIN54 record data on ADATR. 1: not output AIN51/AIN52/AIN53/AIN54 record data on ADATR.	1
6	ADATM_I2SOEN	R/W	Define ADATM pin output 2 word data to make standard I2S output. 0:Mixing Data or Playback Input data are only output on ADATM pin by M_RLSWAP register.(default) 1:L/R data on ADATM pin is selected by I2SO_RSEL / I2SO_LSEL registers.	0
5	MIX_MUTE_A51	R/W	MIX_MUTE_A51: Audio input AIN51=AIN_AUX1 mute function control. 0:Normal 1:Muted	1
4-0	ADET_TH51[4:0]	R/W	AIN51=AIN_AUX1 threshold value for audio detection	03h

0X80 – SOFTWARE RESET CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	COAXRST	W	A 1 written to this bit resets the COAXITRON portion to its default state but all register content remains unchanged. This bit is self-resetting.	0
6	Reserved	W		0
5	AUDIORST	W	A 1 written to this bit resets the Audio portion to its default state but all register content remains unchanged. This bit is self-resetting.	0
4	VOUTRST	W	A 1 written to this bit resets Video data mux output logic to its default state but all register content remain unchanged. This bit is self-resetting.	0
3	VDEC4RST	W	A 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC3RST	W	A 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
1	VDEC2RST	W	A 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC1RST	W	A 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0X81 – ANALOG CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R/W		0h
3	CLKPDN	R/W	0 = Normal clock operation. 1 = All 4Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active.	0
2	YCLEN_2	R/W	1 = VIN5/VIN6/VIN7/VIN8 Y channel clamp disabled (Test purpose only) 0 = Enabled.	0
1	YFLEN_1	R/W	Analog Video VIN1/VIN2/VIN3/VIN4 anti-alias filter control 1 = enable 0 = disable	1
0	YFLEN_2	R/W	Analog Video VIN5/VIN6/VIN7/VIN8 anti-alias filter control 1 = enable 0 = disable	1

0X82 – ANALOG CONTROL REGISTER2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CTEST	R/W	Clamping control for debugging use.(Test purpose only)	0
6	YCLEN_1	R/W	1 = VIN1/VIN2/VIN3/VIN4 Y channel clamp disabled (Test purpose only) 0 = Enabled.	0
5	CKIPOL27	R/W	1/4(27MHz) clock output signal rise/fall timing. 0 : change by 1/2(54MHz) clock output falling edge. 1 : change by 1/2(54MHz) clock output rising edge.	0
4	CKIPOL36	R/W	1/4(36MHz) clock output signal rise/fall timing. 0 : change by 1/2(72MHz) clock output falling edge. 1 : change by 1/2(72MHz) clock output rising edge.	0
3	GTEST	R/W	1 = Test.(Test purpose only) 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0X83 – CONTROL REGISTER I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	IDSNS	R/W	Reserved.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	1 = Bypass Comb filter when no burst presence 0 = No bypass	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0X84 – COLOR KILLER HYSTERESIS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GMEN	R/W	Reserved.	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow	00b
4-0	HSDLY	RW	Reserved for test.	00h

0X85 – VERTICAL SHARPNESS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	SHCOR960	R/W	These bits provide coring function for the sharpness control in 960H WD1 video decoder.	3
3-0	Reserved	R/W		0

0X86 – CORING CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0X87 – CLAMPING GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.	0

0X88 – INDIVIDUAL AGC GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	NMGAIN 960	R/W	These bits control the normal AGC loop maximum correction value for 960H WD1 video deocder.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	Reserved	R	Reserved	0

0X89 – AUDIO FS MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATHROUGH	R/W	0: must be set up in normal mode. 1: test purpose only.	0
6	ASYNSERIAL	R/W	ALINKO/ALINKI bit rate. 0: 27MHz.Effective for all Fs clock mode. 1: 13.5MHz.Effective for Fs 8kHz/16kHz mode.	0
5	ACLKR128	R/W	ACLKR clock output mode for special 16x8bit(total 128bit) data interface. 0: ACLKR output is normal. 1: the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8-bit mode (special purpose).	0
4	ACLKR64	R/W	ACLKR clock output mode for special 4 word output interface.ACLKRMASTER=1 mode only. 0: ACLKR output is normal 1: the number of ACLKR clock per fs is 64.	0
3	AFS384	R/W	Special Audio fs Sampling mode. 0: Audio fs Sampling mode is normal 256xfs if AIN5=0. 1: Audio fs Sampling mode is 384xfs mode.	0
2	AIN5MD	R/W	Audio Input process mode. 0: AIN1/AIN2/AIN3/AIN4 4 Audio input only process. This mode is 256xfs if AFS384=0.In this mode, AIN5 input is not processed. 1: AIN1/AIN2/AIN3/AIN4/AIN5 5 Audio input process. This mode is 320xfs Mode if AFS384=0.	0
1-0	Reserved	R		0h

0X8A – WHITE PEAK THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	D8

0X8B– CLAMP LEVEL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0X8C– SYNC AMPLITUDE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0X8D – SYNC MISS COUNT REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR mode detection threshold.	4

0X8E – WD1 CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP 960	R/W	These bits set the clamping position from the PLL sync edge in 960H WD1 video decoder.	36h

0X8F – VERTICAL CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = short 0 = normal	0

0X90 – VERTICAL CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	BSHT	R/W	Burst PLL center frequency control.	0
4-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0X91 – COLOR KILLER LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

0X92 – COMB FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HTL[3]	R/W	0 = adaptive mode 1 = fixed comb	0
6-4	HTL[2:0]	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0X93 – VSAVE1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	Reserved	R/W		3
3	PD_BIAS1	R/W	VIN1/VIN2/VIN3/VIN4 Video ADC PD_BIAS.	0
2-0	VSAVE1	R/W	VIN1/VIN2/VIN3/VIN4 Video ADC power save control. 0: Highest power 7: Lowest power	6

0X94 – MISCELLANEOUS CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HPLC	R/W	Reserved for internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	Reserved	R/W		0
2	BYPASS	R/W	It controls the standard detection and should be set to ‘1’ in normal use.	1
1-0	Reserved	R/W		0

0X95 – LOOP CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0X96 – MISCELLANEOUS CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X97 – CLAMP MODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	FRM	R/W	Free run mode control 0 = Auto, 2 = default to 60Hz, 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None, 1 = smallest, 2 = small, 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top, 1 = Auto, 2 = Pedestal, 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0X98 – HSLOWCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HSBEGIN[3:0]	R/W	HSYNC Start position Control Bit3-0.	0
3-0	HSEND[3:0]	R/W	HSYNC End position Control Bit3-0.	0

0X99 – HSBEGIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSBEGIN[11:4]	R/W	HSYNC Start position Control Bit11-4.	13h

0X9A – HSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSEND[11:4]	R/W	HSYNC End position Control Bit11-4.	1Fh

0X9B – OVSDLY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	OVSDLY	R/W	VSYNC Start position. Control H position on VSYNC start.	44h

0X9C – OVSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	OFDLY	R/W	FIELD output delay. 0h : 0H line delay FIELD output.Internal fld direct output mode. 1h-7h : 1H-7H line delay FIELD output.	2
3	VSMODE	R/W	1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0X9E – NOVID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDELAYMD	R/W	0 : normal VDELAY mode. 1 : Optional VDELAY mode.	0
6	FC27	R/W	1 : normal ITU-R656 operation 0 : Reserved	1
5-4	CHID_MD	R/W	Select the Channel ID format for time-multiplexed output 0h : No channel ID (default) 1h : CHID with the specific ITU-R BT.656 sync Code 2h : CHID with the specific horizontal blanking code 3h : CHID with the specific ITU-R BT.656 sync & horizontal blanking code	0
3	NOVID_656	R/W	0 : Normal ITU-R BT.656 SA/EAV(default) 1 : AN optional set of ITU-R BT.656 SAV/EAV code for No-video status	0
2	EAVSWAP	R/W	1 : EAV-SAV code is swapped.(special purpose only) 0 : EAV-SAV code is not swapped(standard 656 output mode)	0
1	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code. 1 : Standard ITU-R656 code format.(It's also VIP task-A code format.) 0 : Old VIP task-B code format.	1
0	NTSC656	R/W	1 : Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0 : Number of Even Field Video output line is same as the number of Odd field Video output line.	0

0X9F – CLOCK OUTPUT DELAY CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLKNO_DEL	R/W	Control the clock delay of CLKNO pin. 0h/1h/3h/7h/Fh values are effective. 0h : no delay. 1h : about 0.9ns more delay, 3h : about 2ns more delay, 7h : about 3ns more delay, Fh : about 4ns more delay	0h
3-0	CLKPO_DEL	R/W	Control the clock delay of CLKPO pin. 0h/1h/3h/7h/Fh values are effective. 0h : no delay. 1h : about 0.9ns more delay, 3h : about 2ns more delay, 7h : about 3ns more delay, Fh : about 4ns more delay	0h

0XA8 – HFLT12

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT2	R/W	Reserved for test purpose.	0
3-0	HFLT1	R/W	Reserved for test purpose.	0

0XA9 – HFLT34

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT4	R/W	Reserved for test purpose.	0
3-0	HFLT3	R/W	Reserved for test purpose.	0

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0XAF – VERTICAL PEAKING LEVEL CONTROL 12

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP2	R/W	Select VIN2 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP1	R/W	Select VIN1 Video Vertical peaking level. (*) 0 : none. 7 : highest	0

*Note: VSHP must be set to '0' for WD1 mode.

0XB0 – VERTICAL PEAKING LEVEL CONTROL 34

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP4	R/W	Select VIN4 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP3	R/W	Select VIN3 Video Vertical peaking level. (*) 0 : none. 7 : highest	0

*Note: VSHP must be set to '0' for WD1 mode.

0XB1 – TESTVNUM

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R/W		0
4	TMPPOE	R/W	0 : normal MPP4 function mode. 1 : MPP4 pin output one of legacy MPP1-8 signals. TESTVNUM register select one of mpp1-8 to be output on MPP4 pin. TESTVNUM=0 : MPP1 output. TESTVNUM=1 : MPP2 output. TESTVNUM=2 : MPP3 output. TESTVNUM=3 : MPP4 output. TESTVNUM=4 : MPP5 output. TESTVNUM=5 : MPP6 output. TESTVNUM=6 : MPP7 output. TESTVNUM=7 : MPP8 output.	0
3	CLPOE	R/W	0 : normal mode. 1 : Test purpose only.This is video clamp control signal output purpose.MPP1-8 pins output following clamp control signal. n=1,2,3,4,5,6,7,8. MPP4=CLMPDNXn, MPP3 =CLMPUPXn MPP2=CLMPDNn, MPP1=CLMPUPn When TESTVNUM=0,VIN1 video clamp control signal output. When TESTVNUM=1,VIN2 video clamp control signal output. When TESTVNUM=2,VIN3 video clamp control signal output. When TESTVNUM=3,VIN4 video clamp control signal output. When TESTVNUM=4,VIN5 video clamp control signal output. When TESTVNUM=5,VIN6 video clamp control signal output. When TESTVNUM=6,VIN7 video clamp control signal output. When TESTVNUM=7,VIN8 video clamp control signal output.	0
2-0	TESTVNUM	R/W	Test purpose only. See CLPOE and TMPPOE description.	0

0XB2 – VDLOSS OUTPUT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSSOE8	R/W	0 : not output VDLOSS8 on MPP8 signal path (default). 1 : VIN8 Video Decoder VDLOSS8 output on MPP8 signal path.	0
6	VDLOSSOE7	R/W	0 : not output VDLOSS7 on MPP7 signal path (default). 1 : VIN7 Video Decoder VDLOSS7 output on MPP7 signal path.	0
5	VDLOSSOE6	R/W	0 : not output VDLOSS6 on MPP6 signal path (default). 1 : VIN6 Video Decoder VDLOSS6 output on MPP6 signal path.	0
4	VDLOSSOE5	R/W	0 : not output VDLOSS5 on MPP5 signal path (default). 1 : VIN5 Video Decoder VDLOSS5 output on MPP5 signal path.	0
3	VDLOSSOE4	R/W	0 : not output VDLOSS4 on MPP4 signal path (default). 1 : VIN4 Video Decoder VDLOSS4 output on MPP4 signal path.	0
2	VDLOSSOE3	R/W	0 : not output VDLOSS3 on MPP3 signal path (default). 1 : VIN3 Video Decoder VDLOSS3 output on MPP3 signal path.	0
1	VDLOSSOE2	R/W	0 : not output VDLOSS2 on MPP2 signal path (default). 1 : VIN2 Video Decoder VDLOSS2 output on MPP2 signal path.	0
0	VDLOSSOE1	R/W	0 : not output VDLOSS1 on MPP1 signal path (default). 1 : VIN1 Video Decoder VDLOSS1 output on MPP1 signal path.	0

0XB3 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AADC4OFS[9:8]	R/W	AIN4 Digital ADC input data offset control bit9-8.	0h
5-4	AADC3OFS[9:8]	R/W	AIN3 Digital ADC input data offset control bit9-8.	0h
3-2	AADC2OFS[9:8]	R/W	AIN2 Digital ADC input data offset control bit9-8.	0h
1-0	AADC1OFS[9:8]	R/W	AIN1 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0XB4 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC1OFS[7:0]	R/W	AIN1 Digital ADC input data offset control bit7-0.	00h

0XB5 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC2OFS[7:0]	R/W	AIN2 Digital ADC input data offset control bit7-0.	00h

0XB6 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC3OFS[7:0]	R/W	AIN3 Digital ADC input data offset control bit7-0.	00h

0XB7 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC4OFS[7:0]	R/W	AIN4 Digital ADC input data offset control bit7-0.	00h

0X75 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		0h
1-0	AADC51OFS[9:8]	R/W	AIN_AUX1(AIN51) Digital ADC input data offset control bit9-8.	0h
Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS. AUDnADC is 2's formatted Analog Audio ADC output. AADCnOFS is adjusted offset value by 2's format.				

0X76 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC51OFS[7:0]	R/W	AIN_AUX1(AIN51)Digital ADC input data offset control bit7-0.	00h

0XB8 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AUD4ADC[9:8]	R	Bit9-8 of AIN4 Analog Audio ADC Digital Output Value by 2's format.	X
5-4	AUD3ADC[9:8]	R	Bit9-8 of AIN3 Analog Audio ADC Digital Output Value by 2's format.	X
3-2	AUD2ADC[9:8]	R	Bit9-8 of AIN2 Analog Audio ADC Digital Output Value by 2's format.	X
1-0	AUD1ADC[9:8]	R	Bit9-8 of AIN1 Analog Audio ADC Digital Output Value by 2's format.	X

0XB9 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD1ADC[7:0]	R	Bit7-0 of AIN1 Analog Audio ADC Digital Output Value by 2's format.	X

0XBA – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD2ADC[7:0]	R	Bit7-0 of AIN2 Analog Audio ADC Digital Output Value by 2's format.	X

0XBB – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD3ADC[7:0]	R	Bit7-0 of AIN3 Analog Audio ADC Digital Output Value by 2's format..	X

0XBC – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD4ADC[7:0]	R	Bit7-0 of AIN4 Analog Audio ADC Digital Output Value by 2's format.	X

0X77 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	AUD51ADC[9:8]	R	Bit9-8 of AIN_AUX1(AIN51) Analog Audio ADC Digital Output Value by 2's format.	X

0X78 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD51ADC[7:0]	R	Bit7-0 of AIN_AUX1(AIN51) Analog Audio ADC Digital Output Value by 2's format.	X

0XBD – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	ADJAADC4[9:8]	R	Bit9-8 of AIN4 adjusted Audio ADC Digital Input Data Value by 2's format.	X
5-4	ADJAADC3[9:8]	R	Bit9-8 of AIN3 adjusted Audio ADC Digital Input Data Value by 2's format.	X
3-2	ADJAADC2[9:8]	R	Bit9-8 of AIN2 adjusted Audio ADC Digital Input Data Value by 2's format.	X
1-0	ADJAADC1[9:8]	R	Bit9-8 of AIN1 adjusted Audio ADC Digital Input Data Value by 2's format.	X

The value shows the first input data in front of Digital Audio Decimation Filtering process.

0XBE – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC1[7:0]	R	Bit7-0 of AIN1 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XBF – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC2[7:0]	R	Bit7-0 of AIN2 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC0 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC3[7:0]	R	Bit7-0 of AIN3 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC1 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC4[7:0]	R	Bit7-0 of AIN4 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X79 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ADJAADC51[9:8]	R	Bit9-8 of AIN_AUX1(AIN51) adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X7A – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC51[7:0]	R	Bit7-0 of AIN_AUX1(AIN51) adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC8 – MPP OUTPUT MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GPP_VAL2	R/W	Write value select the general purpose value through the MPP2 output. Read value shows MPP2 input status. 0 : “0” value, 1 : “1” value	0
6-4	MPP_MODE2	R/W	Select the output mode for MPP2. Followings show the status when POLMPP2 register is set to 0. If POLMPP2 register is set to 1, following values have inversed status. 0 : Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7:GPP_VAL.Same as GPP_VAL2 register value. If VDLOSSOE2 register is set to “1”, vdloss2 signal is output to MPP2 and these MPP_MODE2 function is not effective.	7h
3	GPP_VAL1	R/W	Write value select the general purpose value through the MPP1 output. Read value shows MPP1 input status. 0 : “0” value, 1 : “1” value	0
2-0	MPP_MODE1	R/W	Select the output mode for MPP1. Followings show the status when POLMPP1 register is set to 0. If each POLMPP1 register is set to 1, following values have inversed status. 0 : Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7 : GPP_VAL.Same as GPP_VAL1 register value. If VDLOSSOE1 register is set to “1”, vdloss1 signal is output to MPP1 and these MPP_MODE1 function is not effective.	7h

0XC9 – MPP PIN OUTPUT MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GPP_VAL4	R/W	Write value select the general purpose value through the MPP4 output. Read value shows MPP4 input status. 0 : “0” value, 1 : “1” value	0
6-4	MPP_MODE4	R/W	Select the output mode for MPP4. Followings show the status when POLMPP4 register is set to 0. If POLMPP4 register is set to 1, following values have inversed status. 0 : Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7 : GPP_VAL.Same as GPP_VAL4 register value. If VDLOSSOE4 register is set to “1”, vdloss4 signal is output to MPP4 and these MPP_MODE4 function is not effective.	7h
3	GPP_VAL3	R/W	Write value select the general purpose value through the MPP3 output. Read value shows MPP3 input status. 0 : “0” value, 1 : “1” value	0
2-0	MPP_MODE3	R/W	Select the output mode for MPP3. Followings show the status when POLMPP3 register is set to 0. If each POLMPP3 register is set to 1, following values have inversed status. 0:Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7 : GPP_VAL.Same as GPP_VAL3 register value. If VDLOSSOE3 register is set to “1”, vdloss3 signal is output to MPP3 and these MPP_MODE3 function is not effective.	7h

0XCB –POLMPP

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	POLMPP8	R/W	Select MPP8 output polarity. 0 : normal, 1 : inverse polarity.	0
6	POLMPP7	R/W	Select MPP7 output polarity. 0 : normal, 1 : inverse polarity.	0
5	POLMPP6	R/W	Select MPP6 output polarity. 0 : normal, 1 : inverse polarity.	0
4	POLMPP5	R/W	Select MPP5 output polarity. 0 : normal, 1 : inverse polarity.	0
3	POLMPP4	R/W	Select MPP4 output polarity. 0 : normal, 1 : inverse polarity.	0
2	POLMPP3	R/W	Select MPP3 output polarity. 0 : normal, 1 : inverse polarity.	0
1	POLMPP2	R/W	Select MPP2 output polarity. 0 : normal, 1 : inverse polarity.	0
0	POLMPP1	R/W	Select MPP1 output polarity. 0 : normal, 1 : inverse polarity.	0

0XCC – H960EN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	H960EN8	R/W	1 : VIN8 video decoder is in 36MHz WD1 mode. 0 : VIN8 video decoder is in 27MHz D1 mode.	0
6	H960EN7	R/W	1 : VIN7 video decoder is in 36MHz WD1 mode. 0 : VIN7 video decoder is in 27MHz D1 mode.	0
5	H960EN6	R/W	1 : VIN6 video decoder is in 36MHz WD1 mode. 0 : VIN6 video decoder is in 27MHz D1 mode.	0
4	H960EN5	R/W	1 : VIN5 video decoder is in 36MHz WD1 mode. 0 : VIN5 video decoder is in 27MHz D1 mode.	0
3	H960EN4	R/W	1 : VIN4 video decoder is in 36MHz WD1 mode. 0 : VIN4 video decoder is in 27MHz D1 mode.	0
2	H960EN3	R/W	1 : VIN3 video decoder is in 36MHz WD1 mode. 0 : VIN3 video decoder is in 27MHz D1 mode.	0
1	H960EN2	R/W	1 : VIN2 video decoder is in 36MHz WD1 mode. 0 : VIN2 video decoder is in 27MHz D1 mode.	0
0	H960EN1	R/W	1 : VIN1 video decoder is in 36MHz WD1 mode. 0 : VIN1 video decoder is in 27MHz D1 mode.	0

0XCD – O36M

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	O36M8	R/W	0 : VIN8 video decoder output 27MHz video data. 1 : VIN8 video decoder output 36MHz video data.	0
6	O36M7	R/W	0 : VIN7 video decoder output 27MHz video data. 1 : VIN7 video decoder output 36MHz video data.	0
5	O36M6	R/W	0 : VIN6 video decoder output 27MHz video data. 1 : VIN6 video decoder output 36MHz video data.	0
4	O36M5	R/W	0 : VIN5 video decoder output 27MHz video data. 1 : VIN5 video decoder output 36MHz video data.	0
3	O36M4	R/W	0 : VIN4 video decoder output 27MHz video data. 1 : VIN4 video decoder output 36MHz video data.	0
2	O36M3	R/W	0 : VIN3 video decoder output 27MHz video data. 1 : VIN3 video decoder output 36MHz video data.	0
1	O36M2	R/W	0 : VIN2 video decoder output 27MHz video data. 1 : VIN2 video decoder output 36MHz video data.	0
0	O36M1	R/W	0 : VIN1 video decoder output 27MHz video data. 1 : VIN1 video decoder output 36MHz video data.	0

0XCE – ANALOG POWER DOWN CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AAUTOMUTE	R/W	1 : When input Analog data is less than ADET_TH level, output PCM data will be 0x0000(0x00).Audio DAC data input is 0x200. 0 : No effect	0
6	Reserved	R/W		0
5	A_DAC_PWDN	R/W	Power down the audio DAC. 0 : Normal operation 1 : Power down	0
4	A_ADC_PWDN_1	R/W	Power down AIN1/AIN2/AIN3/AIN4/AIN51 audio ADC. 0 : Normal operation 1 : Power down	0
3	VADC_PWDN[3]	R/W	Power down VIN4 video ADC. 0 : Normal operation 1 : Power down	0
2	VADC_PWDN[2]	R/W	Power down VIN3 video ADC. 0 : Normal operation 1 : Power down	0
1	VADC_PWDN[1]	R/W	Power down VIN2 video ADC. 0 : Normal operation 1 : Power down	0
0	VADC_PWDN[0]	R/W	Power down VIN1 video ADC. 0 : Normal operation 1 : Power down	0

0XCF – SERIAL MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	SMD	R/W	Set up cascade Audio Serial mode. When SMD=2hex or 3hex, ALINKO pin output cascaded audio serial data. When SMD=0hex, ALINKO pin output is tri-state. 00 : No Serial mode. ALINKO pin is tri-state output. 10 : ALINKO pin is Serial out pin. ALINKI pin is Serial input pin.	0h
5-0	Reserved	R/W		0h

0XD0, 0XD1, 0X7F - ANALOG AUDIO INPUT GAIN

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD0	7-4	AIGAIN2	R/W	Select the amplifier's gain for each analog audio input AIN1/2/3/4/51.AIN51=AIN_AUX1. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	6h
0xD1		AIGAIN4	R/W		
0x7F		AIGAIN51	R/W		
0xD0	3-0	AIGAIN1	R/W		6h
0xD1		AIGAIN3	R/W		
0x7F		MIXRATIO51	R/W	Audio input AIN51 ratio value for audio mixing. AIN51=AIN_AUX1.	0h

0XD2 – NUMBER OF AUDIO TO BE RECORDED

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	M_RLSWAP	R/W	Define the sequence of mixing and playback audio data on the ADATM pin. If RM_SYNC=0 : I2S format, 0 : Mixing audio on position 0 and playback audio on position 8 1 : Playback audio on position 0 and mixing audio on position 8 If RM_SYNC=1 : DSP format, / 0 : Mixing audio on position 0 and playback audio on position 1 1 : Playback audio on position 0 and mixing audio on position 1	0
6	RM_SYNC	R/W	Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin. 0 : I2S format 1 : DSP format	0
5-4	RM_PBSEL	R/W	Select the output PlayBackIn data for the ADATM pin. 0 First Stage PalyBackIn audio 1 Second Stage PalyBackIn audio 2 Third Stage PalyBackIn audio 3 Last Stage PalyBackIn audio	0h
3-2	R_ADATM	R/W	Select the output mode for the ADATM pin. 0 : Digital serial data of mixing audio 1 : Digital serial data of ADATR format record audio 2 : Digital serial data of ADATM format record audio	0h
1-0	R_MULTCH	R/W	Define the number of audio for record on the ADATR pin. 0 2 audios 1 4 audios 2 8 audios 3 16 audios Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. In addition, each output position data are selected by R_SEQ_0/R_SEQ_1/…/R_SEQ_F registers.	0h

0XD3, 0XD4, 0XD5, 0XD6, 0XD7, 0XD8, 0XD9, 0XDA – SEQUENCE OF AUDIO TO BE RECORDED

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD3	7-4	R_SEQ1	R/W	Define the sequence of record audio on the ADATR pin. Refer to Figure 15 and Table 5 for the detail of the R_SEQ_0 ~ R_SEQ_F. The default value of R_SEQ_0 is “0”, R_SEQ_1 is “1”, and R_SEQ_F is “F”. 0 AIN1 1 AIN2 2 AIN3 : : : : 14 AIN15 15 AIN16	1h
	3-0	R_SEQ0	R/W		0h
0xD4	7-4	R_SEQ3	R/W		3h
	3-0	R_SEQ2	R/W		2h
0xD5	7-4	R_SEQ5	R/W		5h
	3-0	R_SEQ4	R/W		4h
0xD6	7-4	R_SEQ7	R/W		7h
	3-0	R_SEQ6	R/W		6h
0xD7	7-4	R_SEQ9	R/W		9h
	3-0	R_SEQ8	R/W		8h
0xD8	7-4	R_SEQB	R/W		Bh
	3-0	R_SEQA	R/W		Ah
0xD9	7-4	R_SEQD	R/W		Dh
	3-0	R_SEQC	R/W		Ch
0xDA	7-4	R_SEQF	R/W		Fh
	3-0	R_SEQE	R/W		Eh

0XDB –MASTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ADACEN	R/W	Audio DAC Function mode 0 : Audio DAC function disable(test purpose only) 1 : Audio DAC function enable	1
6	AADCEN	R/W	Audio ADC Function mode 0 : Audio ADC function disable(test purpose only) 1 : Audio ADC function enable	1
5	PB_MASTER	R/W	Define the operation mode of the ACLKP and ASYNP pin for playback. 0 : All type I2S/DSP Slave mode(ACLKP and ASYNP is input) 1 : TW2964 type I2S/DSP Master mode (ACLKP and ASYNP is output)	0
4	PB_LRSEL	R/W	Select audio data to be used for playback input. If PB_SYNC=0 I2S format, 0 : 1st Left channel audio data(default), 1 : 1st Right channel audio data. If PB_SYNC=1 DSP format, 0 : 1st input audio data. 1 : 2nd input audio data	0
3	PB_SYNC	R/W	Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin. 0 : I2S format 1 : DSP format	0
2	RM_8BIT	R/W	Define output data format per one word unit on ADATR pin. 0 : 16bit one word unit output 1 : 8bit one word unit packed output	0
1	ASYNROEN	R/W	Define input/output mode on the ASYNR pin. 1 : ASYNR pin is input 0 : ASYNR pin is output	1
0	ACLKRMASTER	R/W	Define input/output mode on the ACLKR pin and set up audio system processing. 0 : ACLKR pin is input. External 256xfs or 320fs or 384xfs clock should be connected to ACLKR pin by AIN5MD/AFS384 setting. 1 : ACLKR pin is output. Internal ACKG generates audio system clock.	0

0XDC –U-LAW/A-LAW OUTPUT AND MIX MUTE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	LAWMD	R/W	Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin. 0 : PCM output 1 : SB(Signed MSB bit in PCM data is inverted) output 2 : u-Law output 3 : A-Law output	0
5	MIX_DERATIO_1	R/W	Disable the mixing ratio value for AIN1/AIN2/AIN3/AIN4/AIN51 audio. 0 : Apply individual mixing ratio value for each AIN1/AIN2/AIN3/AIN4/AIN51 audio 1 : Apply nominal value for all audio commonly	0
4-0	MIX_MUTE_1	R/W	Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0] : Audio input AIN1. MIX_MUTE[1] : Audio input AIN2. MIX_MUTE[2] : Audio input AIN3. MIX_MUTE[3] : Audio input AIN4. MIX_MUTE[4] : Playback audio input. 0 : Normal 1 : Muted.	10h

0XDD – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO2	R/W	Audio input AIN2 ratio value for audio mixing	0
3-0	MIX_RATIO1	R/W	Audio input AIN1 ratio value for audio mixing	0

0XDE – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO4	R/W	Audio input AIN4 ratio value for audio mixing	0
3-0	MIX_RATIO3	R/W	Audio input AIN3 ratio value for audio mixing	0

0XDF – ANALOG AUDIO OUTPUT GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	AOGAIN	R/W	Define the amplifier gain for analog audio output. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	8h
3-0	MIX_RATIOP	R/W	Playback audio input ratio value for audio mixing.	0h

0XE0 – MIX OUTPUT SELECTION 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6	AADCCKPOL	R/W	1 : Analog Audio ADC input clock polarity inverse. 0 : not inverse.	0
5	ADACCKPOL	R/W	1 : Analog Audio DAC input clock polarity inverse. 0 : not inverse.	0

0XE0 – MIX OUTPUT SELECTION 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4-0	MIX_OUTSEL	R/W	Define the final audio output for analog and digital mixing out. 0 Select record audio of channel 1 1 Select record audio of channel 2 2 Select record audio of channel 3 3 Select record audio of channel 4 4 Select record audio of channel 5 5 Select record audio of channel 6 6 Select record audio of channel 7 7 Select record audio of channel 8 8 Select record audio of channel 9 9 Select record audio of channel 10 10(Ah) Select record audio of channel 11 11(Bh) Select record audio of channel 12 12(Ch) Select record audio of channel 13 13(Dh) Select record audio of channel 14 14(Eh) Select record audio of channel 15 15(Fh) Select record audio of channel 16 16(10h) Select playback audio of the first stage chip PB1 17(11h) Reserved 18(12h) Select playback audio of the last stage chip PB3 19(13h) Reserved 20(14h) Select mixed audio 21(15h) Select record audio of channel AIN51 22(16h) Select record audio of channel AIN52 23(17h) Select record audio of channel AIN53 24(18h) Select record audio of channel AIN54 Others no sound. Default 1Fh.	1Fh

0XE1 – AUDIO DETECTION PERIOD AND AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AAMPMD	R/W	Define the audio detection method. 0 : Detect audio if absolute amplitude is greater than threshold(Test purpose only) 1 : Detect audio if differential amplitude is greater than threshold(recommended)	1
6-4	ADET_FILT	R/W	Select the filter for audio detection 0 : Wide LPF. . . . 7 : Narrow LPF	7
3	ADET_TH4[4]*	R/W	MSB bit of AIN4 threshold value for audio detection.	0
2	ADET_TH3[4]*	R/W	MSB bit of AIN3 threshold value for audio detection.	0
1	ADET_TH2[4]*	R/W	MSB bit of AIN2 threshold value for audio detection.	0
0	ADET_TH1[4]*	R/W	MSB bit of AIN1 threshold value for audio detection.	0

* Note:

ADET_TH :Define the threshold value for audio detection.

ADET_TH1: Audio input AIN1.
ADET_TH2: Audio input AIN2.
ADET_TH3: Audio input AIN3.
ADET_TH4: Audio input AIN4.
ADET_TH51: Audio input AIN51.AIN51=AIN_AUX1.

0:Low value (default)

. .

. .

31:High value

0XE2 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH2[3:0]	R/W	Bit3-0 of AIN2 threshold value for audio detection.	3h
3-0	ADET_TH1[3:0]	R/W	Bit3-0 of AIN1 threshold value for audio detection.	3h

0XE3 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH4[3:0]	R/W	Bit3-0 of AIN4 threshold value for audio detection.	3h
3-0	ADET_TH3[3:0]	R/W	Bit3-0 of AIN3 threshold value for audio detection.	3h

0XE4 – YDLY12

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	YDLY2	R/W	VIN2 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h
3	Reserved	R/W		
2-0	YDLY1	R/W	VIN1 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h

0XE5 – YDLY34

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	YDLY4	R/W	VIN4 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h
3	Reserved	R/W		
2-0	YDLY3	R/W	VIN3 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h

0XE7 – VIDEO OUTPUT MODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VD4MD	R/W	VD4[7:0] pin output mode selection 0: single video output 1: dual channel video output with x2 clock rate 2: quad channel video output with x4 clock rate 3: Reserved	1
5-4	VD3MD	R/W	VD3[7:0] pin output mode selection 0: single video output 1: dual channel video output with x2 clock rate 2: quad channel video output with x4 clock rate 3: Reserved	1
3-2	VD2MD	R/W	VD2[7:0] pin output mode selection 0: single video output 1: dual channel video output with x2 clock rate 2: quad channel video output with x4 clock rate 3: Reserved	1
1-0	VD1MD	R/W	VD1[7:0] pin output mode selection 0: single video output 1: dual channel video output with x2 clock rate 2: quad channel video output with x4 clock rate 3: Reserved	1

0XE8 – VD1 OUTPUT CH12 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD1O2SEL	R/W	CH2 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	1
3-0	VD1O1SEL	R/W	CH1 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	0

0XE9 – VD1 OUTPUT CH34 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD1O4SEL	R/W	CH4 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	3
3-0	VD1O3SEL	R/W	CH3 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	2

0XEA – VD2 OUTPUT CH12 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD2O2SEL	R/W	CH2 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	3
3-0	VD2O1SEL	R/W	CH1 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	2

0XEB – VD2 OUTPUT CH34 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD2O4SEL	R/W	CH4 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	5
3-0	VD2O3SEL	R/W	CH3 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	4

0XEC – VD3 OUTPUT CH12 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD3O2SEL	R/W	CH2 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	5
3-0	VD3O1SEL	R/W	CH1 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	4

0XED – VD3 OUTPUT CH34 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD3O4SEL	R/W	CH4 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	7
3-0	VD3O3SEL	R/W	CH3 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	6

0XEE – VD4 OUTPUT CH12 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD402SEL	R/W	CH2 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	7
3-0	VD401SEL	R/W	CH1 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	6

0XEF – VD4 OUTPUT CH34 SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VD404SEL	R/W	CH4 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	1
3-0	VD403SEL	R/W	CH3 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	0

0XF0 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKI[7:0]	R/W	ACKI[7:0], these bits control ACKI Clock Increment in ACKG block.	23h

0XF1 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKI[15:8]	R/W	ACKI[15:8], these bits control ACKI Clock Increment in ACKG block.	48h

0XF2 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0h
5-0	ACKI[21:16]	R/W	ACKI[21:16], these bits control ACKI Clock Increment in ACKG block.	07h

0XF3 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKN[7:0]	R/W	Reserved.	00h

0XF4 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKN[15:8]	R/W	Reserved.	01h

0XF5 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ACKN[17:16]	R/W	Reserved.	0h

0XF6 – SERIAL CLOCK DIVIDER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5-0	SDIV	R/W	These bits control SDIV Serial Clock Divider in ACKG block.	00h

0XF7 – LEFT/RIGHT CLOCK DIVIDER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5-0	LRDIV	R/W	Reserved.	20h

0XF8 – AUDIO CLOCK CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	APZ	R/W	These bits control Loop in ACKG block.	1
6-4	APG	R/W	These bits control Loop in ACKG block.	4h
3	Reserved	R/W		0
2	ACPL	R/W	These bits control Loop closed/open in ACKG block. 0: Loop closed(special purpose only) 1 :Loop open(normal function mode)	1
1	SRPH	R/W	Reserved.	0
0	LRPH	R/W	Reserved.	0

0XF9 – VIDEO MISCELLANEOUS FUNCTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LIM16	R/W	0 : Output ranges are limited to 2~254 1 : Output ranges are limited to 16~235 for Y and 16~239 for CbCr	0
6	PBREFEN	R/W	Audio ACKG Reference (refin) input select for test purpose. When ACPL=1, this function is no effect. 0 : ACKG has video VRST refin input selected by VRSTSEL register 1 : ACKG has audio ASYNP refin input	1
5	YCBCR422	R/W	Control YCbCr 4:2:2 output mode 0 : Normal 4:2:2 output mode 1 : Averaging 4:2:2 output mode	0
4	MPPMD	R/W	0 : MPP4 pin is PTZDAT output. MPP3 pin is PTZADD[2] output MPP2 pin is PTZADD[1] output MPP1 pin is PTZADD[0] output 1 : MPP4 pin is internal MPP4 signal output MPP3 pin is internal MPP3 signal output MPP2 pin is internal MPP2 signal output MPP1 pin is internal MPP1 signal output	0
3	VBI_FRAM	R/W	Test purpose only.	0
2	CNTL656	R/W	Select invalid data value. 0 : 0x80 and 0x10 code will be output as invalid data during active video line. 1 : 0x00 code will be output as invalid data during active video line.	0
1	CLKNF	R/W	CLKNO pin output mode. 0 : output one of 27MHz/54MHz/108MHz. 1 : output one of 36MHz/72MHz/144MHz.	0
0	CLKPF	R/W	CLKPO pin output mode. 0 : output one of 27MHz/54MHz/108MHz. 1 : output one of 36MHz/72MHz/144MHz.	0

0XFA – OUTPUT ENABLE CONTROL AND CLOCK OUTPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6	OE	R/W	Control the tri-state of output pin 0 : Outputs are Tri-state except clock output (CLKPO, CLKNO) pin 1 : Outputs are enabled	0
5	CLKNO_OEB	R/W	Control the tri-state of CLKNO pin 0 : Output is enabled (default) 1 : Output is Tri-state	0
4	CLKPO_OEB	R/W	Control the tri-state of CLKPO pin 0 : Output is enabled 1 : Output is Tri-state	0
3-2	CLKNO_MD	R/W	Control the clock frequency of CLKNO pin 0 : 27MHz or 36MHz clock output 1 : 54MHz or72MHz clock output 2 : 108MHz or 144MHz clock output 3 : always 0 value	0h
1-0	CLKPO_MD	R/W	Control the clock frequency of CLKPO pin 0 : 27MHz or 36MHz clock output 1 : 54MHz or 72MHz clock output 2 : 108MHz or 144MHz clock output 3 : always 0 value	0h

0XFB – CLOCK POLARITY CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLKNO_POL	R/W	Polarity inverse control on output CLKNO signal just before CLKNO pin. 0 : Not inversed. 1 : Polarity inverse.	0
6	CLKPO_POL	R/W	Polarity inverse control on output CLKPO signal just before CLKPO pin. 0 : Not inversed. 1 : Polarity inverse.	0
5	IRQENA	R/W	Enable/Disable the interrupt request through the IRQ pin. 0 : Disable 1 : Enable	0
4	IRQPOL	R/W	Select the polarity of interrupt request through the IRQ pin. 0 : Falling edge requests the interrupt and keeps its state until cleared 1 : Rising edge requests the interrupt and keeps its state until cleared	0
3-2	ADET_MODE	R/W	Define the polarity of state register and interrupt request for audio detection. 0 : No interrupt request by the audio detection 1 : Make the interrupt request rising only when the audio signal comes in 2 : Make the interrupt request falling only when the audio signal goes out 3 : Make the interrupt request rising and falling when the audio comes in and goes out	3
1-0	VDET_MODE	R/W	Define the polarity of state register and interrupt request for video detection. 0 : No interrupt request by the video detection 1 : Make the interrupt request rising only when the video signal comes in 2 : Make the interrupt request falling only when the video signal goes out 3 : Make the interrupt request rising and falling when the video comes in and goes out	3

0XFC – ENABLE VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET1_ENA	R/W	Enable state register updating and interrupt request of video and audio detection for each input. [0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4. 0 : Disable state register updating and interrupt request 1 : Enable state register updating and interrupt request	00h

0XFD – STATUS OF VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET1_STAT	R/W	State of Video and Audio detection. These bits are activated according VDET_MODE and ADET_MODE. [0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4. 0 Inactivated 1 Activated	00h

0XFE – DEVICE ID AND REVISION ID FLAG

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	DEV_ID[6:5]	R	Bit6-5 of Device ID. Together with 0xFF[7:3] indicate TW2968 product ID code. DEV_ID=7'h1E	0
5-3	Reserved	R		0
2-0	TEST	R/W	Test purpose only. This must be 0 in normal mode.	0

0XFF – DEVICE ID AND REVISION ID FLAG

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	DEV_ID[4:0]	R	Bit4-0 of Device ID.	1Eh
0	REV_ID	R	The revision number.	0h

Page1 Registers

The following shows Page1 registers. These registers can be accessed when 0X40 is 1.

0X00(VIN5)/0X10(VIN6)/0X20(VIN7)/0X30(VIN8) – VIDEO STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0X01(VIN5)/0X11(VIN6)/0X21(VIN7)/0X31(VIN8) – BRIGHTNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(VIN5)/0X12(VIN6)/0X22(VIN7)/0X32(VIN8) – CONTRAST CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h

0X03(VIN5)/0X13(VIN6)/0X23(VIN7)/0X33(VIN8) – SHARPNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0X04(VIN5)/0X14(VIN6)/0X24(VIN7)/0X34(VIN8) – CHROMA (U) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X05(VIN5)/0X15(VIN6)/0X25(VIN7)/0X35(VIN8) – CHROMA (V) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(VIN5)/0X16(VIN6)/0X26(VIN7)/0X36(VIN8) – HUE CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(VIN5)/0X17(VIN6)/0X27(VIN7)/0X37(VIN8) – CROPPING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08(VIN5)/0X18(VIN6)/0X28(VIN7)/0X38(VIN8) – VERTICAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(VIN5)/0X19(VIN6)/0X29(VIN7)/0X39(VIN8) – VERTICAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(VIN5)/0X1A(VIN6)/0X2A(VIN7)/0X3A(VIN8) – HORIZONTAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

0X0B(VIN5)/0X1B(VIN6)/0X2B(VIN7)/0X3B(VIN8) – HORIZONTAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0X0C(VIN5)/0X1C(VIN6)/0X2C(VIN7)/0X3C(VIN8) – MACROVISION DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(VIN5)/0X1D(VIN6)/0X2D(VIN7)/0X3D(VIN8) – CHIP STATUS II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(VIN5)/0X1E(VIN6)/0X2E(VIN7)/0X3E(VIN8) – STANDARD SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM(not supported) 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(VIN5)/0X1F(VIN6)/0X2F(VIN7)/0X3F(VIN8) – STANDARD RECOGNITION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0X56(VIN5/VIN6/VIN7/VIN8) – HASYNC

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HASYNC8	R/W	1: the length of EAV to SAV is set up and fixed by VIN8 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN8 HACTIVE registers.	0
6	HASYNC7	R/W	1: the length of EAV to SAV is set up and fixed by VIN7 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN7 HACTIVE registers.	0
5	HASYNC6	R/W	1: the length of EAV to SAV is set up and fixed by VIN6 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN6 HACTIVE registers.	0
4	HASYNC5	R/W	1: the length of EAV to SAV is set up and fixed by VIN5 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by VIN5 HACTIVE registers.	0
3	HBLEN8[8]	R/W	Bit8 of VIN8 HBLEN[8:0].Please see HBLEN description.	0
2	HBLEN7[8]	R/W	Bit8 of VIN7 HBLEN[8:0]. Please see HBLEN description.	0
1	HBLEN6[8]	R/W	Bit8 of VIN6 HBLEN[8:0]. Please see HBLEN description.	0
0	HBLEN5[8]	R/W	Bit8 of VIN5 HBLEN[8:0]. Please see HBLEN description.	0

0X57(VIN5)/0X58(VIN6)/0X59(VIN7)/0X5A(VIN8) – HBLEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HBLENn[7:0] n=5,6,7,8	R/W	These bits are effective when HASYNC bit is set to 1.These bits set up the length of EAV to SAV code when HASYNC bit is 1.Normal value is (Total pixel per line – HACTIVE) value.HBLENn[8] is 0 normally. HBLENn[8] is optional purpose only. 36MHz WD1 Vdeo Decoder mode. NTSC/PAL-M(60Hz): B8h(184dec)=1144-960 PAL/SECAM(50Hz): C0h(192dec)=1152-960 27MHz D1 Vdeo Decoder mode. NTSC/PAL-M(60Hz): 8Ah(138dec)=858-720 PAL/SECAM(50Hz): 90h(144dec)=864-720	90h

0X68(VIN5/VIN6/VIN7/VIN8) – HZOOM_HI

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HZOOM8 [9:8]	R/W	Bit9-8 of VIN8 HZOOM registers.	0
5-4	HZOOM7 [9:8]	R/W	Bit9-8 of VIN7 HZOOM registers.	0
3-2	HZOOM6 [9:8]	R.W	Bit9-8 of VIN6 HZOOM registers.	0
1-0	HZOOM5 [9:8]	R/W	Bit9-8 of VIN5 HZOOM registers.	0

0X69(VIN5)/0X6A(VIN6)/0X6B(VIN7)/0X6C(VIN8) – HZOOM_LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HZOOM [7:0]	R/W	Bit7-0 of Horizontal Zoom Up register.This register has Horizontal Zoom Up fcuntion together HZOOMn[9:8] by following equation. HZOOM[9:0] = 1024 x source H pixel number / output H pixel number. For example, source H pixel numer = 948 Output H pixel number = 960 HZOOM[9:0] = 1024 x 948 / 960 = 1011.2 = 3F3h. If HZOOM=000h is set up,No HZOOM(path through) output.	00h

0XA0(VIN5)/0XA1(VIN6)/0XA2(VIN7)/0XA3(VIN8) – NT50

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register Standard Selection.	0
6-4	VSTD	R/W	Reserved	0h
3-0	CVFMT	R/W	Reserved	8h

0XA4(VIN5)/0XA5(VIN6)/0XA6(VIN7)/0XA7(VIN8) – ID DETECTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0XAA(VIN5/VIN6/VIN7/VIN8) – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AGCEN8	R/W	Select Video AGC loop function on VIN8 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN8	0
6	AGCEN7	R/W	Select Video AGC loop function on VIN7 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN7	0
5	AGCEN6	R/W	Select Video AGC loop function on VIN6 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN6	0
4	AGCEN5	R/W	Select Video AGC loop function on VIN5 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN5	0
3	AGCGAIN8[8]	R/W	AGCGAIN8 MSB bit	0
2	AGCGAIN7[8]	R/W	AGCGAIN7 MSB bit	0
1	AGCGAIN6[8]	R/W	AGCGAIN6 MSB bit	0
0	AGCGAIN5[8]	R/W	AGCGAIN5 MSB bit	0

0XAB(VIN5)/0XAC(VIN6)/0XAD(VIN7)/0XAE(VIN8) – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN bit7-0.	F0h

0XC4(VIN5)/0XC5(VIN6)/0XC6(VIN7)/0XC7(VIN8) – H MONITOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator (Test purpose only)	X

0X54 – ASAVE2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	Reserved	R		00h
2-0	ASAVE2	R/W	AIN5/AIN6/AIN7/AIN8/AIN52 Audio ADC power save control. 7h : normal mode. Others : test purpose only.	7

0X55 – VIN5/6/7/8 VIDEO INPUT ANTI-ALIASING FILTER SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AAFLPF8	R/W	VIN8 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
5-4	AAFLPF7	R/W	VIN7 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
3-2	AAFLPF6	R/W	VIN6 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
1-0	AAFLPF5	R/W	VIN5 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0

0X5D – VIN6 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_6	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_6	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_6	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_6	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_6	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_6	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_6	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_6	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5E – VIN7 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_7	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_7	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_7	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_7	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_7	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_7	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_7	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_7	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5F – VIN8 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_8	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_8	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_8	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_8	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_8	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_8	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_8	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_8	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X73 – A52DET_ENA

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-1	Reserved	R	Reserved	00h
0	A52DET_ENA	R/W	Enable state register updating and interrupt request of audio AIN52 (AIN_AUX2 input in this chip) detection for each input. 0 : Disable state register updating and interrupt request 1 : Enable state register updating and interrupt request	0

0X74 – STATUS OF AUDIO 52 DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-1	Reserved	R		00h
0	A52DET_STATE	R	State of Audio AIN52(AIN_AUX2 input in this chip) detection. This bit is activated according ADET_MODE. 0 : Inactivated 1 : Activated	0

0X7E – MIX_MUTE_A52

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5	MIX_MUTE_A52	R/W	MIX_MUTE_A52: Audio input AIN52=AIN_AUX2 mute function control. 0:Normal 1:Muted	1
4-0	ADET_TH52[4:0]	R/W	AIN52=AIN_AUX2 threshold value for audio detection	03h

0X80 – SOFTWARE RESET CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	VDEC8RST	W	A 1 written to this bit resets the Video8 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC7RST	W	A 1 written to this bit resets the Video7 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
1	VDEC6RST	W	A 1 written to this bit resets the Video6 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC5RST	W	A 1 written to this bit resets the Video5 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0X93 – VSAVE2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	PD_BIAS2	R/W	VIN5/VIN6/VIN7/VIN8 Video ADC PD_BIAS.	0
2-0	VSAVE2	R/W	VIN5/VIN6/VIN7/VIN8 Video ADC power save control. 0: Highest power 7: Lowest power	6

0X96 – VIN5 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_5	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_5	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_5	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_5	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_5	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_5	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_5	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_5	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0XA8 – HFLT56

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT6	R/W	Reserved for test purpose.	0
3-0	HFLT5	R/W	Reserved for test purpose.	0

0XA8 – HFLT78

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT8	R/W	Reserved for test purpose.	0
3-0	HFLT7	R/W	Reserved for test purpose.	0

0XAF – VERTICAL PEAKING LEVEL CONTROL 5/6

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP6	R/W	Select VIN6 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP5	R/W	Select VIN5 Video Vertical peaking level. (*) 0 : none. 7 : highest	0

*Note: VSHP must be set to '0' for WD1 mode.

0XB0 – VERTICAL PEAKING LEVEL CONTROL 7/8

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP8	R/W	Select VIN8 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP7	R/W	Select VIN7 Video Vertical peaking level. (*) 0 : none. 7 : highest	0

*Note: VSHP must be set to '0' for WD1 mode.

0XB3 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AADC8OFS[9:8]	R/W	AIN8 Digital ADC input data offset control bit9-8.	0h
5-4	AADC7OFS[9:8]	R/W	AIN7 Digital ADC input data offset control bit9-8.	0h
3-2	AADC6OFS[9:8]	R/W	AIN6 Digital ADC input data offset control bit9-8.	0h
1-0	AADC5OFS[9:8]	R/W	AIN5 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0XB4 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC5OFS[7:0]	R/W	AIN5 Digital ADC input data offset control bit7-0.	00h

0XB5 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC6OFS[7:0]	R/W	AIN6 Digital ADC input data offset control bit7-0.	00h

0XB6 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC7OFS[7:0]	R/W	AIN7 Digital ADC input data offset control bit7-0.	00h

0XB7 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC8OFS[7:0]	R/W	AIN8 Digital ADC input data offset control bit7-0.	00h

0X75 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		0h
1-0	AADC52OFS[9:8]	R/W	AIN_AUX2(AIN52) Digital ADC input data offset control bit9-8.	0h
Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS. AUDnADC is 2's formatted Analog Audio ADC output. AADCnOFS is adjusted offset value by 2's format.				

0X76 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC52OFS[7:0]	R/W	AIN_AUX2(AIN52)Digital ADC input data offset control bit7-0.	00h

0XB8 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AUD8ADC[9:8]	R	Bit9-8 of AIN8 Analog Audio ADC Digital Output Value by 2's format.	X
5-4	AUD7ADC[9:8]	R	Bit9-8 of AIN7 Analog Audio ADC Digital Output Value by 2's format.	X
3-2	AUD6ADC[9:8]	R	Bit9-8 of AIN6 Analog Audio ADC Digital Output Value by 2's format.	X
1-0	AUD5ADC[9:8]	R	Bit9-8 of AIN5 Analog Audio ADC Digital Output Value by 2's format.	X

0XB9 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD5ADC[7:0]	R	Bit7-0 of AIN5 Analog Audio ADC Digital Output Value by 2's format.	X

0XBA – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD6ADC[7:0]	R	Bit7-0 of AIN6 Analog Audio ADC Digital Output Value by 2's format.	X

0XBB – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD7ADC[7:0]	R	Bit7-0 of AIN7 Analog Audio ADC Digital Output Value by 2's format..	X

0XBC – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD8ADC[7:0]	R	Bit7-0 of AIN8 Analog Audio ADC Digital Output Value by 2's format.	X

0X77 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	AUD52ADC[9:8]	R	Bit9-8 of AIN_AUX2(AIN52) Analog Audio ADC Digital Output Value by 2's format.	X

0X78 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD52ADC[7:0]	R	Bit7-0 of AIN_AUX2(AIN52) Analog Audio ADC Digital Output Value by 2's format.	X

0XBD – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	ADJAADC8[9:8]	R	Bit9-8 of AIN8 adjusted Audio ADC Digital Input Data Value by 2's format.	X
5-4	ADJAADC7[9:8]	R	Bit9-8 of AIN7 adjusted Audio ADC Digital Input Data Value by 2's format.	X
3-2	ADJAADC6[9:8]	R	Bit9-8 of AIN6 adjusted Audio ADC Digital Input Data Value by 2's format.	X
1-0	ADJAADC5[9:8]	R	Bit9-8 of AIN5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

The value shows the first input data in front of Digital Audio Decimation Filtering process.

0XBE – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC5[7:0]	R	Bit7-0 of AIN5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XBF – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC6[7:0]	R	Bit7-0 of AIN6 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC0 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC7[7:0]	R	Bit7-0 of AIN7 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC1 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC8[7:0]	R	Bit7-0 of AIN8 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X79 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ADJAADC52[9:8]	R	Bit9-8 of AIN_AUX2(AIN52) adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X7A – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC52[7:0]	R	Bit7-0 of AIN_AUX2(AIN52) adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC8 – MPP OUTPUT MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GPP_VAL6	R/W	Write value select the general purpose value through the MPP6 output. Read value shows MPP6 input status. 0 : “0” value, 1 : “1” value	0
6-4	MPP_MODE6	R/W	Select the output mode for MPP6. Followings show the status when POLMPP6 register is set to 0. If POLMPP6 register is set to 1, following values have inversed status. 0 : Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7:GPP_VAL.Same as GPP_VAL2 register value. If VDLOSSOE6 register is set to “1”, vdloss6 signal is output to MPP6 and these MPP_MODE6 function is not effective.	7h
3	GPP_VAL5	R/W	Write value select the general purpose value through the MPP5 output. Read value shows MPP5 input status. 0 : “0” value, 1 : “1” value	0
2-0	MPP_MODE5	R/W	Select the output mode for MPP5. Followings show the status when POLMPP5 register is set to 0. If each POLMPP5 register is set to 1, following values have inversed status. 0 : Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7 : GPP_VAL.Same as GPP_VAL1 register value. If VDLOSSOE5 register is set to “1”, vdloss5 signal is output to MPP5 and these MPP_MODE5 function is not effective.	7h

0XC9 – MPP PIN OUTPUT MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GPP_VAL8	R/W	Write value select the general purpose value through the MPP8 output. Read value shows MPP8 input status. 0 : “0” value, 1 : “1” value	0
6-4	MPP_MODE8	R/W	Select the output mode for MPP8. Followings show the status when POLMPP8 register is set to 0. If POLMPP8 register is set to 1, following values have inversed status. 0 : Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7 : GPP_VAL.Same as GPP_VAL4 register value. If VDLOSSOE8 register is set to “1”, vdloss8 signal is output to MPP8 and these MPP_MODE8 function is not effective.	7h
3	GPP_VAL7	R/W	Write value select the general purpose value through the MPP7 output. Read value shows MPP7 input status. 0 : “0” value, 1 : “1” value	0
2-0	MPP_MODE7	R/W	Select the output mode for MPP7. Followings show the status when POLMPP7 register is set to 0. If each POLMPP7 register is set to 1, following values have inversed status. 0:Horizontal sync output. Low is H-sync active. 1 : Vertical sync output. Low is V-sync active. 2 : Field flag output. Low is field1 (Odd), High is field2 (Even). 3 : Horizontal active signal output. High is H-active. 4 : Vertical active & horizontal active signal output. High is VH-active. 5 : 27MHz clock output.This cloock is made from XTI source. 6 : Vertical sync & horizontal sync signal output. Low is sync active. 7 : GPP_VAL.Same as GPP_VAL3 register value. If VDLOSSOE7 register is set to “1”, vdloss7 signal is output to MPP7 and these MPP_MODE7 function is not effective.	7h

0XCE – ANALOG POWER DOWN CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0
4	A_ADC_PWDN_2	R/W	Power down AIN5/AIN6/AIN7/AIN8/AIN52 audio ADC. 0 : Normal operation 1 : Power down	
3	VADC_PWDN[7]	R/W	Power down VIN8 video ADC. 0 : Normal operation 1 : Power down	0
2	VADC_PWDN[6]	R/W	Power down VIN7 video ADC. 0 : Normal operation 1 : Power down	0
1	VADC_PWDN[5]	R/W	Power down VIN6 video ADC. 0 : Normal operation 1 : Power down	0
0	VADC_PWDN[4]	R/W	Power down VIN5 video ADC. 0 : Normal operation 1 : Power down	0

0XD0, 0XD1, 0X7F - ANALOG AUDIO INPUT GAIN

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD0	7-4	AIGAIN6	R/W	Select the amplifier's gain for each analog audio input AIN5/6/7/8/51.AIN53=AIN_AUX2. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	6h
0xD1		AIGAIN8	R/W		
0x7F		AIGAIN52	R/W		
0xD0	3-0	AIGAIN5	R/W		6h
0xD1		AIGAIN7	R/W		
0x7F		MIXRATIO52	R/W	Audio input AIN52 ratio value for audio mixing. AIN52=AIN_AUX2.	0h

0XDC – MIX MUTE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5	MIX_DERATIO_2	R/W	Disable the mixing ratio value for AIN5/AIN6/AIN7/AIN8/AIN52 audio. 0 : Apply individual mixing ratio value for each AIN5/AIN6/AIN7/AIN8/AIN52 audio 1 : Apply nominal value for all audio commonly	0
4-0	MIX_MUTE_2	R/W	Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0] : Audio input AIN5. MIX_MUTE[1] : Audio input AIN6. MIX_MUTE[2] : Audio input AIN7. MIX_MUTE[3] : Audio input AIN8. MIX_MUTE[4] : Reserved for future use. 0 : Normal 1 : Muted.	10h

0XDD – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO6	R/W	Audio input AIN6 ratio value for audio mixing	0
3-0	MIX_RATIO5	R/W	Audio input AIN5 ratio value for audio mixing	0

0XDE – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO8	R/W	Audio input AIN8 ratio value for audio mixing	0
3-0	MIX_RATIO7	R/W	Audio input AIN7 ratio value for audio mixing	0

0XE1 – AUDIO DETECTION PERIOD AND AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	ADET_TH8[4]*	R/W	MSB bit of AIN8 threshold value for audio detection.	0
2	ADET_TH7[4]*	R/W	MSB bit of AIN7 threshold value for audio detection.	0
1	ADET_TH6[4]*	R/W	MSB bit of AIN6 threshold value for audio detection.	0
0	ADET_TH5[4]*	R/W	MSB bit of AIN5 threshold value for audio detection.	0

* Note:

ADET_TH :Define the threshold value for audio detection.

ADET_TH5: Audio input AIN5.
ADET_TH6: Audio input AIN6.
ADET_TH7: Audio input AIN7.
ADET_TH8: Audio input AIN8.
ADET_TH52: Audio input AIN52.AIN52=AIN_AUX2.

0:Low value (default)

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. .

31:High value

0XE2 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH6[3:0]	R/W	Bit3-0 of AIN6 threshold value for audio detection.	3h
3-0	ADET_TH5[3:0]	R/W	Bit3-0 of AIN5 threshold value for audio detection.	3h

0XE3 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH8[3:0]	R/W	Bit3-0 of AIN8 threshold value for audio detection.	3h
3-0	ADET_TH7[3:0]	R/W	Bit3-0 of AIN7 threshold value for audio detection.	3h

0XE4 – YDLY56

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	YDLY6	R/W	VIN6 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h
3	Reserved	R/W		
2-0	YDLY5	R/W	VIN5 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h

0XE5 – YDLY78

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	YDLY8	R/W	VIN8 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h
3	Reserved	R/W		
2-0	YDLY7	R/W	VIN7 Video Decoder Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h

0XFC – ENABLE VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET2_ENA	R/W	Enable state register updating and interrupt request of video and audio detection for each input. [0] : Video input VIN5. [1] : Video input VIN6. [2] : Video input VIN7. [3] : Video input VIN8. [4] : Audio input AIN5. [5] : Audio input AIN6. [6] : Audio input AIN7. [7] : Audio input AIN8. 0 : Disable state register updating and interrupt request 1 : Enable state register updating and interrupt request	00h

0XFD – STATUS OF VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET2_STATE	R/W	State of Video and Audio detection. These bits are activated according VDET_MODE and ADET_MODE. [0] : Video input VIN5. [1] : Video input VIN6. [2] : Video input VIN7. [3] : Video input VIN8. [4] : Audio input AIN5. [5] : Audio input AIN6. [6] : Audio input AIN7. [7] : Audio input AIN8. 0 Inactivated 1 Activated	00h

Page2 Registers

Followings show page2 registers.These registers can be accessed when 0X40 is 2.

0X01 – COAX_CH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	COAX_LINE_NUM	R/W	Number of lines in a field with PTZ data. 0: 1 line, 1: 2 lines, 2: 3 lines, 3: 4 lines	0
5-4	COAX_FLD_MD	R/W	PTZ Tx field mode. 0: Both fields, 1: Even field, 2: Odd field, 3: N/A	0
3	COAX_TX_WEN	R/W	Done output polarity. 0: No inverse, 1: Inverse	0
2-0	COAX_CH	R/W	Define PTZ Tx channel. 0: Channel 1 ~ 7: Channel 8	0

0X02 – COAX_TX_EN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	COAX_VSTRT[9:8]	R/W	MSB of line number with PTZ data	0
5	Reserved	R/W		-
4	COAX_FLD_POL	R/W	Field polarity for PTZ Tx operation. 0: Normal, 1: Reverse	0
3	COAX_DEF_D	R/W	PTZ Tx data output pulse polarity, 0: High active, 1: Low active	0
2	COAX_TX_MODE	R/W	PTZ Tx operation mode. 0: Continuous transmitting data, 1: One time transmission (need to disable then enable pulse generation for next “one time” transmission.)	0
1	COAX_TX_EN	R/W	PTZ Tx pulse generation enable. 0: Disable, 1: Enable	0
0	Reserved	R		-

0X03 – COAX_VSTRT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_VSTRT[7:0]	R/W	Start line number with PTZ Tx data	00h

0X04 – COAX_DATAEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_DATALEN	R/W	Number of valid bits of PTZ data. Standard Pelco: 15x3=45d, Extended Pelco: 16x3=48d	00h

0X05 – COAX_BITCLK_HI

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_BITCLK[15:8]	R/W	Specify fundamental pulse width for start/stop bits and each data bits in 27MHz clock. 0 is prohibited.	00h

0X06 – COAX_BITCLK_LO

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_BITCLK[7:0]	R/W	Specify fundamental pulse width for start/stop bits and each data bits in 27MHz clock	1Bh

0X07 – COAX_HSTART_HI

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_HSTART[15:8]	R/W	Specify start position of PTZ Tx pulse in a line	0

0X08 – COAX_HSTART_LO

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_HSTART[7:0]	R/W	Specify start position of PTZ Tx pulse in a line	0

0X09 – COAX_L0_70

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[7:0]	R/W	PTZ Tx Line 0 data [7:0]	00h

0X0A – COAX_L0_158

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[15:8]	R/W	PTZ Tx Line 0 data [15:8]	0

0X0B – COAX_L0_2316

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[23:16]	R/W	PTZ Tx Line 0 data [23:16]	0

0X0C – COAX_L0_3124

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[31:24]	R/W	PTZ Tx Line 0 data [31:24]	0

0X0D – COAX_L0_3932

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[39:32]	R/W	PTZ Tx Line 0 data [39:32]	0

0X0E – COAX_L0_4740

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[47:40]	R/W	PTZ Tx Line 0 data [47:40]	0

0X0F – COAX_L0_5548

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[55:48]	R/W	PTZ Tx Line 0 data [55:48]	0

0X10 – COAX_L0_6356

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[63:56]	R/W	PTZ Tx Line 0 data [63:56]	0

0X11 – COAX_L0_7164

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[71:64]	R/W	PTZ Tx Line 0 data [71:64]	0

0X12 – COAX_L0_7972

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[79:72]	R/W	PTZ Tx Line 0 data [79:72]	0

0X13 – COAX_L0_8780

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[87:80]	R/W	PTZ Tx Line 0 data [87:80]	0

0X14 – COAX_L0_9588

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L0[95:88]	R/W	PTZ Tx Line 0 data [95:88]	0

0X15 – COAX_L1__70

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[7:0]	R/W	PTZ Tx Line 1 data [7:0]	00h

0X16 – COAX_L1_158

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[15:8]	R/W	PTZ Tx Line 1 data [15:8]	0

0X17 – COAX_L1_2316

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[23:16]	R/W	PTZ Tx Line 1 data [23:16]	0

0X18 – COAX_L1_3124

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[31:24]	R/W	PTZ Tx Line 1 data [31:24]	0

0X19 – COAX_L1_3932

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[39:32]	R/W	PTZ Tx Line 1 data [39:32]	0

0X1A - COAX_L1_4740

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[47:40]	R/W	PTZ Tx Line 1 data [47:40]	0

0X1B - COAX_L1_5548

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[55:48]	R/W	PTZ Tx Line 1 data [55:48]	0

0X1C – COAX_L1_6356

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[63:56]	R/W	PTZ Tx Line 1 data [63:56]	0

0X1D - COAX_L1_7164

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[71:64]	R/W	PTZ Tx Line 1 data [71:64]	0

0X1E - COAX_L1_7972

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[79:72]	R/W	PTZ Tx Line 1 data [79:72]	0

0X1F – COAX_L1_8780

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[87:80]	R/W	PTZ Tx Line 1 data [87:80]	0

0X20 – COAX_L1_9588

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L1[95:88]	R/W	PTZ Tx Line 1 data [95:88]	0

0X21 – COAX_L2_70

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[7:0]	R/W	PTZ Tx Line 2 data [7:0]	00h

0X22 – COAX_L2_158

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[15:8]	R/W	PTZ Tx Line 2 data [15:8]	0

0X23 – COAX_L2_2316

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[23:16]	R/W	PTZ Tx Line 2 data [23:16]	0

0X24 – COAX_L2_3124

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[31:24]	R/W	PTZ Tx Line 2 data [31:24]	0

0X25 – COAX_L2_3932

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[39:32]	R/W	PTZ Tx Line 2 data [39:32]	0

0X26 – COAX_L2_4740

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[47:40]	R/W	PTZ Tx Line 2 data [47:40]	0

0X27- COAX_L2_5548

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[55:48]	R/W	PTZ Tx Line 2 data [55:48]	0

0X28 – COAX_L2_6356

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[63:56]	R/W	PTZ Tx Line 2 data [63:56]	0

0X29 – COAX_L2_7164

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[71:64]	R/W	PTZ Tx Line 2 data [71:64]	0

0X2A – COAX_L2_7972

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[79:72]	R/W	PTZ Tx Line 2 data [79:72]	0

0X2B – COAX_L2_8780

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[87:80]	R/W	PTZ Tx Line 2 data [87:80]	0

0X2C – COAX_L2_9588

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L2[95:88]	R/W	PTZ Tx Line 2 data [95:88]	0

0X2D – COAX_L3_70

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[7:0]	R/W	PTZ Tx Line 3 data [7:0]	00h

0X2E – COAX_L3_158

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[15:8]	R/W	PTZ Tx Line 3 data [15:8]	0

0X2F – COAX_L3_2316

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[23:16]	R/W	PTZ Tx Line 3 data [23:16]	0

0X30 – COAX_L3_3124

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[31:24]	R/W	PTZ Tx Line 3 data [31:24]	0

0X31 – COAX_L3_3932

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[39:32]	R/W	PTZ Tx Line 3 data [39:32]	0

0X32 – COAX_L3_4740

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[47:40]	R/W	PTZ Tx Line 3 data [47:40]	0

0X33 – COAX_L3_5548

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[55:48]	R/W	PTZ Tx Line 3 data [55:48]	0

0X34 – COAX_L3_6356

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[63:56]	R/W	PTZ Tx Line 3 data [63:56]	0

0X35 – COAX_L3_7164

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[71:64]	R/W	PTZ Tx Line 3 data [71:64]	0

0X36 – COAX_L3_7972

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[79:72]	R/W	PTZ Tx Line 3 data [79:72]	0

0X37 – COAX_L3_8780

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[87:80]	R/W	PTZ Tx Line 3 data [87:80]	0

0X38 – COAX_L3_9588

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	COAX_L3[95:88]	R/W	PTZ Tx Line 3 data [95:88]	0

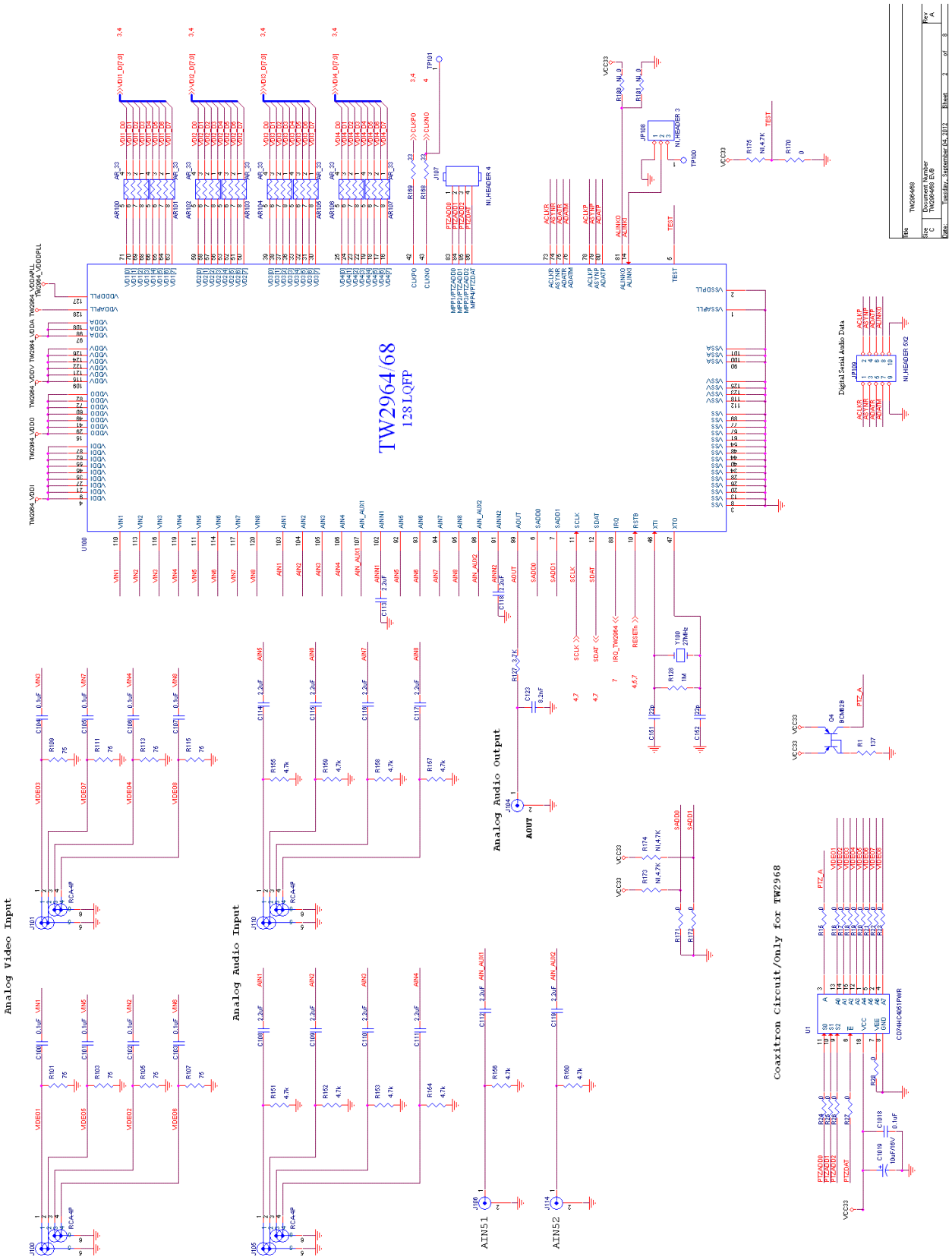
0X39 - IRQMD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IRQMD	R/W	IRQ Pin output mode. 0 : done signal interrupt only. 1 : audio det,video det interrupt only. 2 : all audio det,video det,done,field_o interrupt. 3 : field_o interrupt only.	1
5	FIELDDET_ENA	R/W	1 : field_o signal interrupt enable,0 : disable.	0
4	DONEDET_ENA	R/W	1 : done signal interrupt enable, 0 : disable	0
3-2	FIELDDET_MODE	R/W	Define state register and interrupt request forfield_o signal. 0 : No interrupt request by field_o signal. 1 : Make the interrupt request rising only when field_o signal changes 0 to 1. 2 : Make the interrupt request falling only when field_o signal changes 1 to 0. 3 : Make the interrupt request risign and falling when field_o signal changes 0 to 1 and 1 to 0.	3
1-0	DONEDET_MODE	R/W	Define state register and interrupt request for done signal. 0 : No interrupt request by done signal. 1 : Make the interrupt request rising only when done signal changes 0 to 1. 2 : Make the interrupt request falling only when done signal changes 1 to 0. 3 : Make the interrupt request risign and falling when done signal changes 0 to 1 and 1 to 0.	3

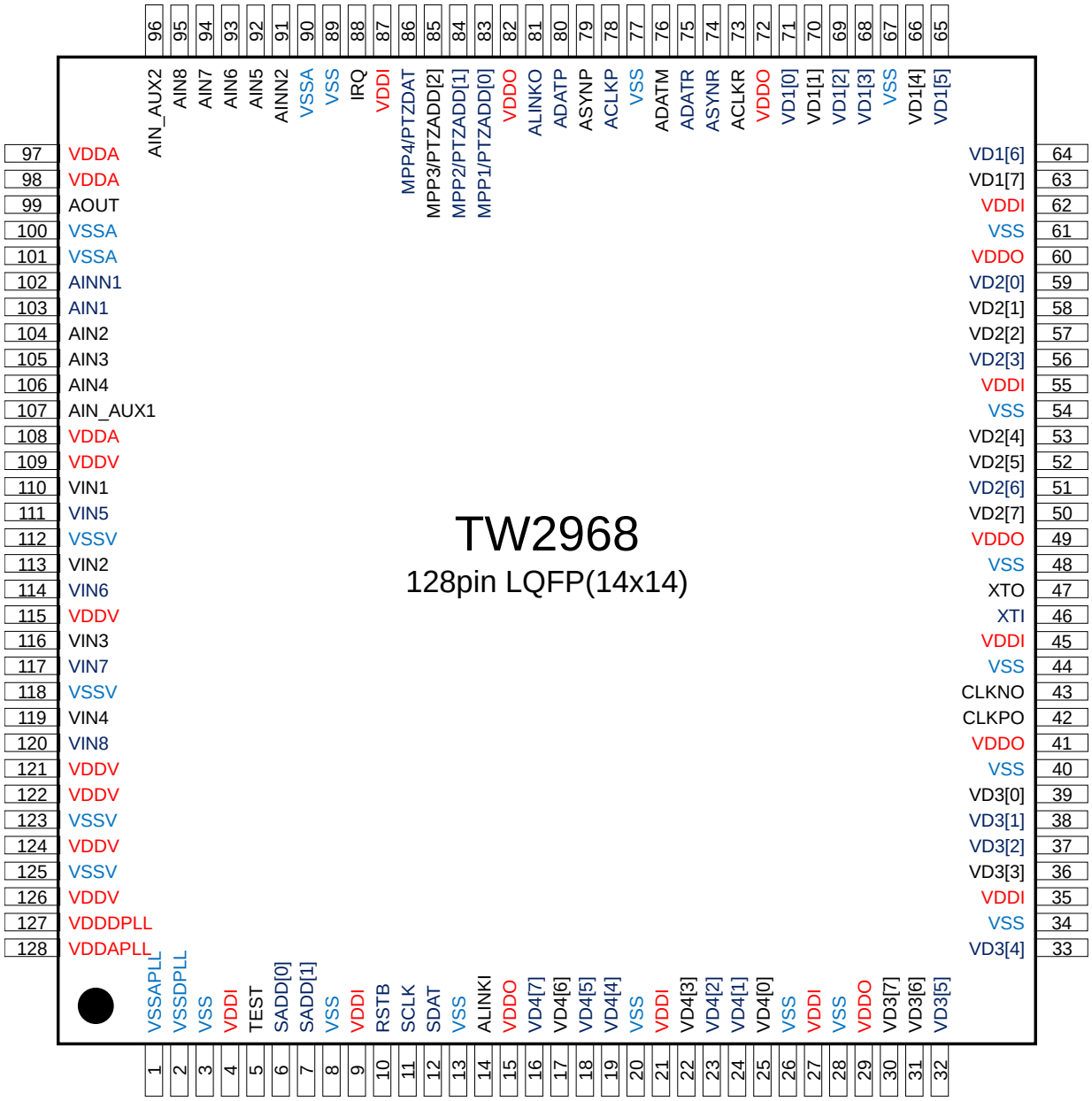
0X3A – COAX_STATE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		0
1	COAX_FLD_STAT	R	Status of currently selected (by COAX_CH) channel's field int register. When FIELDDET_MODE=1 or 3. 1 : ield_oint register is set up,activated. 0 : field_o int register is cleared,inactivated. When FIELDDET_MODE=2, 1 : field_o signal is not falled after field_o int register is celared. This int register is showing not-falled 1 state. 0 : field_o signal falled and int register is showing falled 0 State(activated value) .	-
0	COAX_STATE	R	PTZ Tx status. When DONEDET_MODE=1 or 3. 1 : Done(done int register is set up,activated). 0 : Busy(done int register is cleared,inactivated). When DONEDET_MODE=2, 1 : done signal is not falled after dones int register is celared. This int register is showing not-falled 1 state. 0 : done signal falled and int register is showing falled 0 State(activated value) .	-

Application Schematic



Pin Configuration



Pin Descriptions

Analog Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VIN1	110	A	Composite video input 1. (Multiplexed with VIN5 on TW2964)
VIN2	113	A	Composite video input 2. (Multiplexed with VIN6 on TW2964)
VIN3	116	A	Composite video input 3. (Multiplexed with VIN7 on TW2964)
VIN4	119	A	Composite video input 4. (Multiplexed with VIN8 on TW2964)
VIN5	111	A	Composite video input 5. (Multiplexed with VIN1 on TW2964)
VIN6	114	A	Composite video input 6. (Multiplexed with VIN2 on TW2964)
VIN7	117	A	Composite video input 7. (Multiplexed with VIN3 on TW2964)
VIN8	120	A	Composite video input 8. (Multiplexed with VIN4 on TW2964)
AIN1	103	A	Audio input of channel 1.
AIN2	104	A	Audio input of channel 2.
AIN3	105	A	Audio input of channel 3.
AIN4	106	A	Audio input of channel 4.
AIN_AUX1	107	A	Auxillary Audio input 1.
AINN1	102	A	Audio input negative control for audio inputs 1, 2, 3, 4, and AUX1.
AIN5	92	A	Audio input of channel 5. (NC on TW2964)
AIN6	93	A	Audio input of channel 6. (NC on TW2964)
AIN7	94	A	Audio input of channel 7. (NC on TW2964)
AIN8	95	A	Audio input of channel 8. (NC on TW2964)
AIN_AUX2	96	A	Auxillary Audio input 2. (NC on TW2964)
AINN2	91	A	Audio input negative control for audio inputs 5, 6, 7, 8, and AUX2. (NC on TW2964)
AOUT	99	A	Audio output.

Digital Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VD1[7:0]	63, 64, 65, 66, 68, 69, 70, 71	O	Video data output of channel 1.
VD2[7:0]	50, 51, 52, 53, 56, 57, 58, 59	O	Video data output of channel 2.
VD3[7:0]	30, 31, 32, 33, 36, 37, 38, 39	O	Video data output of channel 3.
VD4[7:0]	16, 17, 18, 19, 22, 23, 24, 25	O	Video data output of channel 4.
MPP1/ PTZADD[0]	83	IO	HS/VS/FLD/ACTIVE/NOVID of channel 1. Optionally PTZADD[0] for external Coaxitron circuit (TW2968 only).
MPP2/ PTZADD[1]	84	IO	HS/VS/FLD/ACTIVE/NOVID of channel 2. Optionally PTZADD[1] for external Coaxitron circuit (TW2968 only).
MPP3/ PTZADD[2]	85	IO	HS/VS/FLD/ACTIVE/NOVID of channel 3. Optionally PTZADD[2] for external Coaxitron circuit (TW2968 only).
MPP4/ PTZDAT	86	IO	HS/VS/FLD/ACTIVE/NOVID of channel 4. Optionally PTZDAT for external Coaxitron circuit (TW2968 only).
ACLKR	73	IO	Audio serial clock input/output of record.
ASYNR	74	IO	Audio serial sync input/output of record.
ADATR	75	O	Audio serial data output of record.
ADATM	76	O	Audio serial data output of mixing.
ACLKP	78	IO	Audio serial clock input/output of playback.
ASYNP	79	IO	Audio serial sync input/output of playback.
ADATP	80	I	Audio serial data input of playback.
ALINKI	14	I	Audio Multi-chip operation serial input.
ALINKO	81	O	Audio Multi-chip operation serial output.

System Control Pins

NAME	NUMBER	TYPE	DESCRIPTION
RSTB	10	I	System reset.
XTI	46	I	Crystal 27MHz connection or Oscillator clock input.
XTO	47	O	For crystal 27MHz connection.
CLKPO	42	O	36/72/144MHz or 27/54/108MHz clock output.
CLKNO	43	O	36/72/144MHz or 27/54/108MHz clock output.
TEST	5	I	Test pin. Connect to ground.
SCLK	11	I	Serial control clock line.
SDAT	12	IO	Serial control data line.
SADD[1:0]	7, 6	I	Serial control address.
IRQ	88	O	Interrupt request output.

Power and Ground Pins

NAME	NUMBER	TYPE	DESCRIPTION
VDDI	4, 9, 21, 27, 35, 45, 55, 62, 87	P	1.0V Power for internal logic.
VDDO	15, 29, 41, 49, 60, 72, 82	P	3.3V Power for output driver.
VSS	3, 8, 13, 20, 26, 28, 34, 40, 44, 48, 54, 61, 67, 77, 89	G	Ground for internal logic and output driver.
VDDV	109, 115, 121, 122, 124, 126	P	3.3V Power for analog video ADC.
VSSV	112, 118, 123, 125	G	Ground for analog video ADC.
VDDA	97, 98, 108	P	3.3V Power for analog audio.
VSSA	90, 100, 101	G	Ground for analog audio.
VDDAPLL	128	P	3.3V Power for clock PLL.
VSSAPLL	1	G	Ground for clock PLL.
VDDDPLL	127	P	3.3V Power for clock PLL.
VSSDPLL	2	G	Ground for clock PLL.

Parametric Information

ESD Ratings

Human Body Model (Analog video inputs to VSSV/VDDV)..... 8000V
Human Body Model (Analog audio inputs to VSSA/VDDA)..... 8000V
Human Body Model (Tested per JESD22-A114E, all pins) 5000V
Machine Model (Tested per JESD22-A115-A) 300V
CDM Model (Tested per JESD22-C101) 2000V

AC/DC Electrical Parameters

TABLE 6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDDVM	-	3.3	3.96	V
VDDA (Measured to VSSA)	VDDAM	-	3.3	3.96	V
VDDAPLL (Measured to VSSAPLL)	VDDAPLLM	-	3.3	3.96	V
VDDDPLL (Measured to VSSDPLL)	VDDDPLLM	-	3.3	3.96	V
VDDI (Measured to VSS)	VDDIM	-	1.0	1.2	V
VDDO (Measured to VSS)	VDDOM	-	3.3	3.96	V
Voltage on any Digital Signal Pin (See the note below)	-	VSS –0.5	-	VDDO + 10%	V
Analog Video Input Voltage	-	VSSV – 0.5	-	VDDV + 10%	V
Analog Audio Input Voltage	-	VSSA– 0.5	-	VDDA + 10%	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-40	-	+125	°C
Reflow Soldering	T_{PEAK}	255 +5/-0 (10-30 seconds)			°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE: **THIS DEVICE EMPLOYS HIGH-IMPEDANCE CMOS DEVICES ON ALL SIGNAL PINS. IT MUST BE HANDLED AS AN ESD-SENSITIVE DEVICE. VOLTAGE ON ANY SIGNAL PIN THAT EXCEEDS THE RANGES LIST IN TABLE 6 CAN INDUCE DESTRUCTIVE LATCH-UP.**

TABLE 7. CHARACTERISTICS

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
SUPPLY					
Power Supply — IO	VDDO	3.0	3.3	3.6	V
Power Supply — Analog Video	VDDV	3.0	3.3	3.6	V
Power Supply — Analog Audio	VDDA	3.0	3.3	3.6	V
Power Supply — Clock PLL Analog	VDDAPLL	3.0	3.3	3.6	V
Power Supply — Clock PLL Digital	VDDDPLL	3.0	3.3	3.6	V
Power Supply — Digital Core	VDDI	0.9	1.0	1.1	V
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, VIN8 Input Range (AC Coupling Required)		0.5	1.0	1.4	V
AIN1, AIN2, AIN3, AIN4, AIN_AUX1, AIN5, AIN6, AIN7, AIN8, AIN_AUX2		0.21	1.4	2.4	V

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Input Range (AC Coupling Required)					
Ambient Operating Temperature	T_A	-40		+85	°C
Analog Video Supply Current	Ivddv	-	162	-	mA
Analog Audio Supply Current	Ivdda	-	41	-	mA
Clock PLL Analog Supply Current	Ivddapll	-	2	-	mA
Clock PLL Digital Supply Current	Ivdddpll	-	2	-	mA
Digital I/O Supply Current	Iddo	-	36	-	mA
Digital Core Supply Current	Iddi	-	106	-	mA
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0	-	V_{DDO} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDO} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} = V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f = 1MHz, V_{IN} = 2.4V)	C_{IN}	-	5	-	pF
DIGITAL OUTPUTS					
Output High Voltage (I_{OH} = –2mA)	V_{OH}	2.4	-	V_{DDO}	V
Output Low Voltage (I_{OL} = 2mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF
ANALOG VIDEO INPUT					
Analog Pin Input Voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
VIDEO ADCS					
ADC Resolution	ADCR	-	10	-	bits
ADC Integral Non-Linearity	AINL	-	±1	-	LSB
ADC Differential Non-Linearity	ADNL	-	±1	-	LSB
ADC Clock Rate	f_{ADC}	-	36	-	MHz
Video Bandwidth (-3db)	BW	-	10	-	MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}	-	15.625	-	kHz
Line Frequency (60Hz)	f_{LN}	-	15.734	-	KHz
Static Deviation	Δf_H	-	-	6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f_{SC}	-	3582056	-	Hz

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Lock In Range	Δf_H	±450	-	-	Hz
CRYSTAL SPEC					
Nominal Frequency (Fundamental)		-	27	-	MHz
Deviation (Note 2)		-	-	±50	ppm
Load Capacitance	CL	-	18	-	pF
Series Resistor (ESR)	RS	-	50	-	Ω
OSCILLATOR INPUT					
Nominal Frequency		-	27	-	MHz
Deviation		-	-	±50	ppm
Duty Cycle		-	-	55	%

NOTE:

1. Supply current measurement is based on 0x93[2:0] = 7 setting.
2. Crystal deviation is base on normal operation condition.
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

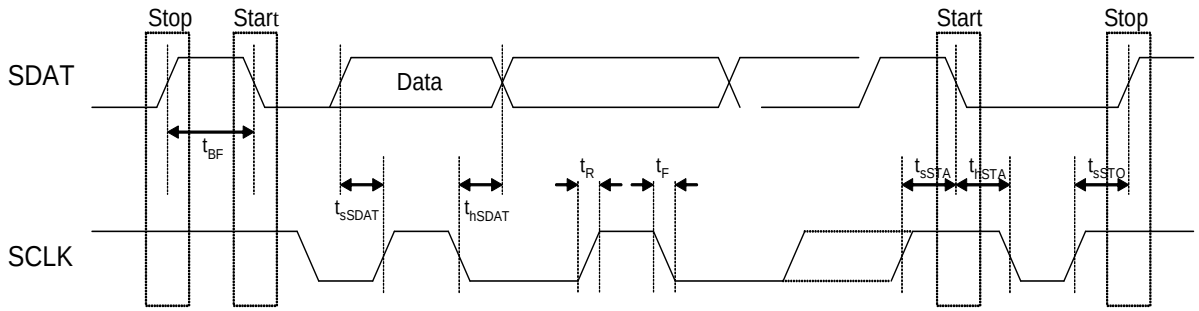
Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	74			ns
SDAT Hold Time	t_{hSDAT}	50		900	ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for each Bus Line	C_{BUS}			400	pF
SCLK Clock Frequency	f_{SCLK}			400	KHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Serial Host Interface Timing Diagram

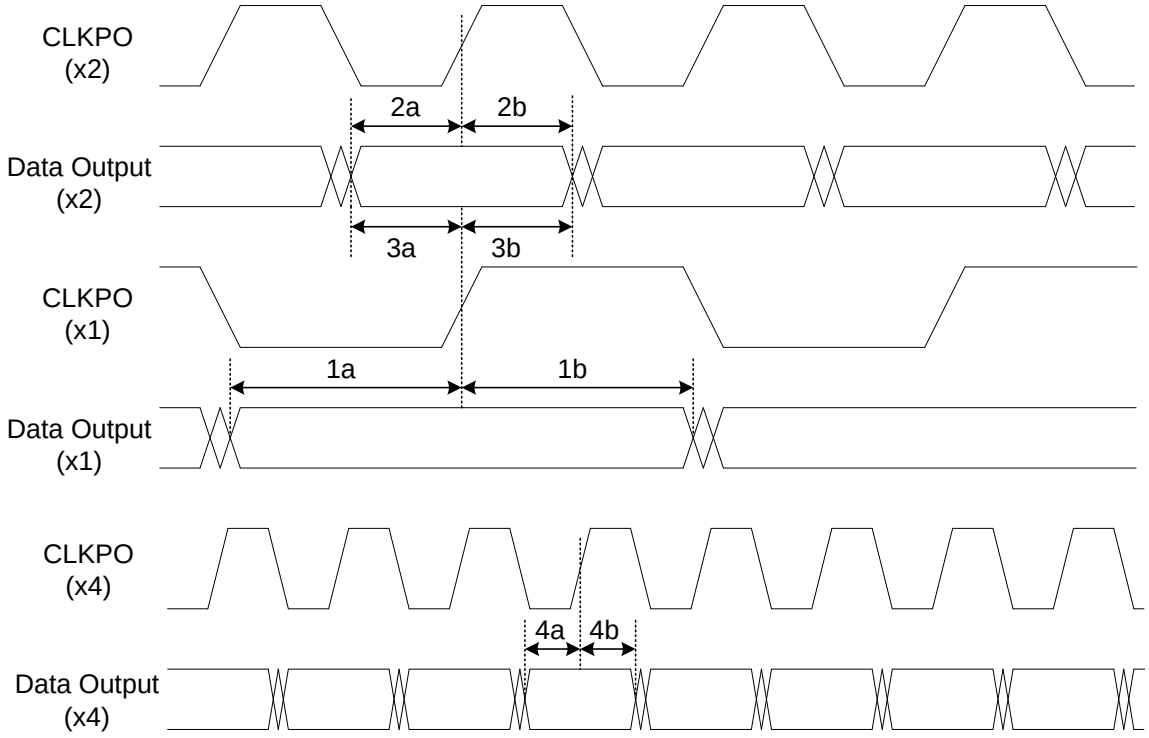


CLKPO and Video Data Timing

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
Setup from CLKPO(x1) to Video Data(x1)	1a	13		15	ns
Hold from CLKPO(x1) to Video Data(x1)	1b	11		15	ns
Setup from CLKPO(x2) to Video Data(x2)	2a	6		8	ns
Hold from CLKPO(x2) to Video Data(x2)	2b	3		6	ns
Setup from CLKPO(x1) to Video Data(x2)	3a	7		10	ns
Hold from CLKPO(x1) to Video Data(x2)	3b	2		6	ns
Setup from CLKPO(x4) to Video Data(x4)	4a	2		3.5	ns
Hold from CLKPO(x4) to Video Data(x4)	4b	3		4	ns

NOTE:

1. CLKPO timing is related with CLKPO_DEL register value. The following timing diagram is illustrated in the case that the CLKPO_DEL is set to 0hex and CLKPO_POL is set to 0.CLKNO timing is inversed CLKPO timing as default setting. CLKPO_DEL/CLKNO_DEL can make more timings.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

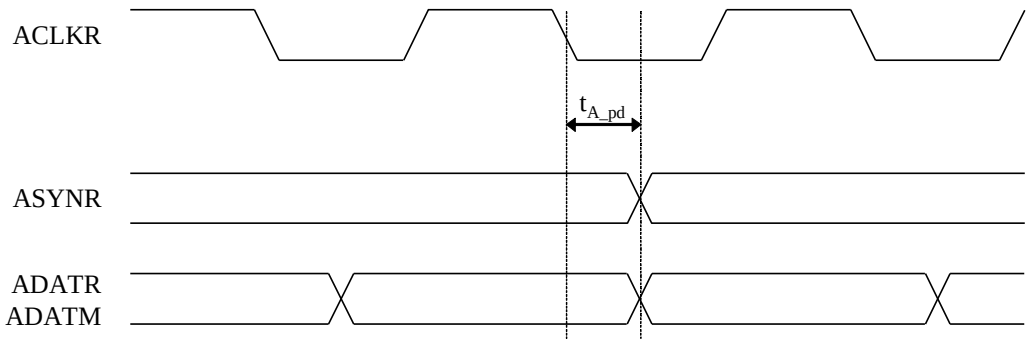


Digital Serial Audio Interface Timing

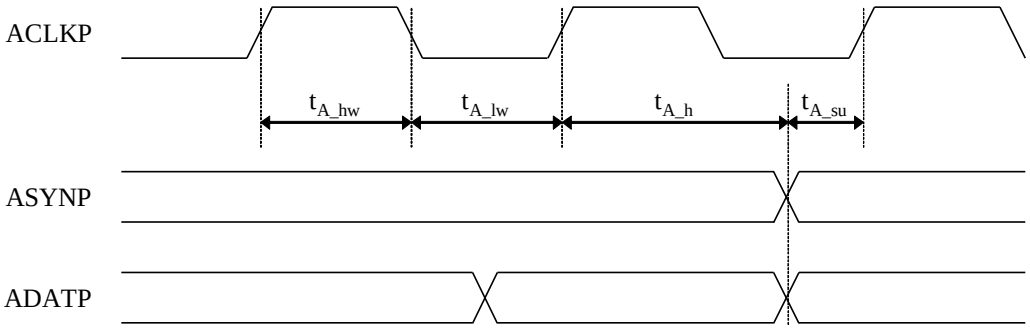
PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
ASYNR, ADATR, ADATM Propagation Delay	T_{A_pd}	-2		4	ns
ACLKP High Pulse Duration	T_{A_hw}	36			ns
ACLKP Low Pulse Duration	T_{A_lw}	72			ns
ASYNP, ADATP Setup Time	T_{A_su}	36			ns
ASYNP, ADATP Hold Time	T_{A_h}	35			ns

NOTE:

1. T_{A_lw} Min value and T_{A_su} Min value are Fs=48KHz mode only.If Fs < 48KHz, these Min values are more bigger. High period of ACLKR/ACLKP is 27MHz one clock period.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.



(A) RECORD AND MIX AUDIO(MASTER MODE)



(B) PLAYBACK AUDIO(MASTER MODE)

Analog Audio Parameters

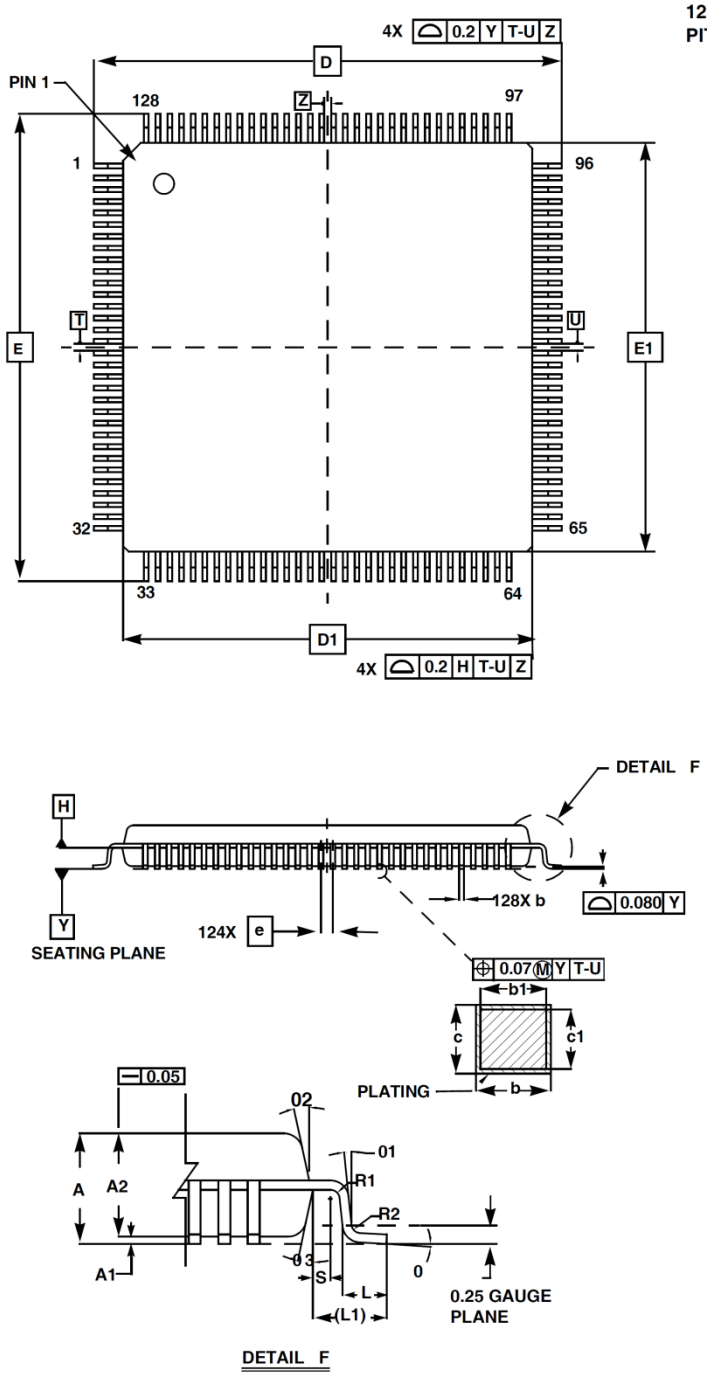
PARAMETER	SYMBOL	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG AUDIO INPUT CHARACTERISTICS					
AIN1, AIN2, AIN3, AIN4, AIN_AUX1, AIN5, AIN6, AIN7, AIN8, AIN_AUX2 Input Impedance	RINX	9	10		kΩ
Interchannel Gain Mismatch			0.2		dB
Input Voltage Range		0	1.4	2.4	Vpp
Full scale input voltage (peak to peak) (Note 1)	ViFULL	0.21	1.4	2.4	Vpp
Interchannel Isolation (Note 2)			85		dB
ANALOG AUDIO OUTPUT CHARACTERISTICS					
AOUT Output Load Resistance	RLAO	300			ohm
AOUT Load Capacitance	CLAO			1	nF
AOUT Offset Voltage	VOSAO			300	mV
Full Scale Output Voltage (Note 3)	VoFULL		1.0	1.4	Vpp

NOTE:

1. Tested at input gain of 0 dB, Fin = 1kHz.
2. Tested at input gain of 0 dB, Fs = 8kHz and 16kHz.
3. Tested at output gain of 0 dB, Fout = 1kHz.
4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Package Outline Drawing

Low Plastic Quad Flatpack Packages (LQFP)



Q128.14x14

128 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE .4 MM PITCH

SYMBOL	MILLIMETERS			NOTES
	MIN	NOM	MAX	
A	-		1.60	-
A1	0.05		0.15	-
A2	1.35	1.40	1.45	-
b	0.13	0.16	0.23	4
b1	0.13	-	0.19	-
c	0.09	-	0.20	-
c1	0.09	-	0.16	-
D	16 BSC			-
D1	14 BSC			3
E	16 BSC			-
E1	14 BSC			3
L	0.45	0.60	0.75	-
L1	1.00 REF			-
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
0	0°	3.5°	7°	-
01	0°	-	-	-
02	11°	12°	13°	-
03	11°	12°	13°	-
N	128			-
e	0.40 BSC			-

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NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

Revision History

DATE	REVISION	CHANGE
April 15, 2014	FN8394.4	Page 1 - Removed 3rd bullet “Software selectable ....” - Changed 5th bullet beginning with "Four 10-bit.." to: "Eight 10-bit ..." Page 3 - Removed TW2968L-LA1-CR from Ordering Information table Page 196 - Updated "About Intersil" verbiage.
March 19, 2013	FN8394.3	Initial release.

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