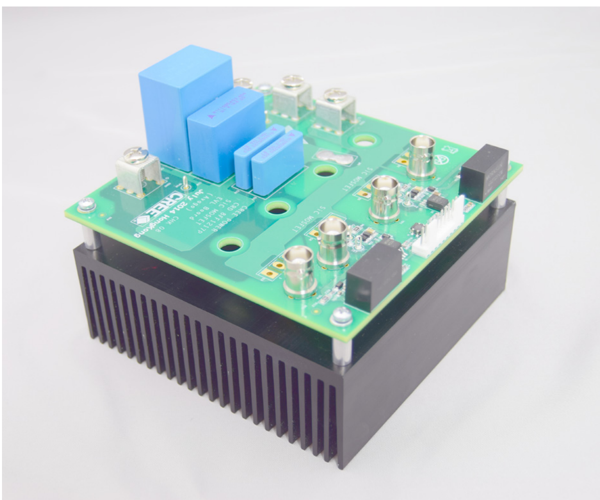
KIT8020-CRD-8FF1217P-1
CREE MOSFET Evaluation Kit
User's Manual

REV B
CREE Power Applications
April 20, 2015



This document is prepared as a user reference guide to install and operate CREE evaluation hardware.

All parts of this User's Manual are provided in English, and the Cautions are provided in English, Mandarin, and Japanese. If the end user of this kit is not fluent in any of these languages, it is your responsibility to ensure that they understand the terms and conditions described in this document, including without limitation the hazards of and safe operating conditions for this kit.

本ユーザーマニュアルは全て英語で作成されており、警告文は、英語、中国語（北京語）及び日本語で作成されています。本キットのエンドユーザーが、これらの言語を理解できない場合は、貴方の責任において、エンドユーザーに、本書の条件（本キットの危険性及びこれを安全に使用するために守るべき事項を含むが、これらに限られない。）を理解させるようにして下さい。

本用户手册的所有部分以英文提供，警示以英文、中文、日文提供。如果套件的终端用户不熟悉上述任何语言，您有责任确保他们理解本文件的条款与条件，包括但不限于本套件的风险及安全操作条件。

Note: This Cree-designed evaluation hardware for Cree components is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. The hardware is not designed to meet any particular safety standards and the tool is not a production qualified assembly.

CAUTION
PLEASE CAREFULLY REVIEW THE FOLLOWING PAGE, AS IT CONTAINS IMPORTANT INFORMATION REGARDING THE HAZARDS AND SAFE OPERATING REQUIREMENTS RELATED TO THE HANDLING AND USE OF THIS KIT.

警告
次のページをよくお読み下さい。次のページには、本キットの使用その他の取り扱いに伴う危険性及びこれを安全に操作するために必要な事項に関する重要な情報が記載されています。

警示
请仔细阅读下一页，因为其包含了关于操作及使用本套件的风险及安全操作要求。

CAUTION

DO NOT TOUCH THE EVAULATION KIT WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE EVALUATION BOARD. THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION KIT WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS KIT CAN REACH TEMPERATURES ABOVE 50° CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE FOR A SHORT TIME AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED.

Please ensure that appropriate safety procedures are followed when assembling and operating this kit, as any of the following can occur if you handle or use this kit without following proper safety precautions:

- **Death**
- **Serious injury**
- **Electrocution**
- **Electrical shock**
- **Electrical burns**
- **Severe heat burns**

You must read this User's Manual in its entirety before operating this kit. It is not necessary for you to touch the evaluation kit while it is energized. The evaluation kit must be fully assembled and all devices to be tested must be attached before the kit is energized. You must never leave this kit unattended or handle it when energized, and you must always ensure that all bulk capacitors have completely discharged prior to handling the evaluation board included in the kit. Do not change the devices to be tested until the kit is disconnected from the electrical source and the bulk capacitors have fully discharged.

警告

本評価キットに電源が入っているときは、これに触らないで下さい。評価ボードを取り扱う前に、コンデンサが完全に放電するまで待って下さい。本キットに電源が入っている間は、非常に高い電圧が流れている可能性があり、本キットの部品の中には、**50**度を超える熱を帯びるものもあります。また、本キットの電源が切られ、コンデンサが完全に放電するまで、この状態がしばらく続きます。

本キットを組み立てて、操作する際には、適切な安全確保手続を守って下さい。適切な安全確保手続を守らずに、本キットを取り扱い、使用すると、以下のいずれかの事故が発生するおそれがあります：

- **死亡**
- **重傷**
- **感電死**
- **電気ショック**
- **電気による火傷**
- **激しい熱傷**

本キットを操作する前に、ユーザーマニュアルを通読して下さい。電源を入れている間は、キットに触れる必要はありません。本キットに電源を入れる前に、本キットを完全に組み立て、全ての試験対象の装置をセッティングして下さい。本キットに電源が入っている間は、本キットから目を離さず、またこれに触れないで下さい。また本キットに含まれる評価ボードを取り扱う前に、全てのコンデンサが完全に放電していることを常に確認して下さい。試験対象の装置を変えるときは、本キットの電源を切り、コンデンサが完全に放電するまで待って下さい。

警示

不得触碰通电的评估套件，且应在大容量电容完全放电后操作评估板。当连接电源后，本评估套件可能带有高电压，且本套件的部分组件可能达到 50 摄氏度以上。此外，在切断电源后，上述情况会在短时间内持续，直至大容量电容完全放电。

请确保在组装及操作本套件时遵循安全程序，因为如果您操作或使用本套件时未能遵守适当的安全防护措施，可能发生下列情形：

- **死亡**
- **重伤**
- **触电身亡**
- **电击**
- **电灼伤**
- **严重热烧伤**

您必须在操作本套件前完整阅读本用户手册。您没有必要触碰通电的评估套件。在通电之前，评估套件应组装完毕，且连接待测试的所有设备。您不得使套件无人照管或在通电时对其进行操作，且您必须时刻确保在操作本套件包含的评估板前，将所有大容量电容完全放电。只有在套件断电且大容量电容完全放电后，方可更换待测试的设备。

1. Introduction

This Evaluation kit has been designed to demonstrate the high performance of CREE C2M 1200V SiC MOSFET and ZRec SiC Schottky diodes (SBD) in the standard TO-247 package. It can be easily configured for several topologies from the basic phase-leg configuration. The evaluation (EVL) board has multiple uses:

- Evaluate the SiC MOSFET performance during switching events and steady state operation.
- Easily configure different topologies with SiC MOSFET and SiC diodes.
- Functional testing with SiC MOSFET, for example double pulse test to measure switching losses (E_{on} and E_{off}).
- PCB layout example for driving the Cree MOSFET.
- Gate drive reference design for a TO-247 packaged Cree MOSFET.
- Comparative testing between Cree devices and IGBTs.

This user manual includes information on the EVL board architecture, hardware configuration, Cree SiC power devices, and an example application when using this board.

Maximum Ratings for Evaluation board:

Input / Output DC Voltage	1100 VDC	Ambient operating temperature range	-35C to 55C
Input / Output Current	50A DC		

2. Package Contents

Item No.	*QTY*	*P/N*	*Description*
1	1	CRD8FF1217P-1	Avago Driver version Eval board
2	4	AOS2182471	Ceramic isolation tile, 1.5mm
3	1	57908	Heat sink with mounting holes
5	2	C2M0080120D	1200V 80 mohm MOSFET
6	2	C4D20120D	1200V 20A Diode
7	1		Copper shorting strip
8	2	74270011	Ferrite Bead
9	8	91166a210	M3 washer, Zn-S, 7mm OD, 3.2mm ID
10	4	92005a129	M3x22mm, Zn-S, Board mounting Screw
11	4	94669a727	Stand offs, Al spacer, 6mm OD x 14mm
12	4	92005a120	M3x10mm, Zn-S, Device mounting screw
13	1		User's Manual

3. EVL Board Overview

The EVL board's general block diagram is shown in Figure 1. There is a phase-leg which can include two SiC MOSFETs (Q1 and Q2) with half bridge phase-leg configuration and two anti-parallel SiC Schottky diodes (D1 and D3) with Q1 and Q2. The gate drive block with electrical isolation is designed on the board to drive SiC MOSFET Q1 and Q2. There are four power trace connectors (CON1, CON2, CON3 and CON5) and one 10 pin signal/supply voltage connector (CON4) on board.

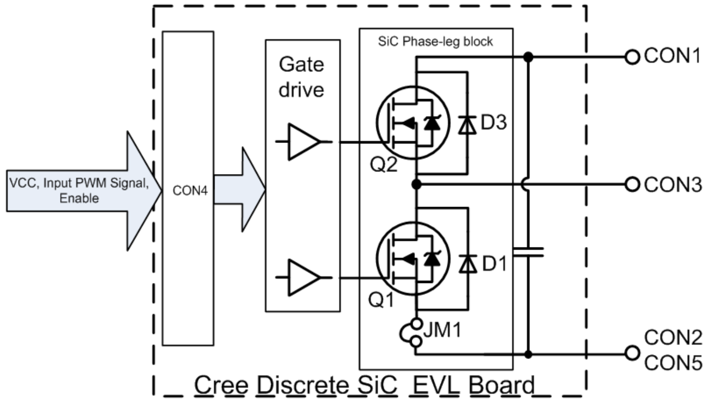


Figure 1. General block diagram of Cree Discrete SiC EVL board

Please note that JM1 as shown in Figure 1 is open circuit. It is necessary to short this with a wire or insert a shunt as shown in section 6.2 to complete the circuit before operation.

CRD8FF1217P-1 includes two 2.5A gate driver integrating opto-couplers from Avago (ACPL-W346) and two 2W isolation DC/DC converters from Mornsun (G1212S-2W) for both high-side and low-side isolated power. The 2W DC/DC converter with +12V Vcc input generates +24V Vcc_out output voltage with 6KVDC isolation that is supplying voltage to W346 on push-pull gate drive on the secondary side as shown in Figure 2. In this circuit, a 5V zener in parallel with 1uF capacitor is used to generate -5V Vgs voltage for the SiC MOSFET turn-off, and turn-on Vgs voltage is equal to 24V-5V=19V. Note that SiC MOSFET can be turned off with zero voltage, and the -5V turn-off voltage helps with faster turn-off and lower turn-off losses and also improves dv/dt induced self turn-on and noise immunity during transient periods with more margin for Vgs turn-on threshold voltage. You can implement any PWM signal to drive the SiC phase leg block, if the board is operating in synchronous mode with high side MOSFET and low side MOSFET, the input signals must have additional dead time to avoid shoot through.

MOSFET, the input signals must have additional dead time to avoid shoot through.

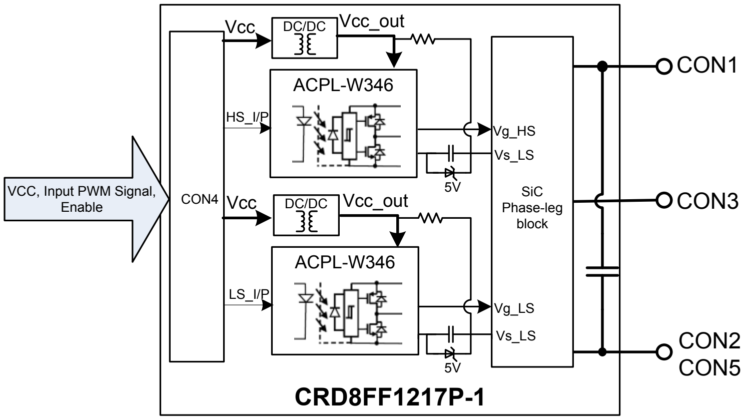


Figure 2. CRD8FF1217P-1 Block diagram with ACPL-W346

The EVL board size is 124mmx120mmx40mm (not including heatsink). Different types of heatsinks can be assembled depending on your cooling requirements. Figure 3 shows the board attached with the heatsink provided in the kit. However, users can use any type of heatsink that works with the standard TO-247 package.

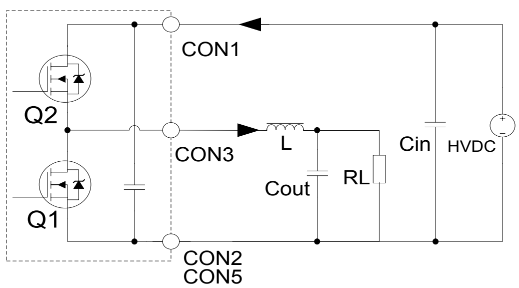
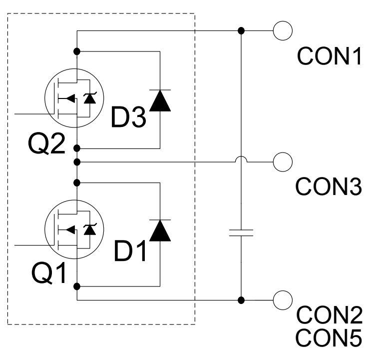
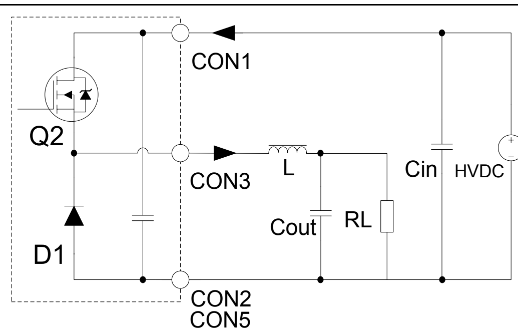
Figure 3. Cree EVL board assembly (see Appendix for assembly instructions).

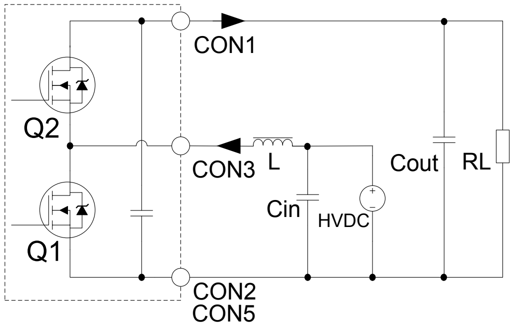
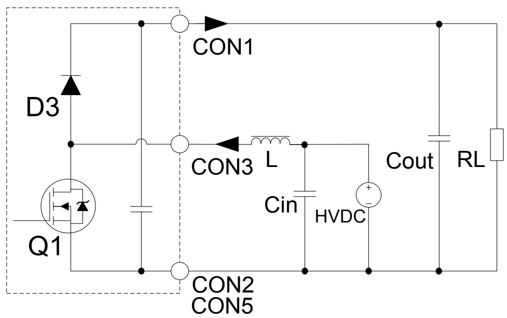
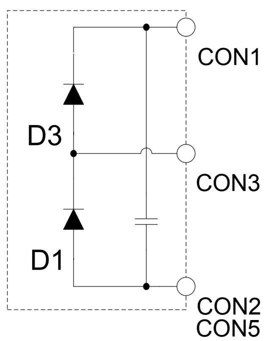
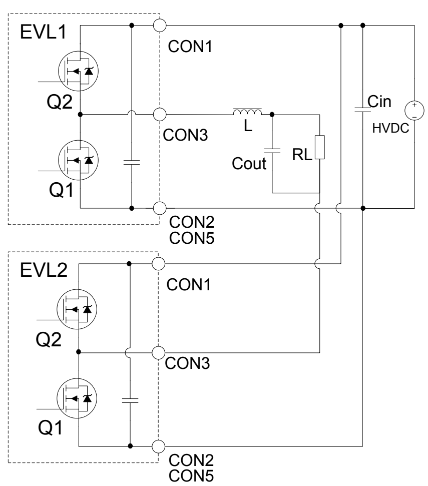
4. Configurations

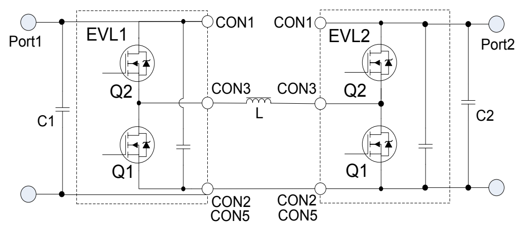
The EVL board can be flexible to implement different topologies when using the different configurations of SiC MOSFETs and SiC diodes. It is possible to test several topologies with this board: synchronous Buck, non-synchronous Buck (or high-side Buck), synchronous Boost, non-synchronous Boost, half phase-leg bridge converter, H bridge converter (2x EVL boards), and bi-directional buck-boost converters. Table 1 summarizes the possible topologies that can be implemented using this EVL board. For the phase-leg configuration, it can either use discrete anti-parallel SiC SBD or body diode of SiC MOSFET. Thus the body diode of SiC MOSFET can be evaluated without anti-parallel diode with option one in the below table.

With two EVL boards, H-bridge converter and bi-directional DC/DC converter can be configured. For H-bridge, with different control architecture, the phase shift full bridge, resonant LLC ZVS converter and single phase DC/ AC converter can all be achieved. For bi-directional DC/DC converter, it can achieve either Buck from port 1 to port 2 or Boost from port 2 to port 1. Furthermore, with three EVL boards, it can even be set up as a three-phase DC/AC inverter for some motor drive or inverter applications.

Table. 1 The EVL board topology configuration

Option One: Syn. Buck converter or Phase-leg bridge topology without anti-parallel diodes		• Step down voltage or phase leg topology w/o anti-parallel diodes • SiC Body diode used • Connect inductor L with CON3 as output • CON1: INPUT • CON3: OUTPUT • CON2, CON5: GND
Option Two: Phase-leg bridge topology with anti-parallel SiC SBD		• Phase-leg, switching with external anti-parallel diode • SiC SBD used • CON1, CON3: Input/output depends on which topology apply to board • CON2, CON5: GND
Option Three: Non-syn Buck converter		• Step down voltage • Connect inductor L with CON3 as output • CON1: INPUT • CON3: OUTPUT • CON2, CON5: GND

Option Four: Syn. Boost converter		• Step up voltage • Connect inductor L with CON3 as input • CON1: OUTPUT • CON3: INPUT • CON2, CON5: GND
Option Five: Non-syn Boost converter		• Step up voltage • Connect inductor L with CON3 as input • CON1: OUTPUT • CON3: INPUT • CON2, CcON5: GND
Option Six: Diode bridge		• Bridge diode with SiC SBD • CON1: OUTPUT (Positive) • CON3: INPUT • CON2, CON5: OUTPUT (Negative)
Option Seven: H bridge topology configuration using two EVL boards		• Full bridge converter with Phase shift or resonant • single phase DC/AC inverter

Option Eight: Bi-directional DC/DC converter		• Port 1 is input and port 2 is output with Buck converter, Q2 of EVL2 is constantly turn-on, and Q1 of EVL2 is constantly turn-off • Port 1 is output and port 2 is input with Boost converter, Q2 of EVL1 is constantly turn-on and Q1 of EVL2 is constantly turn-off

5. Hardware Description

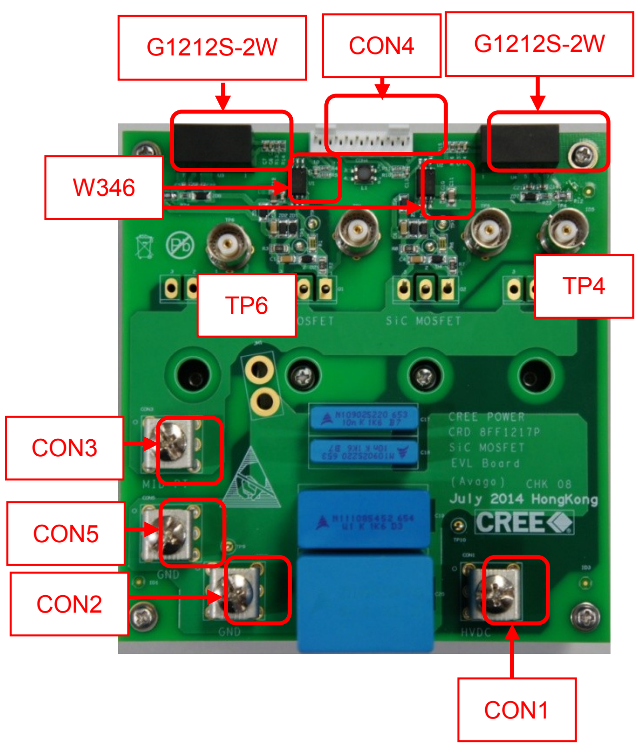


Figure 4. EVL board showing key connectors and components.

The above figures give top view of the EVL board. The picture highlights key test points and connectors on the boards.

5.1 Test points

To make testing more effective and easy, the BNC connectors are added on the board to measure both Vgs and Vds waveforms for SiC MOSFET Q1 and Q2. A current test point with two unpopulated through-hole contacts is available to measure the drain current through the low-side switch. A jumper wire (not provided in the kit) with a short loop (JM1) can be inserted into the test point to measure current using current probe. Another option is to use accurate coaxial shunt resistors (not provided in the kit) from T&M Research (www.tandmresearch.com) to make the measurement. This option can minimize the stray inductance on the switching loops and achieve accurate switching loss measurement. Lastly, one can also simply short JM1 with the small shorting strips provided in the kit if it's not necessary to measure the current waveform. Also, some test points are added between gate resistors for measuring the voltage across the gate resistors. Thus it can estimate the gate current Ig to the SiC MOSFET.

5.2 Connectors

CAUTION

***** HIGH VOLTAGE RISK *****

THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION KIT WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS KIT CAN REACH TEMPERATURES ABOVE 50° CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE EVAULATION KIT WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE EVALUATION BOARD.

Some of the connectors on the evaluation kit are not grounded (i.e., they are floating), so the connectors could have high voltage levels present when the kit is connected to an electrical source and thereafter until the bulk capacitors are fully discharged. Please ensure that appropriate safety procedures are followed when working with these connectors as serious injury, including death by electrocution or serious injury by electrical shock or electrical burns, can occur if you do not follow proper safety precautions. After use the evaluation kit should immediately be disconnected from the electrical source. After disconnection any stored up charge in the bulk capacitors will continue to charge the connectors. Therefore, you must always ensure that all bulk capacitors have completely discharged prior to handling the evaluation board included in the kit.

警告
*****高電圧のおそれ*****

本キットに電源が入っているときは、これに非常に高い電圧が流れているおそれがあり、本キットの部品の中には、50 度を超える熱を帯びるものもあります。また、本キットの電源が切られ、コンデンサが完全に放電するまでは、この状態がしばらく続きます。本キットに電源が入っている間は、本キットに触らないで下さい。また本キットに含まれる評価ボードを取り扱う前に、全てのコンデンサが完全に放電していることを確認して下さい。

本キットのコネクタは、固定されておらず、浮動しているものもあります。このため、本キットに電源が入っている間とコンデンサが完全に放電するまでは、コネクタに高い電圧が流れているおそれがあります。これらのコネクタを扱う際には、感電死や電気ショック及び電気による火傷など重傷の怪我につながるおそれがあるため、適切な安全確保手続を守って下さい。本キットの使用後は、直ちに電源を切って下さい。電源を切った後も、コンデンサに残っている電気がコネクタに流れ続けます。このため、本キットに含まれる評価ボードを扱うときは、全てのコンデンサが完全に放電したことを常に確認して下さい。

警示
***** 高压危险*****

当连接电源后，本评估套件可能带有高电压，且本套件的部分组件可能达到 50 摄氏度以上。此外，在切断电源后，上述情况会持续至大容量电容完全放电。不得触碰通电的评估套件，且应在大容量电容完全放电后操作评估板。

评估套件的部分连接器未接地（而是悬挂的），因此当套件连接电源时及之后，连接器可能带有高电压，直至大容量电容完全放电。请在操作该等连接器时遵循适当的安全程序，否则可能发生触电致重伤直至身亡、电击致重伤或电灼伤。使用后应立即将评估套件切断电源。切断电源后，大容量电容中储存的电量将继续为连接器供电。因此，您必须时刻确保在操作本套件包含的评估板前，将所有大容量电容完全放电。

The connectors CON1, CON2, CON3 and CON5 are power connectors, and their definitions are dependent on the different topology as described in table 1. CON4 is for the signal/logic inputs and supply voltage for ICs. The definition of CON4 for each pin is shown in table 2.

Table. 2 Pin definitions for connector CON4

Connector CON4 Pin	CRD8FF1217P-1
Pin1	N/A
Pin2	N/A
Pin3	N/A
Pin4	N/A
Pin5	VCC: +12Vdc
Pin6	VCC_RTN: GND for +12Vdc
Pin7	Input_HS: signal input for Q2
Pin8	Input_HS_RTN: signal ground for Q2
Pin9	Input_LS: signal input for Q1
Pin10	Input_LS_RTN: signal ground for Q1

5.3 Board design

The SiC device is a fast switching device, and it is important to maximize SiC's high performance and minimize ringing with fast switching. The EVL board introduces some design approaches to minimize the ringing on the board:

- The gate drive and logic signal are put on top of the PCB board, while the main power trace and switching devices are put on the bottom layer. There is no crossover or overlap between gate signal and switching power trace, which can minimize high dv/dt and di/dt noise influence from the switching node to gate signal.
- Four de-coupling film capacitors, with values 10nF, 10nF, 0.1uF and 5uF, respectively, are placed close to the SiC devices and can reduce high frequency switching loop and bypass noise within switching loop.
- The layout of gate drive circuitry is designed with symmetric trace distance, which can introduce balance impendence on the gate drive. Also, the gate drive is placed as close as possible to the SiC MOSFETs.
- The power trace layout is optimized to reduce the switching loops.

6. CREE Devices

SiC devices, including SiC MOSFET and SiC Schottky diodes can provide fast switching with less loss compared to conventional Si devices. Cree is the world's leading manufacturer of silicon-carbide Schottky diodes and MOSFETs for efficient power conversion. Two samples of 80mOhm, 1200V rated SiC MOSFET devices and two 20A, 1200V rated Schottky diodes are provided in the kit. However, other samples ranging from 5A to 50A can be ordered online (www.cree.com/power).

7. Example Application and Measurements

7.1 Board Setup

CAUTION
PLEASE ENSURE THAT APPROPRIATE SAFETY PROCEDURES ARE FOLLOWED WHEN ASSEMBLING AND OPERATING THIS KIT AS SERIOUS INJURY, INCLUDING DEATH BY ELECTROCUTION OR SERIOUS INJURY BY ELECTRICAL SHOCK OR ELECTRICAL BURNS, CAN OCCUR IF YOU DO NOT FOLLOW PROPER SAFETY PRECAUTIONS. HIGH VOLTAGE LEVELS ARE PRESENT ON THE EVALUATION KIT WHEN IT IS CONNECTED TO AN ELECTRICAL SOURCE AND WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. ALL BULK CAPACITORS, INCLUDING THE LARGE BULK CAPACITOR ACROSS THE INPUT TERMINALS, MUST BE COMPLETELY DISCHARGED BEFORE THE EVALUATION BOARD CAN BE HANDLED. IT IS NOT NECESSARY FOR YOU TO TOUCH THE EVALUATION KIT WHILE IT IS ENERGIZED. THE EVALUATION KIT MUST BE FULLY ASSEMBLED BEFORE THE KIT IS ENERGIZED. WHEN DEVICES ARE BEING ATTACHED FOR TESTING, THE KIT MUST BE DISCONNECTED FROM THE ELECTRICAL SOURCE AND ALL BULK CAPACITORS MUST BE FULLY DISCHARGED.

警告

本キットを組み立て、操作するときは、適切な安全確保手続を守って下さい。適切な安全確保手続が守られなければ、感電死や電気ショック及び電気による火傷など重傷の怪我につながるおそれがあります。

本キットに電源が入っている間は、本キットに高い電圧が流れており、電源が切られ、コンデンサが完全に放電するまでは、本キットに高い電圧が流れ続けます。評価ボードを扱う前に、入力ターミナル上にわたる大容量コンデンサを含む全てのコンデンサは、完全に放電されなければなりません。

本キットに電源が入っている間は、本キットに触る必要はありません。本キットに電源を入れる前に、本キットを完全に組み立てて下さい。試験対象の装置をセッティングするときは、本キットの電源を切り、全てのコンデンサを放電させて下さい。

警示

请在组装及操作本套件时遵循适当的安全程序，否则可能发生触电致重伤直至身亡、电击致重伤或电灼伤。

当评估套件连接电源时，其带有高电压，并在切断电源后持续，直至大容量电容完全放电。应在所有的大容量电容，包括穿过输入终端的大容量电容完全放电后操作评估板。

您没有必要触碰通电的评估套件。在通电之前，评估套件应组装完毕。只有在套件断电且所有大容量电容完全放电后，方可连接待测试的设备。

In order to demonstrate the EVL with SiC devices, a synchronous phase-leg Buck converter configuration is used as an example to evaluate the performance of the SiC EVL board. This is option one configuration on table 1. The table below gives the electrical parameters. Please note the switching frequency is at 40KHZ in this case due to the design limitation of the available inductor, but it does not mean the switching frequency is limited to 40KHZ. Because of low switching losses of SiC MOSFET, the switching frequency can increase without sacrificing much switching losses when using SiC MOSFET.

During testing, two 25mohm SiC MOSFETs are assembled on the PCB board with heatsink for both high-side Q2 and low-side Q1. The figure gives the test setup with EVL boards. The signal generators are used to generate high-side and low-side PWM signals with Input_HS and Input_LS. Note that the dead time period must be applied to the input signal between Input_HS and Input_LS.

Table. 3 Electrical parameters

Items	Parameters
Input Voltage	600Vdc
Output Voltage	300Vdc
Output RMS Current	30A
Output Power	9KW
Peak MOS current	40A
Switching Frequency	40KHZ
Duty Cycle	50%
Dead time	~450ns
Inductor	400uH
Output Capacitors	300uF

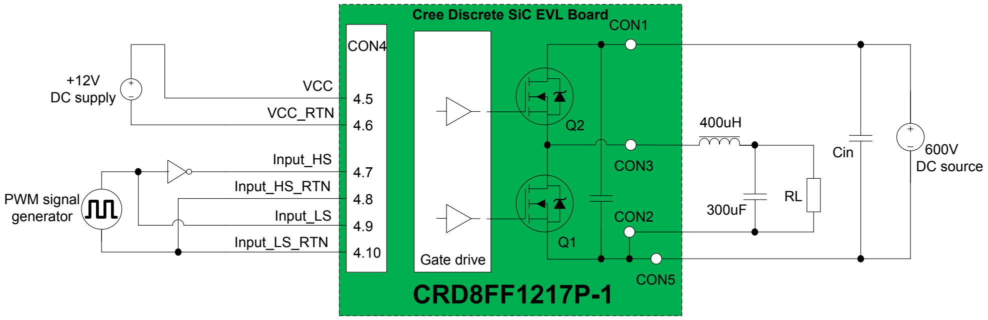


Figure 5. Test setup for the EVL boards with CRD8FF1217P-1

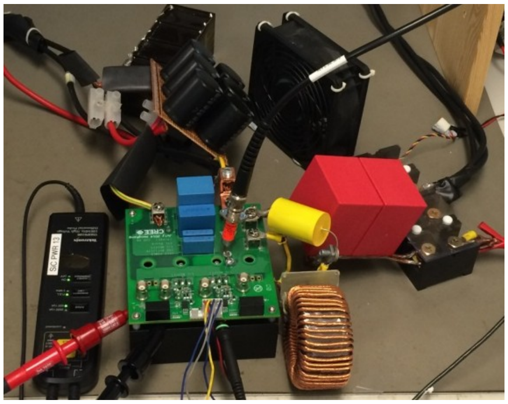


Figure 6. Bench test setup of the EVL boards

7.2 Measurements

To maximize the accuracy of the measurements when using the EVL board, some suggestions are listed below:

- Use a highly accurate 0.0131ohm shunt (not provided in the kit) to measure the low-side current waveform as shown below in Figure 7. This can help to shorten the current sense loop.

Figure 7. Low side current measurement

- A BNC probe is connected to measure low-side Vgs waveform, a x100 HV probe is used to measure low-side Vds waveform, and a differential probe is used to measure high-side Vgs waveform. All probes must be placed as close as possible to reduce incorrect ringing due to probe placement.
- Place the power inductor as close as possible to connect at CON3 to reduce the switching node loop area, and a 1uF 1200V film capacitors should be connected between the output of inductor and ground connector CON5.
- Forced cooling should be used for the heatsink and inductor when measuring waveforms and taking thermal measurements.
- A RC snubber should be added on the drain to source to damp high dv/dt ringing on the switching node and slow the high dv/dt.
- A capacitance (1nF) should be added between gate to source terminal to shunt the miller current from drain to gate. This external capacitor will introduce low impedance path for Cdv/dt from miller capacitance effect and reduce the ringing on the gate pins.
- Use of a ferrite bead (FB) on the gate pin of TO-247 MOSFETs will introduce high impedance on the gate path for MHz high frequency and reduce the Vgs ringing.
- Reduce the stray capacitance of inductor with a single layer structure.

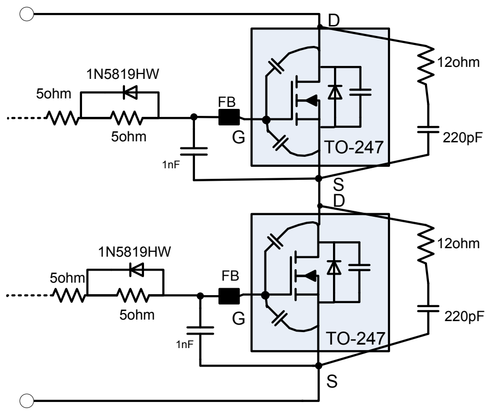
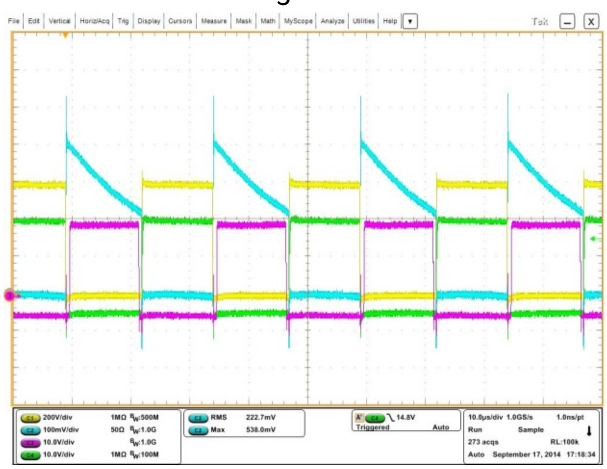


Figure 8. Gate drive and RC snubber configuration

7.3 Test data

The switching waveforms are shown in the below figures. In the operation of the synchronous Buck converter, the low-side body diode conducts before low-side MOSFET is turned on; thus, this low-side MOSFET operates in Zero Voltage Switching (ZVS) mode and the high-side MOSFET operates in hard-switching mode. However, high dv/dt during fast transient of high-side MOSFET will affect the operational behavior of the low-side MOSFET, and the charge stored in miller capacitance will be transferred via its gate loop, inducing some spurious gate voltage in this topology. The methods mentioned in section 6.2 above will help to damp this noise and reduce the ringing on the gate and drain to source. Note that the incorrect test method itself may also introduce some noises from oscilloscope measurement, but it is sometimes not a true representation of the actual transient events on the switching devices.



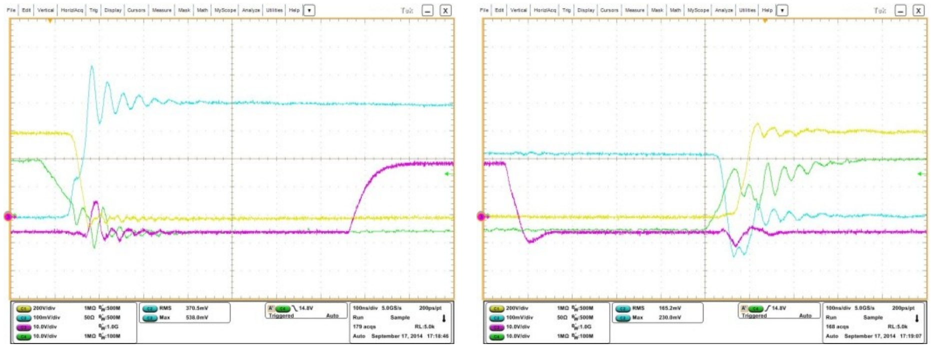


Figure 9. Vgs, Id and Vds waveforms at 9KW loading

(Ch1: low-side Vds yellow 200v/div); (Ch2: low-side Id blue 100mv/0.0131ohm/div);

(Ch3: low-side Vgs pink 10v/div); (Ch4: high-side Vgs green 10v/div)

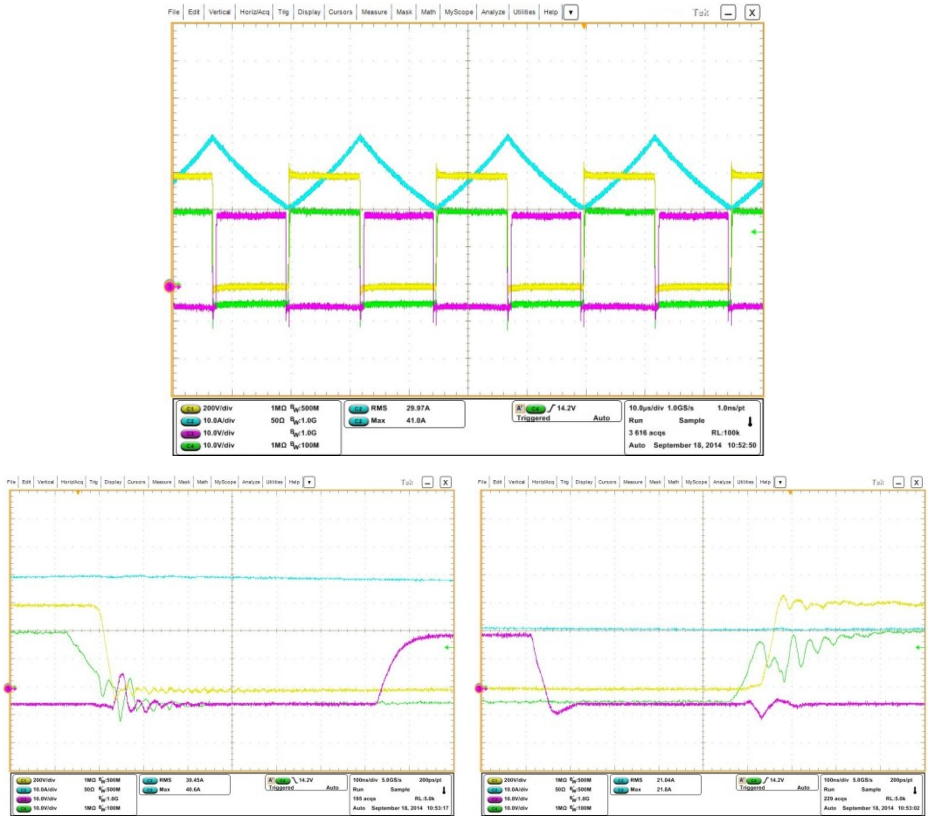


Figure 10. Vgs, Inductor current IL and Vds waveforms at 9KW loading

(Ch1: low- Vds yellow 200v/div); (Ch2: inductor current IL 10A/div); (Ch3: low Vgs pink 10v/div); (Ch4: high-side Vgs green 10v/div)

The EVL board's maximum efficiency in this configuration is around 98.9% at 4KW half load using the Yokogawa WT3000 to measure it. This measurement includes losses from the inductor, switching devices, and capacitors. Considering the high switching frequency (40kHz) and high duty cycle (50%), the efficiency is high compared to conventional Si IGBT solutions.

Figure 11. Efficiency data for this EVL board

Figure 12 shows the thermal performance for this EVL board at full load 9KW after 30 minutes of continuous operation. The test condition is at room temperature with open frame and 12W fan cooling the heatsink and inductor. It demonstrates high performance of SiC MOSFET with low temperature, low losses, and high switching frequency.

CAUTION

IT IS NOT NECESSARY FOR YOU TO TOUCH THE EVALUATION KIT WHILE IT IS ENERGIZED. THE EVALUATION KIT MUST BE FULLY ASSEMBLED BEFORE THE KIT IS ENERGIZED. WHEN DEVICES ARE BEING ATTACHED FOR TESTING, THE KIT MUST BE DISCONNECTED FROM THE ELECTRICAL SOURCE AND ALL BULK CAPACITORS MUST BE FULLY DISCHARGED.

SOME COMPONENTS ON THIS KIT REACH TEMPERATURES ABOVE 50° CELSIUS. PLEASE ENSURE THAT APPROPRIATE SAFETY PROCEDURES ARE FOLLOWED WHEN ASSEMBLING AND OPERATING THIS KIT AS SERIOUS INJURY, INCLUDING DEATH BY ELECTROCUTION OR SERIOUS INJURY BY ELECTRICAL SHOCK OR ELECTRICAL BURNS, CAN OCCUR IF YOU DO NOT FOLLOW PROPER SAFETY PRECAUTIONS.

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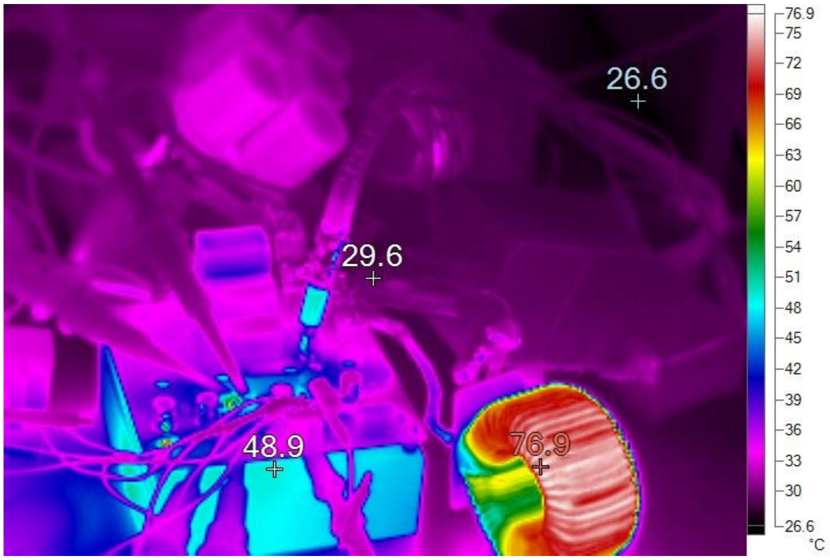


Figure 12. Thermal imaging of the EVL board while under test.

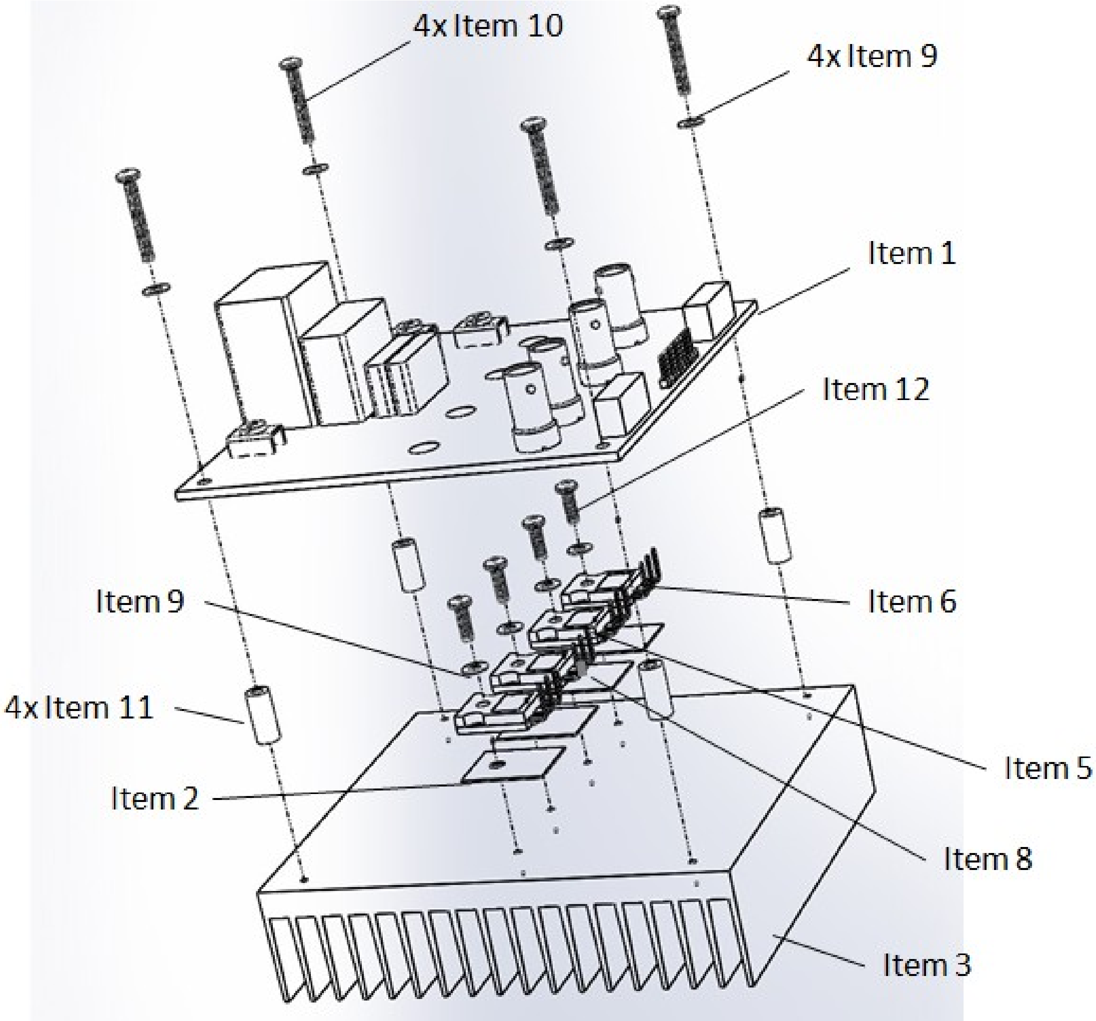
8. Reference

1. C2M0025120D datasheet, Cree, Inc.
2. C4D20120D datasheet, Cree, Inc.
3. 'Performance Evaluations of Hard-Switching Interleaved DC/DC Boost Converter with New Generation Silicon Carbide MOSFETs' Available at Cree website: http://www.cree.com/Power/Document-Library
4. 'Design Considerations for Designing with Cree SiC Modules Part 1. Understanding the Effects of Parasitic Inductance' Available at Cree website: http://www.cree.com/Power/Document-Library
5. 'Design Considerations for Designing with Cree SiC Modules Part 2. Understanding the Effects of Parasitic Inductance' Available at Cree website: http://www.cree.com/Power/Document-Library

9. Appendix

Heatsink assembly instructions:

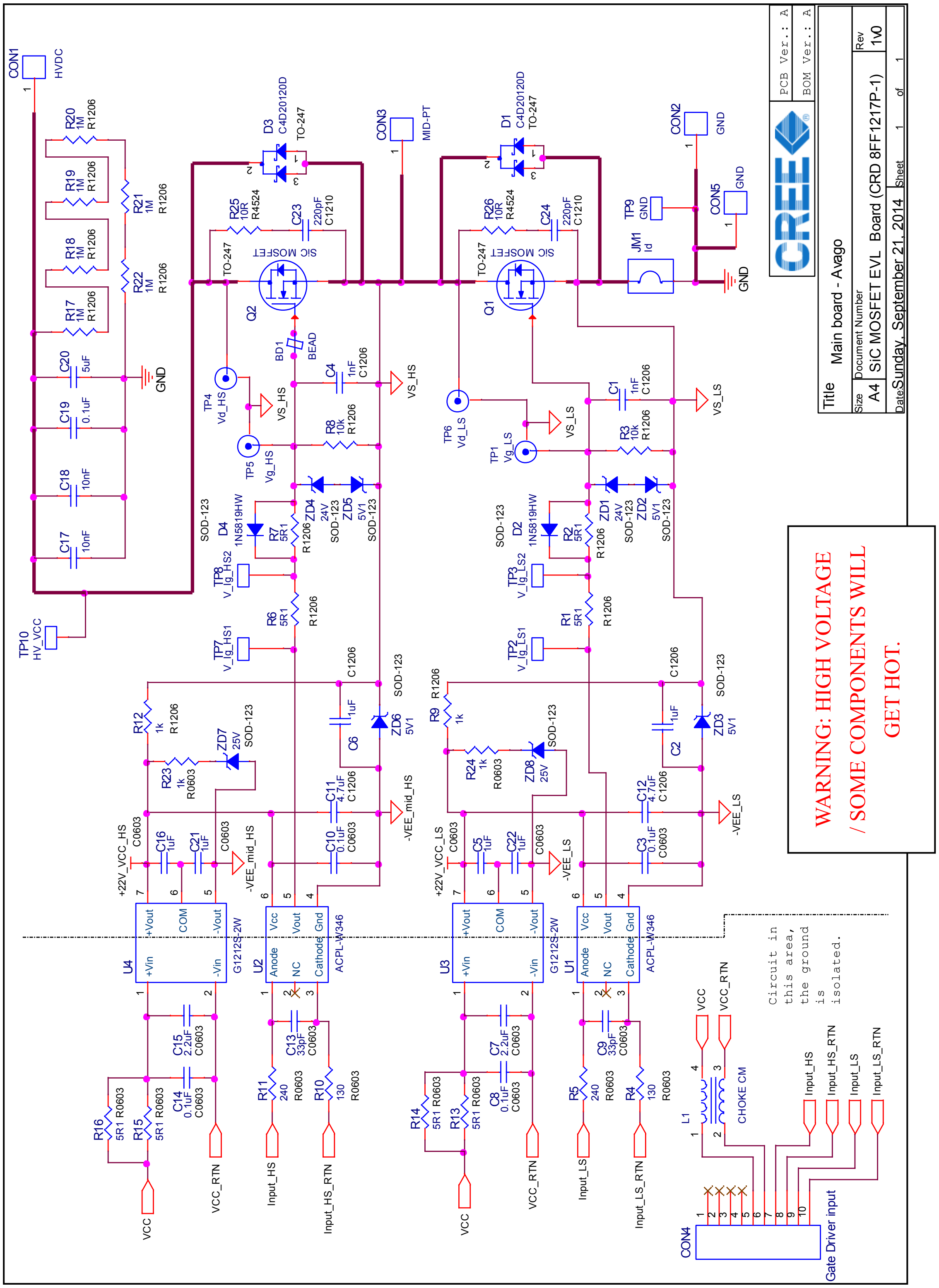
1. Apply thermal grease to the AlN thermal isolator and place it on the heatsink to align with the mounting hole.
2. Apply thermal grease to the back side of the device package and align mounting hole to the thermal isolator and heatsink.
3. Use the M3x10mm screw to secure (0.8 Nm) the device to the heatsink.
4. Attach the EVL board to the heatsink using the 4x standoffs, 4x M3x21mm mounting screws, and 4x washers (1Nm).
5. Solder the MOSFET and Diode devices to the EVL board.



(Reference table for package contents on page 1)

CREE

Schematic of CRD 8FF1217P-1



Component list of CRD 8FF1217P-1

	Part Ref.	Value	Part number	Brand	Description	Type	PCB Footprint
1	BD1	Bead	74270011	Wurth	ferrite bead	THR	
2	C1	1nF			Ceramic, C0G, 10%	SMD	C1206
3	C2	1uF			Ceramic, X7R, 10%	SMD	C1206
4	C3	0.1uF			Ceramic, X7R, 10%	SMD	C0603
5	C4	1nF			Ceramic, C0G, 10%	SMD	C1206
6	C5	1uF			Ceramic, C0G, 10%	SMD	C0603
7	C6	1uF			Ceramic, X7R, 10%	SMD	C1206
8	C7	2.2uF			Ceramic, X7R, 10%	SMD	C0603
9	C8	0.1uF			Ceramic, X7R, 10%	SMD	C0603
10	C9	33pF			Ceramic, C0G, 10%	SMD	C0603
11	C10	0.1uF			Ceramic, X7R, 10%	SMD	C0603
12	C11	4.7uF			Ceramic, X7R, 10%	SMD	C1206
13	C12	4.7uF			Ceramic, X7R, 10%	SMD	C1206
14	C13	33pF			Ceramic, C0G, 10%	SMD	C0603
15	C14	0.1uF			Ceramic, X7R, 10%	SMD	C0603
16	C15	2.2uF			Ceramic, X7R, 10%	SMD	C0603
17	C16	1uF			Ceramic, X7R, 10%	SMD	C0603
18	C17	10nF	B32653A1103K	EPCOS	CAP FILM 10nF 1.6KVDC RADIAL, PP	THR	
19	C18	10nF	B32653A1103K	EPCOS	CAP FILM 10nF 1.6KVDC RADIAL, PP	THR	
20	C19	0.1uF	B32654A1104K	EPCOS	CAP FILM 0.1UF 1.6KVDC RADIAL, PP	THR	
21	C20	5uF	B32774D1505K	EPCOS	CAP FILM 5UF 1.3KVDC RADIAL, PP	THR	
22	C21	1uF			Ceramic, X7R, 10%	SMD	C0603
23	C22	1uF			Ceramic, X7R, 10%	SMD	C0603
24	C23	220pF	C1210C221JGGACTU	Kemet	CAP CER 220PF 2KV 5% NP0 1210	SMD	C1210
25	C24	220pF	C1210C221JGGACTU	Kemet	CAP CER 220PF 2KV 5% NP0 1210	SMD	C1210
26	CON1	HVDC	7808	Skystone	female, M5, 30A, 6P	MECH	
27	CON2	GND	7808	Skystone	female, M5, 30A, 6P	MECH	
28	CON3	MID-PT	7808	Skystone	female, M5, 30A, 6P	MECH	
29	CON4	Gate Driver input	22-27-2101	Molex	10pin, 2.54mm, male	MECH	
30	CON5	GND	7808	Skystone	female, M5, 30A, 6P	MECH	
31	D1	C4D20120D	C4D20120D	CREE	1200V, 20A	THR	TO-247
32	D2	1N5819HW	1N5819HW-7-F	Diodes	DIODE SCHOTTKY 40V 1A SOD123	SMD	SOD-123
33	D3	C4D20120D	C4D20120D	CREE	1200V, 20A	THR	TO-247
34	D4	1N5819HW	1N5819HW-7-F	Diodes	DIODE SCHOTTKY 40V 1A SOD123	SMD	SOD-123
35	JM1	Id			dim. 1.75mm jumper wire x2 for Id connect to GND	MECH	
36	L1	CM CHOKE	ACM4520-142-2P-T000	TDK	CM choke	SMD	
37	Q1	SiC MOSFET	C2M0025120D	CREE	25-mΩ, 1200-V, SiC MOSFET	THR	TO-247

38	Q2	SiC MOSFET	C2M0025120D	CREE	25-mΩ, 1200-V, SiC MOSFET	THR	TO-247
39	R1	5R1			Res, 1%	SMD	R1206
40	R2	5R1			Res, 1%	SMD	R1206
41	R3	10k			Res, 1%	SMD	R1206
42	R4	130			Res, 1%	SMD	R0603
43	R5	240			Res, 1%	SMD	R0603
44	R6	5R1			Res, 1%	SMD	R1206
45	R7	5R1			Res, 1%	SMD	R1206
46	R8	10k			Res, 1%	SMD	R1206
47	R9	1k			Res, 1%	SMD	R1206
48	R10	130			Res, 1%	SMD	R0603
49	R11	240			Res, 1%	SMD	R0603
50	R12	1k			Res, 1%	SMD	R1206
51	R13	5R1			Res, 1%	SMD	R0603
52	R14	5R1			Res, 1%	SMD	R0603
53	R15	5R1			Res, 1%	SMD	R0603
54	R16	5R1			Res, 1%	SMD	R0603
55	R17	1M			Res, 1%	SMD	R1206
56	R18	1M			Res, 1%	SMD	R1206
57	R19	1M			Res, 1%	SMD	R1206
58	R20	1M			Res, 1%	SMD	R1206
59	R21	1M			Res, 1%	SMD	R1206
60	R22	1M			Res, 1%	SMD	R1206
61	R23	1k			Res, 1%	SMD	R0603
62	R24	1k			Res, 1%	SMD	R0603
63	R25	10R	S4-10RF1	Riedon	RES 10 OHM 2W 1% WW SMD	SMD	R4524
64	R26	10R	S4-10RF1	Riedon	RES 10 OHM 2W 1% WW SMD	SMD	R4524
65	TP1	Vg_LS	546-4027	RS	BNC socket, female	MECH	
66	TP2	V_Ig_LS1	5020	keystone	round, 1pin, test point	MECH	
67	TP3	V_Ig_LS2	5020	keystone	round, 1pin, test point	MECH	
68	TP4	Vd_HS	546-4027	RS	BNC socket, female	MECH	
69	TP5	Vg_HS	546-4027	RS	BNC socket, female	MECH	
70	TP6	Vd_LS	546-4027	RS	BNC socket, female	MECH	
71	TP7	V_Ig_HS1	5020	keystone	round, 1pin, test point	MECH	
72	TP8	V_Ig_HS2	5020	keystone	round, 1pin, test point	MECH	
73	TP9	GND	5020	keystone	round, 1pin, test point	MECH	
74	TP10	HV_VCC	5020	keystone	round, 1pin, test point	MECH	
75	U1	ACPL-W346	ACPL-W346-060E	Avago		SMD	
76	U2	ACPL-W346	ACPL-W346-060E	Avago		SMD	
77	U3	G1212S-2W	G1212S-2W	Mornsun		THR	
78	U4	G1212S-2W	G1212S-2W	Mornsun		THR	

79	ZD1	24V			24V, 350mW, 1%	SMD	SOD-123
80	ZD2	5.1V			5.1V, 350mW, 1%	SMD	SOD-123
81	ZD3	5.1V			5.1V, 350mW, 1%	SMD	SOD-123
82	ZD4	24V			24V, 350mW, 1%	SMD	SOD-123
83	ZD5	5.1V			5.1V, 350mW, 1%	SMD	SOD-123
84	ZD6	5.1V			5.1V, 350mW, 1%	SMD	SOD-123
85	ZD7	25V			25V, 350mW, 2%	SMD	SOD-123
86	ZD8	25V			25V, 350mW, 2%	SMD	SOD-123

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The Kit is not a finished end product and is not intended for general consumer use. It is intended solely for use for SiC diode performance evaluation in laboratory or development environments by highly qualified technicians or engineers who are familiar with the dangers associated with handling electrical or mechanical components, systems, and subsystems. The Kit should not be used as all or part of a finished end product. Cree reserves the right in its sole discretion to make corrections, enhancements, improvements, or other changes to the Kit or to discontinue the Kit.

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Your remedies for any breach of warranty are limited to those provided in these additional Terms to the exclusion of all other remedies, including without limitation incidental or consequential damages. No warranty or agreement varying or extending the foregoing warranty and limitation of remedy provisions may be relied upon by you unless it is in writing and signed by the President or a Vice President of Cree, Inc. No representation or affirmation of Cree, whether by words or action, shall be construed as a warranty. If any model or sample was shown to you, such model or sample was used merely to illustrate the general type and quality of the Kit and not to represent that the Kit would necessarily conform to the model or sample.

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CREE'S AGGREGATE LIABILITY IN DAMAGES OR OTHERWISE SHALL IN NO EVENT EXCEED THE AMOUNT, IF ANY, RECEIVED BY CREE IN EXCHANGE FOR THE KIT. IN NO EVENT SHALL CREE BE LIABLE FOR INCIDENTAL, CONSEQUENTIAL, OR SPECIAL LOSS OR DAMAGES OF ANY KIND, HOWEVER CAUSED, OR ANY PUNITIVE, EXEMPLARY, OR OTHER DAMAGES. NO ACTION, REGARDLESS OF FORM, ARISING OUT OF OR IN ANY WAY CONNECTED WITH ANY KIT FURNISHED BY CREE MAY BE BROUGHT BY YOU MORE THAN ONE (1) YEAR AFTER THE CAUSE OF ACTION ACCRUED.

Indemnification

You shall defend, indemnify, and hold Cree and its directors, officers, employees, affiliates, contractors, representatives, agents, and designees harmless from and against any and all claims, expenses, losses, costs, liabilities, or damages (collectively, “Claims”), including those related to property damage, injury, or death, arising from any breach of any term or condition set forth in these Terms by you or anyone for whom you are legally liable. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the Kit fails to perform as described, intended, or expected.

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power