

Final Product Change Notification

201812001F01

Issue Date: 14-Jan-2019
Effective Date: 28-Apr-2019
 Dear *Gordon Love*,

Here's your personalized quality information concerning products Premier Farnell PLC purchased from Nexperia. For detailed information we invite you to [view this notification online](#)



Change Category

- | | | | | |
|---|---|--|---|---|
| <input checked="" type="checkbox"/> Wafer Fab Process | <input type="checkbox"/> Assembly Process | <input type="checkbox"/> Product Marking | <input type="checkbox"/> Test Location | <input type="checkbox"/> Design |
| <input checked="" type="checkbox"/> Wafer Fab Materials | <input type="checkbox"/> Assembly Materials | <input type="checkbox"/> Mechanical Specification | <input type="checkbox"/> Test Process | <input type="checkbox"/> Errata |
| <input type="checkbox"/> Wafer Fab Location | <input type="checkbox"/> Assembly Location | <input type="checkbox"/> Packing/Shipping/Labeling | <input type="checkbox"/> Test Equipment | <input type="checkbox"/> Electrical spec./Test coverage |

Release of 8 inch wafer diameter for resistor-equipped Transistors (RET) in SOT363

Details of this Change

Release of production using 8 inch wafer diameter, 2nd source epitaxy, new doping material for the poly silicon resistors and increased top side metallization thickness from 1.4 μm to 1.5 μm for resistor-equipped Transistors (RET) in SOT363 package.

Old Products:

- 6 inch wafer diameter
- inhouse epitaxy
- current doping material for the poly silicon resistors
- 1.4 μm top metallization thickness

Changed Products:

- 6 inch or 8 inch wafer diameter
- inhouse epitaxy (6 inch and 8 inch) or external epitaxy (8 inch) wafer diameter
- old doping material (6 inch) or new doping material (8 inch) for the poly silicon resistors
- 1.4 μm (6 inch) or 1.5 μm (8 inch) top metallization thickness

Production on 8 inch wafer diameter implies the use of the respective 8 inch wafer process technology.

Why do we Implement this Change

- (1) To increase flexibility and volume ramp-up.
- (2) To increase flexibility, volume ramp-up and reduced supply chain risk.
- (3) Improved resistance linearity.
- (4) Align to 8 inch wafer diameter process and to increase process robustness.

Identification of Affected Products

The 8 inch products can be identified by a marker on the die surface.
Changed products can be identified by date code after implementation.

Product Availability

Sample Information

Samples are available upon request
Latest sample request date for PCN samples is 31-January-2019.

Production

Planned first shipment 01-May-2019

Impact

No impact to the products' functionality anticipated.

Disposition of Old Products

Supply using 6 inch wafer will be continued in parallel to 8 inch wafer production.

Additional information

Affected products and sales history information: see attached file

Self qualification: [view online](#)



Timing and Logistics

Your acknowledgement of this change, conform JEDEC J-STD-046, is expected till 13-Feb-2019. Lack of acknowledgement of the PCN constitutes acceptance of the change.

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please [contact Nexperia "Global Quality Support Team"](#).

For all Quality Notification content inquiries, please contact your local Nexperia Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

e-mail address PCN-Bipolar.Discretes@nexperia.com

At Nexperia B.V. we are constantly striving to improve our product and processes to ensure they reach the highest possible Quality Standards.

About Nexperia B.V.

We at Nexperia are the efficiency semiconductor company. We deliver over 70 billion products a year and as such service thousands of global customers, both directly and through our extensive network of channel partners. We are at the heart of billions of electronic devices in the Automotive, Mobile, Industrial, Consumer, Computing, and Communication Infrastructure segments.

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